A 96% Alumina based Packaging System for 500°C Test of SiC Integrated Circuits

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Abstract

Along with the development of silicon carbide (SiC) sensors and electronic devices for operation at 500°C, compatible packaging technologies are needed for long term high temperature test and deployment of these sensors and electronic devices. 96% Al_2O_3 ceramic is a good electrically insulating material with acceptable dielectric constant and low dielectric loss over wide temperature and frequency ranges. This paper presents a packaging system for low power integrated circuits including a prototype 8-I/O chip-level package and printed circuit board (PCB) based on 96% Al_2O_3 ceramic substrates and Au thick-film metallization for 500°C applications. The details related to designs of packages and PCBs, packaging materials, and specific packaging step recipes including wire - bonding and die-attach, are presented. Some test results of this prototype packaging approach applied to SiC integrated circuits at 500°C are reviewed.

Key words

High Temperature, Packaging, Alumina, Thick Film

I. Introduction

Sensors and electronics capable of operation at 500 °C are required for long term Venus surface missions, as well as for *in situ* monitoring and control of next generation aeronautical engines [1a]. High temperature sensors and electronics can also find many applications in military, and energy and automobile industries [1b,1c]. Various silicon carbide (SiC) sensors and electronic devices have been developed and demonstrated for operation at 500°C and above [2a,2b]. This paper details an initial version of a compatible and durable packaging technology needed for beneficial long term high temperature test and deployment of these sensors and electronic devices at high temperature.

In the initial stage of this development work, alumina including 96% and 92% Al_2O_3 and AlN ceramic substrates with Au thick-film metallization [3a,3b] based high temperature prototype packages were developed [3c] in parallel to facilitate the test of SiC integrated circuits (ICs) at high temperatures up to 500 °C in laboratory environment. While AlN substrates have better thermo-mechanical properties such as lower CTE and higher thermal conductivity, experimental study of dielectric properties of these ceramic substrate materials indicated that 96% Al_2O_3 ceramics offered better electrical insulation with more acceptable dielectric constant and low dielectric loss over wide temperature and frequency ranges [4]. Thus, the 96% alumina was selected as the primary ceramics for development of long-term durable 500 °C electronic packaging substrate.

This paper describes a packaging system including a low power prototype 8-I/O chip-level package and printed circuit board (PCB) based on pre-fired 96% Al_2O_3 ceramic substrate and Au thick-film metallization successfully used for long-term 500°C testing of SiC integrated circuits. In particular, the details related to designs of packages and PCBs, packaging materials, and specific packaging step recipes, such as wire-bonding and die-attach, are discussed. This ceramic substrate and precious metal based foundation material system has for many years enabled long term test of SiC ICs at 500 °C, some of these tests lasted for over a year.

This paper documents this foundational technology at a detailed level beyond that previously provided. Examples of test results of this packaging approach applied to SiC integrated circuits at 500 ºC are reviewed in this paper.

II. Chip Package

The package for housing a single SiC IC die with up to eight inputs/outputs (I/Os) for long-term 500 °C operational testing was developed based on this material system. Figure 1 shows optical pictures of the package with 8 I/Os without a lid on [3c]. The package was composed of four stacked and bonded layers including substrate, wire-bond, spacer, and lid. All four layers were pattern-cut pre-fired 96% ceramic alumina substrate with patterned DuPont 5771 gold (Au) thick - film metallization [5] pads/traces. The package layers including the lid were in-house designed and

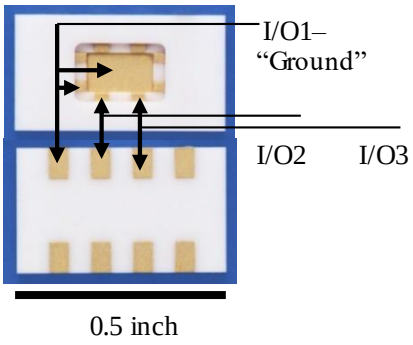

Figure 1: Prototype high-temperature chip-level packages made of 96% Al_2O_3 (on right) substrates and Au thick-film metallization [5b]. The metallization pads on the bottom side are 50 mil wide and 75 mil long with spacing of 55 mil between.

commercially fabricated to the design specifications using industrial standard thick-film processes, such as screen printing and dry - firing, recommended by the thick-film manufacturer [5]. Figure 1 shows optical pictures of the package after integration of three layers without a lid on [3c]. Figure 2 shows the drawings of each layer of the package including the lid. The drawing dimensions are all shown in inches.

The metallization on the top side of the substrate layer (Figure 2a) is basically for die mechanical attachment and electrical contact to the backside metallization of the IC die, as well as for electro-magnetic (EM) shielding. The pads on the bottom side of the substrate layer (shown in the lower picture of Figure 1) are for electrical interconnections as well as attachment/bonding of the package to the ceramic circuit board. The wire-bond layer (Figure 2b) provides eight Au thick-film bond-pads for wire-bonding to interconnect the high temperature durable metallization pads [6a,6b] on the IC die to the package. These eight metallization pads/traces extend to the side walls (of wire-bond layer) where these traces are connected subsequently to those on the side walls

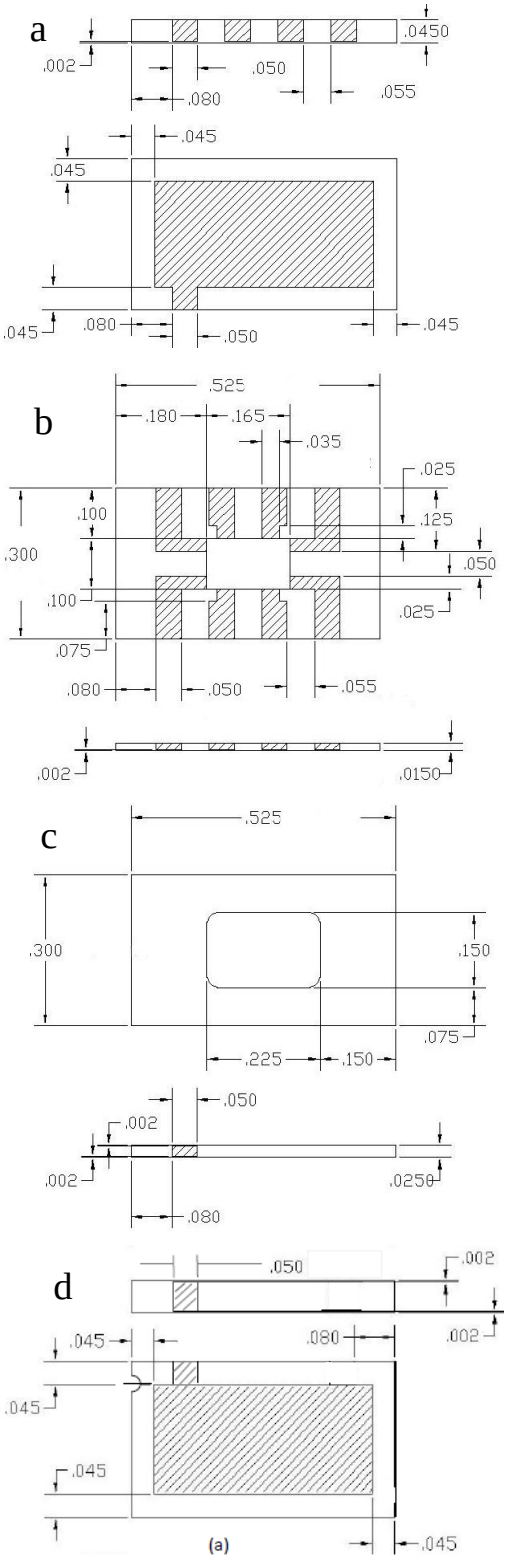

Figure 2: Design of metallization dimensions at various layers and sides. a) Substrate layer. b) Wire bond layer. c) Spacer layer. d) Lid [3c]. The bottom side metallization of Substrate layer is shown in Figure 1. All dimensions are shown in inches.

Table 1: The distributed capacitance and AC conductance between I/O1 (ground) and the nearest neighbor I/O (I/O2) of prototype Al_2O_3 package. The upper number is capacitance in unit of pF or otherwise specified as nF, the lower number is conductance in unit of μS [3c].

T (°C) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
100	0.00nF	0.00nf	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00	5	5
	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.005	0.00	0.00
120	1.5	-	1	1	1.5	2	2.0	2.0	2.5	4	4
	0.000	0.000	0.000	0.000	0.00	0.00	0.000	0.000	0.0015	0.002	0.0025
1K	1.5	1.3	1.3	1.4	1.35	1.5	1.6	1.75	1.85	2.15	2.35
	0.001	0.000	0.00	0.000	0.000	0.001	0.001	0.002	0.0025	0.004	0.0055
10K	1.36	1.33	1.3	1.36	1.35	1.46	1.43	1.56	1.54	1.63	1.74
	0.003	0.000	0.000	0.001	0.001	0.002	0.004	0.006	0.010	0.015	0.020
100K	1.33	1.38	1.28	1.36	1.36	1.44	1.36	1.427	1.42	1.53	1.47
	0.015	0.006	0.006	0.007	0.009	0.0135	0.018	0.0255	0.036	0.052	0.071
1M	1.29	1.30	1.29	1.40	1.35	1.45	1.33	1.39	1.42	1.45	1.47
	-	-	-	-	-	-	-	-	-	0.043	0.12

Table 2: The distributed capacitance and AC conductance between two neighbor I/Os (I/O2 and I/O3) of prototype Al_2O_3 package. The upper number is capacitance in unit of pF or otherwise specified as nF, the lower number is conductance in unit of μS [3c].

T (°C) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
100	0.00nF	0.00nf	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	< 5	5
	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.005	0.00	0.00
120	0.5	0.5	0.5	1	1	1	1.5	1.5	1.5	1.5	2
	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.0005	0.001	0.001
1K	0.5	0.5	0.5	0.5	0.5	0.5	0.6	0.7	0.7	0.8	0.95
	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.001	0.001	0.002	0.0025
10K	0.49	0.50	0.50	0.490	0.49	0.52	0.53	0.58	0.59	0.65	0.69
	0.001	0.000	0.000	0.000	0.000	0.001	0.002	0.003	0.004	0.006	0.008
100K	0.492	0.486	0.497	0.493	0.487	0.517	0.539	0.535	0.563	0.585	0.57
	0.005	0.006	0.0015	0.002	0.003	0.005	0.007	0.011	0.015	0.022	0.030
1M	0.501	0.497	0.485	0.506	0.499	0.529	0.533	0.55	0.556	0.544	0.55
	-	-	-	-	-	-	-	-	-	-	-

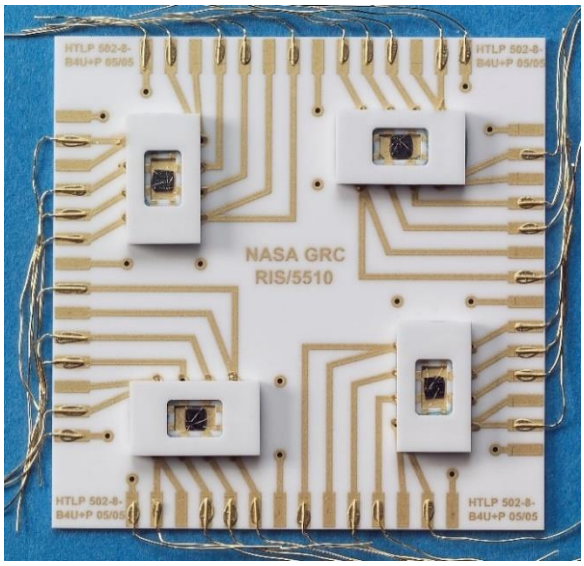

Figure 3. A ceramic circuit board with four packaged SiC IC chip and I/O wires before 500 °C test.

of the substrate layer, the pads on the side walls of the substrate layer lead to the attachment / connection pads on the bottom of the substrate layer, as shown in the lower picture of Figure 1. The spacer layer (Figure 2c) provides a side wall connection to the lid metallization pad to the die-attach pad for EM shielding purpose. The eight I/Os are electrically accessed through metallization pads on either two package side walls or the package bottom.

A screen printable insulation glass paste, Ferro FX10-054, was used as a high temperature durable "adhesive" to bond the package layers [7a,7b]. This glass paste was selected during the early development stage since it bonded to both alumina and aluminum nitride substrates. The package assembly stacked with interlayers of the wet glass paste was

horizontally mechanically aligned against a vertical "wall" for each side of the assembly, and then dried at 150 °C for 20 minutes (min) with a ramp rate of 40 °C/min followed by firing at manufacturer recommended (for the Ferro glass paste) temperature of 850 °C for 20 min also with ramp rate of 40 °C/min, in air ambient using a box oven. After the firing the oven was naturally cooled, it took several hours. The metallization traces/pads on the side walls of the substrate and wire-bond layers for the same I/O were then connected by hand-adding DuPont 5771 Au thick-film paste to pad gaps, and was then dried at 150 °C for 15 min and fired at 850 °C for 20 min in air ambient, as recommended by the thick-film paste manufacturer, but using a box oven. The ramping rates was the same as that for processing the glass adhesive, and the final cooling was also natural.

The low frequency parasitic parameters between two neighboring I/Os of an assembled sample package (without a lid on) was characterized using LCZ meter in a temperature range between room temperature to 550 °C. The measurement results are shown in Table 1 and 2 which are reproduced from Ref [3c]. The detailed electrical measurement was discussed in Ref [3c]. The parasitic capacitance and conductance between I/O1 (connected to the die-attach pad) and I/O2 (see Figure 1) is bellow 5pF and 0.052μS between 100 Hz and 1MHz in the temperature range from room temperature to 500 °C. In the same frequency and temperature range, the parasitic capacitance and conductance between I/O2 and I/O3 (see Figure 1) is below 5pF and 0.022μS [3c]. The parasitic data indicate that the prototype package can be used for packaging many envisioned SiC ICs.

III. Circuit Board and Assembly

A circuit board compatible to the high temperature alumina chip packages based on the same substrate and metallization material system was in-house designed and commercially fabricated using the same Au thick-film processes described above for the package layers. The circuit board measures 2 in. x 2 in. x 25 mil (thick), and it can accommodate four packages, each with eight I/Os, as shown in Figure 3. The width of metallization traces connecting the packages to the I/O pads at circuit board edges is 25 mil, the spacing between neighboring traces in majority area are 60 mil and above. The width of the I/O pads at board edges for attaching (I/O) wires is 50 mil wide with 50 mil spacing. The metallization pads (not shown) on the board for connection to packages were round-shaped, and the diameter of these pads was same as the width of the pads on the bottom side of the package.

Ten mil diameter Au wires were attached to the I/O pads along the edges of the board first to facilitate later electrical connection with measuring instruments (outside the oven). Both a section of a wire and the bond pads were coated with same (DuPont 5771) Au thick film paste, then the wire was placed flat at the center of the pad. The assembly was then heated with temperature ramp rate of 40 °C/min to 150 °C and dwelled for 15 min followed by firing at 850 °C for 20 min in a box oven with a ramp rate of 40 °C/min. The cooling was natural after the firing. It took several hours. Glass fiber based sleeves (not shown) were used to insulate wires from each other, as well as the metal oven door/frame. Multiple (or all) wires can be attached simultaneously to reduce the times of firing.

After all the I/O wires were attached, the packages were mounted onto the board using a very similar process as attaching I/O wires. Both the Au bond pads on the bottom side of the package and the pads on the circuit board were hand coated with same type of Au thick-film paste (DuPont 5771). While the paste was still wet, the package was set onto the board and visually hand-aligned to the position on the board. The assembly was then dried at 150 °C for 15 min. and fired at 850 °C for 20 min. in air ambient in a box oven. The temperature profile was same as for attaching I/O wires. It should be noted that for package attachment the Au paste with above normal viscosity was needed. The higher viscosity could be achieved by reducing 10-15% (volume) of organic carrier in the normal DuPont 5771 paste material. The excessive carrier can be drained after the solid particles in the paste naturally precipitated after sufficient shelf storage.

Conventionally, IC die are packaged at chip level first, then the packaged IC chips are mounted on a circuit board for application. However, the process attaching the ceramic packages to the ceramic board involved firing at 850 °C. In order to avoid unnecessary exposure of IC die to this temperature the packages were attached to the circuit board before IC die were packaged at chip level. This was a limitation of this foundational high temperature electronic packaging approach.

IV. Die Attachment

A prototype conductive die-attach material and process was developed for SiC IC die with Ti/TaSi2/Pt backside metallization stacks [6a,6b] and Au die-attach pad on alumina package for use in long duration 500°C air ambient. One of the technical goals to develop this die-attach was limiting the maximum processing temperature to the designated IC operation temperature (500 °C) at the time before it was documented that SiC ICs developed in-house could/can actually take much higher temperature. A wet mixture of Pt thick-film (DuPont 9896R [8]) with a low solidification temperature glass powder (SEM-COM SCB-1 [9]) was prepared at room temperature. Pt particles in the thick-film paste provided electrical conductivity, and the glass provided adhesion to Pt die backside surface as well as to the surface of Au thick-film pad on the package. The glass

solidification temperature was ~ 480 °C and softening temperature was above ~ 525 °C. The weight mixture ratio between glass power and Pt thick-film was ~ 1.5:1, the standard thinner recommended for the Pt paste (specified for the Pt paste and labeled on the Pt paste bottle) was added to adjust the viscosity to make it as a paste more suitable for die-attach. The IC die were placed onto the die attach pad of the package with wet applied die-attach paste. The die-packages-circuit-board assembly was heated at the rate of 40 °C/min to 150°C and dwelled for 15 min followed by heat treatment at rate of 40 °C/min to 500 °C and dwelled for two to three hours in air ambient. The afterward cooling process was natural, and typically took several hours. This prototype high temperature conductive die-attach scheme was only intended for packaging applications with very low die substrate current. Four SiC device chips attached to ceramic packages using this scheme are shown in Figure 3.

V. Wire – Bonding

Bond pad surfaces on SiC IC die were thin-film Pt [6b] and the bond pads on the alumina package were thick-film gold. Thermo-sonic gold wire bonding was used for interconnecting the IC die to the package. One of the challenges of high temperature packaging is electromigration of conductors under electrical bias at high temperature. In order to reduce and control electromigration in thin gold wire, 1 mil diameter 98% (2% impurity) pure gold wire [10] was used with commercial ball-wedge thermal sonic wire-bonder [10]. The ball bond was applied on Pt pad surface on SiC IC die as the first bond, and wedge bond was applied on the package bond-pad with typical wire-bonder setting for 1 mil Au wire. When the packaged ICs were tested in high temperature (500 °C) air, the impurities in the wire material migrated to the surface and quickly formed a low-reflective oxides surface layer passivating the wire surface, therefore beneficially slowed down electromigration process at wire surfaces (This topic needs to be explored more in the future to optimize Au wire formula for high temperature applications). Figure 3 shows four packaged SiC ICs on a circuit board after wire-bonding before high temperature test (1 mil diameter Au wires were still gold colored), without lids on.

VI. High Temperature Testing Results

This prototype high temperature durable packaging system successfully facilitated tests of various SiC devices and ICs in 500°C oxidizing air ambient for up to 10,000 hours. The basic packaging components such as chip-level package, circuit board, attaching and joining technologies were also tested with a SiC JFET during Shuttle launching and landing flights, and in low earth orbit space environment for 18 months on the International Space Station [11].

For example, Figure 4 shows I-V curves of a packaged SiC JFET transistor measured at the first hour, 100 hours, 1000 hours, and 10,000 hours in 500 °C air ambient [12]. This was the first report of long-term testing for such a duration of a 500 °C electronic device facilitated with a packaging system.

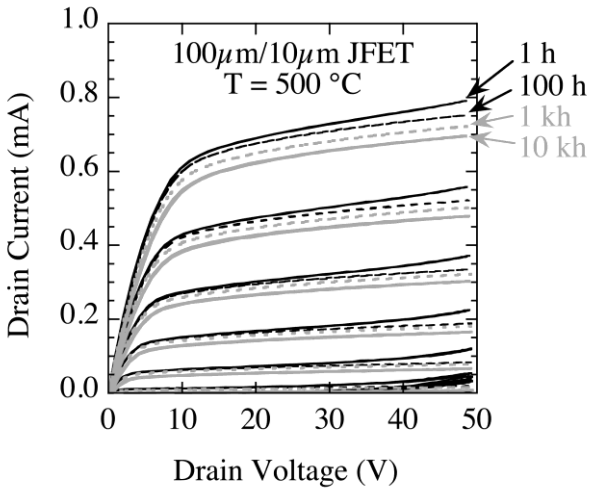

Figure 4: Drain I-V curves of a packaged 100μm/10μm NASA Glenn 6H-SiC JFET measured during the 1st, 100th, 1000th, and 10000th hour at 500 °C. Gate voltage steps are -2 V starting from 0V as the topmost [12].

Figure 5 shows the test waveforms of input and output signals of a packaged SiC differential amplifier measured at 500 °C at the first hour and 2000 hours indicating very stable performance of the circuit at the temperature [13].

These test results of packaged SiC ICs basically validated this prototype packaging system for facilitating long term high temperature electrical testing SiC ICs in 500 °C air

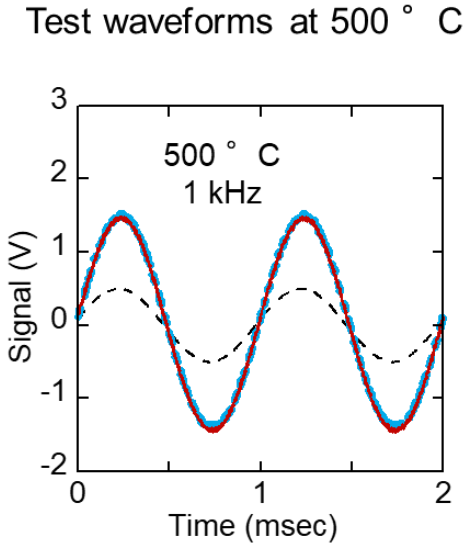

Figure 5: Test waveforms of input (dark, 1 kHz) and output signals of a packaged SiC differential amplifier measured at 500 °C at the first hour (blue) and 2000 hours (red) [13].

ambient.

VII. Summary

A 96% alumina and Au thick-film metallization based prototype high temperature electronic packaging system for 500°C test is reviewed in detail. This packaging system includes a chip-level package with 8 I/Os, a circuit board designed to accommodate 4 such packages, attachment of wire connecting the board to the instrument outside an oven, attachment of packages to the board, die-attach, and wire-bonding connecting IC die to the package. This packaging system was developed for high temperature SiC ICs with Pt capped thin-film metallization on the die backside and Pt or Au capped wire bond pads on the active side for long-term 500 °C operation. The maximum process temperature that the SiC die was exposed to in the entire packaging process was limited to 500 °C even though the SiC ICs developed by NASA GRC have experimentally demonstrated operation at higher temperatures. Various SiC devices and ICs have been successfully long-term tested using this prototype packaging system up to 10,000 hours in 500 °C air ambient. A packaged SiC JFET was also tested in space station orbit for 18 months with sun light induced thermal cycling.

Even though all the packaged SiC ICs tested during that period of time were facilitated by this foundational prototype packaging system based on ceramic alumina and precious metallization, significant further advancements have already been demonstrated [14,15]. For example, a high temperature durable co-fired material system with multilayer capability [14] that eliminates the labor intensive package integration by stacking pre-fired multi-layers, and enables multilayer circuit board capability to accommodate more components per board has been established [15]. The die-attach needs to be improved for higher electrical and thermal conductivities, and compatibility with standard die-attach machines. As discussed in Section III, the package attachment needs to be significantly improved to reduce the maximum packaging processing temperature, to implement more conventional packaging sequence starting from chip-level packaging followed by circuit board level assembly. A repairable package/component attachment technology should also be pursued.

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