2021 iMAPS HiTEC *3:00-3:45 PM April 28, 2021*

A 96% Alumina based Packaging System for 500 °C Test of SiC Integrated Circuits

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Background

- 500 °C long duration electronics for NASA aeronautics and space applications
- SiC JFETs based analog and digital ICs, chemical sensors, MEMS based pressure sensors developed and demonstrated at 500 °C and beyond at NASA GRC
- A compatible packaging system needed for long-term test and deployment of SiC ICs at 500 °C
- Started with ceramic substrates and precious metal material systems
  - 96% Al_2O_3, 90% Al_2O_3, AlN
  - Au thick film metallization* **
- 96% alumina based system was further developed
- Foundation system of alumina and precious metal (metallization)

This presentation provides comprehensive details of this prototype packaging system not previously reported

*J. S. Salmon, R. Johnson, and M. Palmer, in Trans. Fourth HiTEC, June 15-19, 1998. Albuquerque, NM.

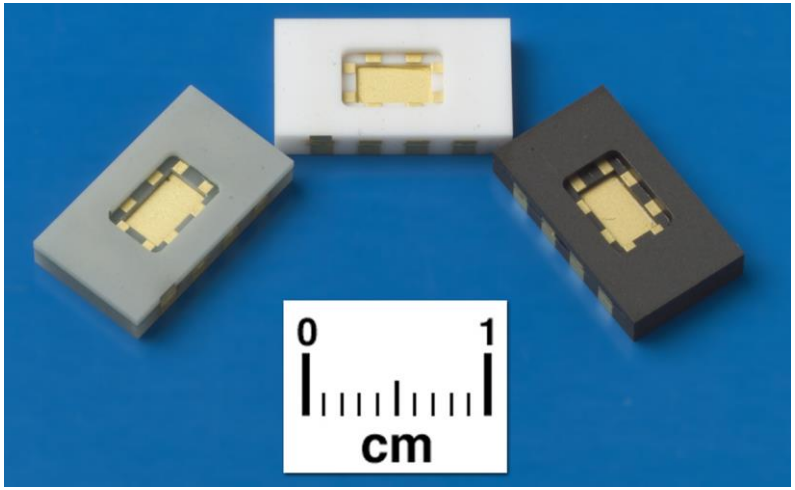
** L. Chen, G. W. Hunter, and P. G. Neudeck, in Trans. 1st International AVS Conference on Microelectronics and Interfaces, Feb. 7, 2000.

Ceramic Substrates and Au Thick-film Metallization based Chip Level Packages

Electronic Packages for High Temperature ICs

96% Al_2O_3

AlN



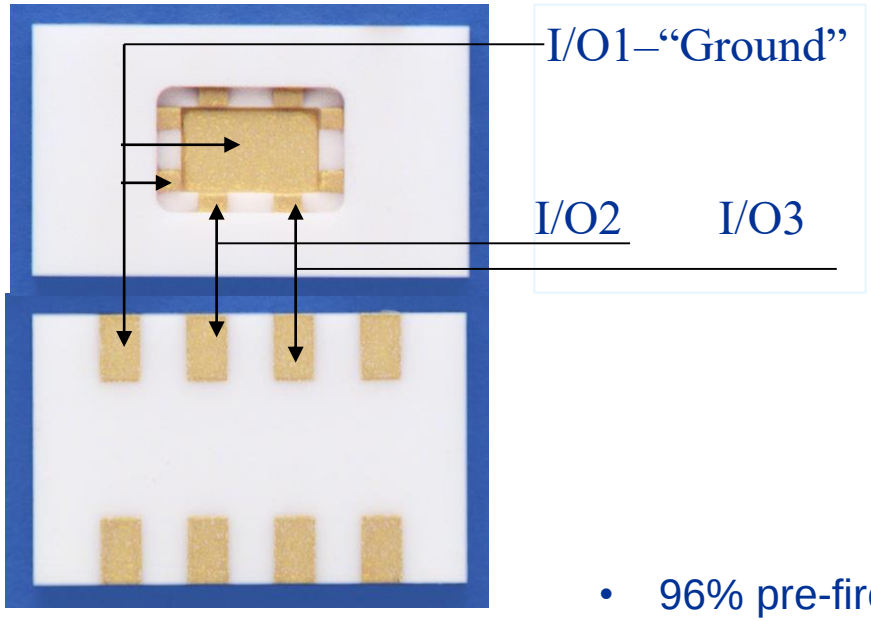
90% Al_2O_3

- Three types of ceramic substrate and Au thick-film metallization based chip-level packages
- 96% alumina has best high temperature dielectric performance
- AlN has better thermo-mechanical properties
- 90% alumina easier for fab
- Au thick-film metallization

L. Chen et al, in Proceedings ICSCRM 2011. Edited by R. Devaty, M Dudley, T P. Chow, ans P. G. Neudeck

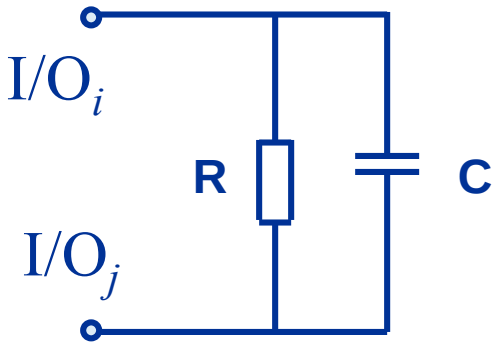
96% Alumina Chip-level Packages

96% alumina 8 I/Os Prototype Package



0.5 inches

Parasitic Equivalent

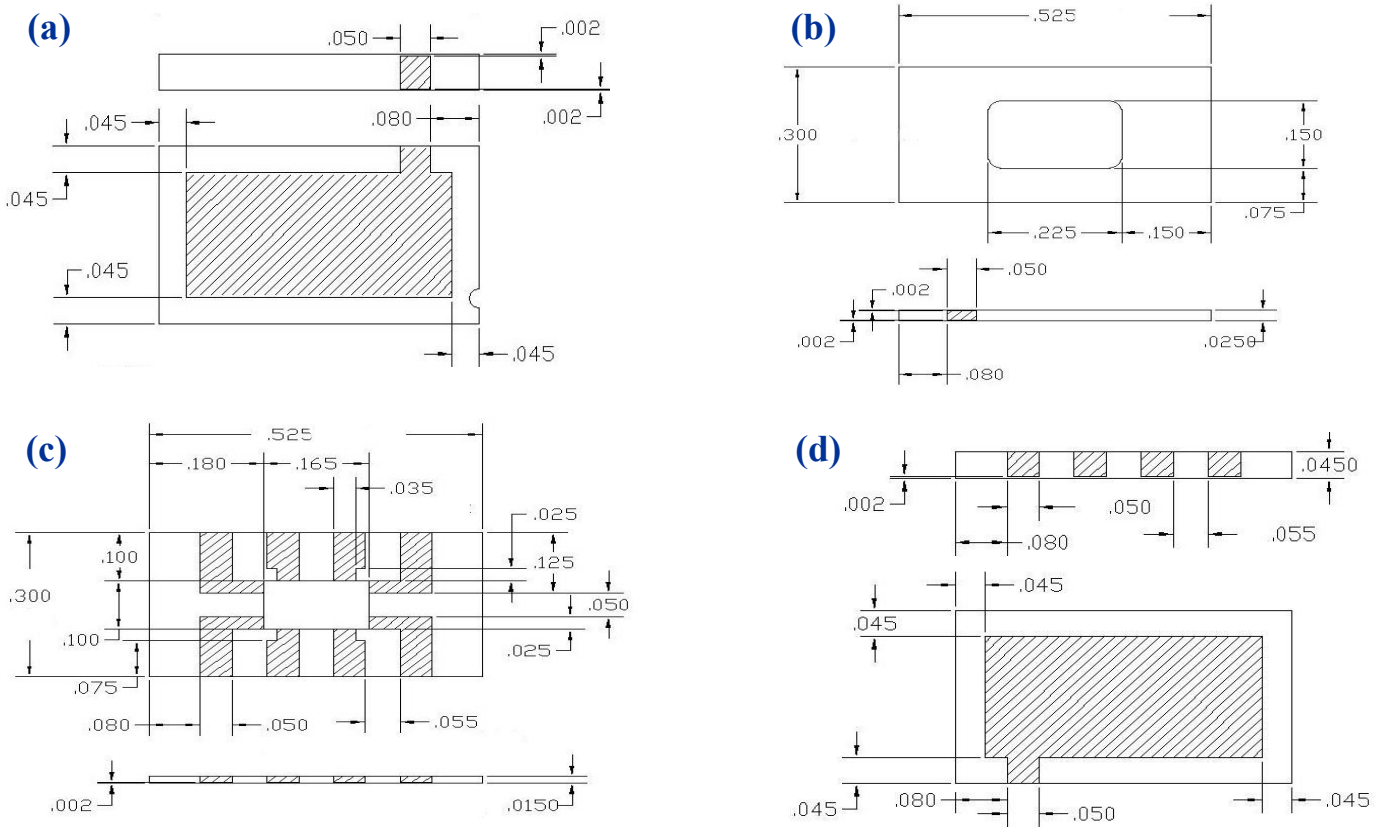


C: Dielectric polarization
R: DC and dielectric loss

- 96% pre-fired alumina substrate
- DuPont 5771 Au metallization
- Structure: 3 stacked layers + lid
- In-house designed, and commercially individually made layers
- 8 I/Os

L. Chen and G. W. Hunter, in Proceedings of HiTEN, Paris, France, Sept. 6-8, 2005.

96% Alumina Chip-level Packages



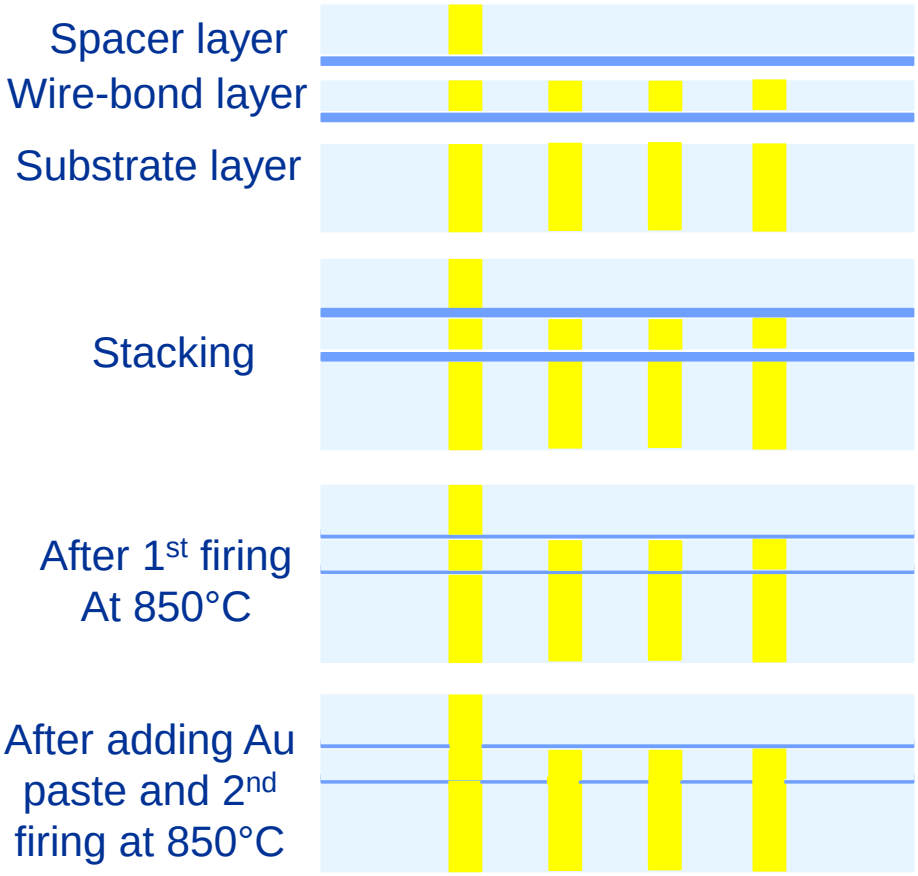
a) Lid (backside). b) Space layer c) Wire-bond layer d) Substrate layer

In-house designed, commercially fabricated

L. Chen and G. W. Hunter, in Proceedings of HiTEN, Paris, France, Sept. 6-8, 2005.

96% Alumina Chip Package

96% Alumina Package Assembly Flow



- All layers: 96% alumina substrate and DuPont 5771 Au thick-film metallization
- In-house designed, commercially made

Step I

- Ferro 10-054 glass as adhesive (blue)
- Stacked while glass adhesive wet
- Horizontally aligned against a vertical “wall”

Step II

- Dried at 150°C for 20 min with ramp rate 40°C/min, fired at 850°C for 20 min with ramp rate 40°C/min in a box oven in air.

Step III

- Adding Au paste (5771) to the space between Au pads on the side wall
- Dried at 150°C for 20 min with ramp rate 40°C/min, fired at 850°C for 20 min with ramp rate 40°C/min in a box oven in air

96% Alumina Chip-level Packages

Impedance between I/O1 and I/O2

T (°C) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
100	0.00nF	0.00nf	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00	5	5
	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.005	0.00	0.00
120	1.5	-	1	1	1.5	2	2.0	2.0	2.5	4	4
	0.000	0.000	0.000	0.000	0.00	0.00	0.000	0.000	0.0015	0.002	0.0025
1K	1.5	1.3	1.3	1.4	1.35	1.5	1.6	1.75	1.85	2.15	2.35
	0.001	0.000	0.00	0.000	0.000	0.001	0.001	0.002	0.0025	0.004	0.0055
10K	1.36	1.33	1.3	1.36	1.35	1.46	1.43	1.56	1.54	1.63	1.74
	0.003	0.000	0.000	0.001	0.001	0.002	0.004	0.006	0.010	0.015	0.020
100K	1.33	1.38	1.28	1.36	1.36	1.44	1.36	1.427	1.42	1.53	1.47
	0.015	0.006	0.006	0.007	0.009	0.0135	0.018	0.0255	0.036	0.052	0.071
1M	1.29	1.30	1.29	1.40	1.35	1.45	1.33	1.39	1.42	1.45	1.47
	-	-	-	-	-	-	-	-	-	0.043	0.12

Parasitic capacitance and conductance between I/O1 and I/O2 is 5pF and 0.052μS or less between 100 Hz and 1MHz between T_R - 500 °C

L. Chen and G. W. Hunter, in Proceedings of HiTEN, Paris, France, Sept. 6-8, 2005.

96% Alumina Chip-level Packages

Impedance between I/O2 and I/O3

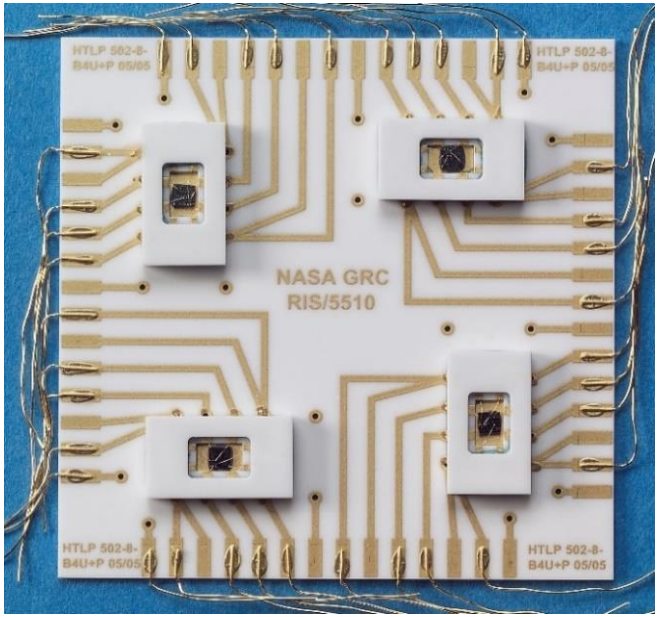
T (°C) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
100	0.00nF	0.00nf	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	< 5	5
	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.005	0.00	0.00
120	0.5	0.5	0.5	1	1	1	1.5	1.5	1.5	1.5	2
	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.0005	0.001	0.001
1K	0.5	0.5	0.5	0.5	0.5	0.5	0.6	0.7	0.7	0.8	0.95
	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.001	0.001	0.002	0.0025
10K	0.49	0.50	0.50	0.490	0.49	0.52	0.53	0.58	0.59	0.65	0.69
	0.001	0.000	0.000	0.000	0.000	0.001	0.002	0.003	0.004	0.006	0.008
100K	0.492	0.486	0.497	0.493	0.487	0.517	0.539	0.535	0.563	0.585	0.57
	0.005	0.006	0.0015	0.002	0.003	0.005	0.007	0.011	0.015	**0.022**	0.030
1M	0.501	0.497	0.485	0.506	0.499	0.529	0.533	0.55	0.556	0.544	0.55
	-	-	-	-	-	-	-	-	-	-	-

Parasitic capacitance and conductance between I/O2 and I/O3 is 5pF and 0.022μS or less between 100 Hz and 1MHz between T_R - 500 °C

L. Chen and G. W. Hunter, in Proceedings of HiTEN, Paris, France, Sept. 6-8, 2005.

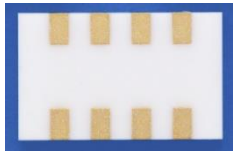
96% Alumina Circuit Board for Four 8-I/O Packages

96% Circuit Board and Assembly Flow



1 inch

Bottom side of package



- 96% alumina with DuPont 5771 Au thick-film metallzation
- In-house designed, commercially made
- 2 in x 2 in x 25 mil thick
- Double sided, with conductive via holes
- Width of traces 25 mil, spacing ≥ 60 mil
- Width of I/O pads 50 mil, 50 mil spacing
- Accommodates 4 packages with 8 I/Os with some diagnostic traces

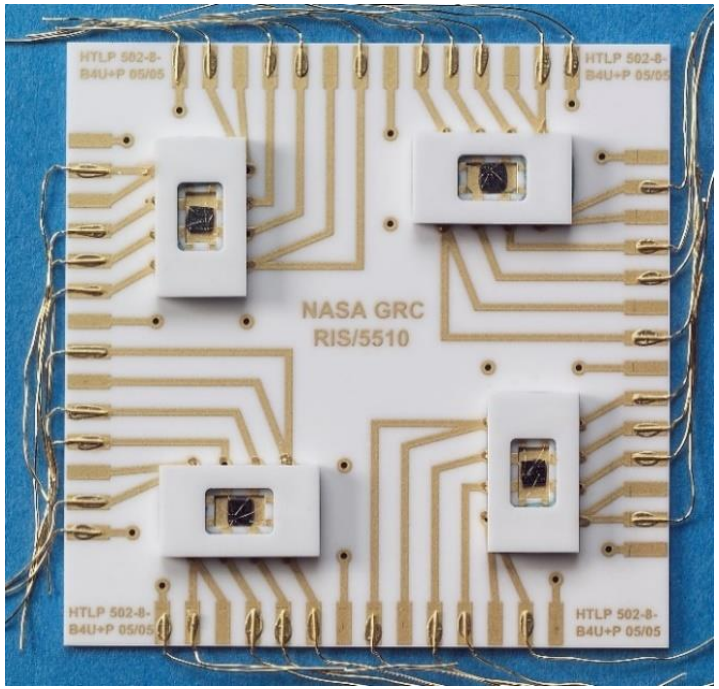
I/O wire attach

- Both I/O pads and 10 mil Au wires coated with DuPont 5771
- Place wet-coated wire onto the wet-coated pad
- Dried in box oven in air at 150°C for 20 min with ramp rate 40°C/min

L. Chen et al, in Proceedings ICSCRM 2011. Edited by R. Devaty, M Dudley, T P. Chow, ans P. G. Neudeck

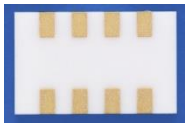
96% Alumina Circuit Board for Four 8-I/O Packages

96% Circuit Board and Assembly (continued)



1 inch

Bottom side of package



- Fired at 850°C for 20 min, with ramp rate of 40°C/min in box oven in air
- Natural cooling process after firing

Package attach

- Pads on both package bottom side and the board are coated with DuPont 5771 Au paste
- Set packages onto board with wet paste
- Dried in box oven in air at 150°C for 20 min with ramp rate 40°C/min
- Fired at 850°C for 20 min, with ramp rate of 40°C/min in box oven in air
- Natural cooling process after firing

L. Chen et al, in Proceedings ICSCRM 2011. Edited by R. Devaty, M Dudley, T P. Chow, ans P. G. Neudeck

500°C Conductive Die Attachment

Die-attach Material and Process

- In-house developed prototype die-attach paste recipe
  - Mixture of wet DuPont 9896R (Pt paste) and glass powder (SEM-COM SCB-1) with weight ratio ~ 1.5:1 (ratio is not critical)
  - SCB-1: annealing temperature was ~ 480 °C and softening temperature was above 525 °C
  - Added thinner for DuPont 9896R to decrease viscosity for die-attach
  - Glass provides with adhesion to bottom Pt surface of SiC IC die and Au pad on package
  - Pt particles provide with electrical conduction
  - Only intended for very low though current application
- Die-attach Process
  - Coat die-attach package pad with the die-attach paste
  - Place SiC IC die onto the die-attach pad with wet paste
  - Paste material wicks partially up of SiC die sides
  - Die-package-board assembly dried in box oven in air at 150°C for 20 min with ramp rate 40°C/min
  - Cured at 500°C for 2-3 hours in air with a box oven, with ramp rate of 40°C/min
  - Naturally cool down after curing

Au Wire-bonding for 500°C Operation

Wire Material and Wire Bonding Process

Wire material

- Electro-migration issue of conductors under electrical bias at high temperature
- 1 mil diameter 98% pure Au wire from K&S Wire
- Impurities in Au wire diffuse to surface at high temperature and form oxides and stay
- Surface-oxide layer slows down electro-migration process

Wire-bonding process

- Thermo-sonic ball-wedge bonding, convention bonding parameters
- Ball bond first on Pt/Au surfaces of bond pads on SiC ICs (T=150°C)
- Second wedge bond on Au thick-film pads of packages (T=150°C)

Wire annealing

- Electro-migration occurs under electrical bias and high temperature
- A gradual process
- High temperature exposure during high temperature (500°C) test of packaged device

Packaging Sequence Discussion

Packaging Sequence

1. Chip packages assembled

2. Circuit board assembly

- I/O Wire attachment
  - Au thick-film paste fired at 850°C
- Packages attachment
  - Au thick-film paste fired at 850°C

Both I/O wire and package attachment need 850 °C heating, in order to avoid unnecessary exposure of SiC IC die to such high temperature, chip level packaging (die-attach, wire-bonding) was delayed

3. Chip level packaging

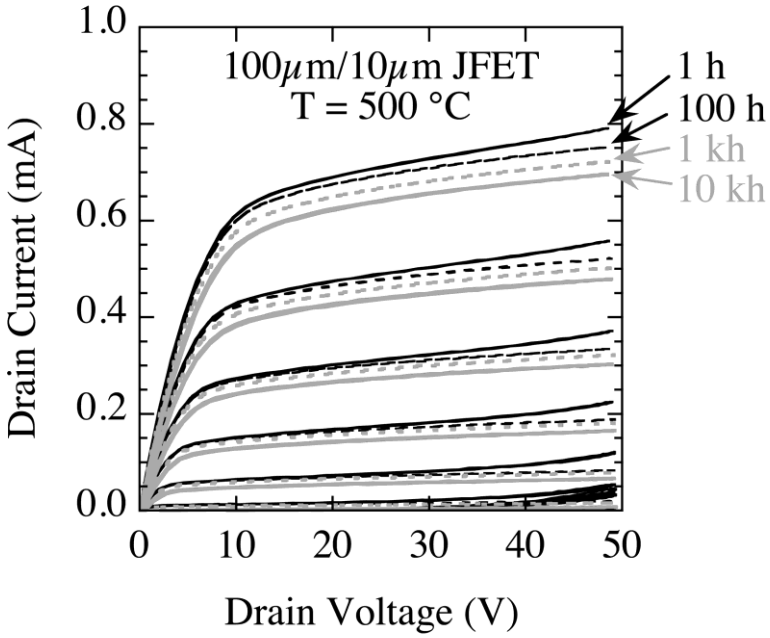
- Die-attach using home made paste: 500°C
- Au wire-bonding 150°C

This sequence order differs from packaging sequence used in mainstream IC packaging and assembly

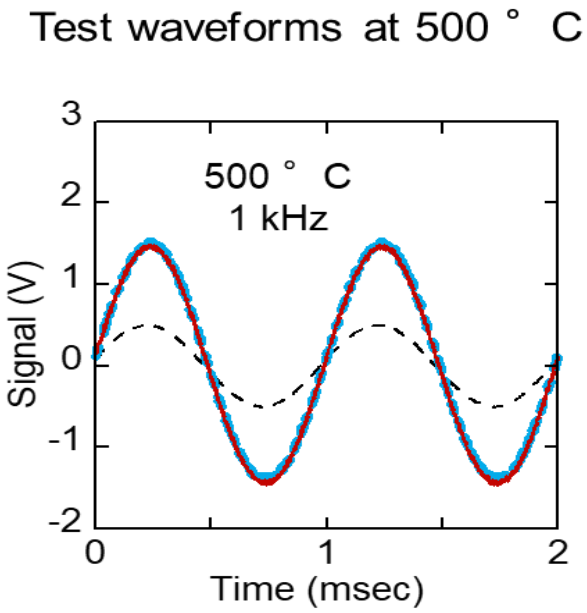
Lower processing temperatures required to adopt mainstream sequence of step of package attachment

Test Results of Packaged SiC ICs at 500°C

Test Data of Packaged SiC ICs



I-V curves of a packaged 100μm/10μm NASA Glenn 6H-SiC JFET, during the 1st, 100th, 1000th, and 10000th hour at 500 °C.



Input (dark, 1 kHz) and output signal waveforms of a packaged SiC differential amplifier at 500 °C at 1 hour (blue) and 2000 hours (red).

P. G. Neudeck et al, phys. stat. sol. (a), 206: 2329–2345.

P. G. Neudeck et al, IEEE Electron Device Letter, Vol.29, Iss. 5, May 2008

A 96% Alumina based Packaging System for 500°C Test of SiC Integrated Circuits

3:00-3:45 PM April 28, 2021

Summary

- A 96% alumina and Au thick-film metallization based prototype packaging system for 500°C test of SiC ICs reviewed in detail
- This packaging system includes chip-level package with 8 I/Os and a circuit board for four packages
  - Compatible I/O wire attachment, package attachment, die-attach, and wire-bonding developed in parallel
  - Die attach developed for 500°C SiC ICs with Pt metallization on backside, and Pt or Au capped wire bond pads on active side
- The maximum process temperature IC die exposed limited to 500 °C
- Various packaged SiC devices and ICs successfully long-term tested, up to 10,000 hours in 500 °C in air ambient

These technologies laid the base foundation for subsequent more advanced technologies

Further Development

- Package assembly labor intensive, not industry compatible
  - Co-fired material system with multi-layer capability developed
- Package attached onto circuit board before chip level packaging
  - Package attachment temperature 850°C
  - Avoid SiC IC die exposure to 850°C
  - Package / component attachment technology at lower temperature needed
  - Conventional packaging sequence from chip-level to board assembly can be implemented
  - Repairable package/component attachment technology to be pursued
- More conductive more stable die-attach needed

Processing details of the above more-advanced technologies to be reported soon

Thank You Very Much for Your Attention!

Acknowledgements

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