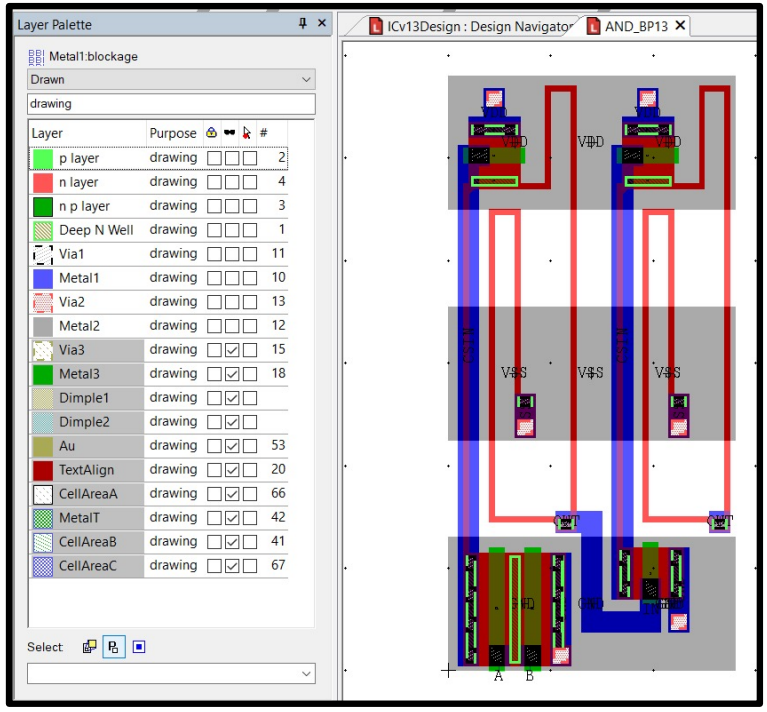
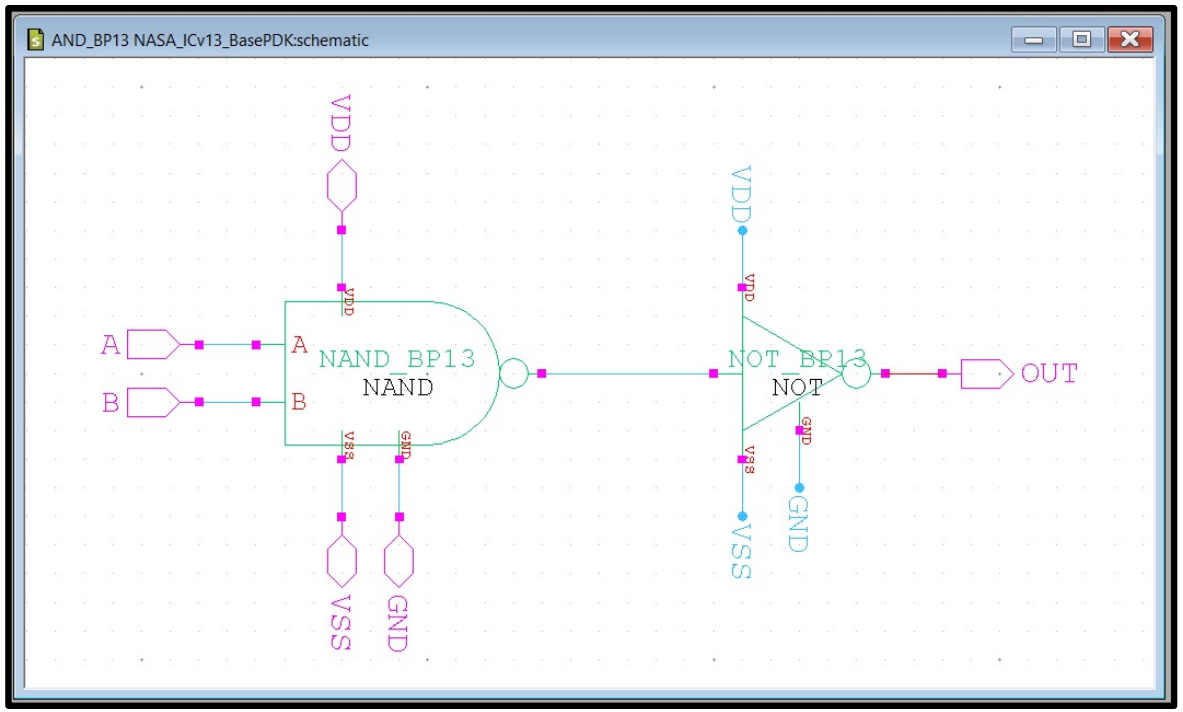
Graphical Primer of NASA Glenn SiC JFET Integrated Circuit (IC) Generation 13 Layout

How to layout 500 °C durable integrated circuit cells for fabrication by NASA Glenn





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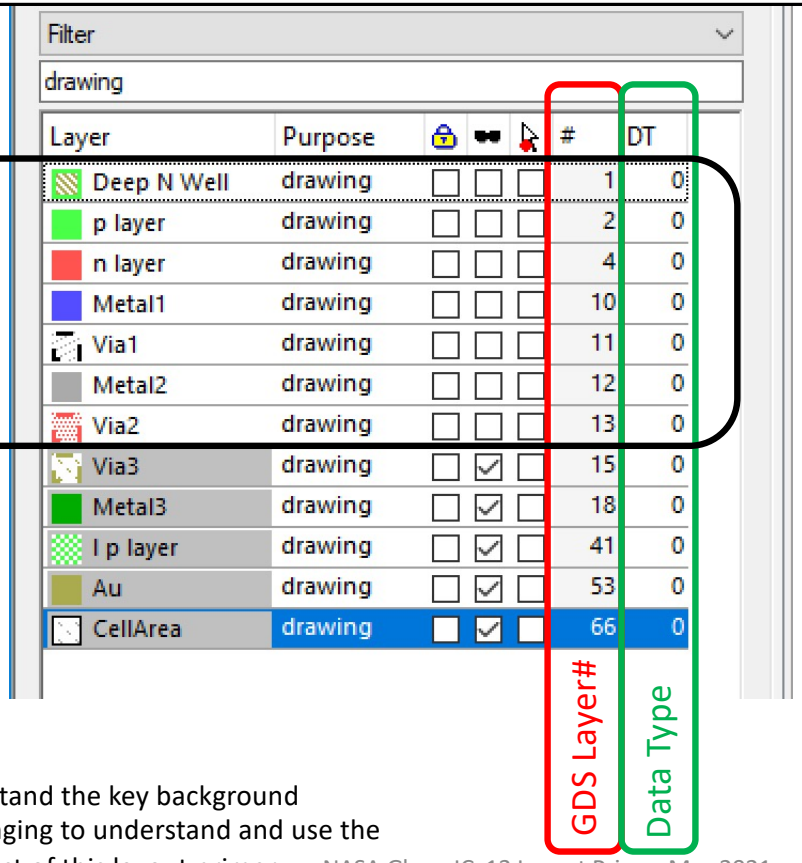
NASA Glenn SiC JFET IC Generation 13
7 Drawn Layers Needed to Define Circuit Mask Layout

Key Background Info: See https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170001674.pdf slides 20-32 for a series of cross-sections illustrating the use of these 7 layers to build SiC JFETs, resistors, and integrated circuits [1].

All circuits (transistors and resistors) are implemented/defined in these 7 drawn layers.

Other layers in grey are for chip bond pads that NASA designs and implements.



The NASA SiC JFET IC fabrication process mask order [1]:
1. "p layer" defines JFET p+ gate mesa.
2. "n layer" defines JFET and resistor n mesa channel.
3. "Deep N Well" defines n+ contact implant.
4. "Via1" defines where Metal1 contacts the SiC devices.
5. "Metal1" defines 1st layer interconnect pattern.
6. "Via2" defines Metal1 to Metal2 connections.
7. "Metal2" defines 2nd layer interconnect pattern.

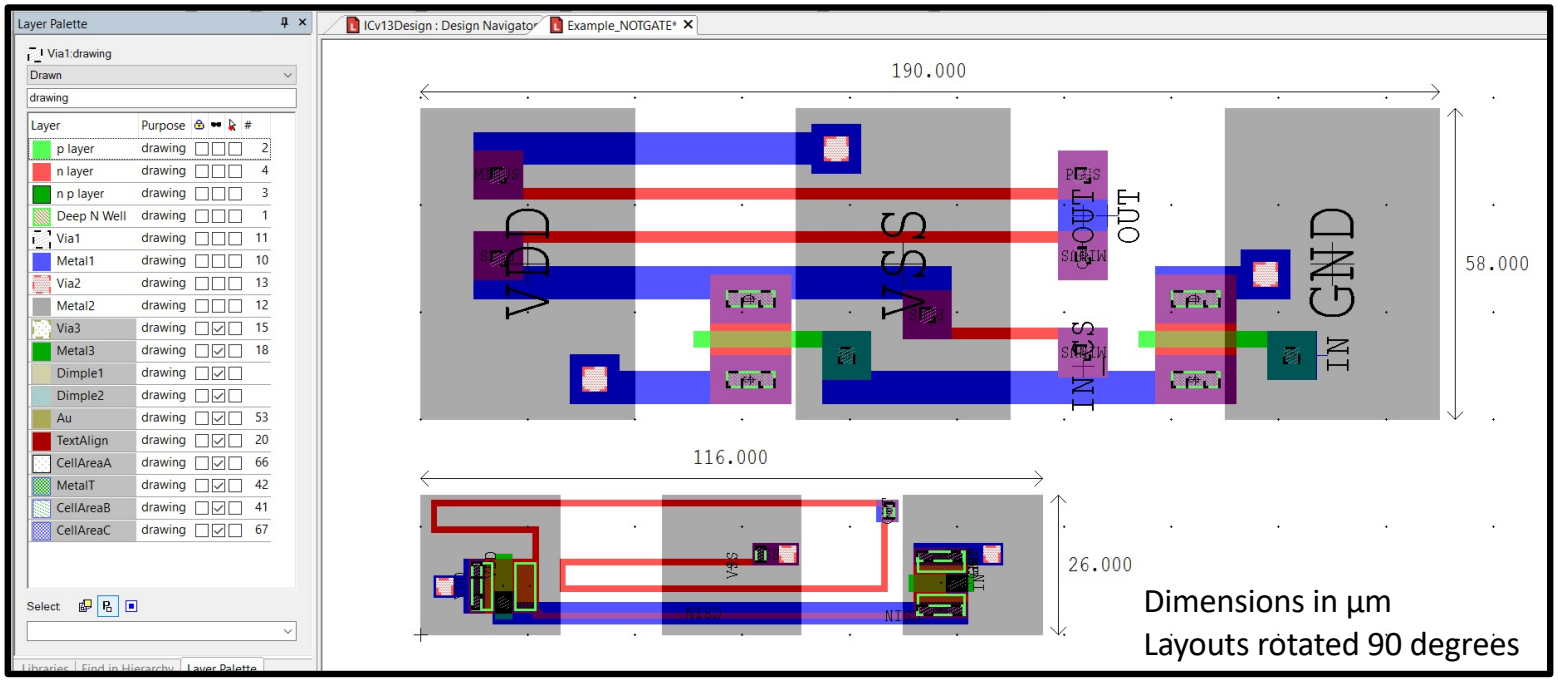
So long as layout geometries and layers described in this document are followed, NASA Glenn can import a GDS file of your design into its master IC mask design for fabrication[2].

[1] If you do not read and understand the key background information, it may prove challenging to understand and use the information that follows in the rest of this layout primer.

[2] Under mutually agreed Space Act Agreement.

NASA Glenn SiC JFET IC

Size Comparison of Generation 12 (top) and Generation 13 (bottom) of “Base Power” NOT Logic Gate Layouts



Important Notice: Generation 13 layout rules outlined in this document are enabled by anticipated switch to stepper-based lithography executed at non-NASA SiC fabrication foundry. If NASA does not receive sufficient funding for moving the 7 masks to stepper-based SiC fabrication foundry, Generation 12 layout rules (posted online since April 2019) will be used in the next fabrication run instead of the Generation 13 rules described here in this document.

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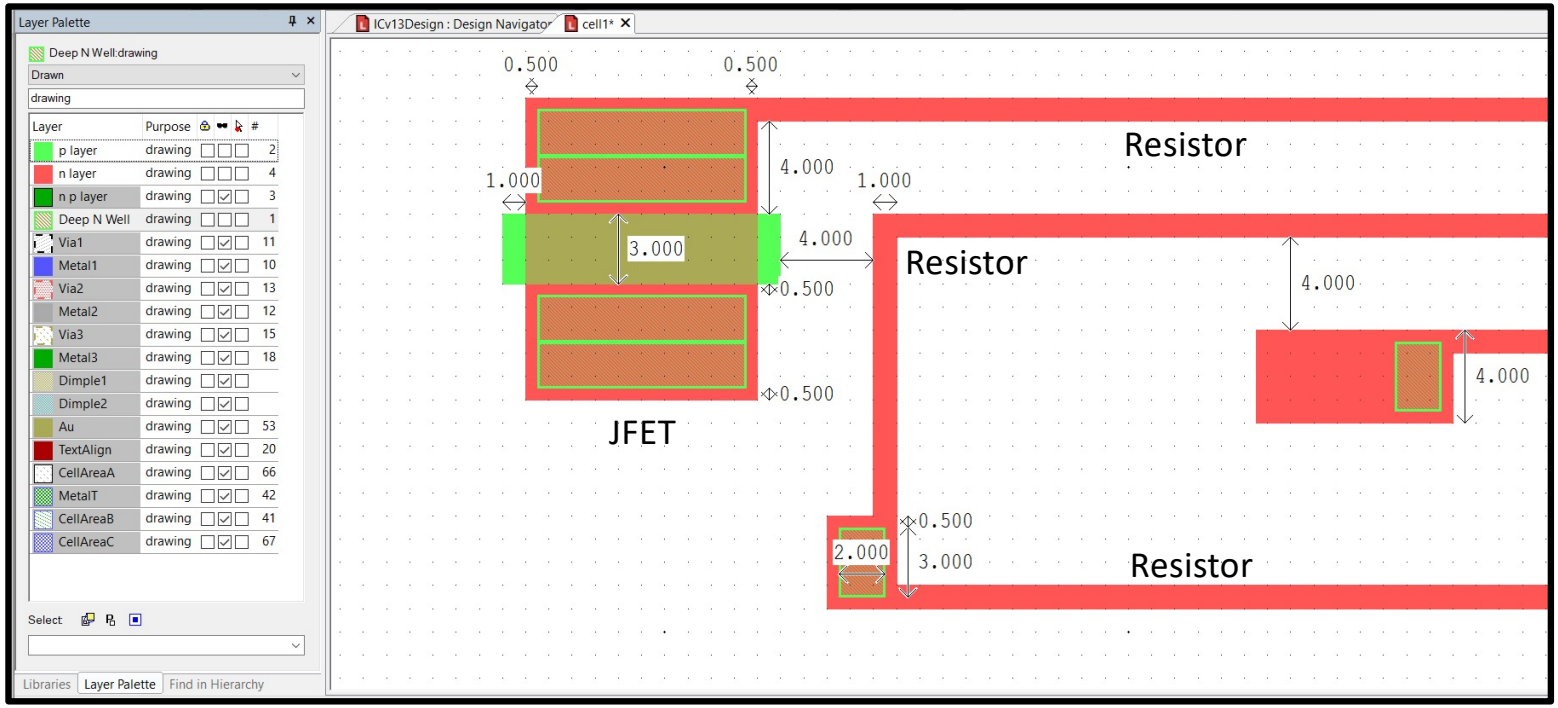
Illustration of p+ Gate Mesa (p layer), N-Channel Mesa (n layer), N+ Implant (Deep N Well) Layout Rules (Dimensions in µm)



Additional Mesa Layout Rules.

1. JFET gate lengths longer than 3 µm are permitted, unlimited JFET gate width.
2. Minimum resistor width of 1 µm, up to 300 squares. S-Shape, C-Shape, U-shape, and serpentine features are permitted.
3. Joining of multiple device n-mesa regions permitted.
4. DO NOT join multiple p-mesa regions of separate JFETs.
5. Minimum N+ Implant size is 2 µm by 3 µm, at least 0.5 µm inside n mesa periphery.

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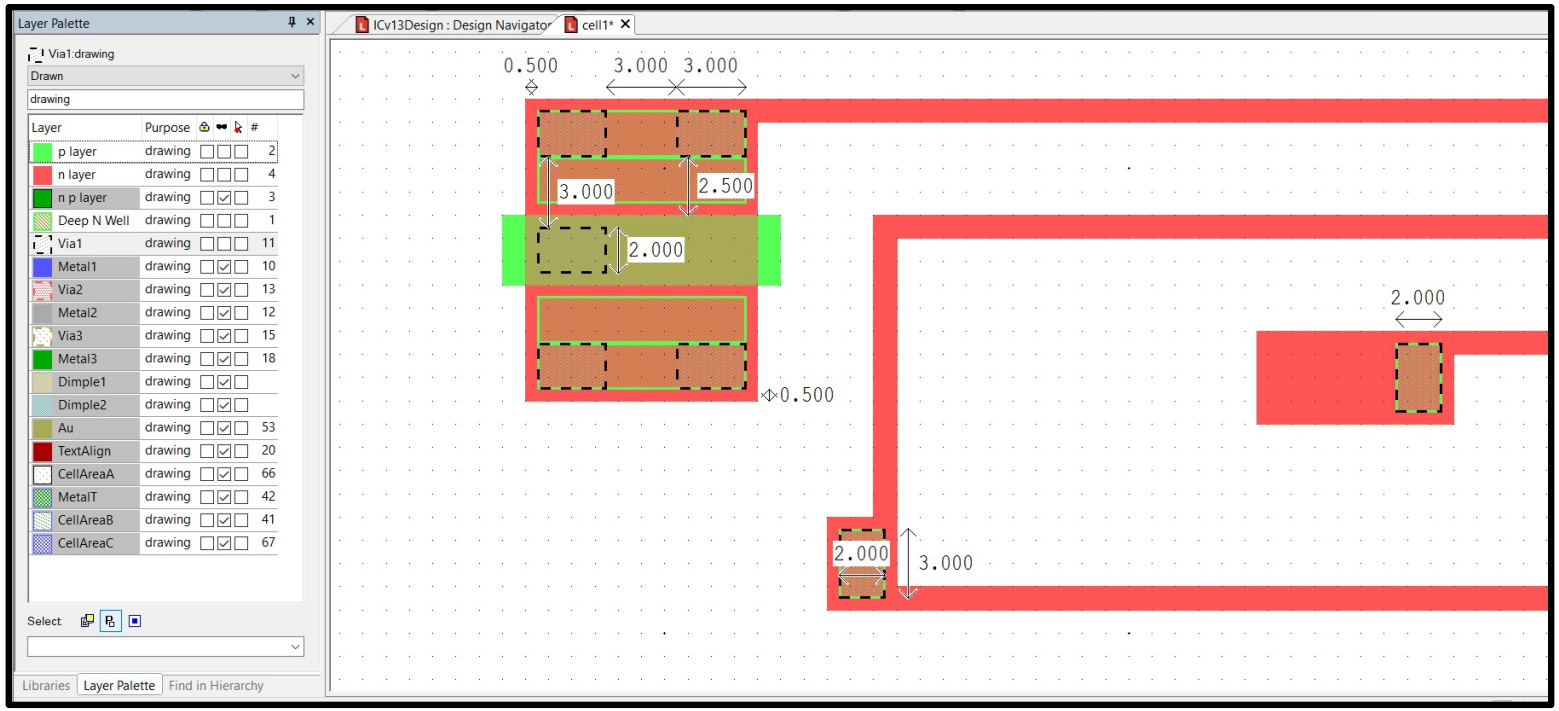
Illustration of **Via1** Layout (Dimensions in µm)



Via1 features must:

1. Reside on either an n-mesa or p-mesa and are intended to form ohmic contact to the SiC.
2. Be 2µm x 3 µm in dimension and residing in flat area without any underlying n mesa or p mesa edge topology.
3. Reside at least 0.5 µm from n-mesa or p-mesa edge if enclosed by the mesa.
4. Reside at least 2.5 µm from p-mesa edge if not enclosed by the p-mesa.
5. Reside at least 3 µm from any adjacent **Via1** feature.

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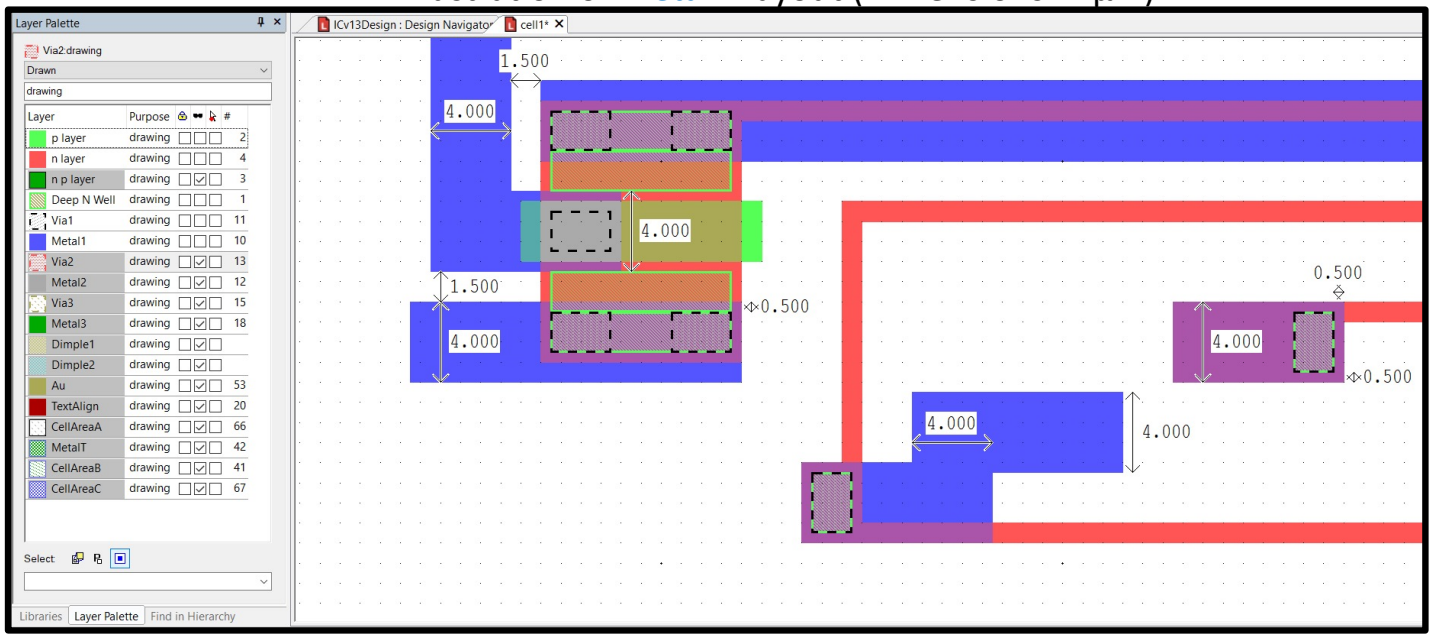
Illustration of Metal1 Layout (Dimensions in µm)



Metal1 Layout:

1. Surround all **Via1** features by 0.5 µm of Metal1.
2. 1.5 µm minimum Metal1 to Metal1 Isolation spacing.
3. 4 µm minimum Metal1 feature width.
4. 2 mm maximum length of Metal1 trace.
5. Do not route Metal1 traces that traverse separated n layer mesa features that are supposed to be electrically isolated from each other.
   - Such features have potential to create undesired parasitic inversion channel MOSFET (especially for positive signal bias).
     - Exception: Can traverse in cases where Metal1 and resistor traces are always negative bias with respect to GND.
6. Parasitic resistance of Metal1 is roughly 5 ohms per square.

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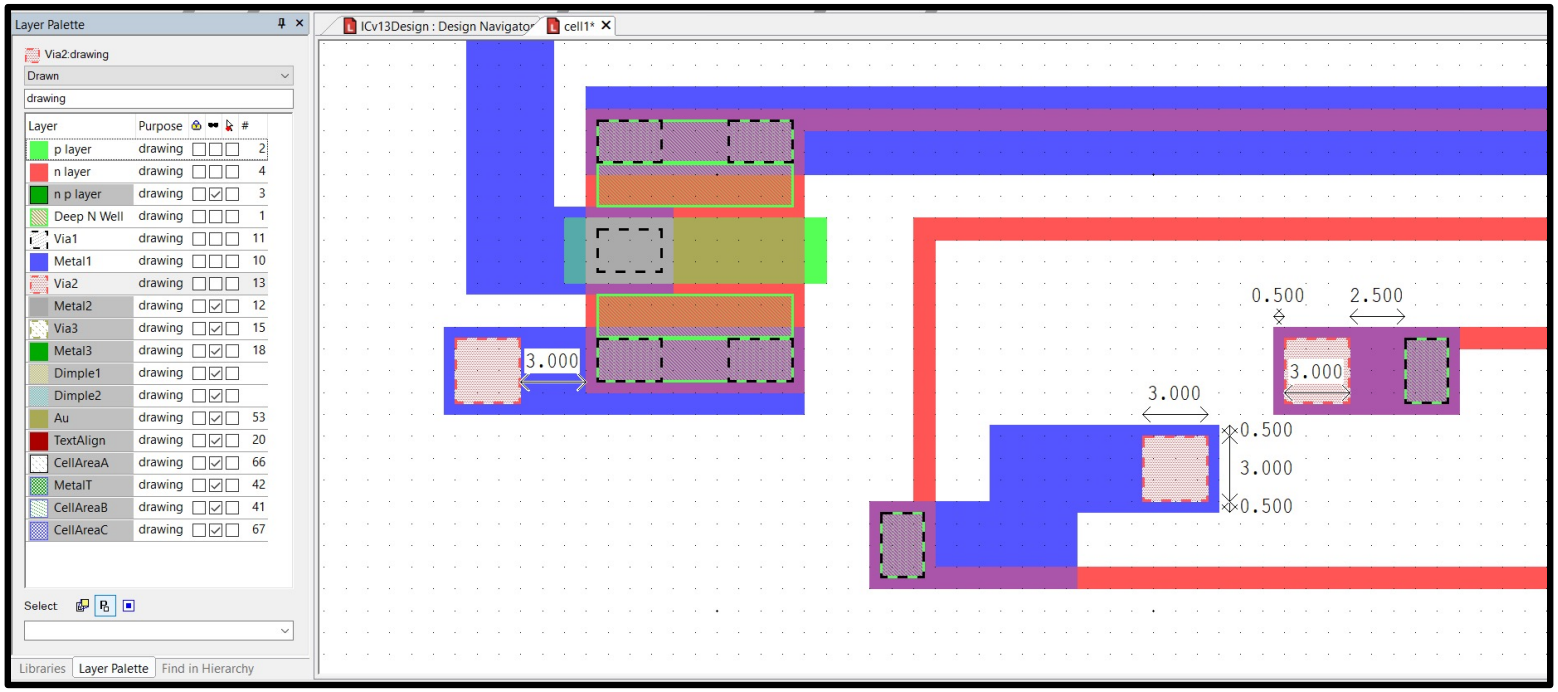
Illustration of Via2 Layout (Dimensions in µm)



Via2 Layout:

1. Surround all Via2 features by 0.5 µm of Metal1
2. All Via2 features are 3 µm x 3 µm.
3. All **Via2 features must reside on flat SiC topography.**
   - If Via 2 resides in flat field region, at least 3.0 µm from the edge of adjacent n-mesa or p-mesa feature.
   - If Via 2 resides inside flat area of n-mesa, at least 2.5 µm from edge of adjacent **Via 1** or p-mesa feature.
4. Each Via2 is < 5 ohm resistance.

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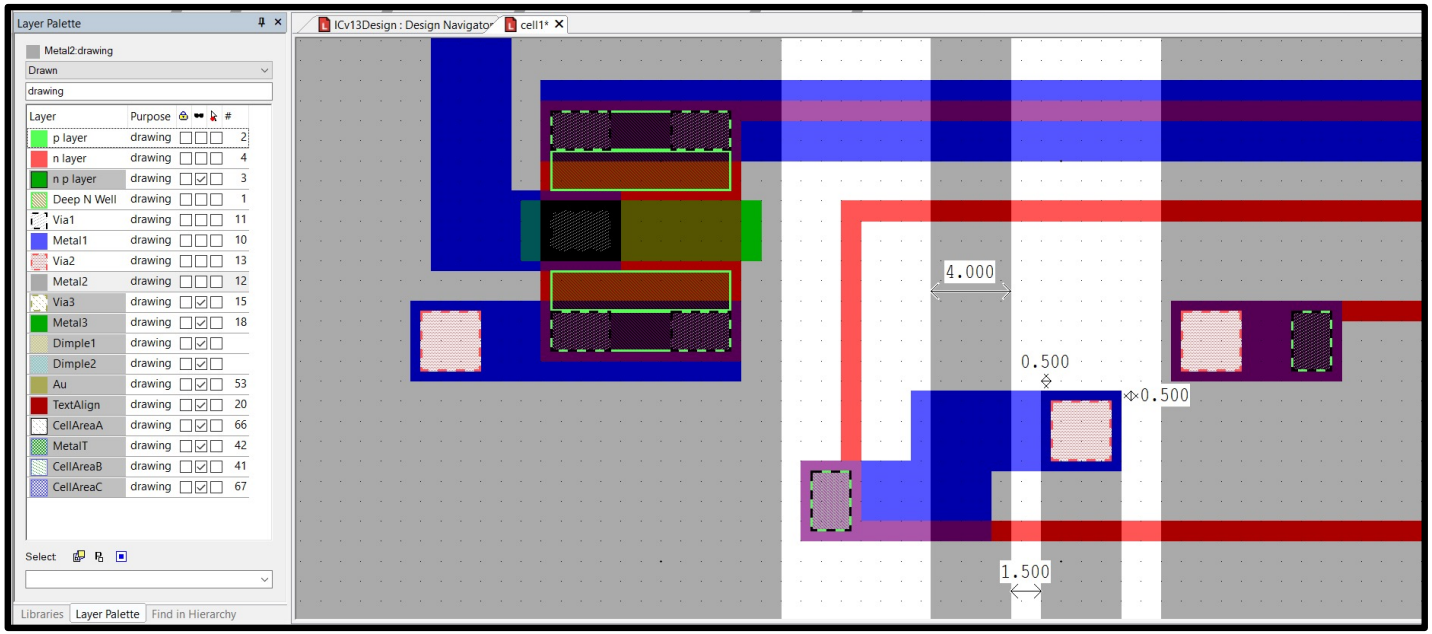
Illustration of Metal2 Layout (Dimensions in µm)



Metal2 Layout:

1. Surround all Via2 features by 0.5 µm of Metal2
2. 1.5 µm minimum Metal2 to Metal2 Isolation spacing.
3. 4 µm minimum Metal2 feature width.
4. 2 mm maximum length of Metal2 trace.
5. OK to traverse adjacent underlying n layer mesa features with Metal2 traces.
6. Parasitic resistance of Metal2 is roughly 5 ohms per square.

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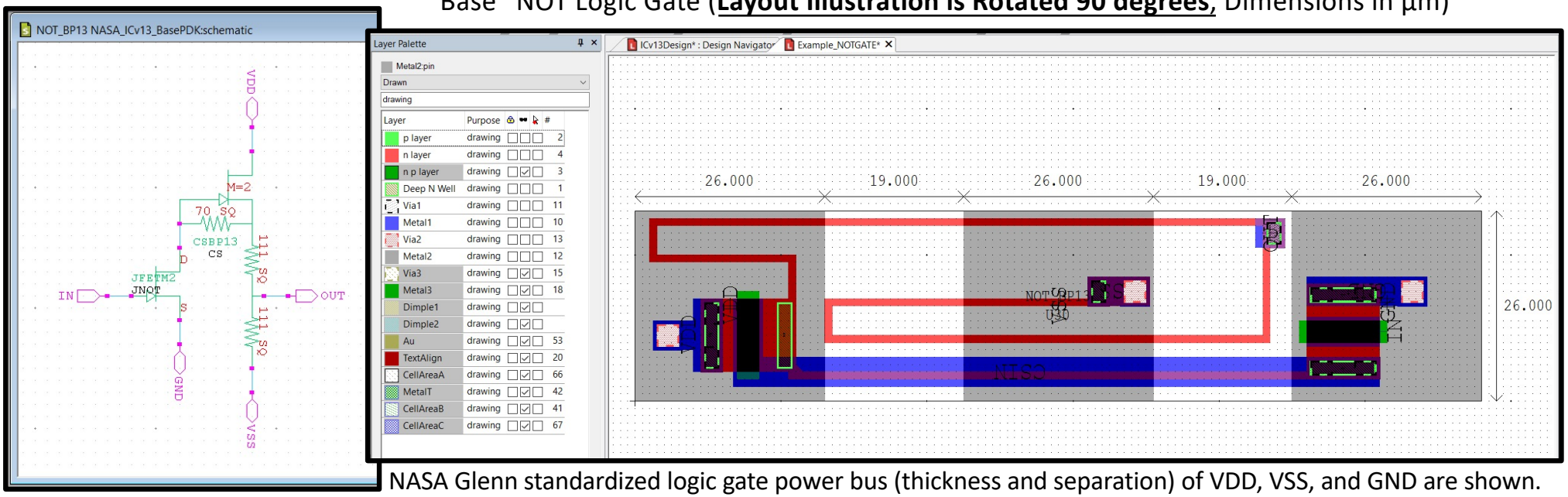
"Base" NOT Logic Gate (**Layout Illustration is Rotated 90 degrees**, Dimensions in µm)

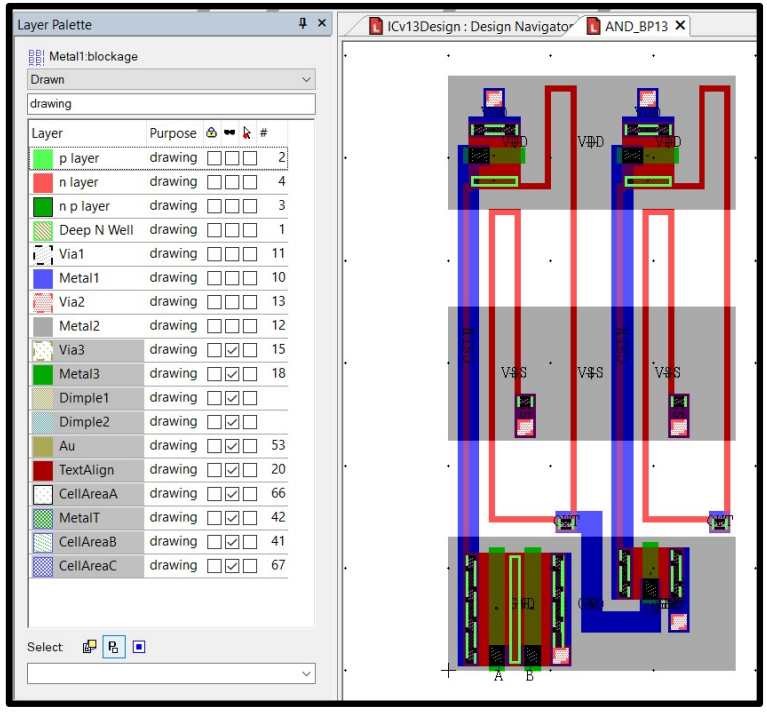


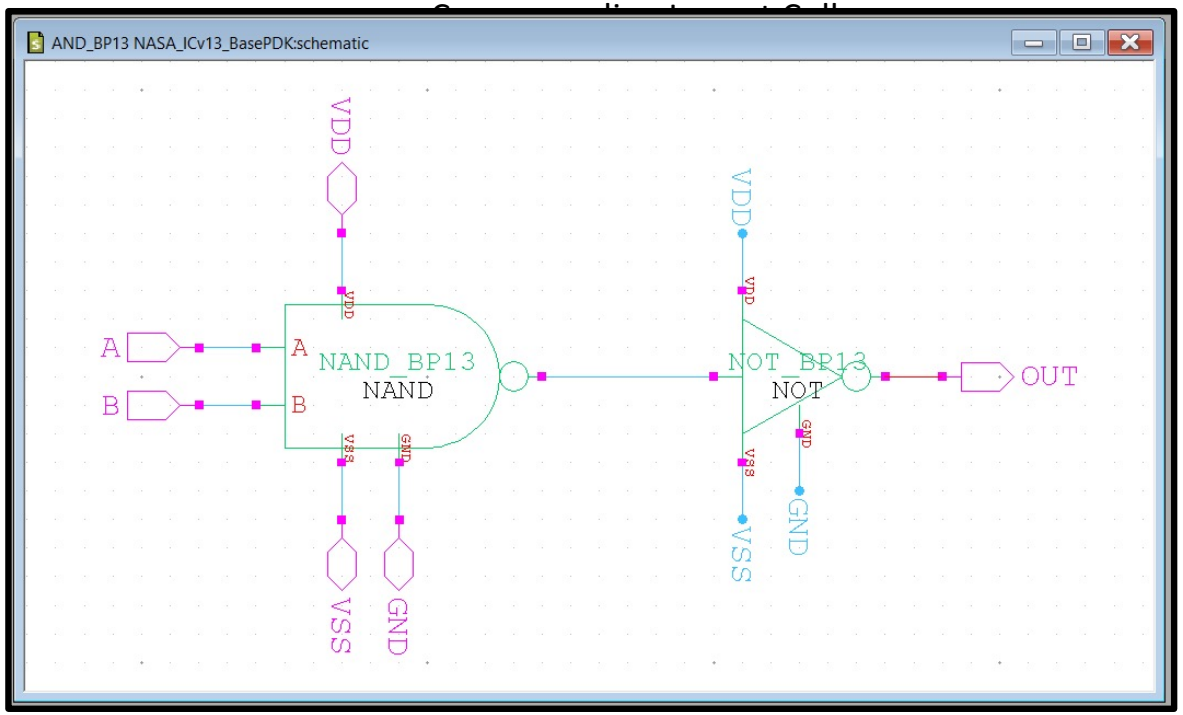
NASA Glenn standardized logic gate power bus (thickness and separation) of VDD, VSS, and GND are shown.

- Use of labeled electrical connection ports (e.g., "VDD", "IN", etc. shown above) is not required.
  - Labeled electrical connection ports reside on Metal1:**pin** and Metal2:**pin** separate layers (Data Type 5).
  - Ports can assist with documentation and verification of layouts vs. circuit schematics.

Corresponding schematic circuit diagram of NASA Glenn "Base" NOT gate, including corresponding ports.

NASA Glenn SiC JFET IC Generation 13
Example AND Logic Gate (constructed using NAND + NOT base cells)





In NASA Glenn Layouts:
Metal1 traces predominantly run along vertical direction.
Metal2 traces predominantly run along horizonal direction.

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Illustration of NASA Glenn Multiple-Finger JFET Layout

Features of Mult-Finger JFET Layout:

1. Via 2 resides on top of (and is 0.5µm surrounded by) flat Metal1 and flat n layer mesa without **Via1**.
   - Deep N Well source/drain implant produces no surface topography, so it is allowed to extend underneath Via2.
   - No **Via1** feature exists underneath or within 2.5µm of Via2 feature.
2. In this 4-gate-finger example, electrical connection to Multi-Finger JFET Drain and Source is made in Metal2.
3. In this 4-gate-finger example, electrical connection of the multiple adjacent p layer gate fingers is made in Metal1.
   - Metal 2 and Via 2 could also be used to connect gate fingers IF underlying p layer made locally wider to meet Via2 flat topography rule.

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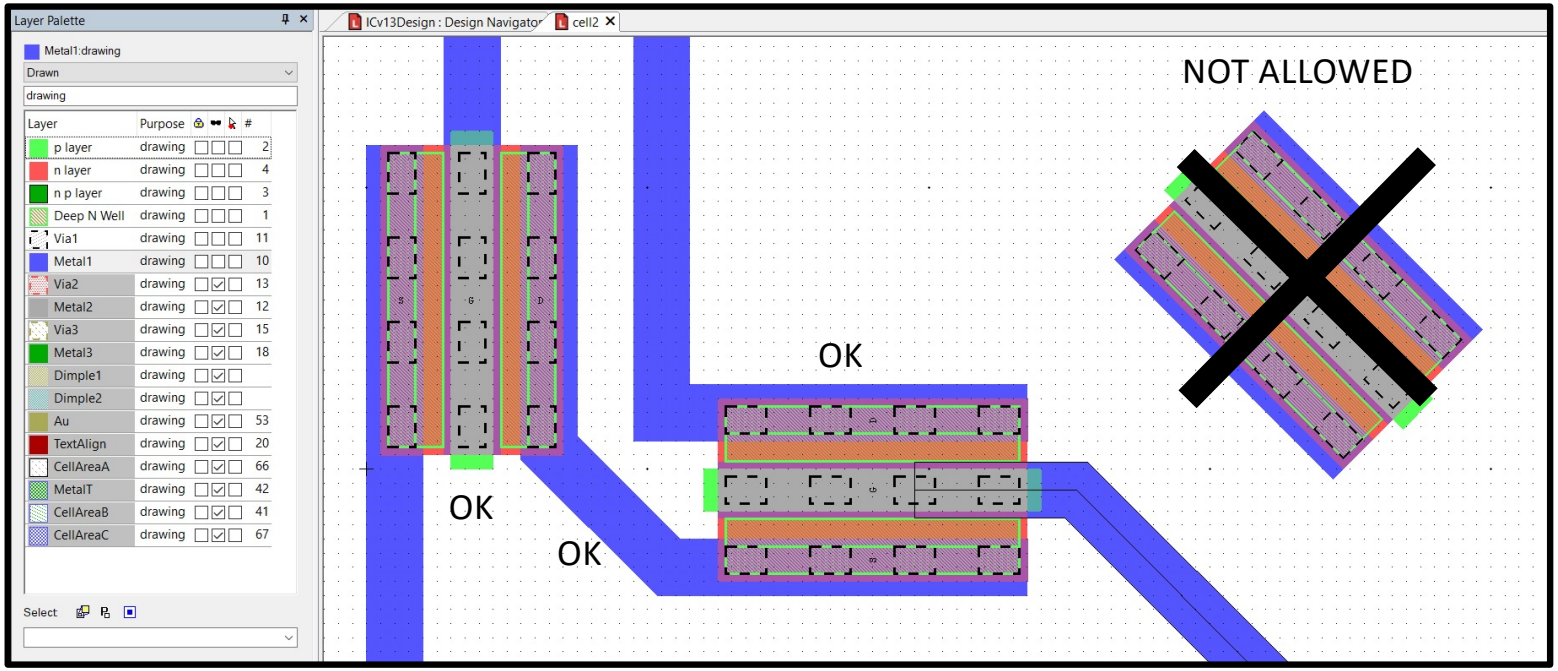
Device Orientation



Use vertical and horizontal 90° JFET and via orientations.

DO NOT use JFETs or vias oriented at non-90° angles.

No restriction on Metal1 and Metal2 trace orientations.

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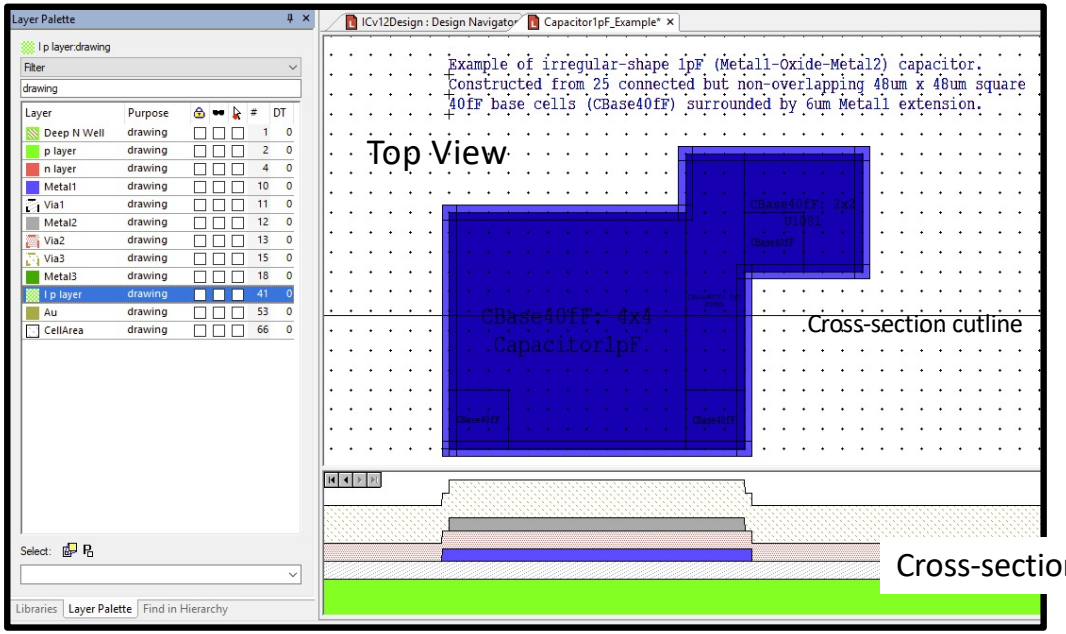
Illustration of NASA Glenn Metal1 to Metal2 Capacitor Layout



Capacitor Layout (unchanged from Generation 12)

"Unit cell" (CBase40fF) consists of 48µm x 48µm square of Metal2 residing on top of 48µm x 48µm square of Metal 1

- Capacitance of a unit cell is 40 fF.

Repeat (adjacently connect) 48µm x 48µm square unit cells to build larger capacitors of desired shape.

- Larger capacitor can be any overall shape so long as it is comprised of adjacently connected unit cells.
- **Capacitor peripheries must be surrounded by a 6 um extension "ring" of only Metal1.**

Maximum size is 2 mm x 2 mm (per 2 mm Metal1 and Metal2 length rules on slides 5 and 7)

NASA Glenn SiC JFET IC Generation 13 Chip Size and Bond Pad Configuration

NASA Glenn will place the GDS layout file you send of your circuit layout into its standard IC Version 13 chip frame cell.

Your integrated circuit cell (including power bus traces) must fit within less than a square 4 mm x 4 mm area.

The NASA standard chip frame provides for an even distribution of at least 72 high-temperature durable bond pads.

- Bond pads are evenly distributed around the chip frame cell periphery, NO bond pads permitted in chip middle.
- Bond pads are designed to be compatible with either gold wire bonding or flip chip.
- Each high-temperature bond pad has a parasitic electrical series resistance of roughly 100 ohms.
  - Because of this series resistance, larger-current (power bus) connections should use multiple bond pads.
- **Route your top-level cell signals and power to the cell periphery, NASA will route from there to chip bond pads.**
  - Metal1 is preferred for larger-current (power bus) connections to bond pads.

NASA will carve (add) stress-management hole patterns into selected larger Metal1 and Metal2 traces and capacitors.

- Stress-management patterns will only be added to flat metal areas larger than 30 µm by 30 µm in your layout.

Key Online Technical References

Yearlong 500 °C Operational Demonstration of Up-Scaled 4H-SiC JFET Integrated Circuits (2018):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180003391.pdf
Presentation: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20190001885.pdf

Processing and Characterization of Thousand-Hour 500 °C Durable 4H-SiC JFET Integrated Circuits (2016):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014879.pdf
Presentation: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170001674.pdf

First-Order SPICE Modeling of Extreme-Temperature 4H-SiC JFET Integrated Circuits (2016):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014886.pdf
Presentation: https://sic.grc.nasa.gov/files/HiTEC2016-NeudeckV1A.pdf

Experimental and Theoretical Study of 4H-SiC JFET Threshold Voltage Body Bias Effect from 25 °C to 500 °C (2016):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160005307.pdf

Inclusion of Body Bias Effect in SPICE Modeling of 4H-SiC Integrated Circuit Resistors (2018):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180000657.pdf
Poster Presentation: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170009460.pdf