

Technical Primer on Design and SPICE Modeling of Circuits for NASA Glenn SiC JFET IC Generation 13 Prototype Wafer Run Part 1: SiC JFET Behavior and SPICE Modeling

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Outline

Goal: Enable anyone to SPICE-model and design 500 °C durable integrated circuits for their intended application.

IC Technology Overview:

- SiC n-channel JFETs (this document)
- SiC n-channel Resistors

Part 1: SiC JFET Behavior and SPICE Modeling

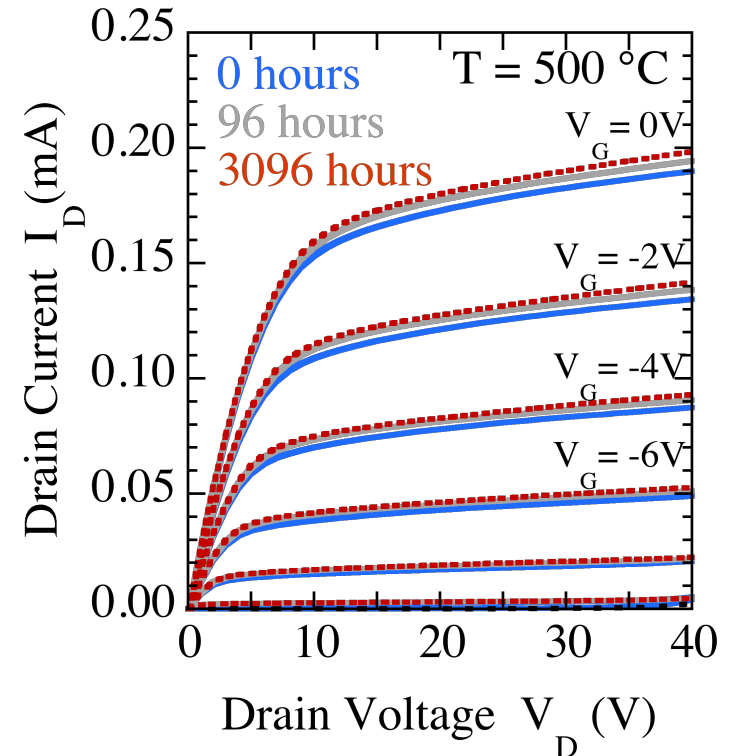
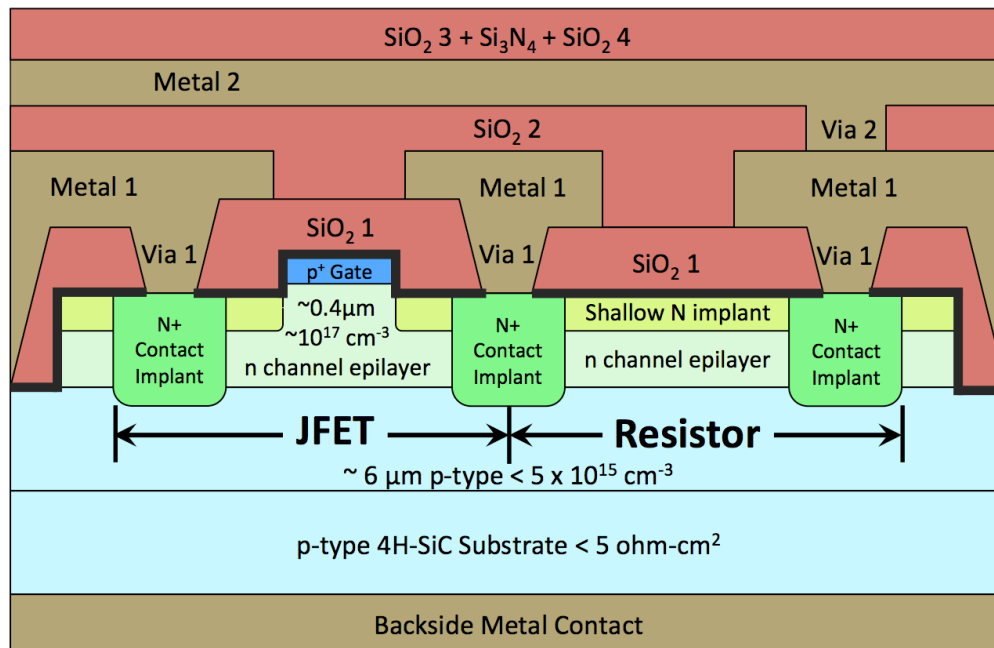
Part 2: SiC Resistor Behavior and SPICE Modeling

NOTE: Background information in web links provided in these presentations are key to technology understanding.

Device Approach

Most applications require long-term circuit operation.

SiC n-JFETs and n-resistors offer the highest durability and stability for long-term circuit operation at $T \geq 500 \text{ } ^\circ\text{C}$.



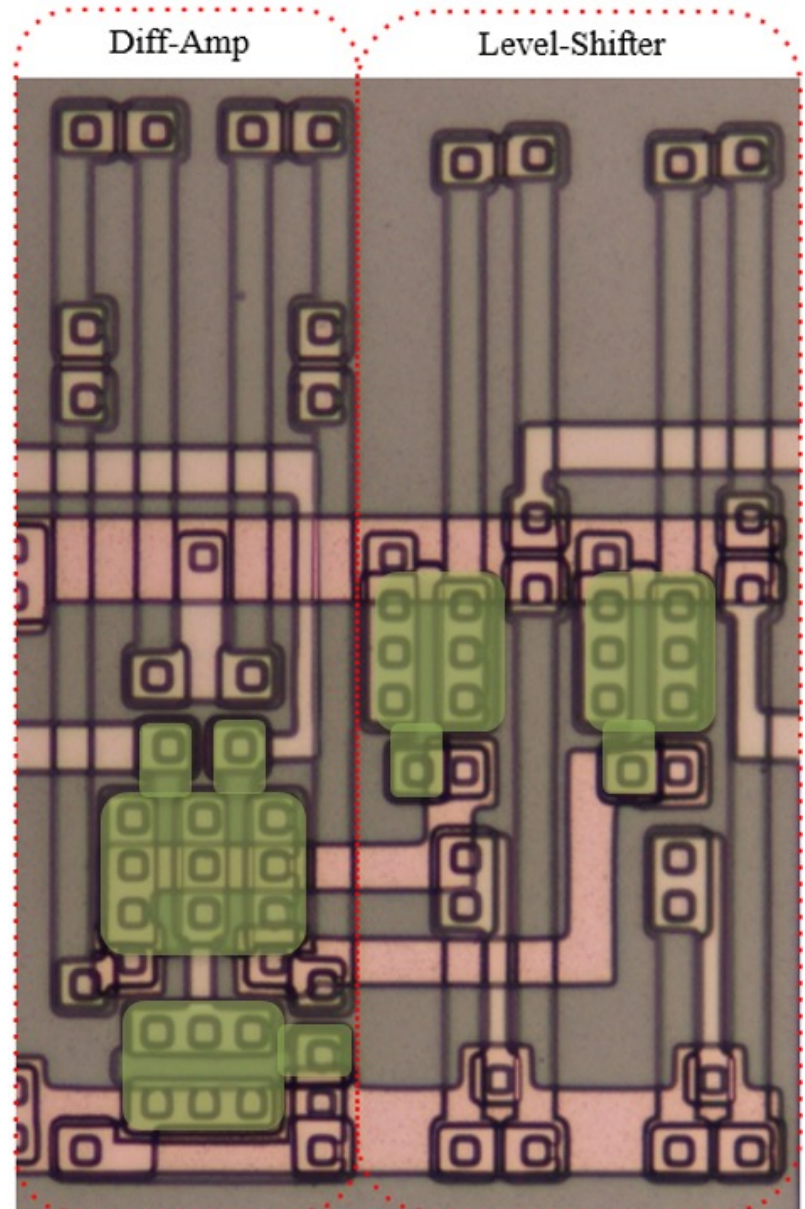
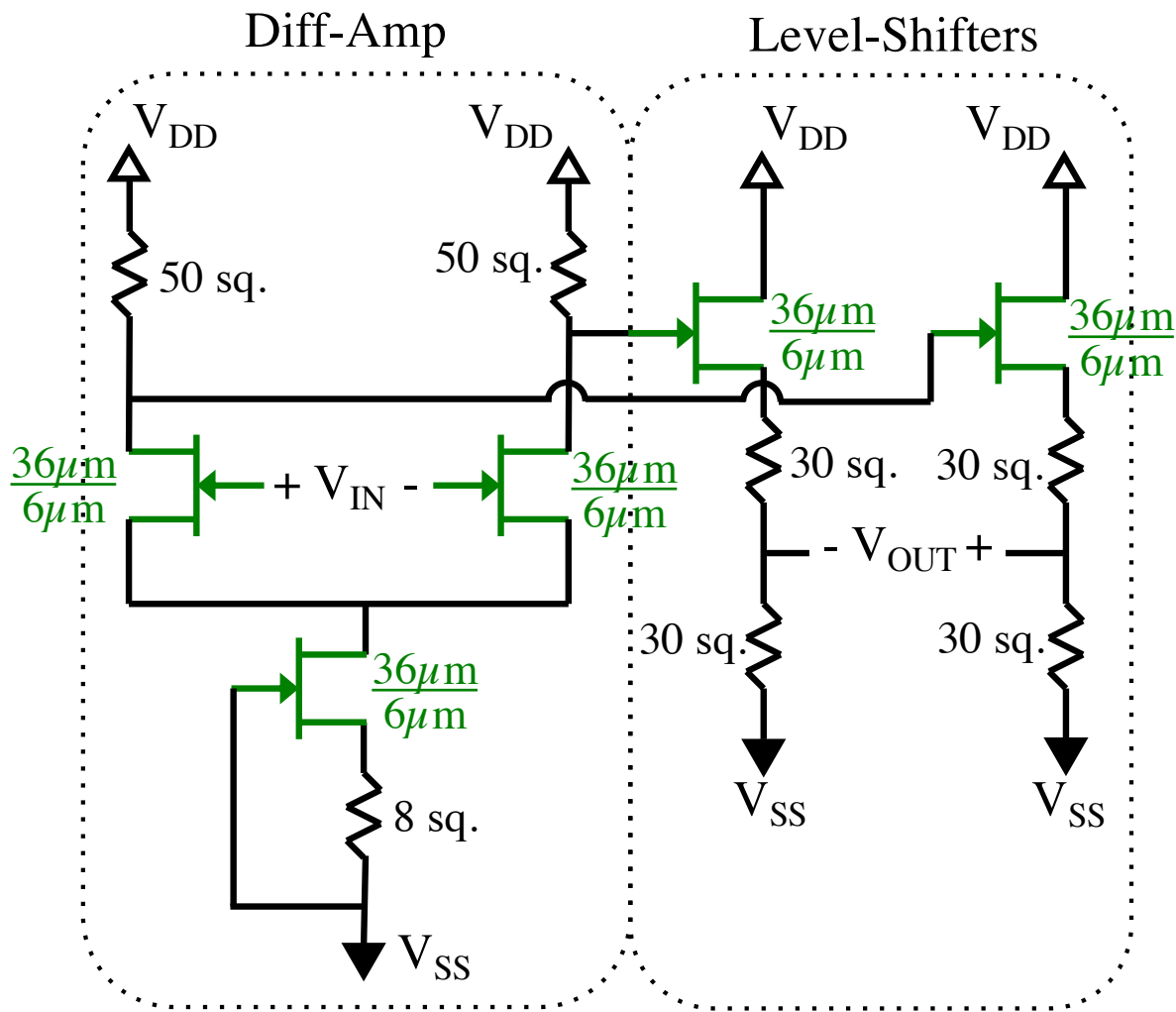
Other device structures and materials have yet to demonstrate 1000+ hours of 500 °C stable electrical operation.

See: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180003391.pdf>

Circuit Approach

See: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014879.pdf>

All integrated circuits in this project are comprised of interconnected 4H-SiC n-JFET's and 4H-SiC n-resistors.

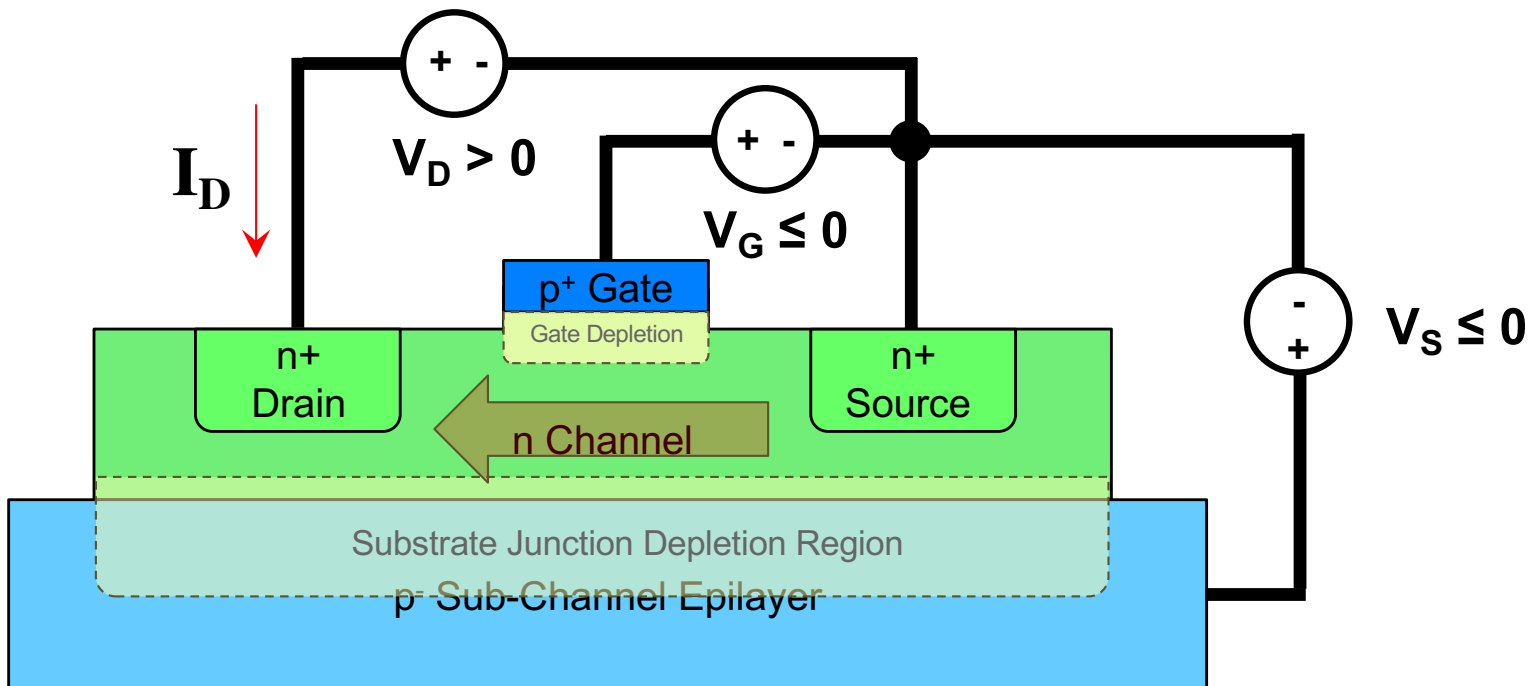


SiC JFET Behavior

The following 4 slides summarize the SiC JFET device structure and substantial temperature, wafer position, and substrate body bias dependence of JFET electrical properties observed in past NASA Glenn IC wafer runs.

The substantial wafer position, temperature, and substrate body bias dependencies must be understood and taken into account when conducting design and SPICE modeling of circuits to be implemented in the NASA Glenn SiC JFET IC Version 12 wafer run.

N-Channel JFET Bias Limitations



N-channel electron current flow from Source to Drain is modulated by Gate voltage V_G .

Forward bias of gate pn junction and substrate pn junction is to be avoided.

- Keeps desired signal currents confined/isolated to n-channel.

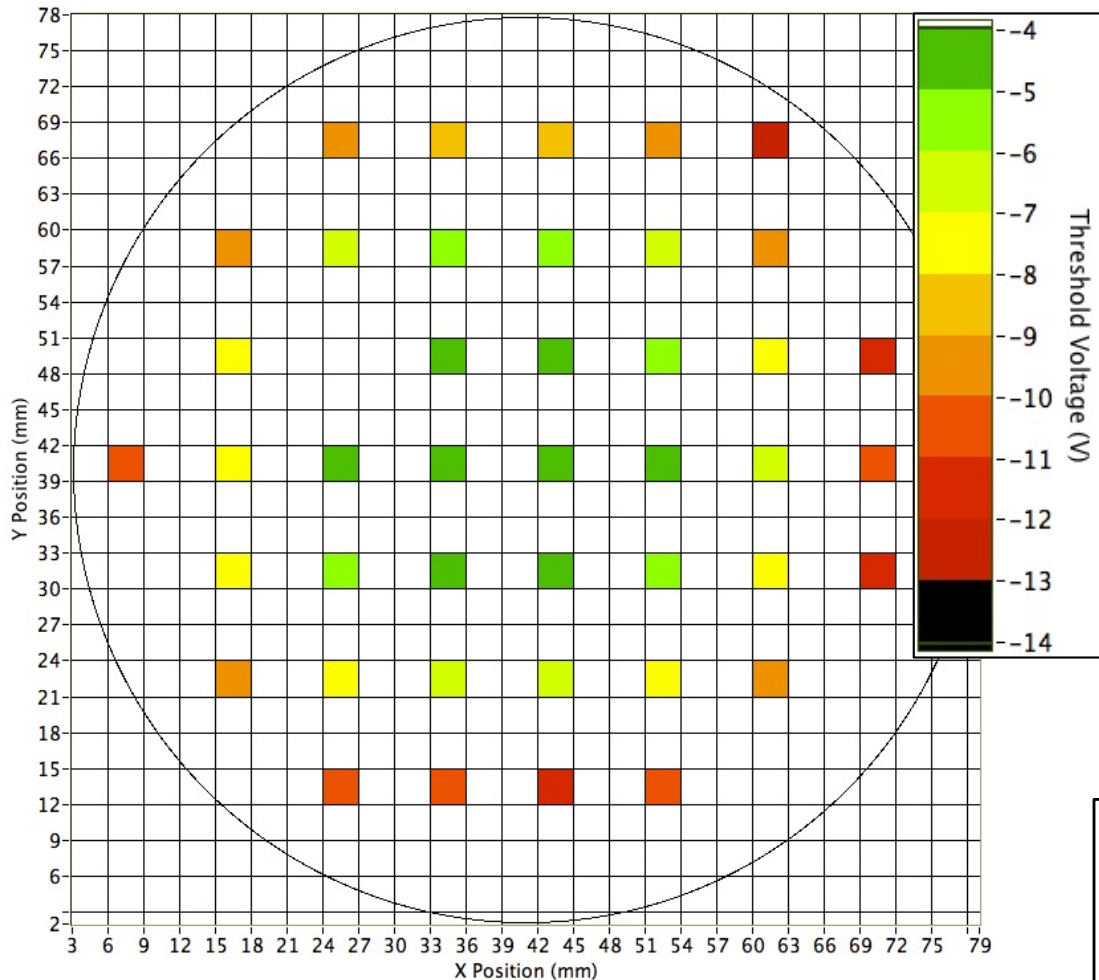
JFETs are “normally ON” - n-channel is “on” to current flow at $V_G = 0$ V.

- JFET “turn-off” requires application of $V_G \leq V_T$ “Threshold Voltage” < 0 V.
- N-channel epilayer control is not yet sufficient for “normally OFF” JFET approach
- $V_S < 0$ is needed to guarantee substrate pn junction reversed bias in all circuits.
 - Impacts JFET current-voltage characteristics through “body bias effect”
 - See: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160005307.pdf>

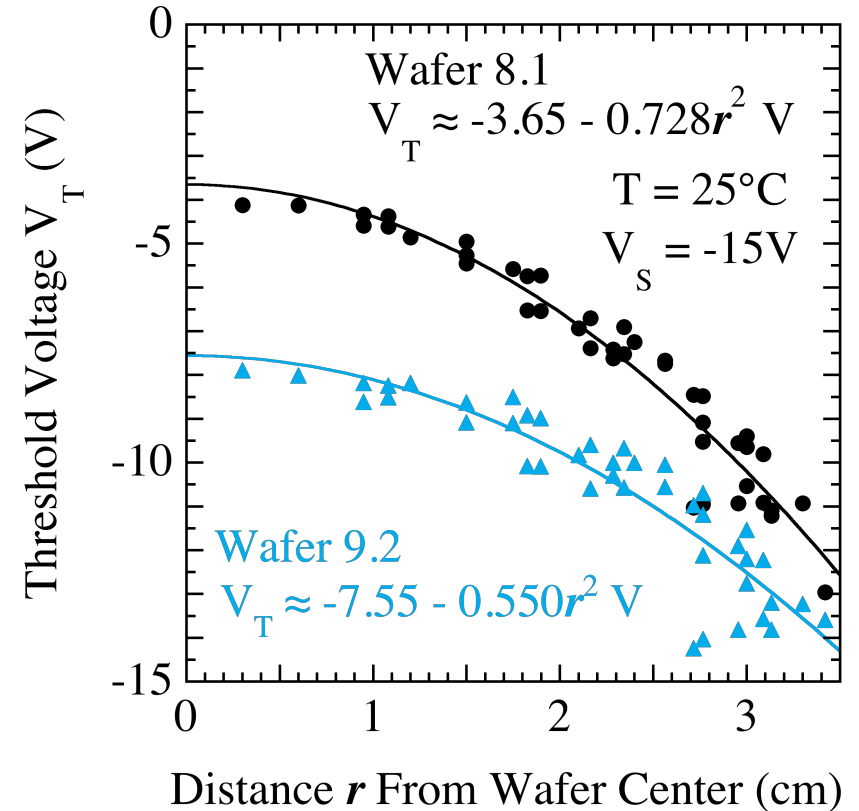
Substantial SiC JFET Threshold (V_T) Non-Uniformity

See more at: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160005307.pdf>

Wafer Probe Map of Wafer 8.1 JFET V_T
 $T = 25^\circ \text{C}$, $V_D = 20\text{V}$, $V_S = -15\text{V}$
(76 mm diameter wafer)

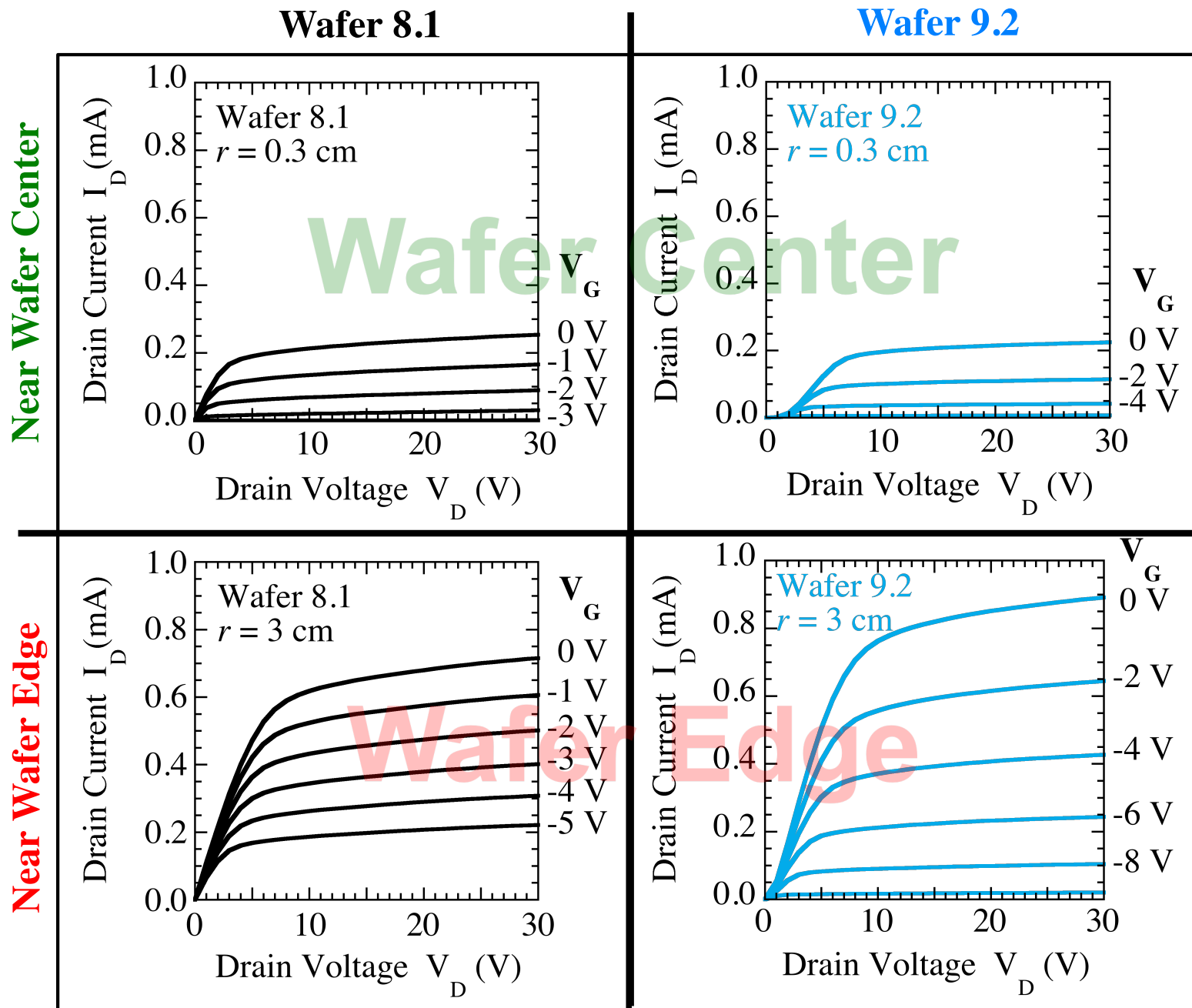


Plot of Measured JFET V_T
vs. Radial Distance (r)
from Wafer Center

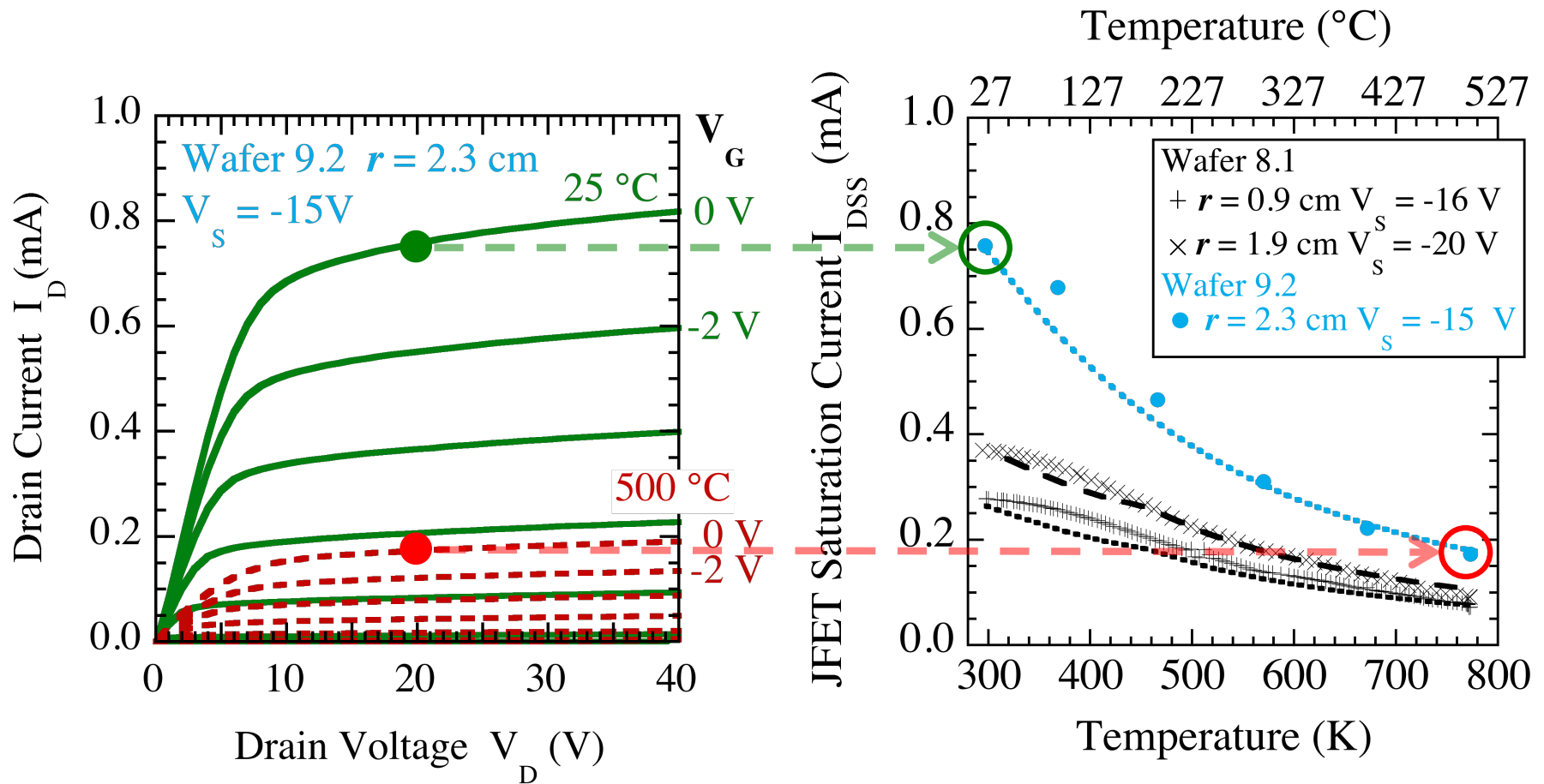


Positional variation of JFET V_T is radial and due to non-uniformity in as-grown epilayers from commercial wafer supplier.

Effect of V_T dependence on measured 25 °C JFET Characteristics



SiC JFET Dependence on Temperature



Significant change in JFET parameters with increasing T , consistent with prior works.
 - Some channel mobility loss offset by more negative JFET threshold voltage.

See: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014886.pdf> and <https://sic.grc.nasa.gov/files/HiTEC2016-NeudeckV1A.pdf>

SiC JFET SPICE Modeling

NASA Glenn SiC JFET SPICE Modeling Approach

Many different SPICE versions and enhancements are available, but most share “baseline” features and device models from original SPICE version (developed at UC Berkeley).

However, baseline version SPICE JFET model **DOES NOT include body bias effect** that significantly impacts electrical behavior of NASA-implemented IC devices.

Baseline SPICE NMOS LEVEL 1 model (n-channel MOSFET, that includes body effect via SPICE model parameter GAMMA) is therefore employed to model SiC JFET’s to first-order accuracy PROVIDED:

- Forward bias IS AVOIDED for gate and substrate pn junctions.
- Wafer substrate bias voltage (body bias effect) is connected to all devices.
- “Situationally correct” SPICE JFET (and resistor) models & parameters are employed.

Handle JFET temperature, wafer position, and body bias dependence by selecting the corresponding JFET SPICE model from the table on the next slide.

- DO NOT change the SPICE TEMP (temperature) parameter from its default value (of 27 °C).
- NASA Glenn uses “.include” SPICE statement to load the corresponding SPICE model file from the “ICv13Models” folder.

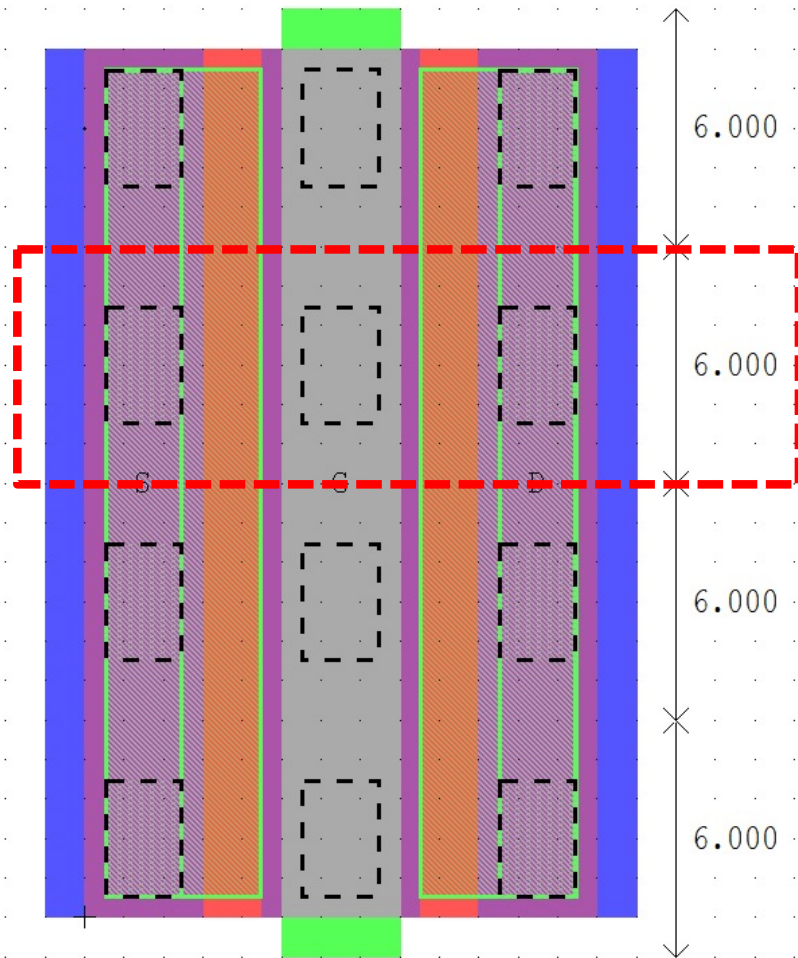
Estimated SPICE Models for IC Generation 13 JFETs vs. Temperature (T) and Radial Wafer Position (r)

T	r	Estimated SPICE Models for Unit Cell $M=1$ $W_G = 6 \mu\text{m}$ / $L_G = 3 \mu\text{m}$ NASA Glenn IC Version 13 JFET
25 °C	10 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-5.702 KP=1.186E-5 GAMMA=0.6521 LAMBDA=0.0200 RSH=0.000E+0 CJ=5.959E-5 PB=2.863 CGDO=7.009E-10 CGSO=7.009E-10 JS=0.00E+0 PHI=1.431 RD=5208 RS=5208
25 °C	20 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-7.355 KP=1.123E-5 GAMMA=0.7168 LAMBDA=0.0200 RSH=0.000E+0 CJ=5.959E-5 PB=2.863 CGDO=7.009E-10 CGSO=7.009E-10 JS=0.00E+0 PHI=1.431 RD=5208 RS=5208
25 °C	30 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-10.425 KP=1.032E-5 GAMMA=0.8246 LAMBDA=0.0200 RSH=0.000E+0 CJ=5.959E-5 PB=2.863 CGDO=7.009E-10 CGSO=7.009E-10 JS=0.00E+0 PHI=1.431 RD=5208 RS=5208
25 °C	40 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-15.382 KP=9.268E-6 GAMMA=0.9756 LAMBDA=0.0200 RSH=0.000E+0 CJ=5.959E-5 PB=2.863 CGDO=7.009E-10 CGSO=7.009E-10 JS=0.00E+0 PHI=1.431 RD=5208 RS=5208
460 °C	10 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-6.280 KP=2.689E-6 GAMMA=0.6521 LAMBDA=0.0200 RSH=0.000E+0 CJ=7.033E-5 PB=2.056 CGDO=7.489E-10 CGSO=7.489E-10 JS=0.00E+0 PHI=1.028 RD=6779 RS=6779
460 °C	20 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-7.950 KP=2.544E-6 GAMMA=0.7168 LAMBDA=0.0200 RSH=0.000E+0 CJ=7.033E-5 PB=2.056 CGDO=7.489E-10 CGSO=7.489E-10 JS=0.00E+0 PHI=1.028 RD=6779 RS=6779
460 °C	30 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-11.048 KP=2.334E-6 GAMMA=0.8246 LAMBDA=0.0200 RSH=0.000E+0 CJ=7.033E-5 PB=2.056 CGDO=7.489E-10 CGSO=7.489E-10 JS=0.00E+0 PHI=1.028 RD=6779 RS=6779
460 °C	40 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-16.044 KP=2.093E-6 GAMMA=0.9756 LAMBDA=0.0200 RSH=0.000E+0 CJ=7.033E-5 PB=2.056 CGDO=7.489E-10 CGSO=7.489E-10 JS=0.00E+0 PHI=1.028 RD=6779 RS=6779
500 °C	10 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-6.341 KP=2.430E-6 GAMMA=0.6521 LAMBDA=0.0200 RSH=0.000E+0 CJ=7.171E-5 PB=1.977 CGDO=7.544E-10 CGSO=7.544E-10 JS=0.00E+0 PHI=0.989 RD=7423 RS=7423
500 °C	20 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-8.012 KP=2.299E-6 GAMMA=0.7168 LAMBDA=0.0200 RSH=0.000E+0 CJ=7.171E-5 PB=1.977 CGDO=7.544E-10 CGSO=7.544E-10 JS=0.00E+0 PHI=0.989 RD=7423 RS=7423
500 °C	30 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-11.113 KP=2.109E-6 GAMMA=0.8246 LAMBDA=0.0200 RSH=0.000E+0 CJ=7.171E-5 PB=1.977 CGDO=7.544E-10 CGSO=7.544E-10 JS=0.00E+0 PHI=0.989 RD=7423 RS=7423
500 °C	40 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-16.113 KP=1.891E-6 GAMMA=0.9756 LAMBDA=0.0200 RSH=0.000E+0 CJ=7.171E-5 PB=1.977 CGDO=7.544E-10 CGSO=7.544E-10 JS=0.00E+0 PHI=0.989 RD=7423 RS=7423

These are ESTIMATED/EXTRAPOLATED ballpark models, NOT exact.

- See data scatter in slides 7 and 9.
- IC Generation 12 and IC Generation 13 runs remain to be fabricated and characterized.
 - Gen. 13 n-channel epilayer specified slightly thinner than Gen. 12 n-channel epilayer spec.
- Above are the SPICE models NASA Glenn is using for IC Gen. 13 circuit design and simulation.

Instancing JFETs



Layout Drawing
of $M=4$
 $L_G=3\mu\text{m}$
 $W_G=22\mu\text{m}$

All JFETs in NASA Glenn Version 12 IC process have gate length $L_G = 3\mu\text{m}$

Gate width W_G is effectively approximated by:

$$W_G = M * 6\mu\text{m} \quad (M = \text{Integer})$$

SPICE models represent a “Unit Cell JFET” of gate dimensions $W_G = 6\mu\text{m} / L_G = 3\mu\text{m}$

Larger JFETs (such as $W_G = 22\mu\text{m} / L_G = 3\mu\text{m}$ depicted) must be approximated using SPICE parallel instance parameter M (such as $M = 4$ for this JFET).

Example SPICE text instance (of depicted device):

```
MJFET22BY3 D G S B JFETModel L=3u W=6u M=4
```

For correct Version 13 SPICE modeling:

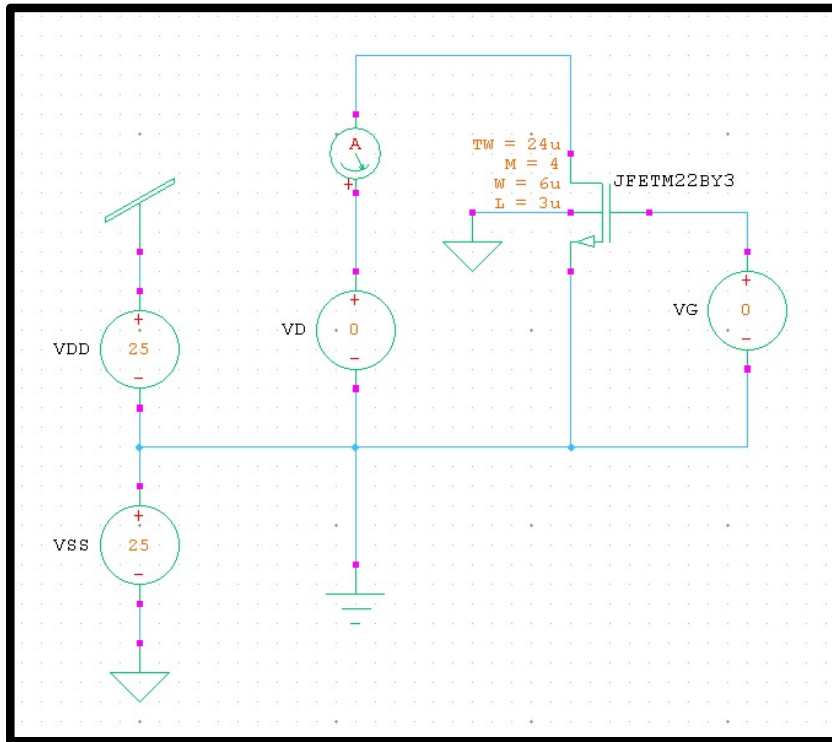
- **ONLY CHANGE M**
- **NEVER CHANGE L OR W from values shown above.**
 - Changing W instead of M will lead to incorrect SPICE simulations (due to incorrect accounting of device contact resistances).

Example SPICE Simulation of SiC JFET I-V Characteristics

Simulation example for a $W=22\mu\text{m}$ x $L=3\mu\text{m}$ SiC JFET at $T=460^\circ\text{C}$ at wafer position $r=10\text{ mm}$.

SPICE Input Deck Text

```
* Example JFET DC IV at wafer position r=20mm for T=460C
.INCLUDE "..\ICv13_Models\ICv13Models_460C_20mm.txt"
MJFETM22BY3 N_2 N_3 Gnd Vss JFETModel W=6u L=3u M=4
VVD N_1 Gnd DC 0
VDD Vdd Gnd DC 25
VVG N_3 Gnd DC 0
VVSS Gnd Vss DC 25
VID N_1 N_2 0v
.PRINT DC ID=I(VID)
.DC VVD INCR 1 0 40 VVG INCR -1 0 -6
.end
```



Included "ICv13Models_460C_20mm.txt" file (corresponds to 6th row of table in slide 12):

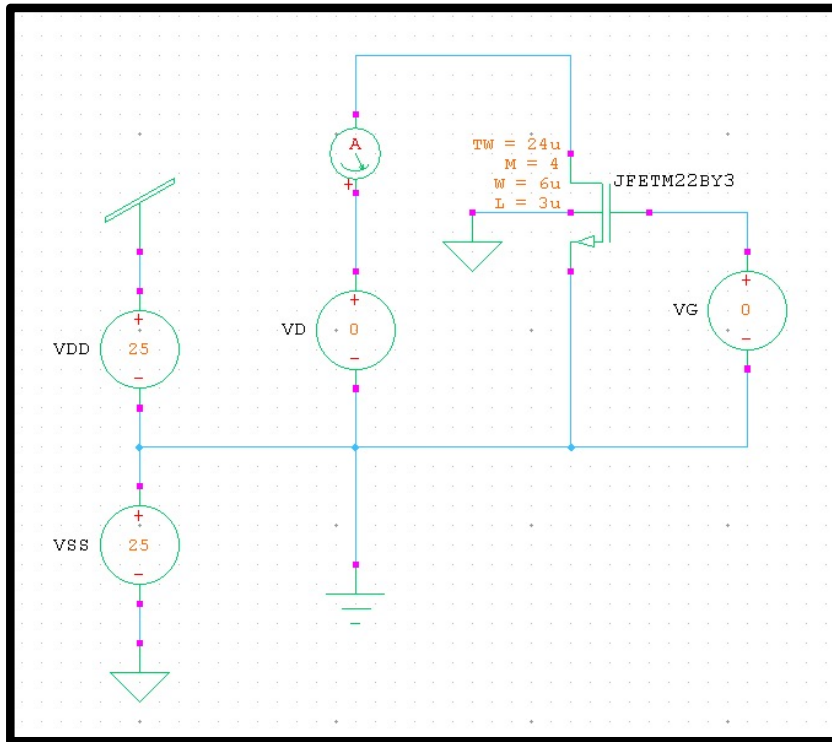
```
*SPICE Models for NASA JFET IC Version 13 T=733.0 K (460.0 C) and r=20.0 mm from wafer center.
.MODEL JFETModel NMOS LEVEL=1 VTO=-7.950 KP=2.544E-6 GAMMA=0.7168 LAMBDA=0.0200 RSH=0.000E+0
CJ=7.033E-5 PB=2.056 CGDO=7.489E-10 CGSO=7.489E-10 JS=0.00E+0 PHI=1.028 RD=6779 RS=6779
.MODEL RSheetModel R RSH=1.289E+4
.MODEL RBodyBiasModel NMOS LEVEL=1 VTO=-182.167 KP=4.258E-7 CJ=7.033E-5 PB=2.056 PHI=1.028
RSH=0.000E+0 GAMMA=1.00E-12 RS=333 RD=333 JS=1.00E-25
.MODEL RSourceImplant R RSH=607.0
```

NOTE: The FET body/bulk terminal is always connected to VSS supply!

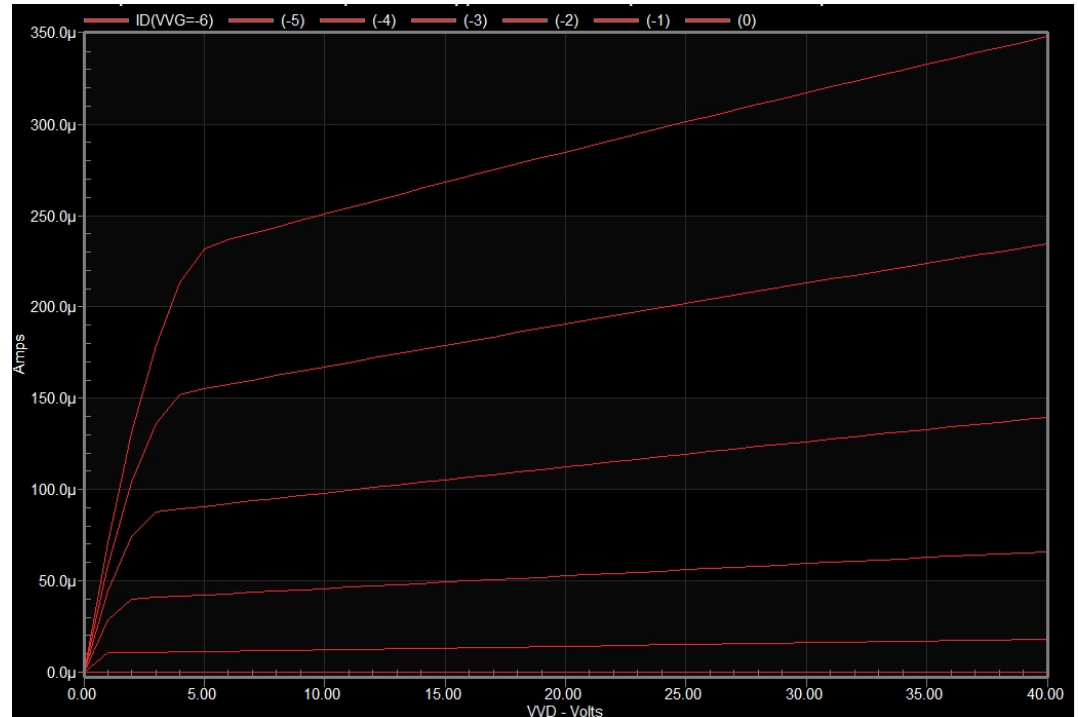
- This accurately reflects the way FETs are biased and used in NASA Glenn SiC JFET ICs.

Example SPICE Simulation of SiC JFET I-V Characteristics

Simulation example for a $W=22\mu\text{m} \times L=3\mu\text{m}$ SiC JFET at $T=460\text{ }^\circ\text{C}$ at wafer position $r=20\text{ mm}$.



SPICE Input Deck (Text File)



```
* Example JFET DC IV at wafer position r=20mm for T=460C
.INCLUDE "..\Cv13_Models\Cv13Models_460C_20mm.txt"
MJFETM22BY3 N_2 N_3 Gnd Vss JFETModel W=6u L=3u M=4
VVD N_1 Gnd DC 0
VVDD Vdd Gnd DC 25
VVG N_3 Gnd DC 0
VVSS Gnd Vss DC 25
VID N_1 N_2 0v
.PRINT DC ID=I(VID)
.DC VVD INCR 1 0 40 VVG INCR -1 0 -6
.end
```

JFET current-voltage characteristics change with substrate bias V_{SS} , temperature, and wafer position.

Key Online Technical References

Yearlong 500 °C Operational Demonstration of Up-Scaled 4H-SiC JFET Integrated Circuits (2018):

Article: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180003391.pdf>

Presentation: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20190001885.pdf>

Processing and Characterization of Thousand-Hour 500 °C Durable 4H-SiC JFET Integrated Circuits (2016):

Article: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014879.pdf>

Presentation: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170001674.pdf>

First-Order SPICE Modeling of Extreme-Temperature 4H-SiC JFET Integrated Circuits (2016):

Article: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014886.pdf>

Presentation: <https://sic.grc.nasa.gov/files/HiTEC2016-NeudeckV1A.pdf>

Experimental and Theoretical Study of 4H-SiC JFET Threshold Voltage Body Bias Effect from 25 °C to 500 °C (2016):

Article: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160005307.pdf>

Inclusion of Body Bias Effect in SPICE Modeling of 4H-SiC Integrated Circuit Resistors (2018):

Article: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180000657.pdf>

Poster Presentation: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170009460.pdf>