



Progress Towards Prolonged IC Deployment Into Previously Inaccessible Hostile Environments Via Development of SiC JFET-R ICs

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(CS MANTECH)

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<https://go.nasa.gov/sic>

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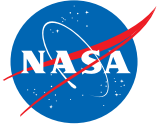
Amir Avishai



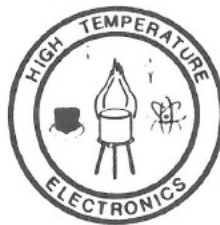
Outline

- Introduction
- 500 °C Durable SiC IC Technology
- Impact on Venus Exploration

Potential Benefits of High Temperature Electronics Has Been Recognized for Decades



First International High Temperature Electronics Conference



Albuquerque Marriott Hotel
Albuquerque, New Mexico USA

June 16 - 20, 1991

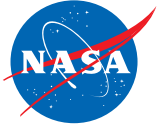
1991

HITEC

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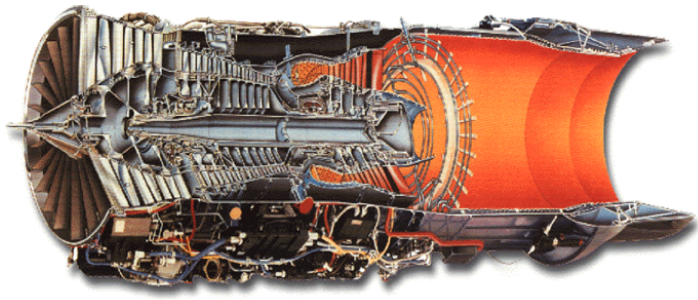
SESSION I: Users and Needs

- | | | | |
|----|---|---------------|----|
| 1. | Military Needs for High Temperature Electronics
W.G. Taschek, <i>Belvoir Research Development and Engineering Center</i> | Automotive | 3 |
| 2. | A Data Acquisition and Control System for Long Term Deployments in Hot Geothermal Wells
R. Gillatt, <i>Camborne School of Mines</i> | Well Drilling | 10 |
| 3. | High Temperature Power Electronics for Space
A.N. Hammoud, <i>Sverdrup Technology, Inc.</i> ; E.D. Baumann, I.T. Myers, E. Overton, <i>NASA Lewis Research Center</i> | Aerospace | 11 |
| 4. | High Temperature Radiation Hardened Devices Technology Assessment
J.L. Davidson, <i>Vanderbilt University</i> ; K.K. Blankenship, <i>U.S. Army Strategic Defense Command</i> ; J.J. Sheehy, <i>Physitron Inc.</i> | Automotive | 17 |
| 5. | High Temperature Electronics for Supersonic Aircraft
D.W. Christenson, <i>General Dynamics</i> | Aerospace | 23 |



High-T Electronics Benefits to NASA Missions

Intelligent Propulsion Systems

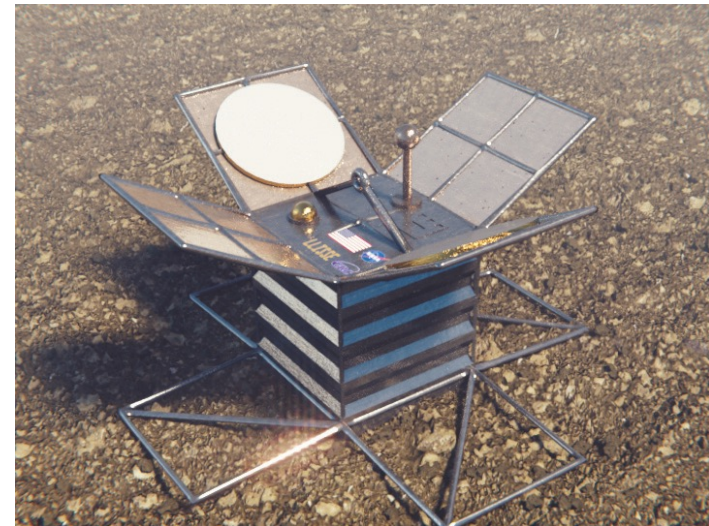


$T > 450\text{ }^{\circ}\text{C}$ sensors with electronics in key engine areas for realizing advanced concepts in distributed control and compressor/combustion instability detection and avoidance for improving engine performance

- Thrust to weight ratio
- Fuel efficiency & emissions

Power devices for aerospace electric propulsion and actuation

Venus Exploration Landers



Venus surface: **460 °C**
AND 92X Earth pressure
AND chemically reactive gasses

Long duration landers require electronics that endure the Venus surface environment

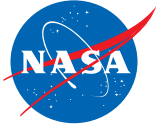


NASA Glenn SiC IC Technology Development Goals

Greatly expand the application-viable IC operating temperature envelope

Bring initial IC electronics capability reliably to previously unthinkable places

- Enable new approaches to systems dealing with harsh environments
- At least 500 °C operation for long duration
 - More than 200 °C above silicon-on-insulator practical limit
- At least 2000 hours of stable electrical operation at 500 °C
 - Jet engine ground test, Venus surface missions
- At least 2 levels of 500 °C durable on-chip interconnect
 - Enable more complex, higher density ICs
- Chip packaging and multi-chip circuit boards for 500 °C operation
 - Integration with sensors, wireless communications, subsystems
- Infusion of beneficial 500 °C ICs into missions and systems



NASA Glenn SiC IC Development Philosophy

“Over-design” every aspect to make high temperature durable ICs

- De-prioritize other device metrics (such as power & frequency)
- Seek compatibility IC manufacturing materials, tools, and techniques

Device Foundation

- SiC epilayer PN homojunction transistor (not MS or MOS gate)
- Stable ohmic contacts

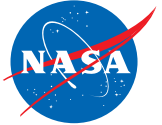
On-chip Integration

- Stable interconnect
- High circuit density (2-level interconnect, small devices & isolation)
- Temperature and process tolerant circuit design

Ceramic packaging and circuit boards

Demonstrate initial 500 °C durable IC capability, infuse and improve in parallel

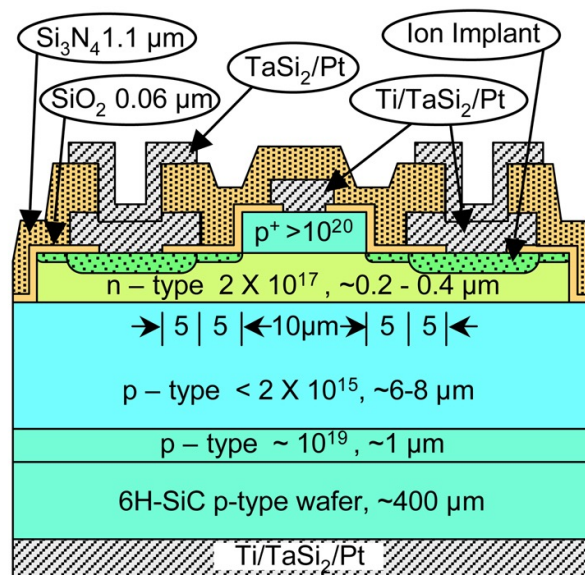
**“LEARN BY DOING” OVER SUCCESSIVE GENERATIONS (CYCLES) OF
PROTOTYPE IC FABRICATION AND CHARACTERIZATION.**



Transistor Device Approach

Epitaxial SiC n-JFETs developed as the most straightforward foundational transistor for achieving long-term device stability at $T \geq 500^\circ\text{C}$

2007 NASA 6H-SiC JFET [1]



SiC is the most stable/inert semiconductor crystal

- Low impurity diffusion, low reactivity

Inherent JFET High-T Stability Advantages

- Majority carrier device
- Low-leakage epilayer PN homojunctions
- Minimal sensitivity to p-type (gate) contact
- N-type ohmic contacts/implants

Other transistor types more challenging to render stable/durable at $T > 450^\circ\text{C}$.

- Bipolar transistors: n-type AND p-type contact AND minority carrier sensitivity
- MOSFETs/CMOS: MOS junction sensitivity
- MESFETs: Rectifying metal-semiconductor junction leakage & sensitivity
- III-N HFETs: Heterojunction sensitivity, more diffusion, more reactive than SiC

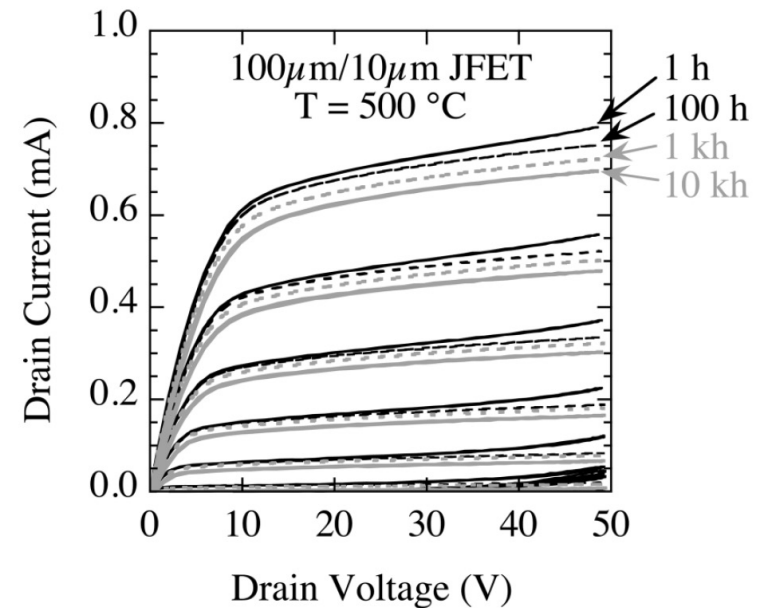
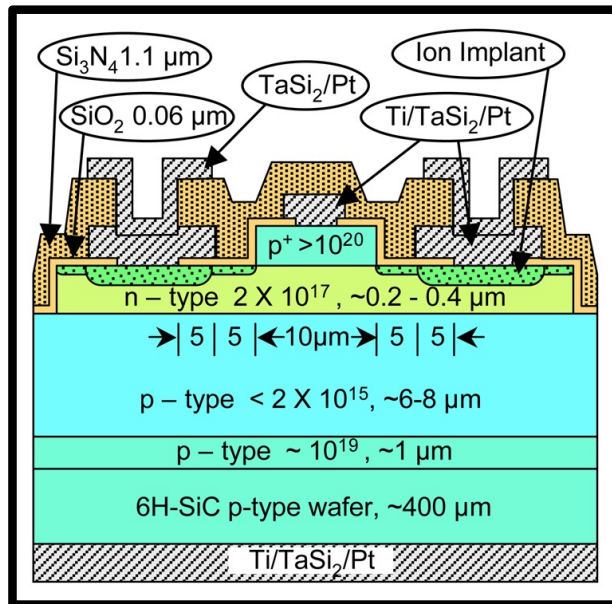
[1] Neudeck et al., IEEE Electron Device Lett. vol. 25, no. 5, pp 456-459 (2008).

NASA Glenn Low-Power 6H-SiC JFET ICs

(Results from ICSCRM 2007 & ECSCRM 2008)



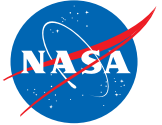
Discrete packaged JFETs operate with excellent stability for 10,000 hours at 500 °C



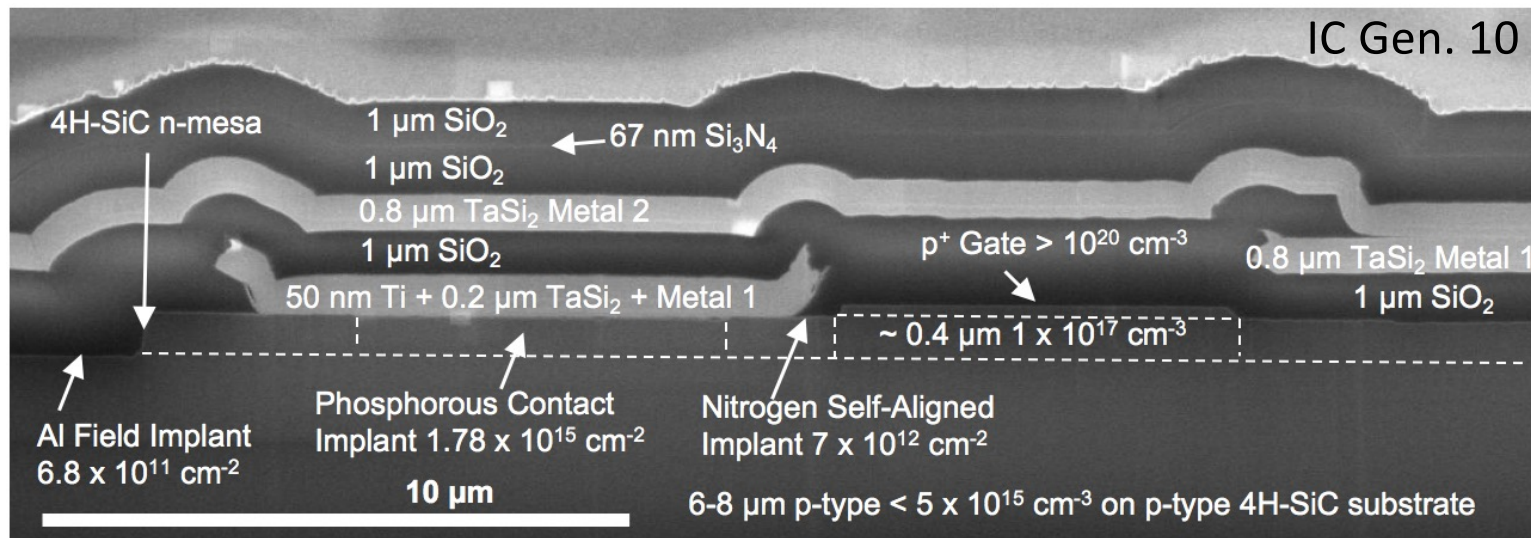
< 10% changes during 10000 hours of electrical operation in air at 500 °C!

D. Spry et al, Mat. Sci. Forum vol. 600-603, p. 1079 (2008)

Ohmic Contacts from R. Okojie et al, J. Appl. Phys, vol. 91, p. 6553, (2002)



500 °C Stable Two Levels Interconnect¹



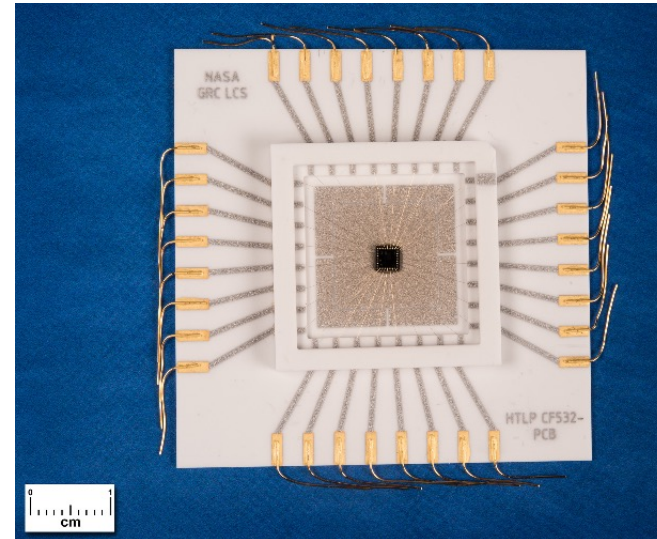
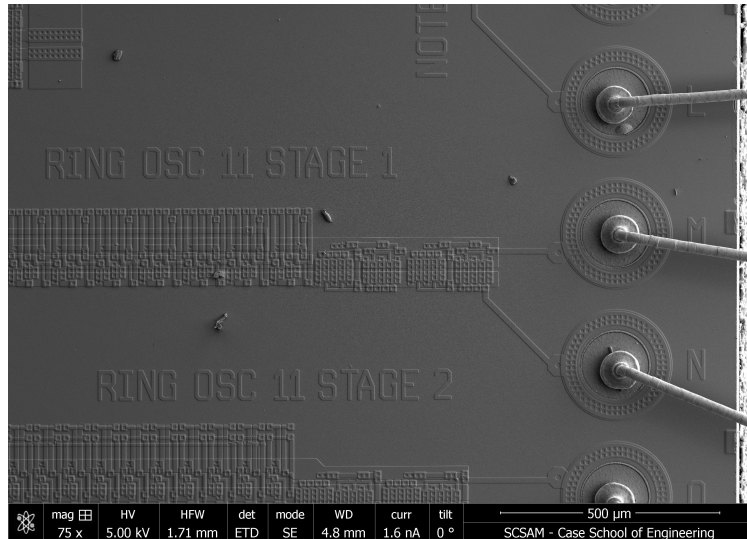
IC processing and materials compatible with SiC power device tools & manufacturing

- Close-proximity sputtering of TaSi₂ (21mm target to substrate spacing)
- LPCVD tetraethyl orthosilicate (TEOS) and Si₃N₄ layers deposited at 720 °C
- Interconnect completely buried beneath dielectric

See D. Spry 2021 CS MANTECH Presentation 4.3.

¹P. G. Neudeck, et al., 2018 IMAPS High Temperature Electronics Conf. pp. 71-78

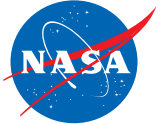
500 °C Stable Bond Pads and Packaging^{1,2}



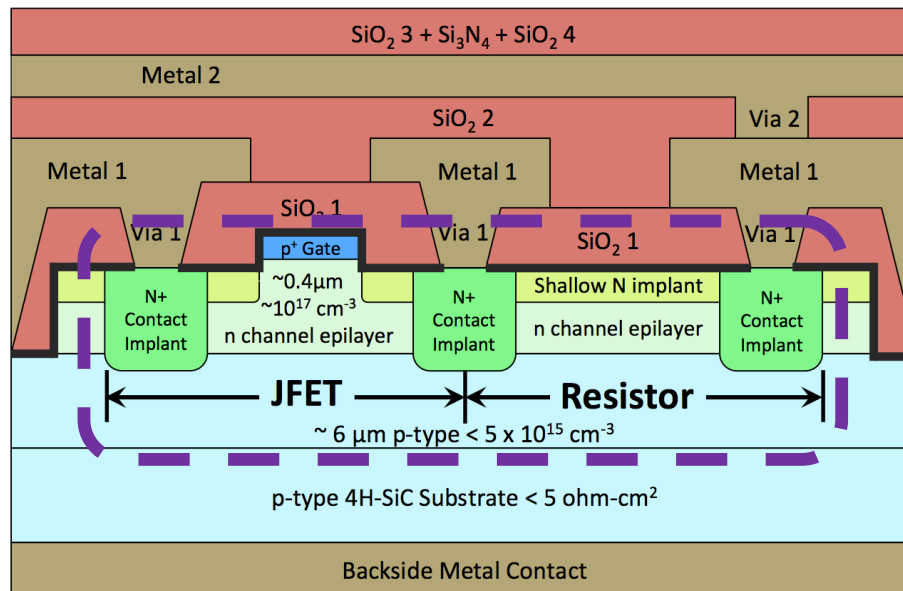
- “IrIS” bond pad metal stack anchored directly to SiC¹ (D. Spry Presentation 4.3)
- Pt thick-film traces, Au/Pt pads, Au die attach (600 °C), and Au ball bonding².

¹D. Spry & D. Lukco, J. Electronic Materials 41 p. 915 (2012)

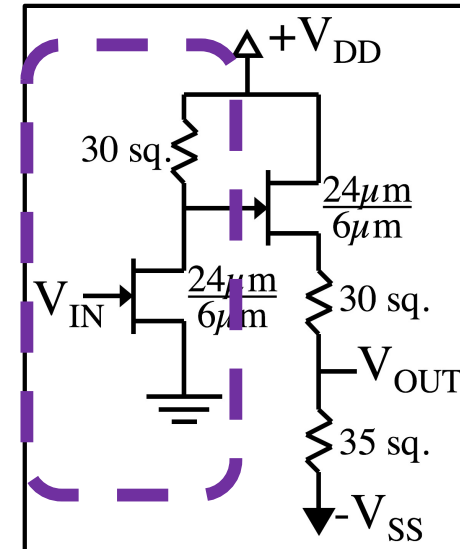
²L. Chen, et al., Proc. 2016 IMAPS High Temperature Electronics Conf. pp. 66-72



Circuit Approach^{1,2}



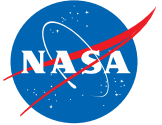
NOT Logic Gate Schematic



- Resistors made with same epi as JFET → well-matched T dependence
- Layout ratio based circuit design (not absolute component values)
- Negative threshold voltage V_T → negative signal voltages (roughly -1V to -10V logic)
- Typical $V_{DD} = +25$ V, $V_{SS} = -25$ V Chip backside is biased at V_{SS}

¹M. J. Krasowski, US Patent 7,688,117 (2010).

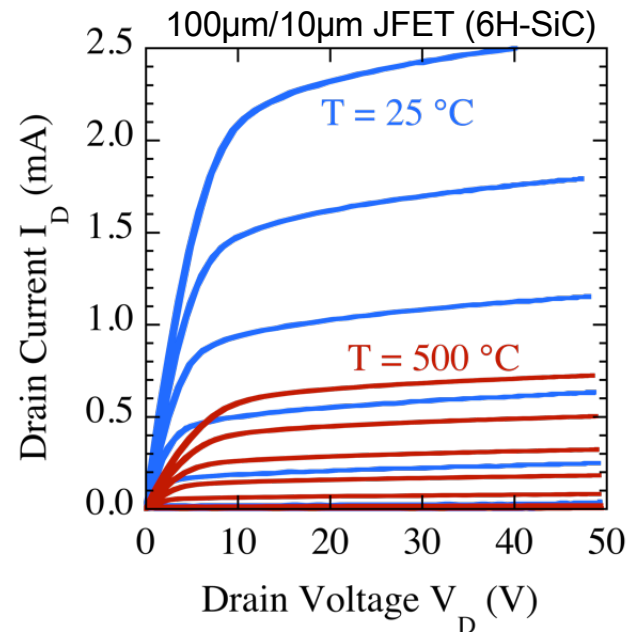
²P. G. Neudeck, et al., Proc. IMAPS High Temperature Electronics Conf., 2016, pp. 263-271.



Temperature Performance

(Slide Presented at 2011 Electrochemical Society Meeting)

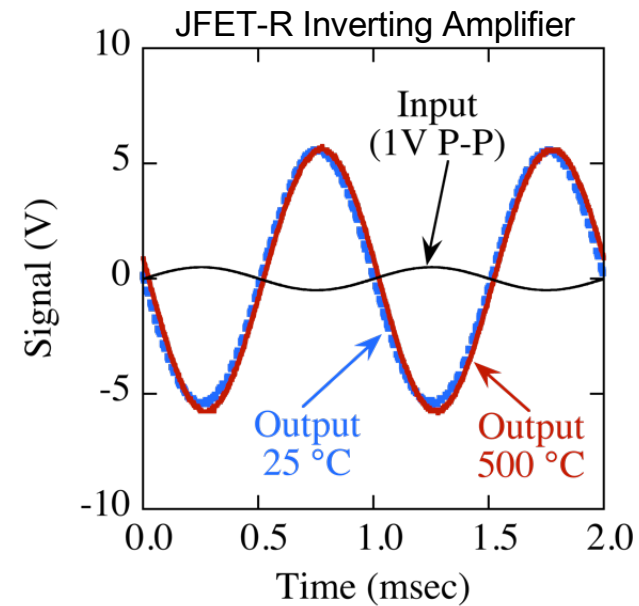
Transistor Characteristics



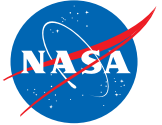
Despite large ($> 3\times$) change in JFET characteristics...



Circuit Characteristics

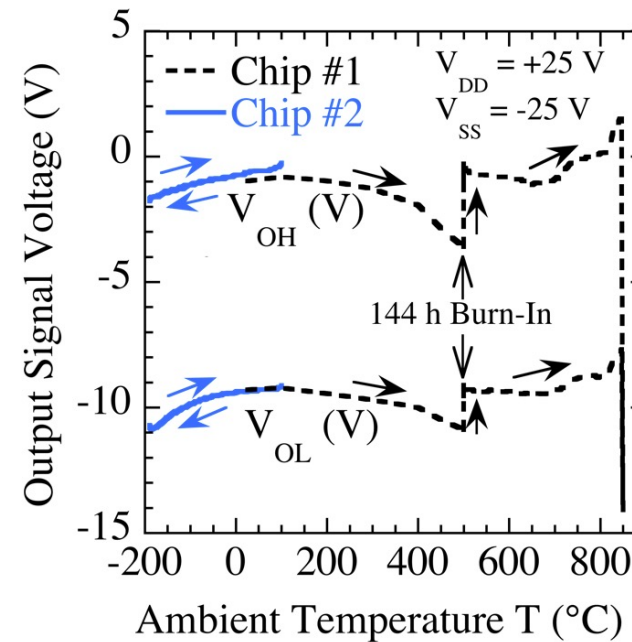
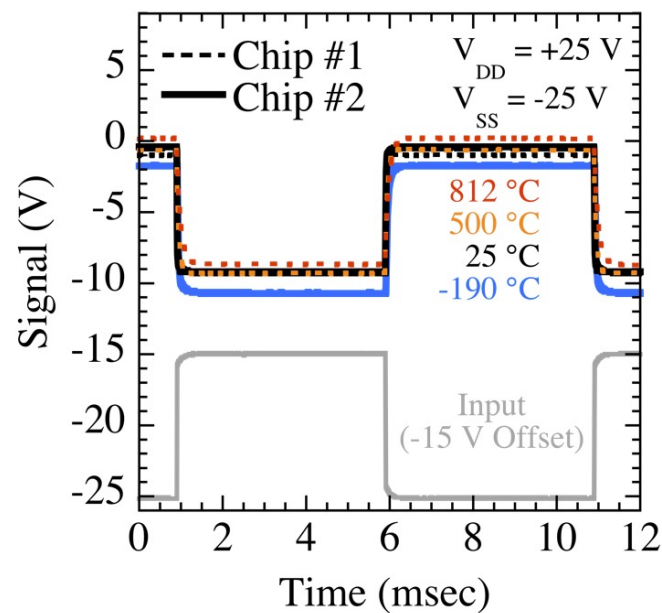


...nearly temperature-independent circuit operation can be achieved!



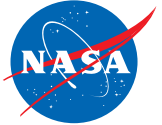
-190 °C to +812 °C Functionality¹

(Generation 10.1 NOT Gate Testing)



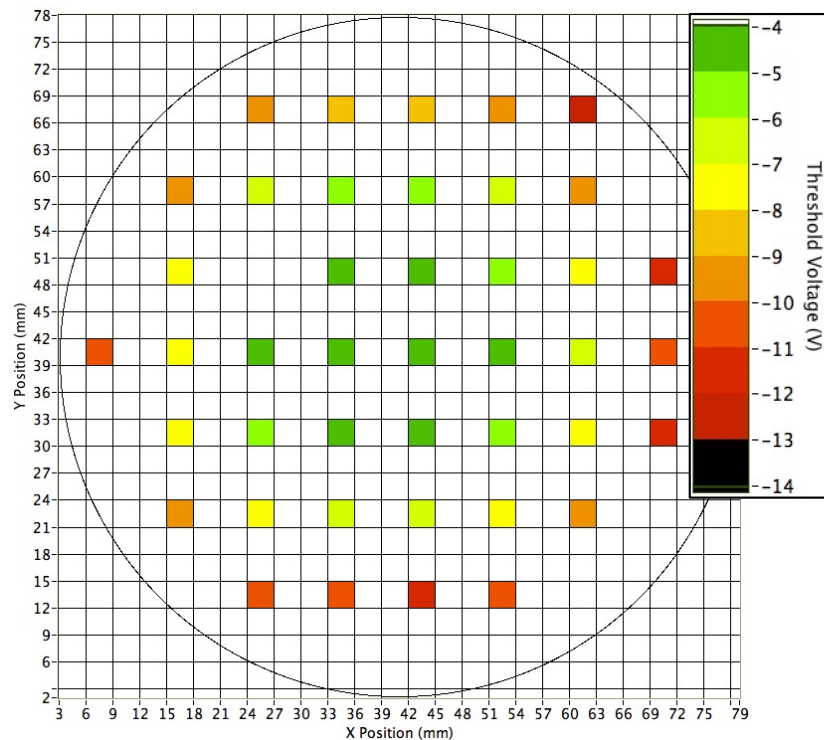
- 1000 °C temperature span without changing signal/supply input voltages.
- Straightforward functional yield screening at 25 °C (on-wafer probe test).

¹Neudeck, Spry, Krasowski, Prokop, Chen, Materials Science Forum, vol. 963, pp. 813-817 (2019).

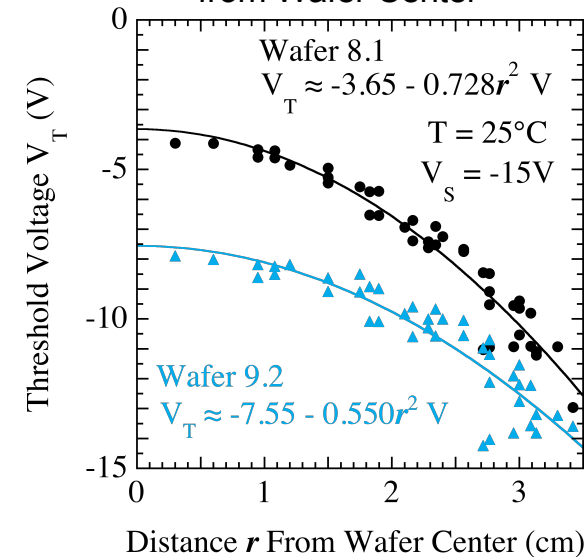


Experimental JFET Threshold (V_T) Non-Uniformity

Wafer Probe Map of Wafer 8.1 JFET V_T
 $T = 25^\circ\text{C}$, $V_D = 20\text{V}$, $V_S = -15\text{V}$
(76 mm diameter wafer)

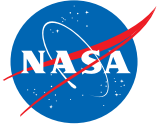


Plot of Measured JFET V_T
vs. Radial Distance (r)
from Wafer Center



Positional variation of JFET V_T is radial
and due to thickness non-uniformity in
as-grown epilayers.

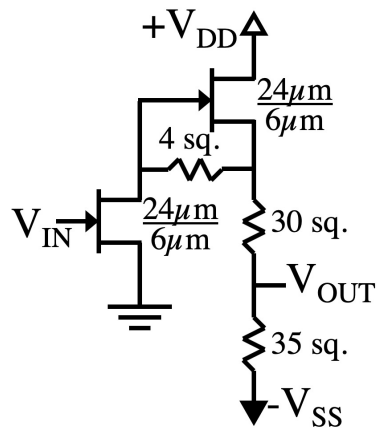
[1] P. Neudeck et al., Materials Science Forum **858** p. 903 (2016).



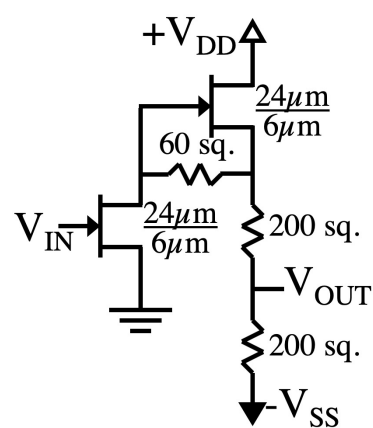
Generation 11 “Current Source” Logic Gate Design

Two families implemented based on different speed/power/area application tradeoffs.

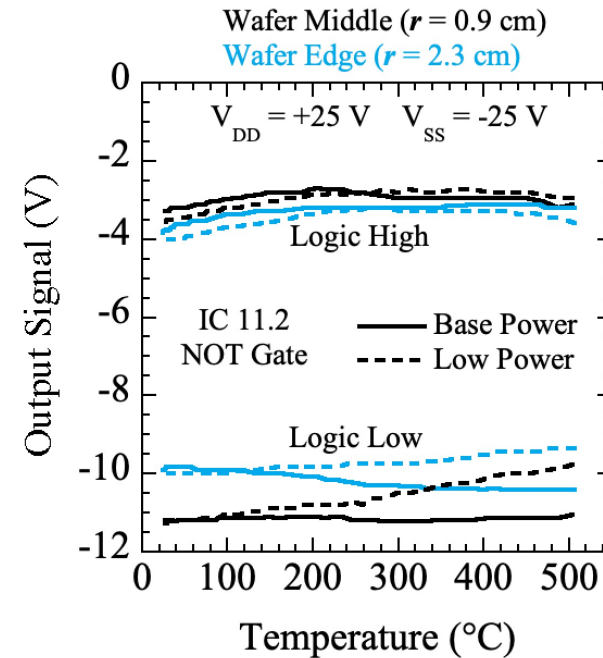
Base Power NOT Gate



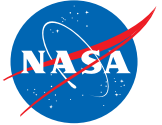
Low Power NOT Gate



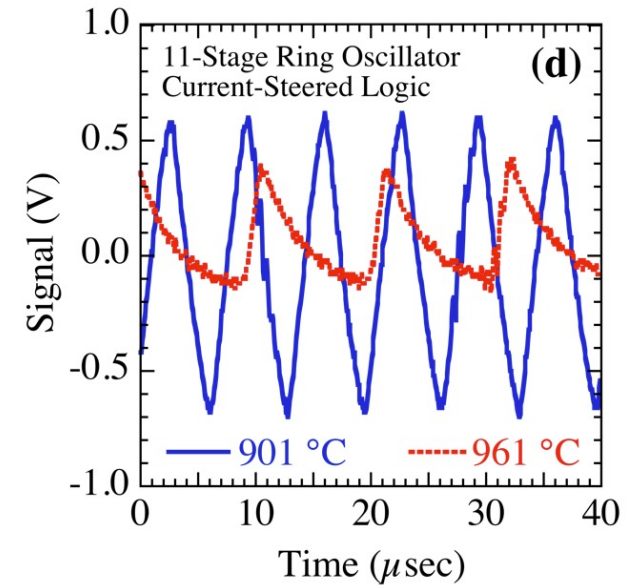
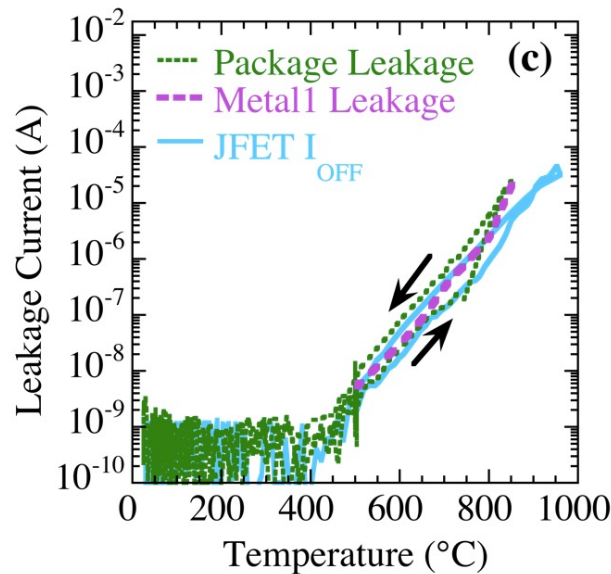
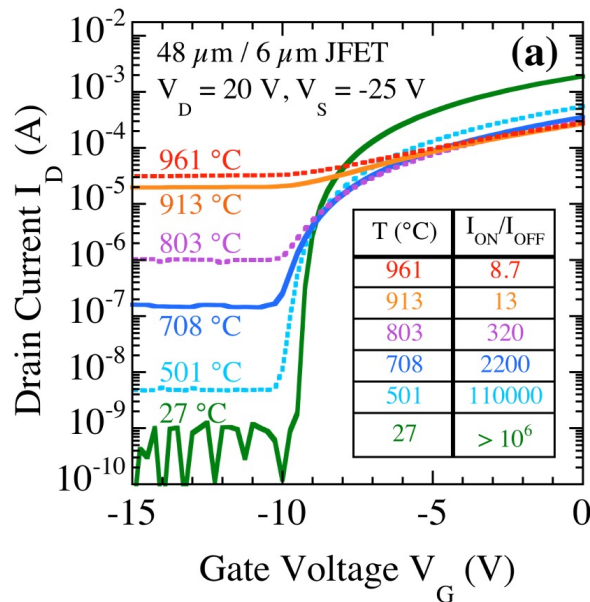
- Smaller resistors → smaller layout area
- Improved output voltage uniformity



Operation Demonstrated Above 900 °C¹



Enables temperature-accelerated lifetime qualification testing for 500 °C applications.

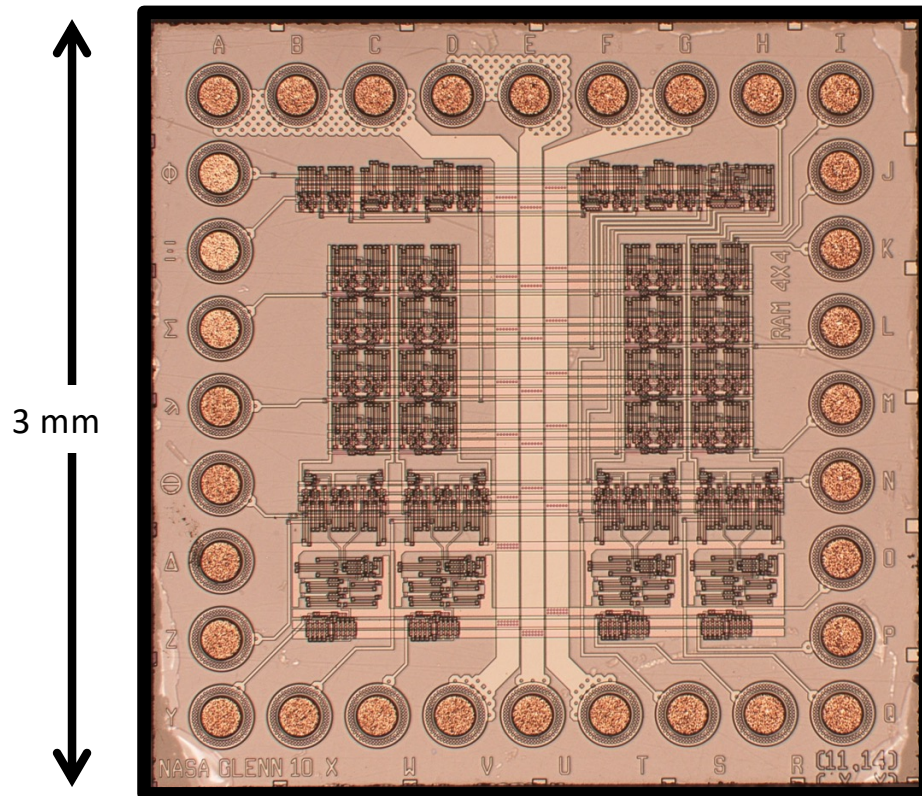


(Note: Waveforms are probe-loaded)

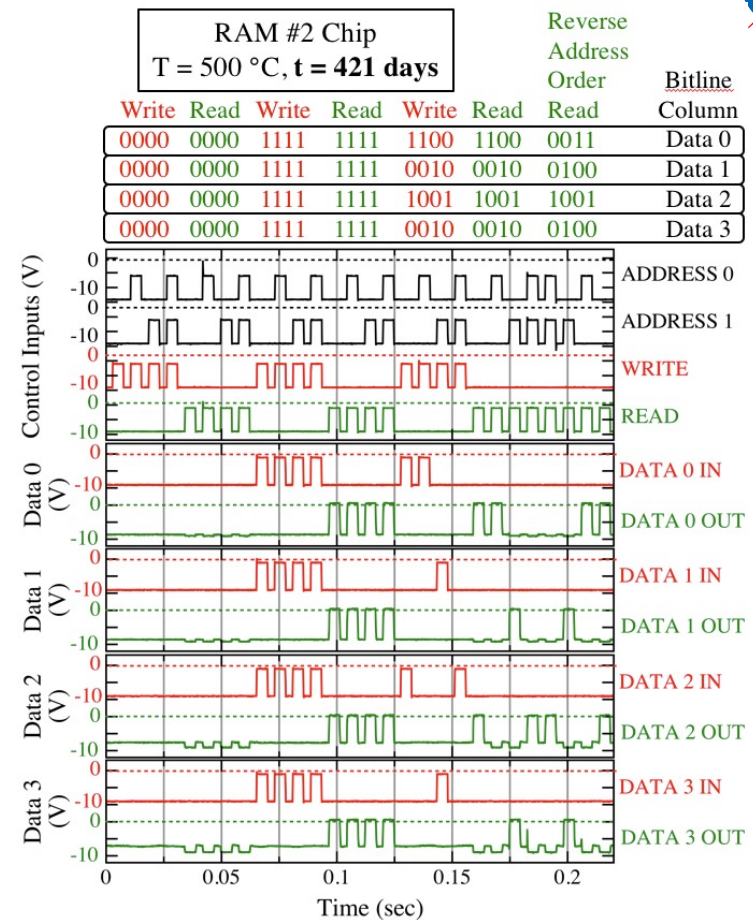
- Packaging leakage was limiting experimental factor, package was designed for 500 °C.
- “Intrinsic” JFET-R IC high-temperature limit remains to be ascertained.

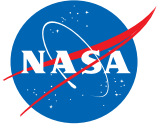
¹P. Neudeck, et al., IEEE Electron Device Lett. 38 (2016) 1082-1085.

500 °C Durable NASA Glenn Gen. 10 SiC JFET-R RAM Chip¹



¹P. G. Neudeck, et al., 2018 IMAPS High Temperature Electronics Conf. pp. 71-78

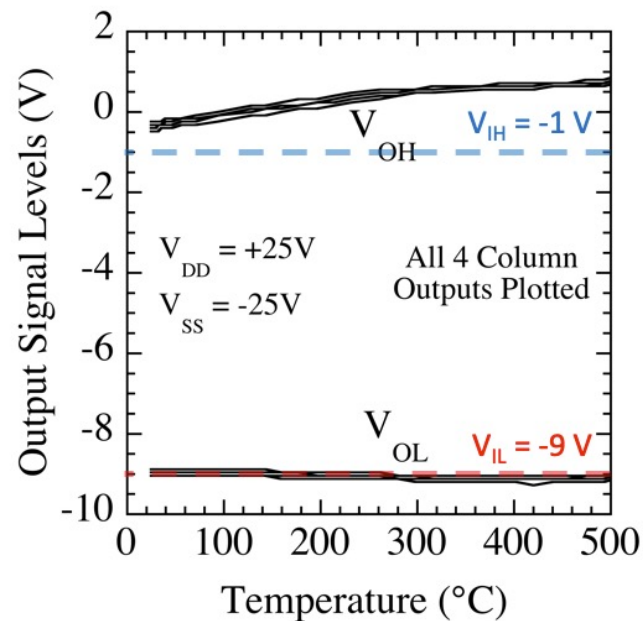




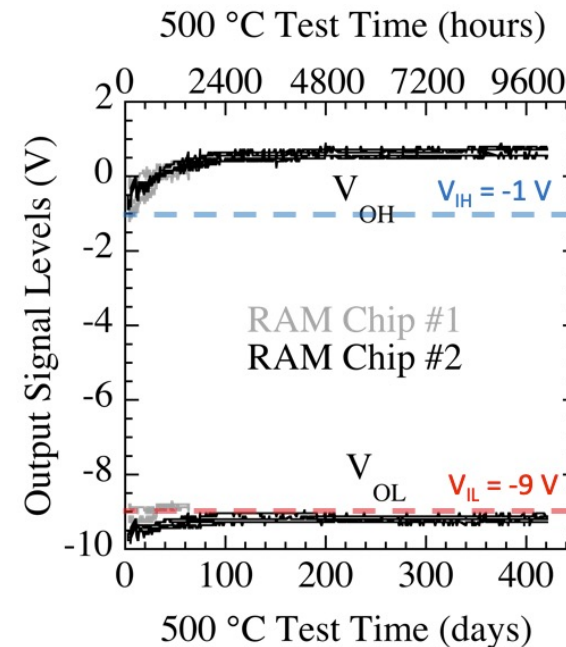
NASA Glenn Gen. 10 RAM Chip Output Levels

(2018 IMAPS High Temperature Electronics Conference)

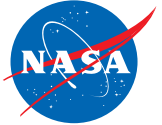
vs. Temperature



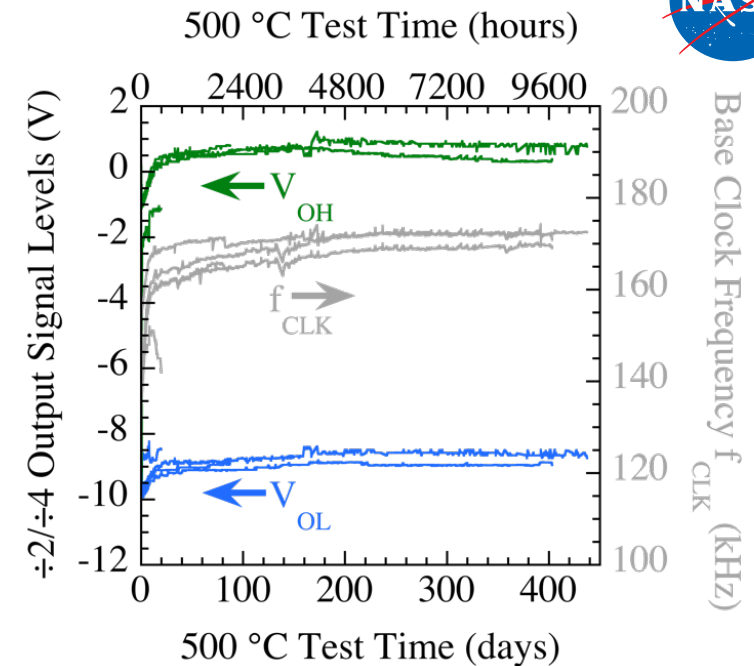
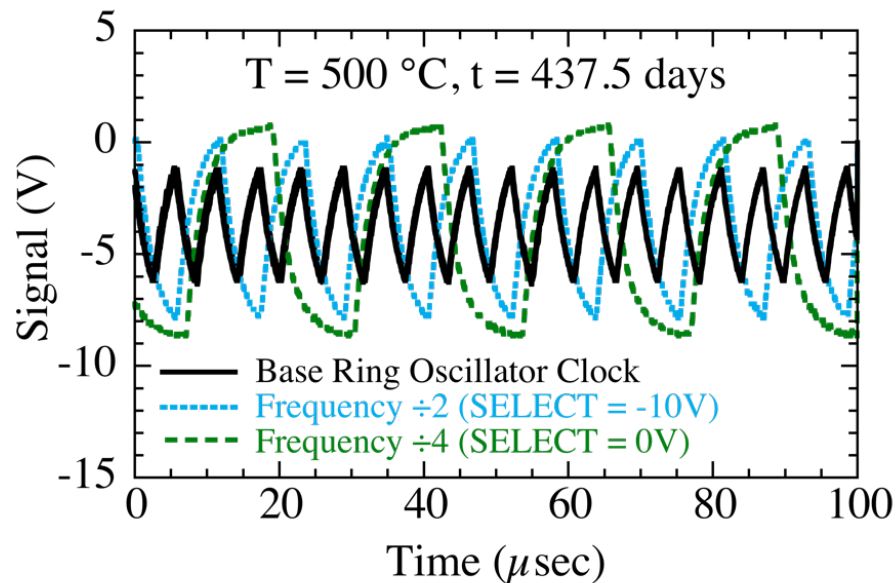
vs. Time @ 500 °C



- ✓ Operation over broad application temperature range
- ✓ Prolonged (year+) operation at $T > 450$ °C for applications

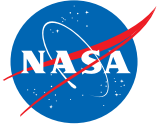


500 °C Oven-Test Results¹



- Some IC Gen. 10 chips last more than 1 year, but a few “infant fail” much sooner
- After initial burn-in, output characteristics change < 10%

¹P. G. Neudeck, et al., 2018 IMAPS High Temperature Electronics Conf. pp. 71-78

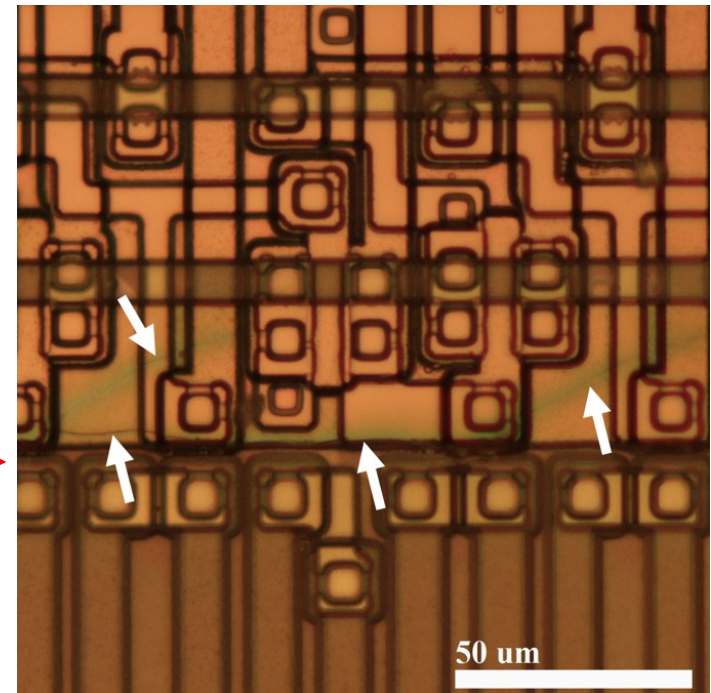


Primary Failure Mode: Cracks in Dielectric¹

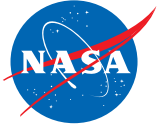
TaSi₂ interconnects oxidize beneath cracks
leading to open-circuit failure

Table I. 500 °C JFET IC Test Summary

Packaged IC Sample	<i>r</i> (mm)	500 °C Time	Test Status
RAM #1	13.4	63 days	Suspended
RAM #2	6.7	420 days	Running
Clock #1	24.2	19 days	Failed
Clock #2	15.3	437 days	Running
Clock #3A	12.4	403 days	Running
Clock #3B	12.4	403 days	Running
Clock #3C	13.4	87 days	Failed

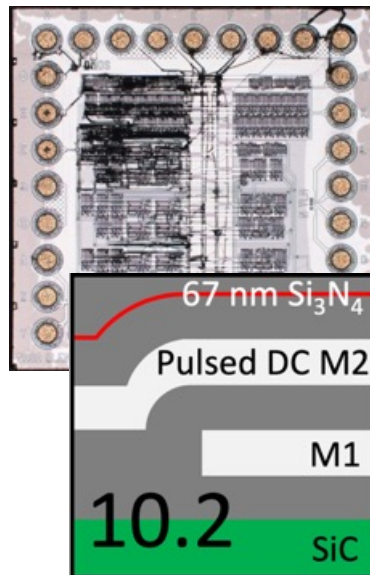


¹P. G. Neudeck, et al., Proc. 2018 IMAPS High Temperature Electronics Conf., pp. 71-78

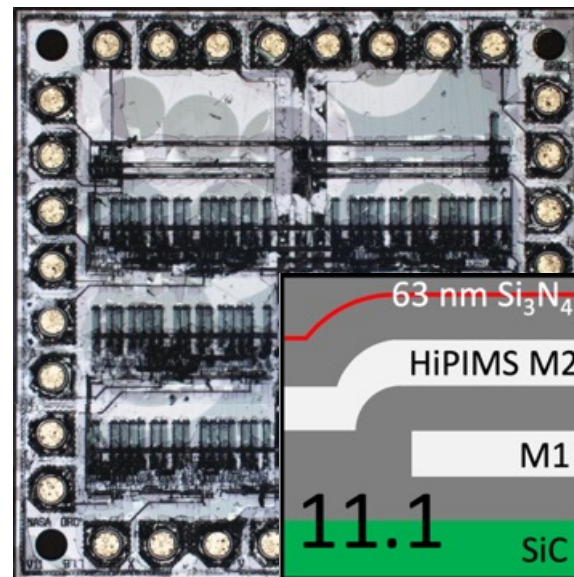


10-cycle **720 °C** Anneal Test Results¹

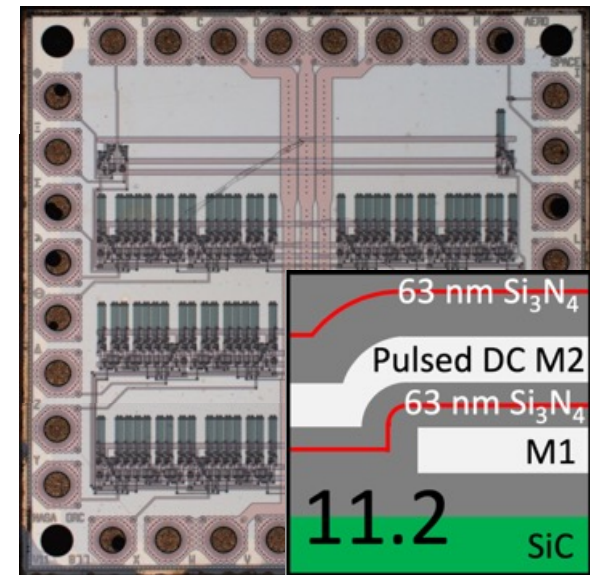
Cracks & oxidation
500 °C durable



Cracks & oxidation
NOT 500 °C durable



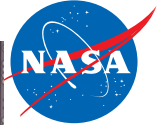
No cracks, no metal oxidation
NOT 25 °C functional



¹See D. Spry et al., Materials Science Forum, vol. 1004, pp. 1148-1155



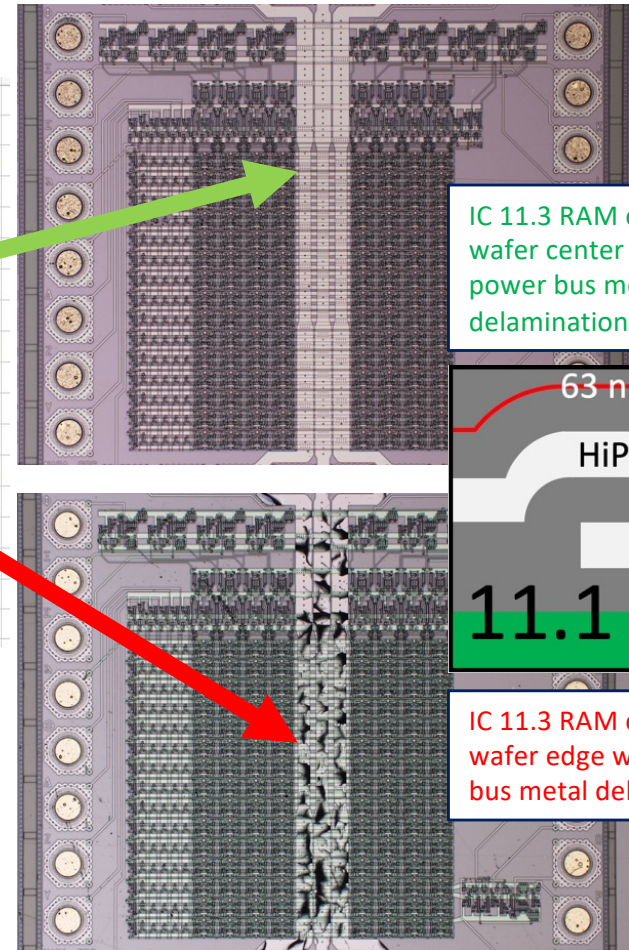
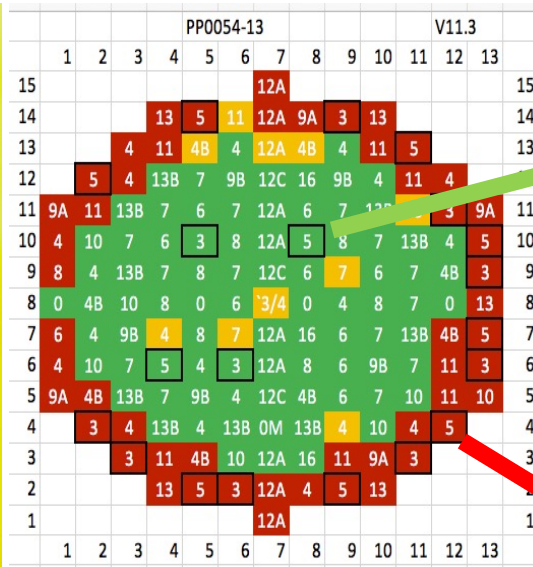
IC Gen. 11 Power Bus Metal Delamination ("Process 11.1")



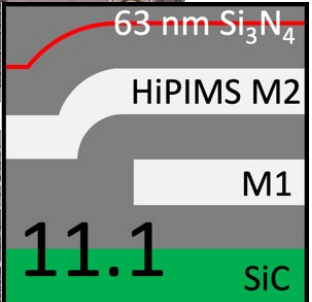
75 mm Diameter Gen. 11 Wafer
Just After Metal1 Deposition



Wafer 11.3 Post-Nitride Optical
Inspection Grading Map



IC 11.3 RAM chip near
wafer center without
power bus metal
delamination



IC 11.3 RAM chip near
wafer edge with power
bus metal delamination

Central wafer regions were free of observable metal delamination.

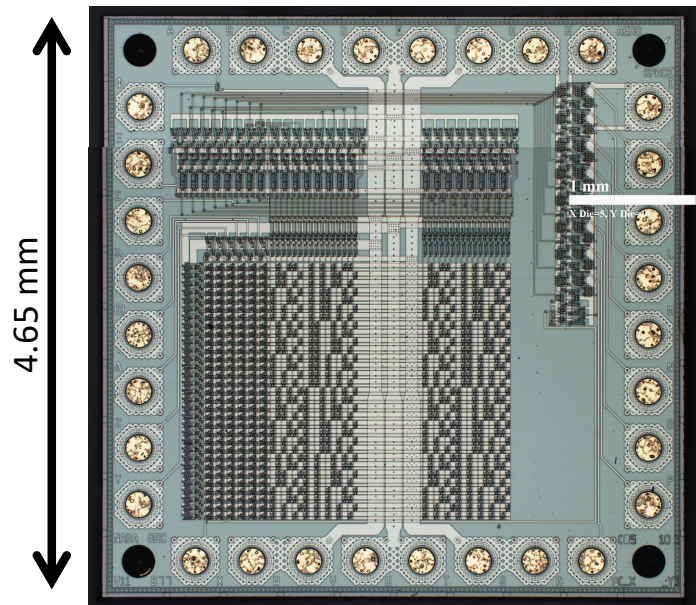
Delamination of long/wide metal power bus features occurred in the outer ($r > 24$ mm) wafer regions.

Inferior IC yield < 25% for Gen. 11 (compared to > 75% for Gen. 10).

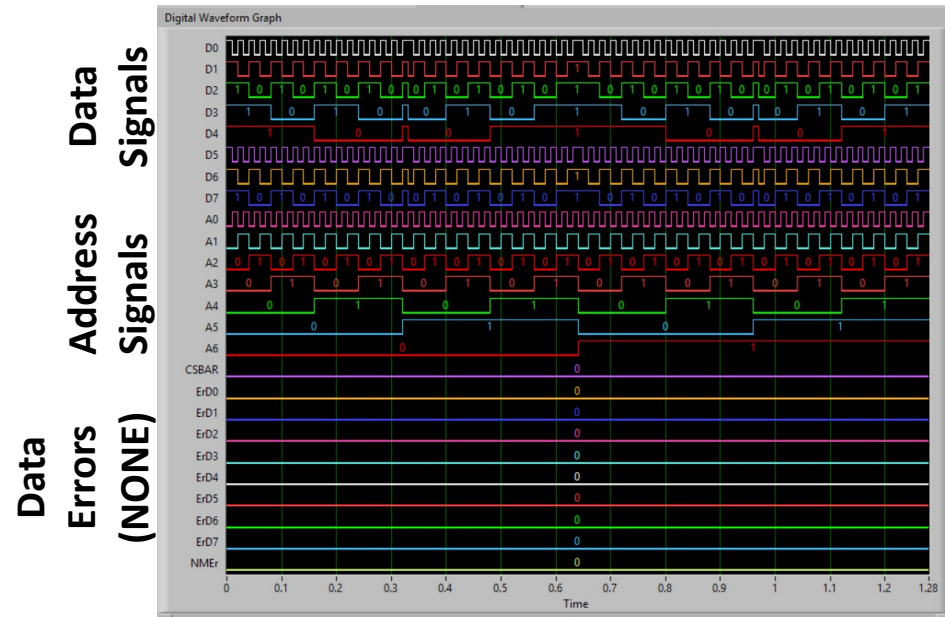
Inferior 500 °C durability < 500 hours for Gen. 11.

Gen. 11.1 124x8 bit Read Only Memory (ROM)

Chip Prior to Packaging



Error Free 500 °C Oven-Test



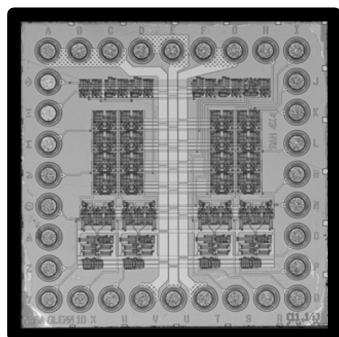
- Bits started to fail less than 200 hours into 500 °C testing, surmised related to Gen. 11 interconnect process shortcomings presented in prior slides.
- Failure analysis delayed by COVID-19 NASA Glenn SiC lab closure.

Upscaling from MSI to LSI



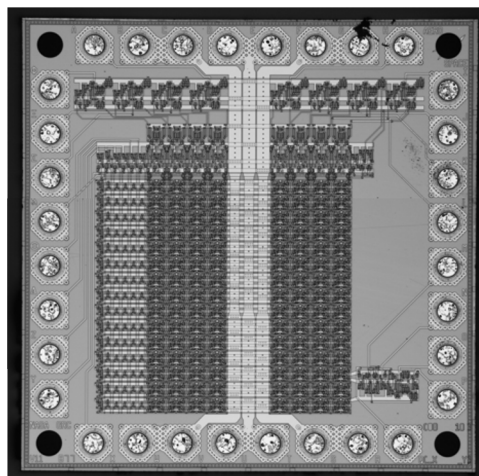
“IC Gen. 10” (2017)

16-bit RAM



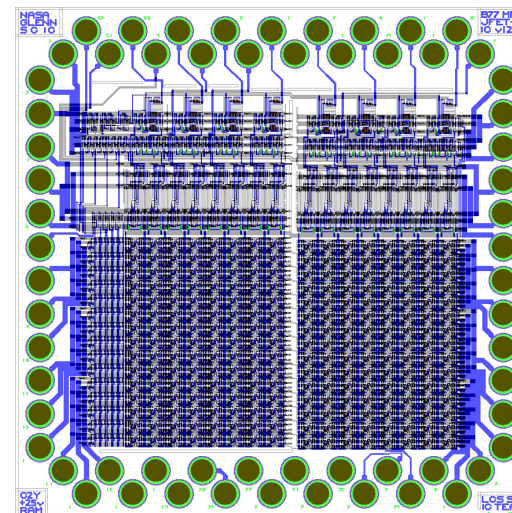
“IC Gen. 11” (2018-19)

120-bit RAM, ~ 1000 JFETs



“IC Gen. 12” (2022*)

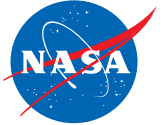
248-bit RAM, ~ 2000 JFETs



	Gen. 10	Gen. 11	Gen. 12	Gen. 13
Gate Length	6 μm	6 μm	3 μm	3 μm
Res. Width	6 μm	3 μm	2 μm	1 μm
Contact Via	6 μm	6 μm	3 μm	2 μm
JFETs/Chip	~ 200	~ 1000	~ 3000	~ 10000
Die Width	3 mm	4.65 mm	5 mm	5 mm
Year	2017	2019	2022*	2023

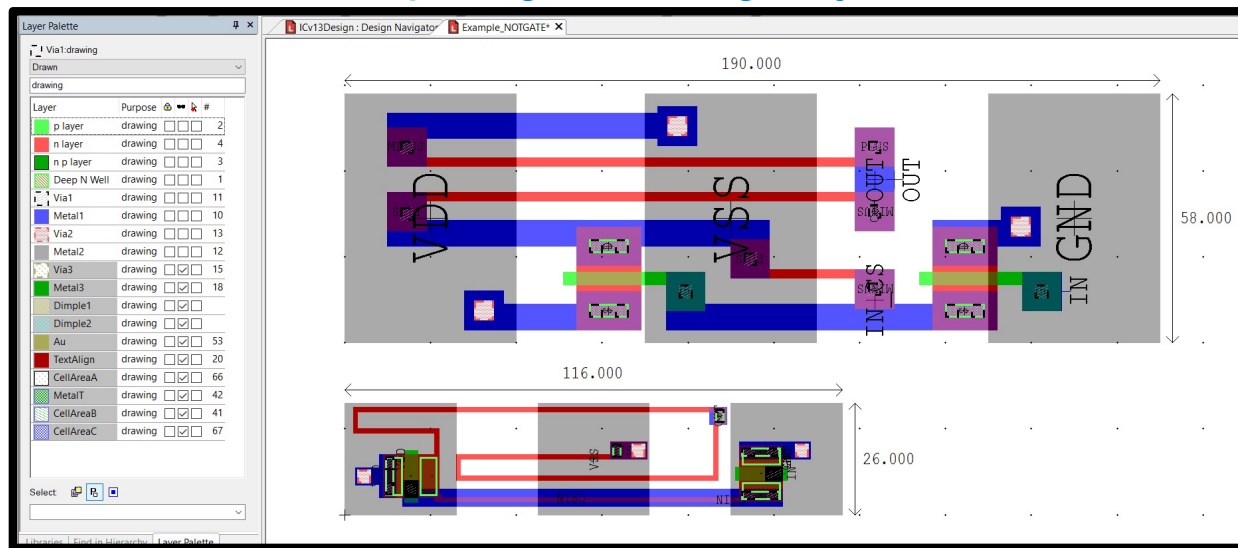
* Fabrication delayed by prolonged COVID-19 NASA Glenn SiC lab closure.

Shift from contact-aligner lithography to stepper lithography planned for IC Gen 13.



Online SiC JFET IC Design Guide

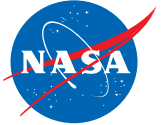
<https://go.nasa.gov/jfetic>



Gen. 12
NOT Gate Area
11021 μm^2

Gen. 13
NOT Gate Area
3016 μm^2

- SPICE models for circuit design and mask layout rules (Gen. 12 and Gen. 13)
- External partner IC designs are in Gen. 12 fabrication run (Space Act Agreements)
- Commercial SiC JFET-R IC design services available (<https://www.ozarkic.com>)

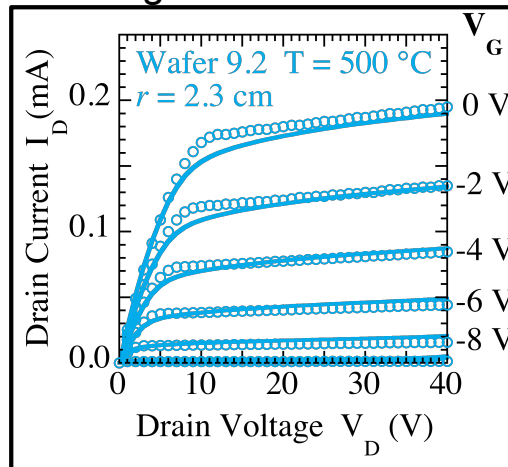


SPICE Modeling^{1,2}

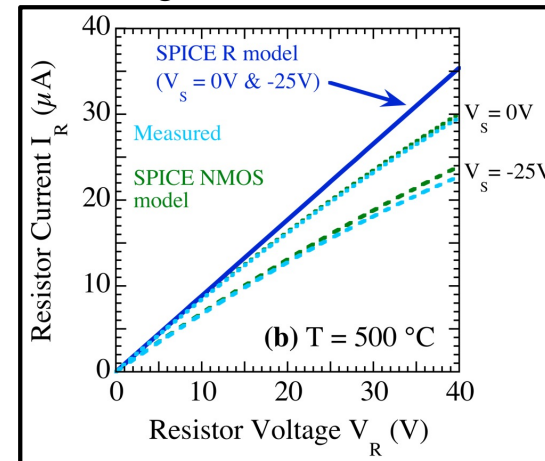
NASA Glenn models JFETs and Resistors using SPICE NMOS Level 1 device model.

- Matrix of models for key cases of temperature and wafer position.
 - Refined for each JFET-R IC generation using measurements and physics calculations.
 - First order accuracy only. Adequate given experimentally measured data scatter.
- **Substrate body bias effect very important!** (Especially since substrate biased at $V_{SS} \sim -25V$)

Integrated SiC JFET¹



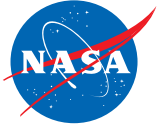
Integrated SiC Resistor²



Estimated SPICE models for present NASA Glenn Generation 12 IC run and upcoming Generation 13 run posted at <https://go.nasa.gov/jfetic>

¹P. Neudeck et al., 2016 IMAPS International High Temperature Electronics Conf. p. 263.

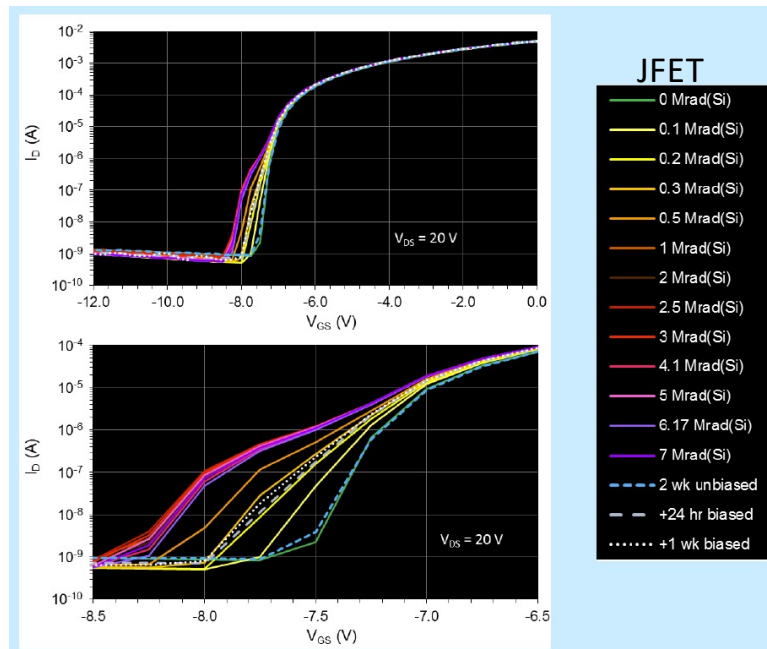
²P. Neudeck, Materials Science Forum 924 p. 962 (2018).



Radiation Testing of NASA Glenn JFET ICs¹

Generation 10 JFETs, Oscillators, Flip-Flops, Op-Amps tested by NASA Goddard

Total Ionizing Dose (Gamma)



Single Event Effects (Heavy Ion Strike)

Ring Oscillator

- No destructive effects at $\text{LET}(\text{Si}) = 86 \text{ MeV-cm}^2/\text{mg}$
- Only small glitches recorded

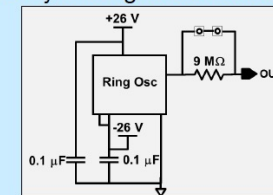


Fig.16. Ring oscillator test circuit.

Summary

Prototype 4H-SiC JFET ICs developed & fabricated at NASA GRC for harsh Venus conditions demonstrate potential for Jovian-type environments as well:

- > 7 Mrad(Si) TID tolerance
- No destructive SEE at $\text{LET}(\text{Si}) = 86 \text{ MeV-cm}^2/\text{mg}$
- SEUs occurred in the clock circuit
 - $3.5 \text{ MeV-cm}^2/\text{mg} \leq \text{onset LET}(\text{Si}) \leq 9.6 \text{ MeV-cm}^2/\text{mg}$

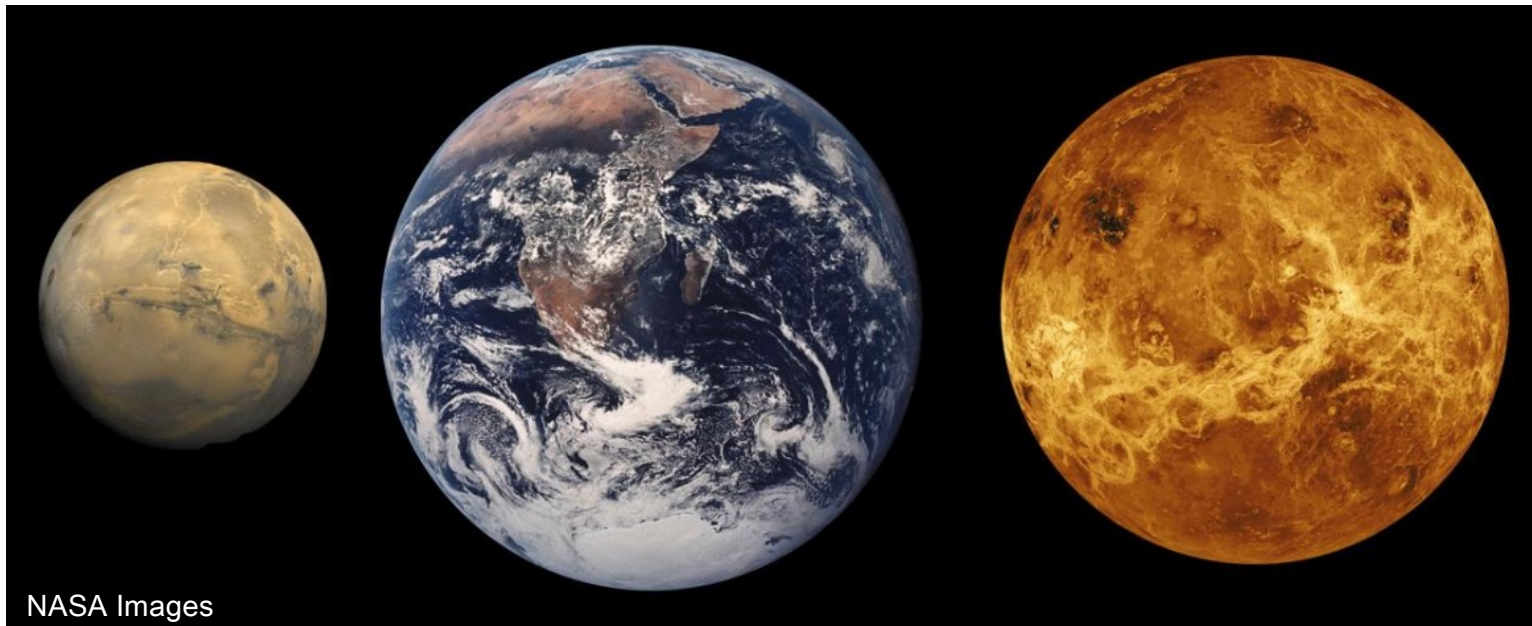
¹Lauenstein et. al., 2019 IEEE Radiation Effects Data Workshop (REDW)



Outline

- Introduction
- 500 °C Durable SiC IC Technology
- Impact on Venus Exploration

Which Planet is Earth's Closest Planetary Neighbor?



Mars

Mass: 10% Earth

Orbit: 150% Earth

T (surface): -143 °C to +35 °C

Lander Missions: Years of data

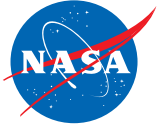
Venus (Radar Image)

Mass: 82% Earth

Orbit: 72% Earth

T (surface): +460 °C

Lander Missions: Hours of data



Surface of Venus: Toughest Place In Solar System

Combination of Temperature, Pressure, and Reactive Gas Extremes.

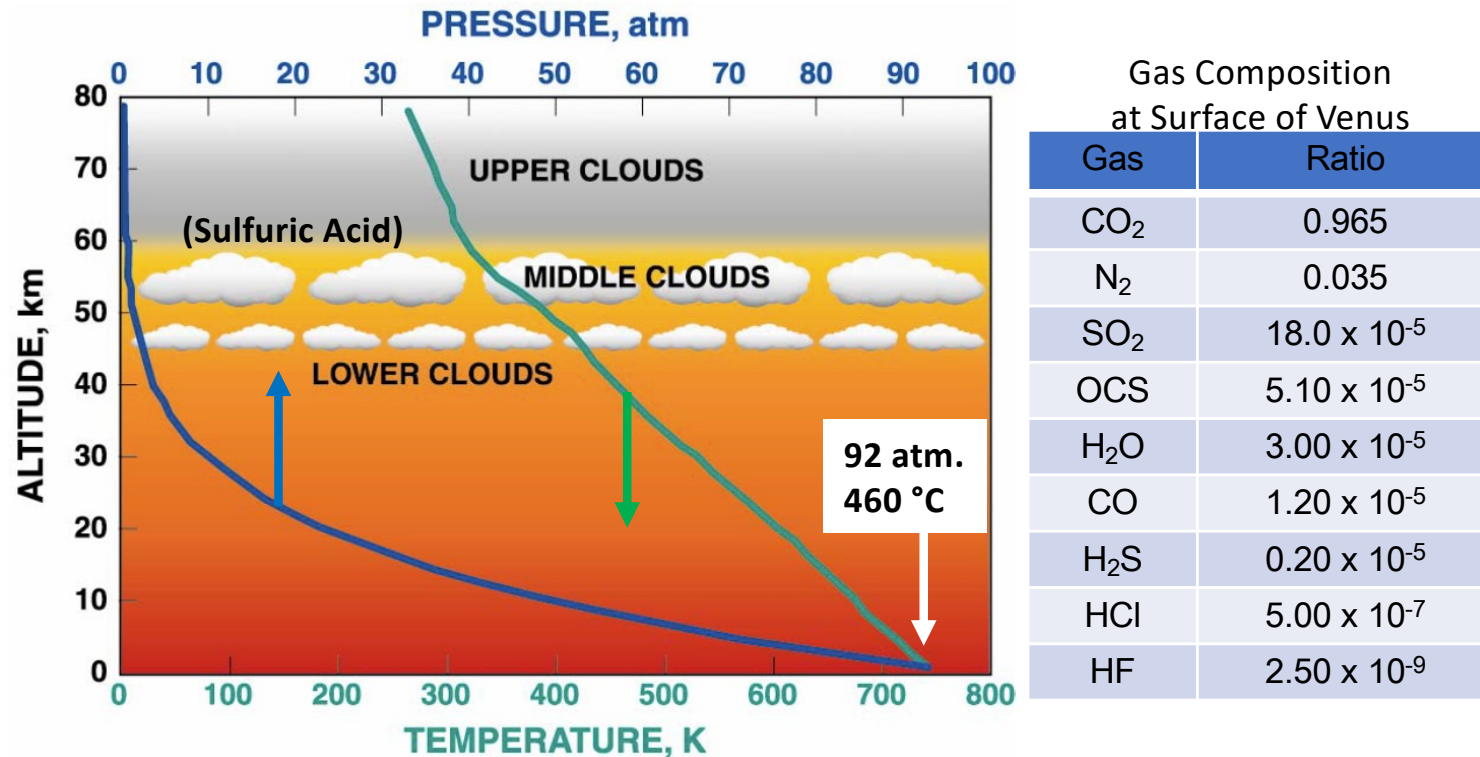


Figure modified from E. Kowala et al., Extreme Environment Technologies for Future Space Science Missions, NASA Jet Propulsion Laboratory, Pasadena, CA, USA, 2007, Report JPL D-32832. p. 49.



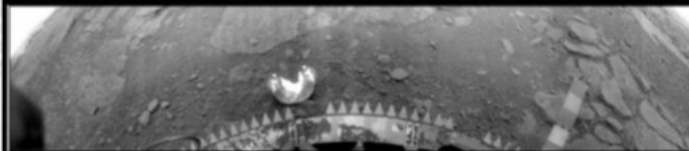
Past Missions: Close-up Surface Features on Venus (USSR)



Venera 9



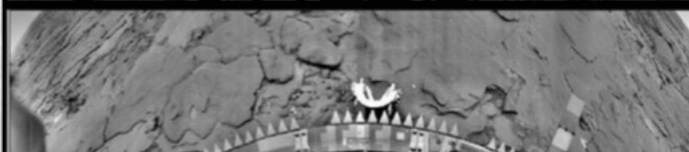
Venera 10



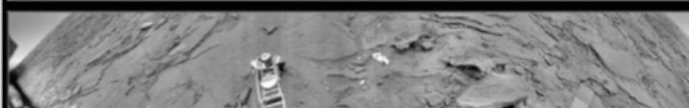
Venera 13A



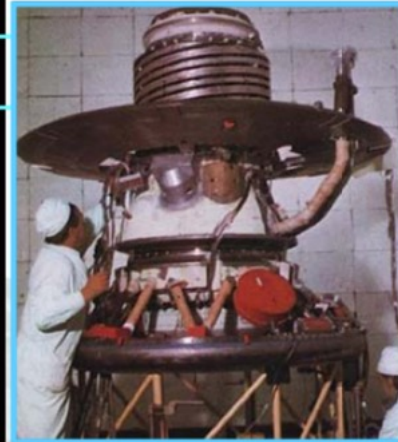
Venera 13B



Venera 14A



Venera 14B



Source: https://www.lpi.usra.edu/vexag/chapman_conf/presentations/ocampo_for_saunders.pdf

4





Past Missions:

Russian Venus Lander Missions (1965-1981)

Source: https://www.lpi.usra.edu/vexag/chapman_conf/presentations/ocampo_for_saunders.pdf



Venus	Year	Type / Method	Comment	Method EDL
Venera 3 <i>FAILED</i>	1965	Venus Lander	Impacted Venus, Contact Lost	Parachute
Venera 4 <i>FAILED</i>	1967	Venus Probe	Failed at altitude 24.96 km	Parachute ~ 380 kg, Capsule Crushed
Venera 5 <i>FAILED</i>	1969	Venus Probe	During parachute descent data was transmitted from the atmosphere for 53 minutes before failure	Parachute ~ 380 kg, Capsule Crushed
Venera 6 <i>FAILED</i>	1969	Venus Probe	During parachute descent data was transmitted from the atmosphere for 51 minutes before failure	Parachute ~ 380 kg, Capsule Crushed
Venera 7 <i>PARTIAL FAILURE</i>	1970	Venus Lander	35 minutes of data during descent, 23 min. weak signal from the surface (1 st man made object to return data after landing on another planet)	Aerobraking then parachute ~ 500 kg
Venera 8	1972	Venus Lander	Data during descent, plus 50 minutes after landing	Aerobraking/ D2.5m parachute at 60km ~ 500 kg
Venera 9	1975	Venus Orbiter and Lander	Operated for 53 minutes after landing	Protective hemispherical shell/ three parachutes/ disk shaped drag brake/ metal, compressible doughnutshaped landing cushion
Venera 10	1975	Venus Orbiter and Lander	Operated for 65 minutes after landing	See Venera 9 ~ 660 kg
Venera 11	1978	Venus Lander	Transmitted data after touchdown for 95 minutes, until it moved out of range with Earth.	Aerodynamic ~/ parachute ~/ atmospheric braking/ soft landing
Venera 12	1978	Venus Lander	Worked until out of range , transmitted from the surface for 110 minutes.	See Venera 11
Venera 13	1981	Venus Lander	The lander survived for 117 minutes.	Parachute/ at 47km parachute released/ aerobraking
Venera 14	1981	Venus Lander	The lander survived for 57 minutes	See Venera 13

The longest surface mission survived for almost 2 hours

NASA's Flagship Mission to Venus

A Future Mission Concept



Venus Flagship Science Themes and Objectives

Science Theme	Science Objective
What does the Venus greenhouse tell us about climate change?	Understand radiation balance in the atmosphere and the cloud and chemical cycles that affect it Understand how superrotation and the general circulation work Look for evidence of climate change at the surface
How active is Venus?	Identify evidence of current geologic activity and understand the geologic history Understand how surface/atmosphere interactions affect rock chemistry and climate Place constraints on the structure and dynamics of the interior
When and where did the water go?	Determine how the early atmosphere evolved Identify chemical and isotopic signs of a past ocean Understand crustal composition differences and look for evidence of continent-like crust

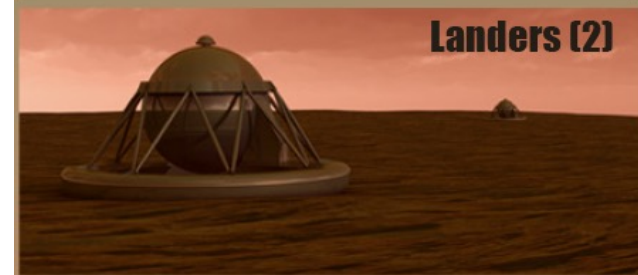
Science Payload for the Design Reference Mission

Orbiter	2 Balloons	2 Landers	
Lifetime (4 years)	(1 month)	Descent Phase (1–1.5 hour)	Landed Phase (5 hours)
InSAR — Interferometric Synthetic Aperture Radar	ASI — Atmospheric Science Instrument (pressure, temperature, wind speed.)	ASI	Microscopic imager
Vis-NIR Imaging Spectrometer	GC/MS — Gas Chromatograph / Mass Spectrometer	Vis-NIR Cameras with spot spectrometry	XRD / XRF
Neutral Ion Mass Spectrometer	Nephelometer	GC / MS	Heat Flux Plate
Sub-mm Sounder	Vis-NIR camera	Magnetometer	Passive Gamma Ray Detector
Magnetometer	Magnetometer	Net Flux Radiometer	Sample acquisition, transfer, and preparation
Langmuir Probe	Radio tracking	Nephelometer	Drill to ~10 cm
Radio Subsystem (USO — Ultra Stable Oscillator)			Microwave corner reflector

Mass (CBE + Cont.)
686 kg; Payload mass: 106.2 kg
Lander Design
0.9-m diameter titanium shell (1-cm wall thickness); Rotating pressure vessel; Drill to 10-cm (2 samples)
Thermal Design
Passive thermal management: Lithium nitrate phase change material (PCM); Silica insulation: 5-cm external; 1-cm internal; Carbon dioxide backfilled pressure vessel
Power
Lithium-thionyl chloride primary batteries (the same cells used on the balloons), (6 kWh, 12.6 kg)
Telecom
S-band LGA to Orbiter with Electra (backup to flyby s/c)
Functions
Descent science for ~1 hour; Surface science for 5 hours

Despite ~ 30-year technology update:

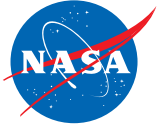
- Electronics remains environmentally shielded.
- Lander mass remains prohibitively large (686 kg).
- **5 hours of science on surface.**



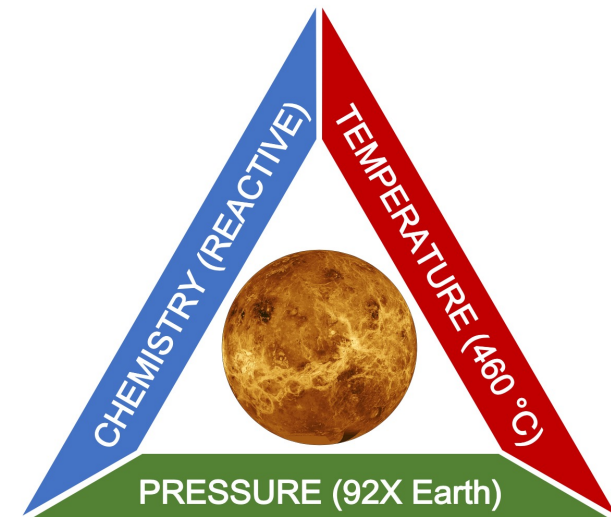
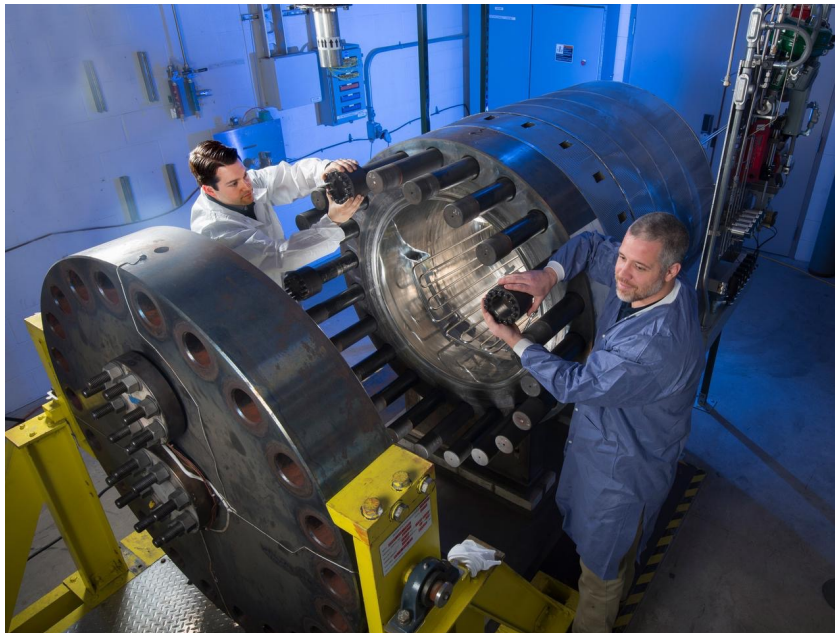
Landers (2)

NASA Glenn Extreme Environment Rig (GEER)

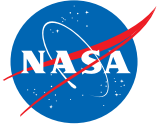
<https://geer.grc.nasa.gov>



800-liter test chamber for high-fidelity simulation of Venus surface environment



- **First 10 chemical constituents of Venus atmosphere.**
- **460 °C (860 °F), 1350 psia (~ 92 Earth atmospheres).**
- **Long duration (months) test runs.**

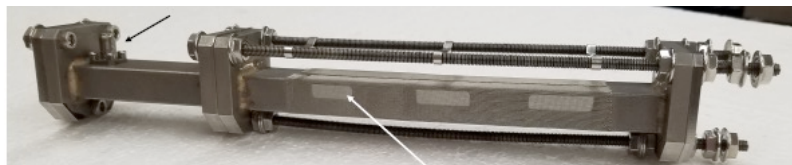


NASA Glenn GEER Testing Experience

Full surface conditions (including gas composition to small concentrations) is relevant!

Many commonly-used elements react badly. **Sulfidization instead of oxidation.**

Encapsulation/passivation of parts against Venus surface atmosphere is problematic.



Before
Test



After
Test



Large sulfide crystals formed on metal-alloy waveguide exposed to Venus surface conditions for 60 days in GEER.

Venus Atmosphere	
Gas	Ratio
CO ₂	0.965
N ₂	0.035
SO ₂	18.0 x 10 ⁻⁵
OCS	5.10 x 10 ⁻⁵
H ₂ O	3.00 x 10 ⁻⁵
CO	1.20 x 10 ⁻⁵
H ₂ S	0.20 x 10 ⁻⁵
HCl	5.00 x 10 ⁻⁷
HF	2.50 x 10 ⁻⁹

Evolving "Handbook" of Materials Reactions in Venus Surface Ambient

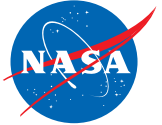
D. Lukco et al., Earth and Space Science 5, 270 (2018)

<https://agupubs.onlinelibrary.wiley.com/doi/full/10.1029/2017EA000355>



Table 1 What works and what doesn't

Devices	Materials	Outcome
Electronics Packaging	Pb	PbS
	Al ₂ O ₃	No reaction
Insulation	CaO	CaSO ₃ , CaSO ₄
SiC Electronics	Pt	PtS; fibers when present as thin film
	Pt (in the presence of Au)	PtS spheres
	Au	No reaction, but mobile
	Ir	No reaction, but mobile
	SiC	No reaction
	SiO ₂	No reaction
Feedthrough Materials	Cu	Cu ₂ S crystals
	Ni	NiS crystals
	CuBe	Cu ₂ S crystals on surface
SiC Pressure Sensor	Kovar (Ni-Co-Fe)	NiS, Fe _x O _y
	AlN	No reaction
	Ag-Cu Braze	segregation into Cu ₂ S and Ag; Ag mobile
GEER Components	Inconel 625 (Ni-Cr-Mo-Fe)	NiS, Cr _x O _y
	304 SS	Mirror finish, low corrosion rate
	Al foil/Mg doped	MgO on surface, MgF inner layer, Al bulk no reaction



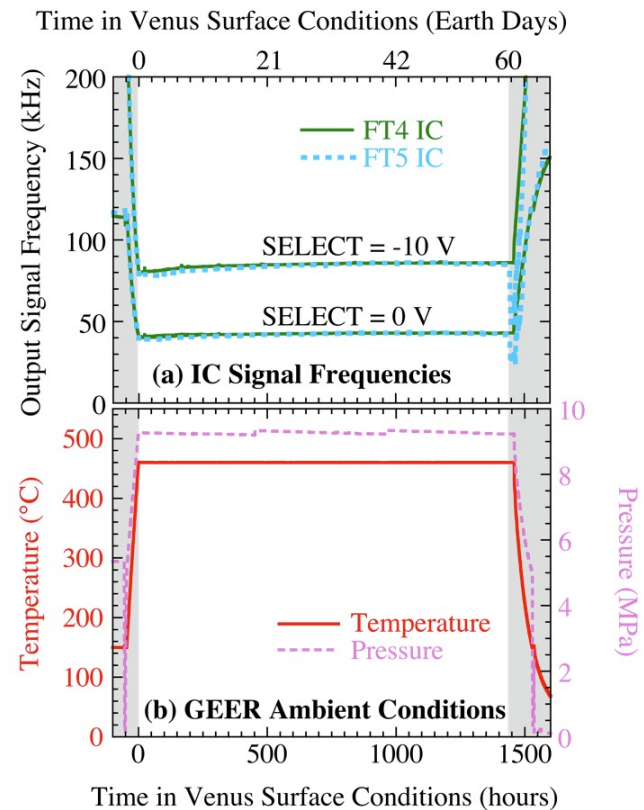
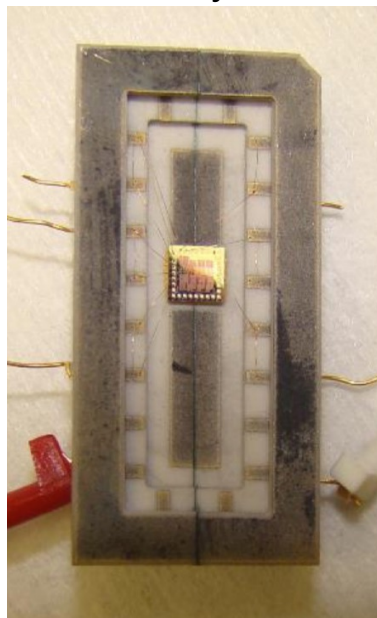
60-Day Venus Environment IC Test (in GEER)^{1,2}

Two Generation 10 $\div 2 \div 4$ Clock ICs (175 JFETs/chip) successfully operated in GEER Venus surface conditions for 60 days duration (lidless package).

Before GEER



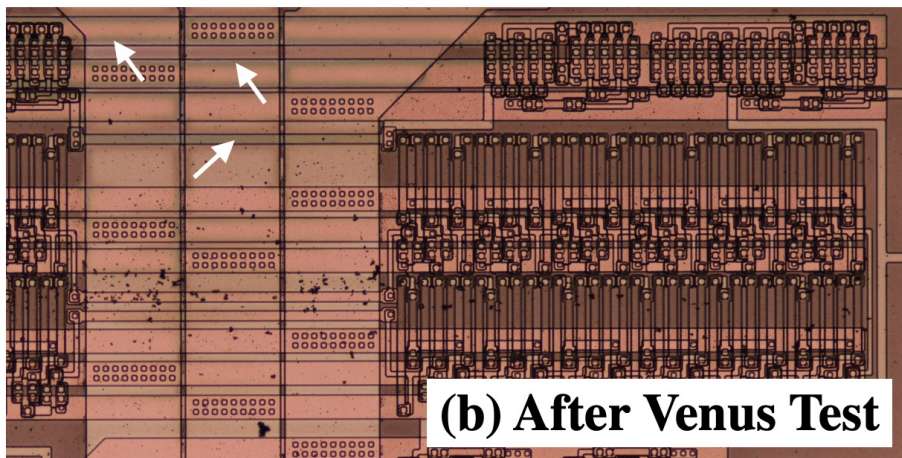
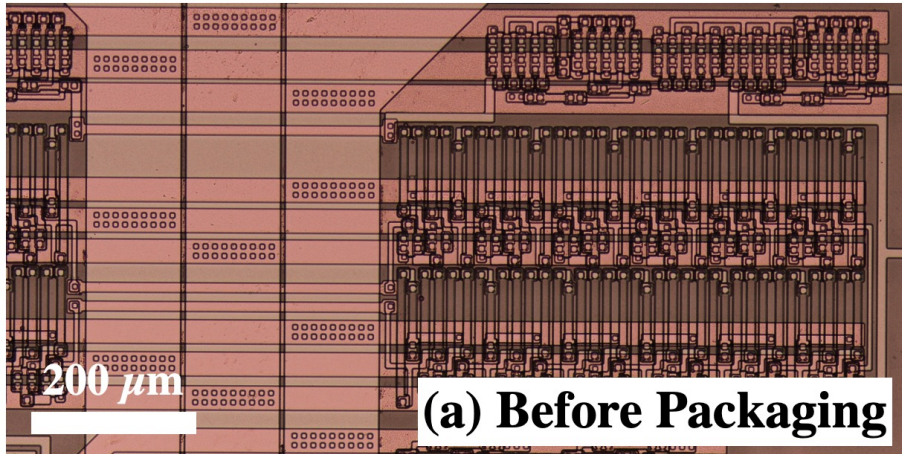
After 60 days GEER



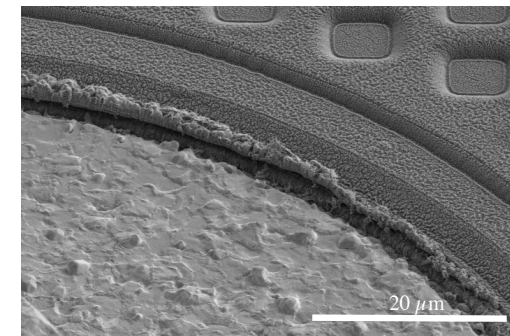
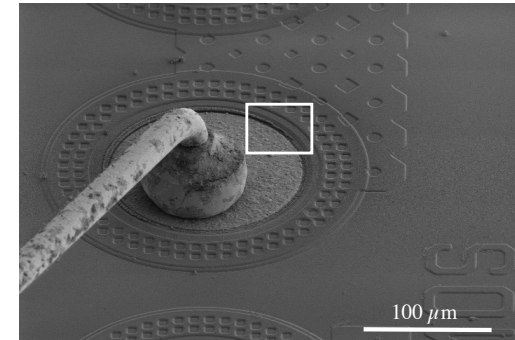
¹Neudeck et al., IEEE J. Electron Devices Soc., vol. 7, p. 100 (2018).

²Chen et al., Proc. 2018 Int. High Temperature Electronics Conf.

60-Day Venus Environment IC Test (in GEER)¹



Bondpad After Venus Test



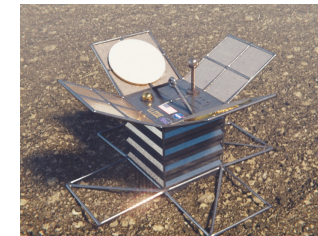
¹Neudeck et al., IEEE J. Electron Devices Soc., vol. 7 p. 100 (2018).

Impact of Extreme Environment SiC Electronics

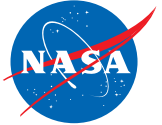


NASA Venus Flagship Lander Design Proposed in 2009
1 meter diameter Ti sphere to shelter silicon ICs and equipment
686 kg
5-hour surface mission

New Venus Lander Concept
Unsheltered SiC ICs
< 20 kg (mostly battery)
60-day surface mission



Completely new engineering approach enabled by Venus-durable SiC ICs.

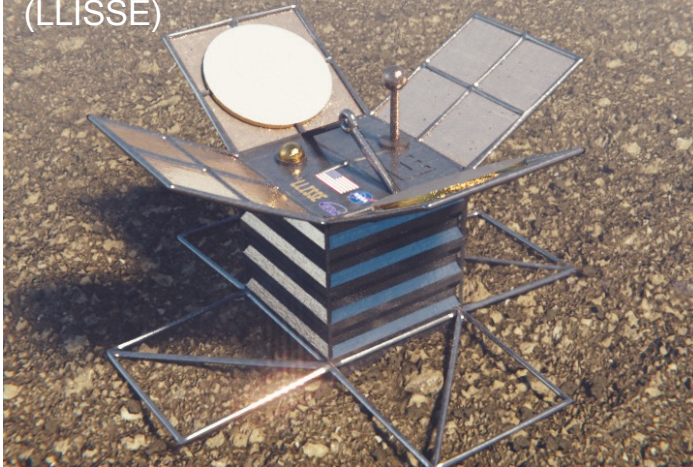


Revised NASA Vision for Venus Surface Exploration

Lightweight (< 20 kg) but Long-Duration (Months) NASA Venus Surface Mission Concepts

- SiC transistor-enabled by complete elimination of electronics protection measures
- Sporadic transmission of data to orbiter (sleep-mode, transmit-only communications)
 - Simple “state machine”, low power operation is key to mission duration
- Aiming for 2020’s first “Tech Demo” on Venus (after operational demonstrations in GEER)

Long-Lived In-Situ Solar System Explorer (LLISSE)



Temperature, pressure, wind, and gas composition over Venus day/night transition (60 Earth days)

<https://www.hou.usra.edu/meetings/lpsc2017/pdf/29864.pdf>

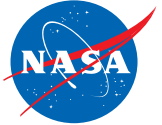
Seismic and Atmospheric Exploration of Venus (SAEVe)



Adds seismic and heat flux monitoring to LLISSE dataset, 120 Earth days mission

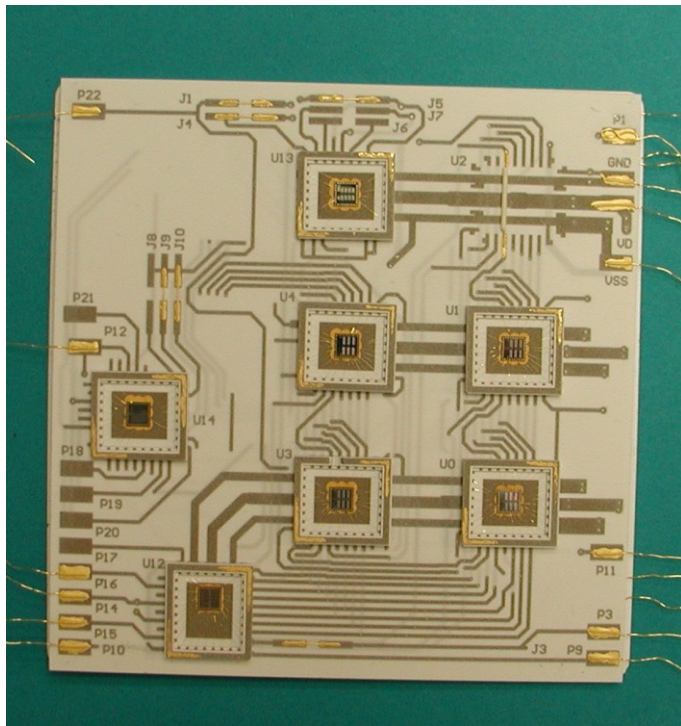
<https://www.hou.usra.edu/meetings/lpsc2018/pdf/2744.pdf>

Illustrations by J. Wrbanek, NASA Glenn

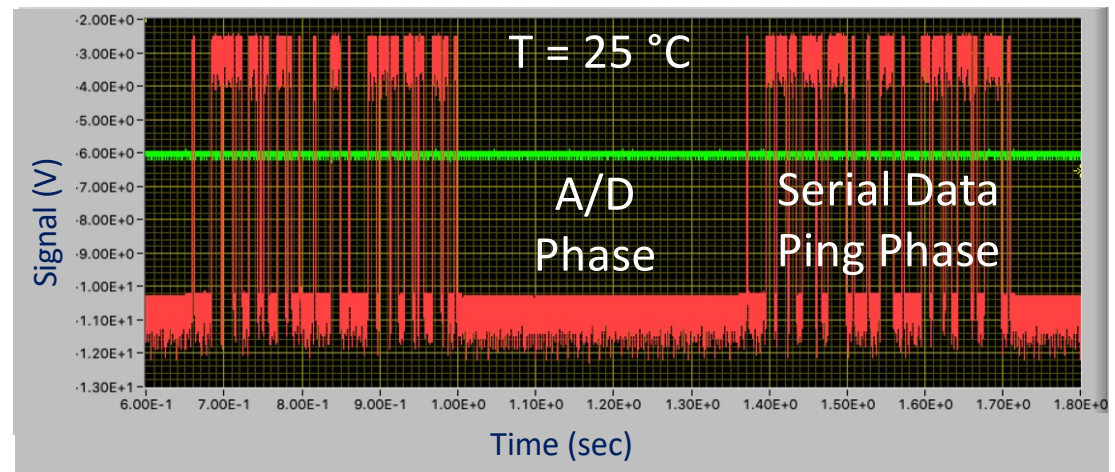


Prototype Venus Lander Circuit Board

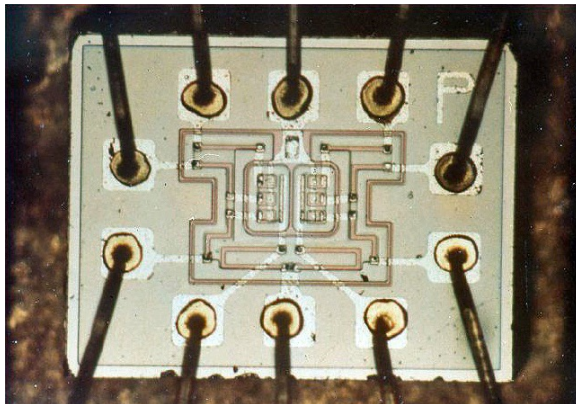
Simple “state machine” to digitize and serial data ping signals from analog sensors



8-bit A/D with serial data ping for 6 sensor channels
4-layer HTCC circuit board 4.5 inches x 4.5 inches
9 packages of Gen. 11.1 chips (7 topside, 2 underside)
Awaiting GEER Venus chamber test (Post-COVID)

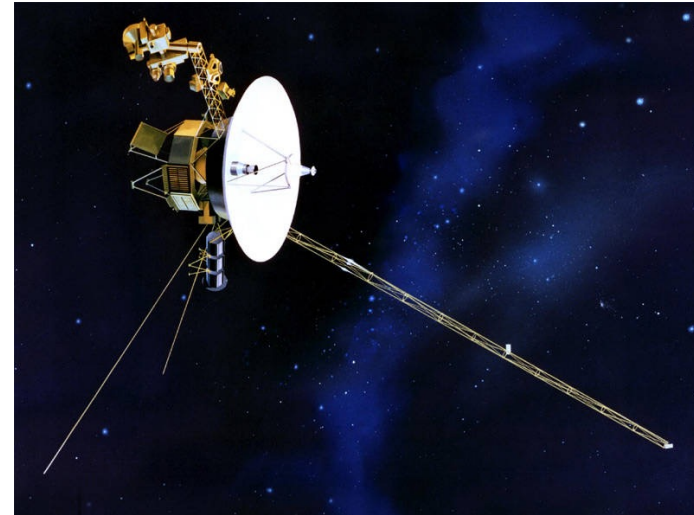


“Simple” ICs Explored The Solar System



David Thornley, Computer History Museum

<https://commons.wikimedia.org/wiki/File:ApolloGuidanceComputerwithDSKY.dwt.jpg>

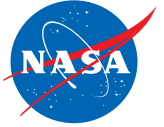


Apollo flew using 6 transistors per chip ICs.

Voyager spanned the solar system using few thousand transistors/chip ICs.

500 °C durable SiC ICs are already reaching a useful level of complexity.

Summary



SiC JFET-R ICs now demonstrating application-viable prolonged functionality in previously inaccessible extreme temperature environments.



Potentially “Go Anywhere” ICs

- High temperature +500 °C
- Low temperature -190 °C
- High radiation 7 MRad(Si)
- Venus surface +460 °C
- Analog and digital
- Ceramic packaging

Important new extreme environment operational capability becoming available.

<https://go.nasa.gov/sic>

<https://go.nasa.gov/jfetic>

