Single-Event Effects (SEE) Symposium
Military and Aerospace Programmable Logic Devices (MAPLD)
Combined Workshop

The Use of High Energy Heavy Ion Facilities for Single Event Effects (SEE) Testing: A Perspective on Return on Investment (ROI)

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Submission Type: SEE

Acronyms

- Atomic Mass Unit (amu)
- Brookhaven National Laboratories (BNL)
- Complementary Metal Oxide Semiconductor (CMOS)
- Device Under Test (DUT)
- Figure Of Merit (FOM
- Integrated Circuits (ICs)
- Lawrence Berkeley National Laboratories (LBNL)
- Linear Energy Transfer (LET)
- Minutes (min)
- NASA Space Radiation Laboratory (NSRL)
- Printed Circuit Board (pcb)
- Return on Investment (ROI)
- Single Event Effects (SEE)
- Texas A&M University (TAMU)

Abstract

- With challenges related to testing highly complex integrated circuits as well as entire systems continuing to grow, the use of higher energy heavy ions for single-event effects (SEE) testing becomes a critical technical need.
- This presentation, however, focuses only partially on the technical side with the main emphasis on the economics of using a high-energy heavy ion beam and comparing via notional cost models for testing.

Outline

- Assumptions: description of high energy heavy ion beams (energy/irradiation area)
- SEE test scenarios
- Test metrics and thoughts
  - Additional resource considerations: travel and workforce
  - Unique circumstance
- Summary

Assumptions: “High Energy” Heavy Ion SEE Test Facility

- For the purposes of this presentation, a high energy heavy ion SEE test facility is defined as having kinetic energy for ions of interest of >100 MeV/amu
  - There’s nothing magical about this definition, but simply something to use as a figure of merit (FOM)
- In addition and using a facility such as NASA Space Radiation Laboratory (NSRL) at Brookhaven National Laboratories (BNL) as an example, the beam diameter for irradiation is variable from individual integrated circuits (ICs) to moderate-sized assemblies.
- This is a SIMPLIFIED comparison: no specific discussion, for example, on test system design or device under test (DUT) board constraints, etc…

SEE Test Scenarios

- Baseline: traditional IC test
- Board-level test: testing of large amounts of individual ICs on a single test board
  - 2 sub-scenarios: using traditional one part at a time irradiation, then all samples at the same time
- Board-level test: functional purpose board (e.g., space computer)
- Board-level test: SEE mitigation validation
- Assembly or stacked board test

Caveat: all scenarios are notional in that the results are meant to viewed on a relative basis for comparison and not as hard and fast results for an actual specific device, board, or assembly.

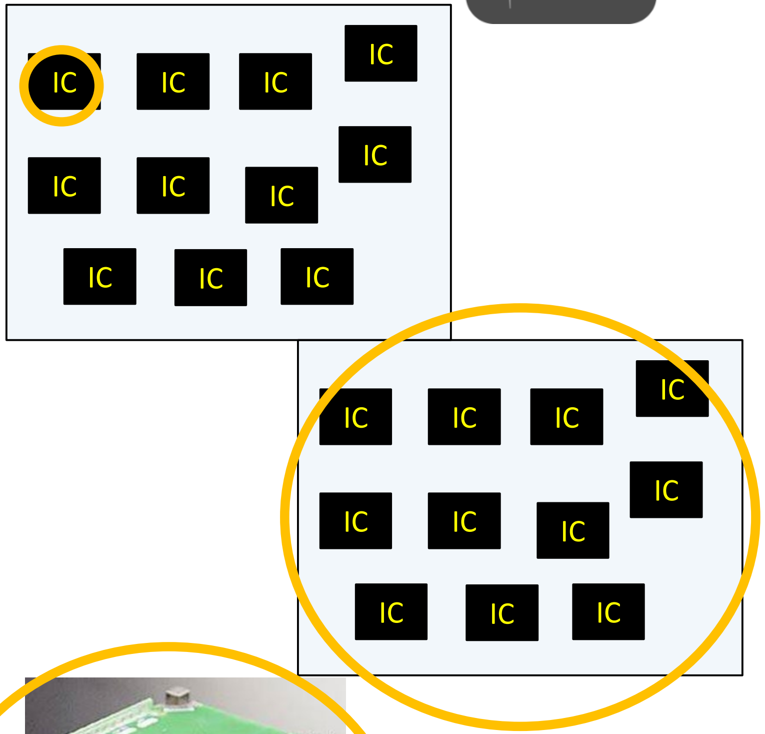
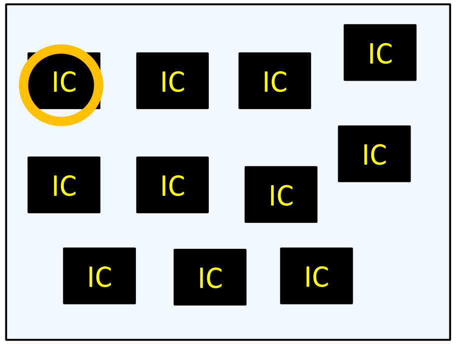


Image courtesy of Vanderbilt University

Scenario 1: Traditional IC Test

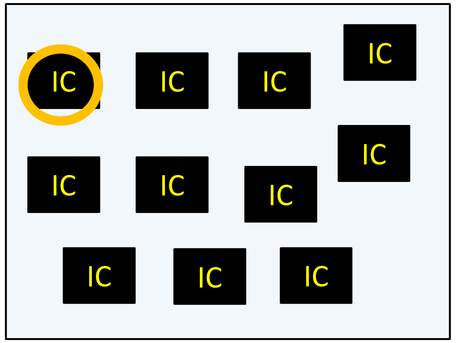


- This is the traditional test for an individual IC to use as frame of reference
- Assumptions:
  - 3 samples of the same device on the test board being irradiated in turn
  - 4 ions used with 2 energies and 3 angles (no board rotation)
  - 3 test runs per ion/energy/angle combination
  - No changes of power supply voltage or temperature
  - Setup and teardown time not included

Standard single IC test	Value
# of samples on the same board	3
# of ions	4
# of energies per ion	2
# of test runs (per ion/energy/angl	3
# of angles (per ion/energy)	3
Avg time per test run - min	2
Avg time between test runs - min	1
Ion change time - min	30

216	# of test runs
648	Beam run time in minutes
12.3	Total hours needed for test

Scenario 2a: Traditional IC Test w/ Sample Size of 15 devices

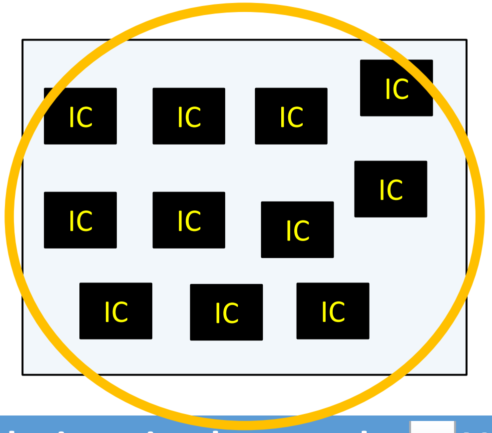


- This is the traditional test for an individual IC to use as frame of reference
- Assumptions:
  - 15 samples of the same device on the test board being irradiated in turn
  - 4 ions used with 2 energies and 3 angles (no board rotation)
  - 3 test runs per ion/energy/angle combination
  - No changes of power supply voltage or temperature
  - Setup and teardown time not included

Irradiate each device in turn	Value
# of test parts on the board	15
# of boards	1
# of ions	4
# of energies per ion	2
# of test runs (per ion/energy/angl	3
# of angles (per ion/energy)	3
Avg time per test run - min	2
Avg time between test runs - min	1
Board change time in minutes	45
Ion change time - min	30

1080	**# of test runs**
3240	**Beam run time in minutes**
55.5	**Total hours needed for test**

Scenario 2b: Irradiate Sample Size of 15 Devices Simultaneously



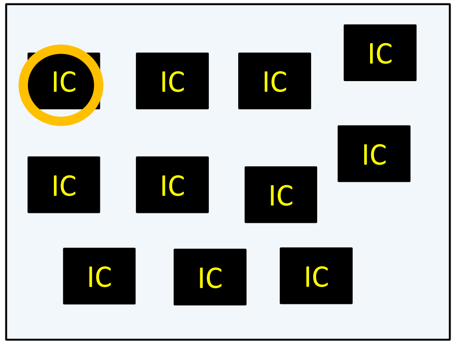
- This is a board level irradiation of entire board
- Assumptions:
  - 15 samples of the same* device on the test board being irradiated **simultaneously**
  - 4 ions used with 2 energies and 3 angles (no board rotation)
  - 3 test runs per ion/energy/angle combination
  - Assumes lower flux for larger beam: 4x longer test run needed
  - No changes of power supply voltage or temperature
  - Setup and teardown time not included

* = can be different devices (increases test system complexity)

Irradiate all devices simultaneously	Value
# of test parts on the board	15
# of boards	1
# of ions	4
# of energies per ion	2
# of test runs (per ion/energy/angle)	3
# of angles (per ion/energy)	3
Avg time per test run - min	8
Avg time between test runs - min	1
Board change time in minutes	45
Ion change time - min	30

72	# of test runs
648	Beam run time in minutes
12.3	Total hours needed for test

Scenario 2c: Traditional IC Test w/ Sample Size of 45 devices

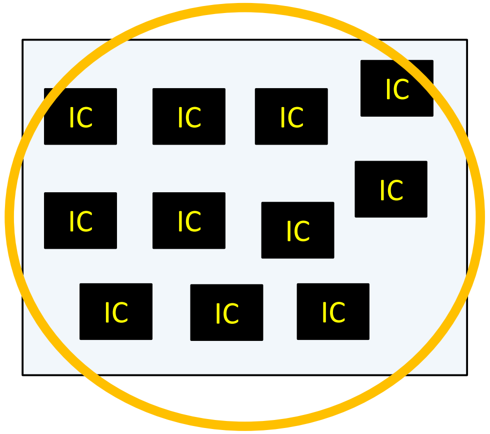


- This is the traditional test for an individual IC to use as frame of reference
- Assumptions:
  - 15 samples of the same device on the test board being irradiated in turn
  - 3 boards
  - 4 ions used with 2 energies and 3 angles (no board rotation)
  - 3 test runs per ion/energy/angle combination
  - No changes of power supply voltage or temperature
  - Setup and teardown time not included

Irradiate each device in turn	Value
# of test parts on the board	15
# of boards	3
# of ions	4
# of energies per ion	2
# of test runs (per ion/energy/angl	3
# of angles (per ion/energy)	3
Avg time per test run - min	2
Avg time between test runs - min	1
Board change time in minutes	45
Ion change time - min	30

3240	# of test runs
9720	Beam run time in minutes
168	Total hours needed for test

Scenario 2d: Irradiate Sample Size of 45 Devices w/ One Board at a Time

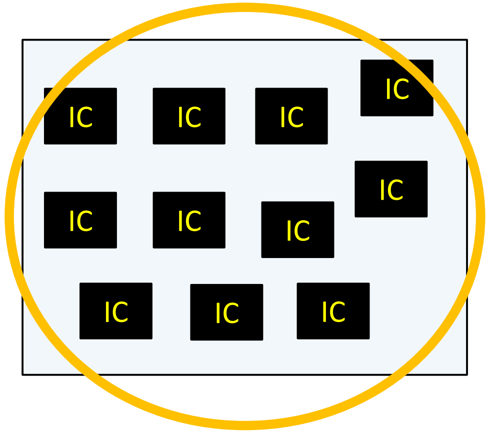


- This is a board level irradiation of entire board
- Assumptions:
  - 15 samples of the same device on the test board being irradiated **simultaneously**
  - 3 boards
  - 4 ions used with 2 energies and 3 angles (no board rotation)
  - 3 test runs per ion/energy/angle combination
  - Assumes lower flux for larger beam: 4x longer test run needed
  - No changes of power supply voltage or temperature
  - Setup and teardown time not included

Irradiate all devices simultaneously	Value
# of test parts on the board	15
# of boards	3
# of ions	4
# of energies per ion	2
# of test runs (per ion/energy/angle)	3
# of angles (per ion/energy)	3
Avg time per test run - min	8
Avg time between test runs - min	1
Board change time in minutes	45
Ion change time - min	30

216 **# of test runs**
1944 **Beam run time in minutes**
38.4 **Total hours needed for test**

Scenario 3: Irradiate a Functional Board

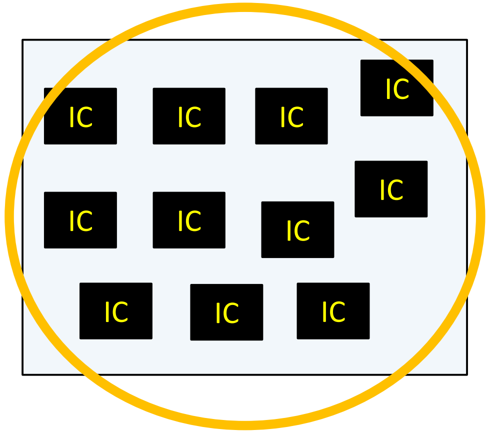


- This is a board level irradiation of entire board
- Assumptions:
  - DUT is entire board
  - 4 ions used with 2 energies and 3 angles (no board rotation)
  - 3 test runs per ion/energy/angle combination
  - Assumes lower flux for larger beam: 4x longer test run needed
  - Assumes additional test runs needed for statistics
  - No changes of power supply voltage or temperature
  - Setup and teardown time not included

Irradiate all devices simultaneously	Value
# of test parts on the board	
# of boards	1
# of ions	4
# of energies per ion	2
# of test runs (per ion/energy/angle)	12
# of angles (per ion/energy)	3
Avg time per test run - min	8
Avg time between test runs - min	1
Board change time in minutes	45
Ion change time - min	30

288	# of test runs
2592	Beam run time in minutes
44.7	Total hours needed for test

Scenario 4: Irradiate a Board w/SEE Mitigation (aka, *validation test*)



- This is a board level irradiation of entire board
- Assumptions:
  - DUT is entire board
  - 2 ions used with 1 energy and 2 angles (no board rotation)
  - 3 test runs per ion/energy/angle combination
  - Assumes lower flux for larger beam: 4x longer test run needed
  - Assumes additional test runs needed for statistics
  - No changes of power supply voltage or temperature
  - Setup and teardown time not included

Irradiate all devices simultaneously	Value
# of test parts on the board	
# of boards	1
# of ions	2
# of energies per ion	1
# of test runs (per ion/energy/angle)	12
# of angles (per ion/energy)	2
Avg time per test run - min	8
Avg time between test runs - min	1
Board change time in minutes	45
Ion change time - min	30

48	**# of test runs**
432	**Beam run time in minutes**
7.7	**Total hours needed for test**

Scenario 5: Irradiate an Assembly or Board Stack

- This is notionally the same as Scenario 3 – Functional Board Test
  - Numbers (hours/runs) should be similar, but may vary depending on statistics and physics
- Caveat
  - Detailed transport analyses should be considered for both test design and analysis
  - Modeling highly recommended

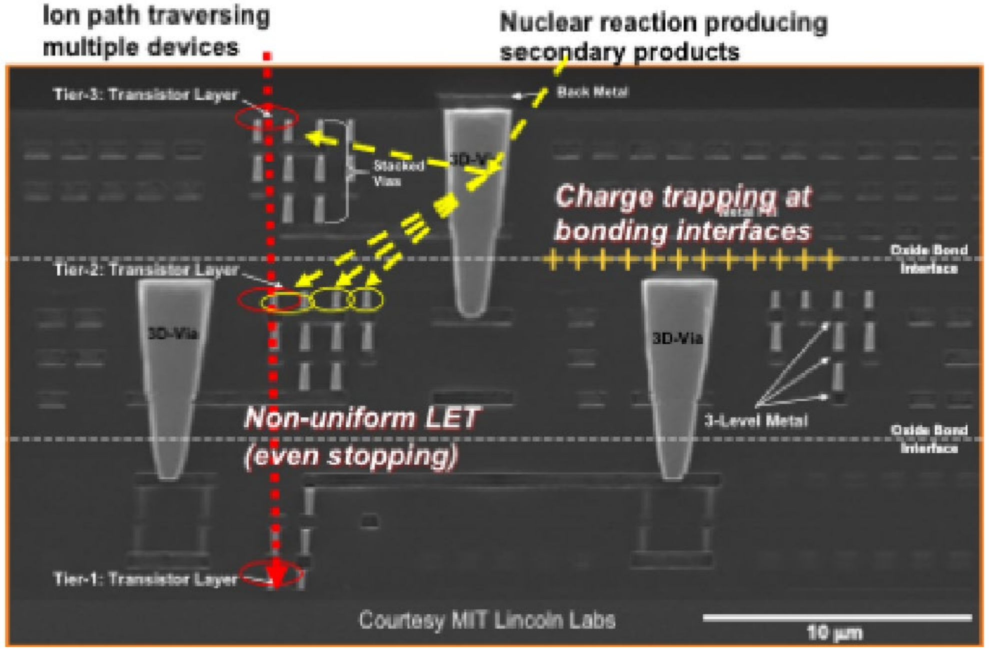


Image courtesy of Vanderbilt University

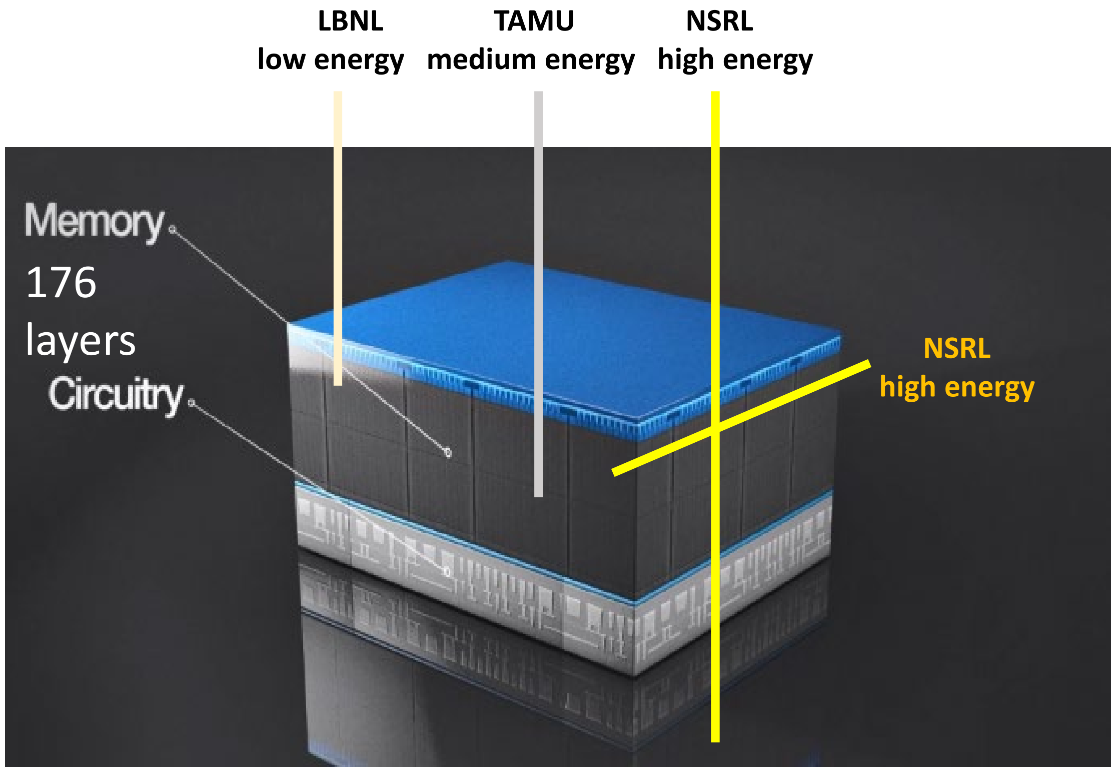
Test Metrics and Thoughts - 1

- Beam hour ratio of 4:1 (traditional to large beam)
  - Total beam costs are approximately the same (based on notional facility hour costs), however,
  - Travel and workforce hours for test performance is significantly higher for a traditional test version
    - If a large beam test takes 1 day, you'd save 3 days of test performance time needed versus a traditional part level test (4 days)
    - Test workforce may also be smaller if sufficiently lower amount of test time is needed
      - 8 hours and one shift versus 32 hours and "2" painful shifts with overtime
- Device Deprocessing
  - Not needed for high energy (typically), but often needed for traditional testing
    - $$$ at risk due to deprocessing failures

To be clear, these are notional "relative" comparisons

Test Metrics and Thoughts - 2

- Example capabilities not available elsewhere
  - Large field beam tests (system) require a unique facility and high energy
    - Do you really want to deprocess expensive parts already mounted on an expensive printed circuit board (pcb)?
  - Full 3D part test capability
  - Oblique angle testing
  - Backside testing



Micron's proprietary CMOS-under-Array technique constructs the multilayered stack over the chip's logic, packing more memory into a tighter space and shrinking 176-layer NAND's die size, yielding more gigabytes per wafer.

Courtesy of Micron , https://www.eetimes.com/micron-leapfrogs-to-176-layer-3d-nand-flash-memory/#

Conclusions

- The bottom line is that both standard piece part level testing and high-energy heavy ion testing will be needed in the future
- This presentation made the argument that there are scenarios where the ROI for high-energy makes sense for large field tests and large sample size tests
- There are also unique capabilities where a high energy source is required to sufficiently test complex devices

<u>Opinion</u>

Guidelines should be developed on best practices for high energy SEE testing