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SEE Test Report for Texas Instruments TLV5618 2.7-V to 5.5-V Low-Power Dual 12-Bit Digital-to-Analog Converter with Power Down

Raymond Ladbury

June 2021

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Raymond Ladbury
Goddard Space Flight Center, Greenbelt, MD

Test Engineer: Ted Wilcox
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Goddard Space Flight Center
Greenbelt, Maryland 20771

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1. Reference Documents

- TLV5618 Datasheet, http://www.ti.com/lit/ds/symlink/tlv5618a.pdf ,9/15/2014
- Malou, F., “Compendium of TID and SEL Test Results for Various Candidate Spacecraft Electronics,” Radiation and Its Effects on Components and Systems, 2007. RADECS 2007. 9th European Conference on, Sept. 10-14, 2007, Deauville, France.
- Johnston, A.H.; , "The influence of VLSI technology evolution on radiation-induced latchup in space systems," *IEEE Trans. Nucl. Sci.*, vol.43, no.2, pp. 505-521, Apr 1996.
- "IEEE Recommended Practice for Latchup Test Methods for CMOS and BiCMOS Integrated-Circuit Process Characterization," *IEEE Std 1181-1991*. (Deprecated)
- JEDEC JESD57

2. Purpose

The primary purpose of this testing was to characterize the Texas Instruments TLV5618 12-bit digital-to-analog converter (DAC) for single-event latchup (SEL) susceptibility. These data will be used to assess the SEL risk for the OSIRIS-REx Laser Altimeter (OLA). A secondary goal is to assess the susceptibility of the DAC to single-event transients (SET), single-event upsets (SEU), and other nondestructive SEE. Note that this device has already been shown to be SEL-susceptible (see Malou reference).

3. Test Samples

Six (6) parts were being provided to Code 561 for de-encapsulation and SEL testing. Two devices survived the process of de-encapsulation and were exposed to heavy ion irradiation. More information about the devices can be found in Table I.

The parts were prepared for testing by removing the plastic encapsulation from the target die. The parts were fabricated in bulk CMOS technology. Since we do not know the number of overlayers used in these processes, linear energy transfer calculations were recorded based on the top-surface incident ion species and kinetic energy, and we ensured that the particles had a range in Si of more than 100 microns from the top of the die.

Table I: Part Identification Information

Qty	Part Number	LDC	Source	Package
2 after thinning	TLV5618	0801A	Texas Instruments	8-pin SOIC

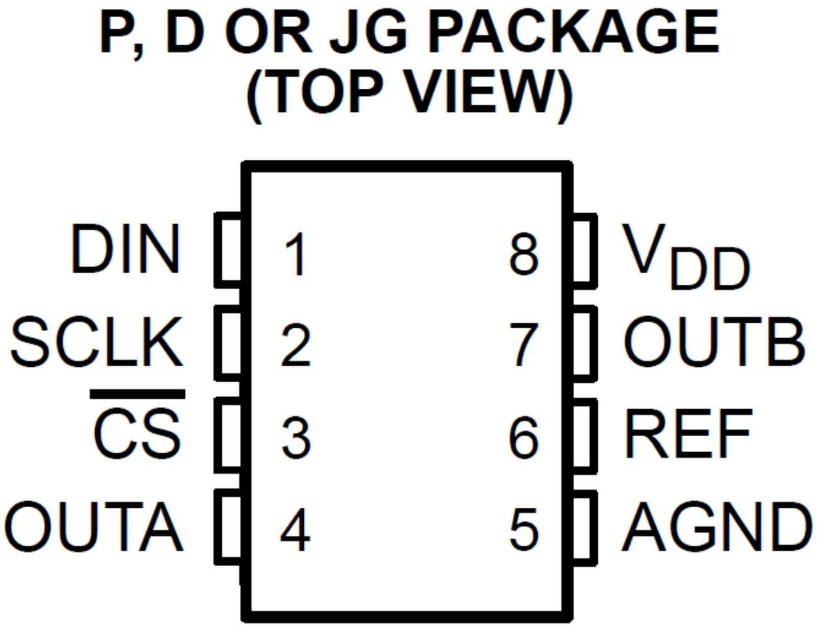

Figure 1: Pin diagram for TLV5618 DAC

4. Test Facility

Facility: Texas A&M University Radiation Effects Facility. Tune: 15 MeV/amu
Flux: 5×10^3 to 5×10^5 ions cm^{-2} s^{-1}
Fluence: All tests will be run to a fluence of 1×10^7 cm^{-2} or until a latchup event is observed

Table II: Possible Ions Used for Device Irradiation

Ion	Energy (MeV)	Range in Silicon	Silicon LET (MeV cm^2/mg)
^{197}Au	2954	155	80.2
^{129}Xe	1934	156	47.3
^{109}Ag	1634	156	38.5
^{84}Kr	1259	170	25.4
^{40}Ar	599	229	7.7
^{20}Ne	300	316	2.5

Note that energy, range, and LET are those characteristic of ions before traversing the aramica window and 50 mm of air prior to the silicon target.

5. Test Conditions and Error Modes

Table III: Test Conditions for TLV5618

	TLV5618
Test Temperature	Ambient and 75° C
Operating Frequency	20 kHz
Power Supply Voltage	3.3,5.5 Vdc
Parameters of Interest	LET_{th}, temperature, supply voltage
SEE Conditions	Prolonged and self-sustained high-current state, SETs

Current limit was set to 110% of maximum application rating.

6. Test Methods

The test circuits for all three devices were built to approximate the intended application. The accompanying figure captures the essentials of the application.

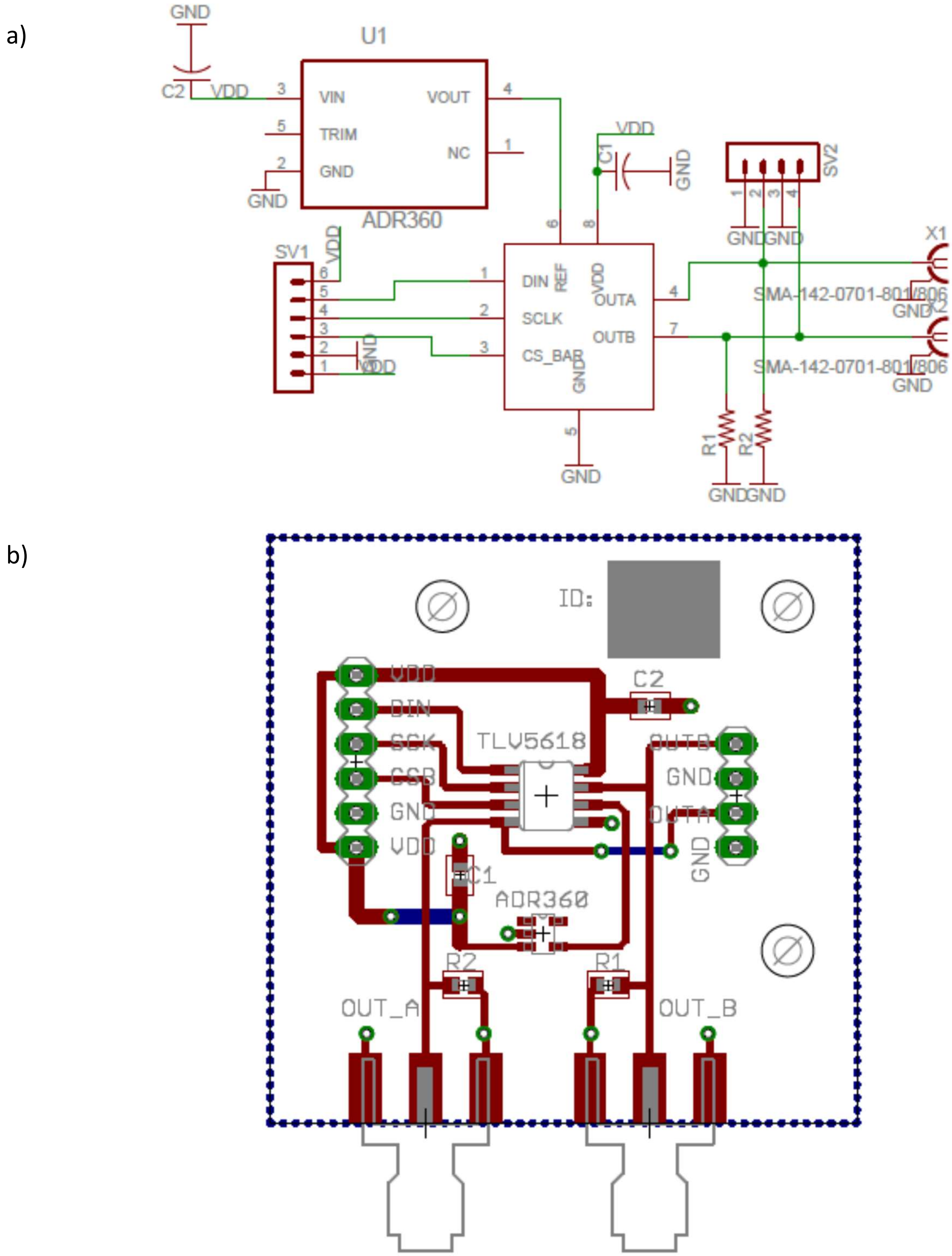

Figure 2: a) Simplified schematic and b) daughter card layout for TLV5618

The test setup requires only power supplies and data logging equipment. The power supplies were in the irradiation cave, while the data logging equipment were in the control room. Each test board had a single device under test, with new samples switched by hand.

7. Test Performance

Test personnel included the principal investigator and the test engineer. Eight hours were allotted for the test. A test was stopped if an SEL was seen or if the effective fluence reached 1×10^7 ions/cm^2. The following table is a rough outline of the tests planned during the test slot.

Table IV: Test Condition Plan

Condition	Temp (°C)	Tilt (°)	Roll (°)	Ion	Notes
1	75	0	0	Ne, Ar, Kr, Au,	Worst-case temp. , normal incidence
2	75	30,45,60	0	Ne, Ar, Kr, Au,	Repeat first condition at steeper angles
3	25	0	0	Ne, Ar, Kr, Au	Nondestructive SEE + SEL ambient temp. behavior

8. Results and Test Report

SETs were seen down to the lowest test linear energy transfer (LET): Ne at normal incidence with an LET of 1.8 MeVcm^2/mg. SEUs were seen starting at an LET of 5.7 MeVcm^2/mg (Ar at normal incidence). An SEU required the digital code to be rewritten to recover normal functionality. Some errors caused shifts in output A or output B alone while some affected both outputs. Some errors cause the loss of either output A or output B. No SEL was seen for LET values below 11.4 MeVcm^2/mg (Ar at 60° to the normal). The two test parts performed similarly. Figure 3 shows the cross section vs. LET curves for SET and SEU. Figure 4 shows the SEL cross section vs. LET for the parts. Based on the fits to these data, we anticipate that the SET rate for this part will be less than once per device, an SEU rate of less than once in 40 years per device and an SEL rate of less than once in 100 years per device. Based on the low onset LET for all three phenomena, it is possible that protons could also cause these effects. As such, during solar particle events, these rates could be a factor of 1000 or more higher for a period of up to a few days.

We note that the results obtained in this test are roughly consistent with those of Malou in 2012. Although Malou did observe SEL at lower LET than we did, the fit to the data suggests a very slowly saturating cross section vs. LET curve and a low onset (~2.5 MeVcm^2/g). This coupled with the fact that the two devices tested yielded consistent results suggests that part-to-part (as well as lot-to-lot) variation is not significant.

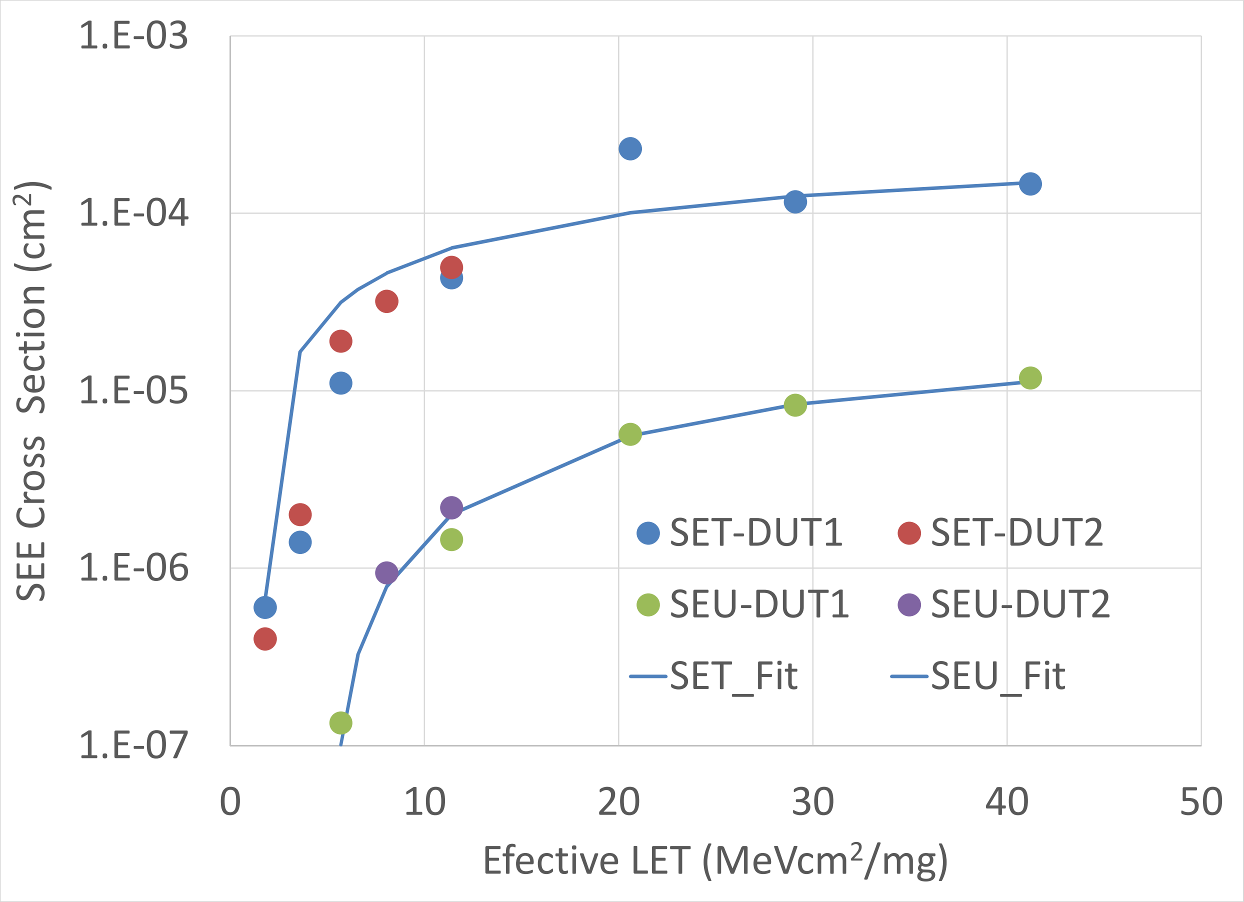

Figure 3: SEU and SET cross section vs. LET

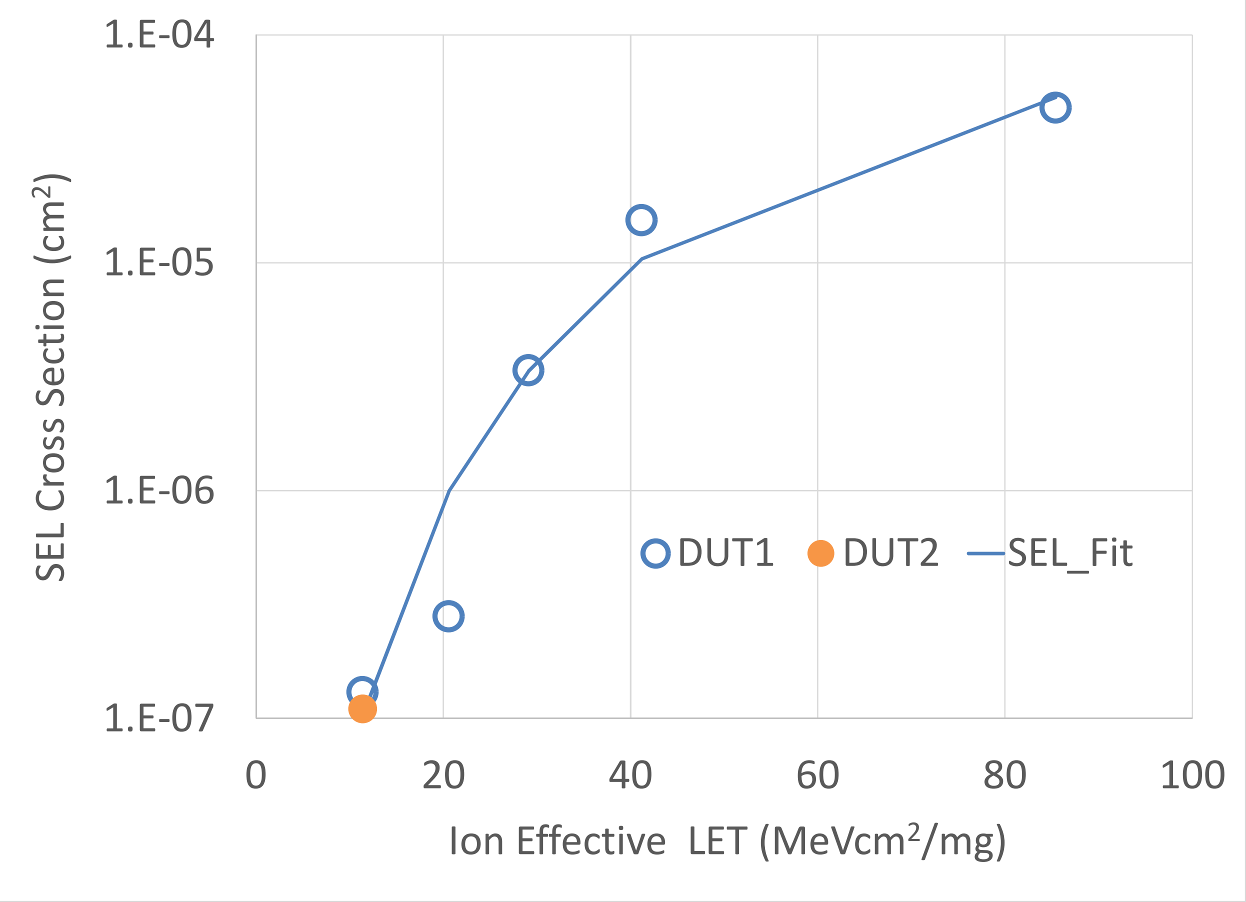

Figure 4: SEL cross section vs. LET

9. Implications of Results

The onset LETs for SET, SEU and SEL are low for these devices, the saturated cross sections are low, resulting in low rates for these error/failure modes. These rates are sufficiently low that they are unlikely to significantly affect performance of OLA during the active phase of the mission unless this phase coincides with high solar activity. Moreover, the consistency of the results between the two parts tested here and the previous test done by Malou, et al. suggests that the test results here will be representative of flight parts. The main concern for use of these parts would occur during solar particle events, during which error and failure rates could rise by more than 1000x. This factor depends critically on the shielding of these devices. If the devices are heavily shielded, the increase over quiescent solar periods would be much smaller.