

Safe and Precise Landing – Integrated Capabilities Evolution (SPLICE) Descent and Landing Computer (DLC)

Space Computing Conference

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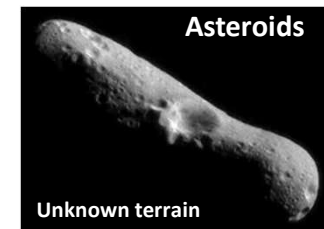
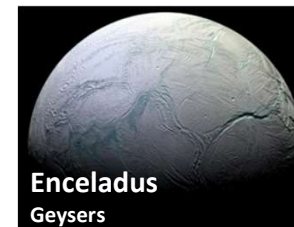
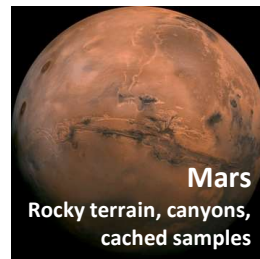
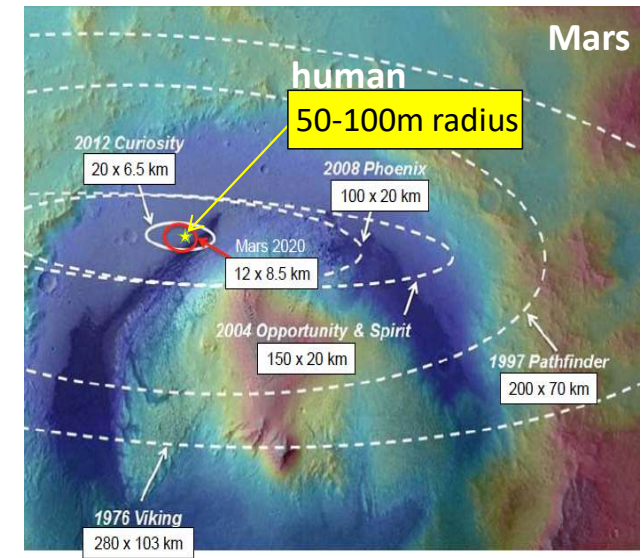
Outline



- Introduction to PL&HA and SPLICE
- SPLICE Descent and Landing Computer (DLC)
 - Engineering Design Unit (EDU)
 - Engineering Test Unit (ETU)
- Future work

The Motivation for PL&HA Technology

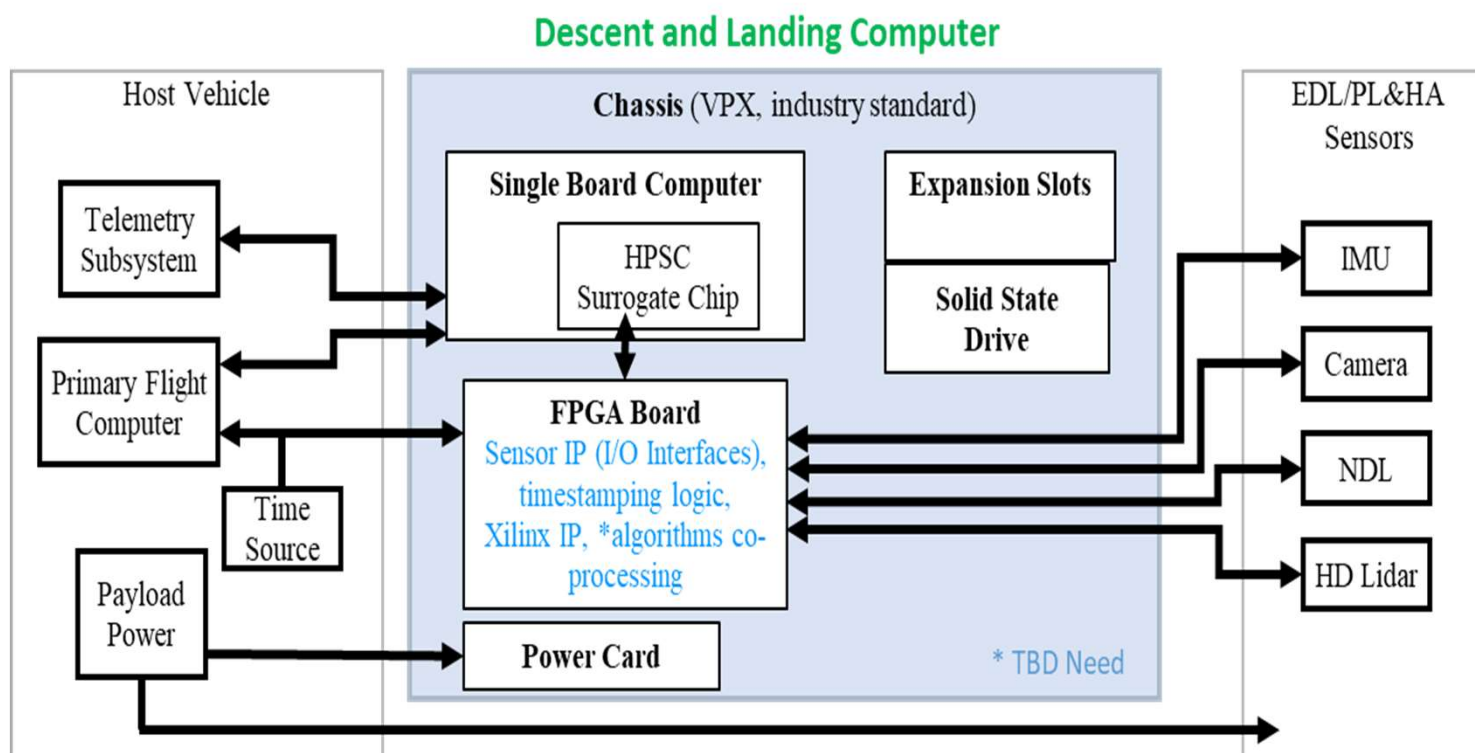
- Enable landing at locations that pose significant risk to vehicle touchdown or payload deployment (including near pre-positioned surface assets)
 - Multicore Processing
 - HPSC
 - Technology development (SPLICE)



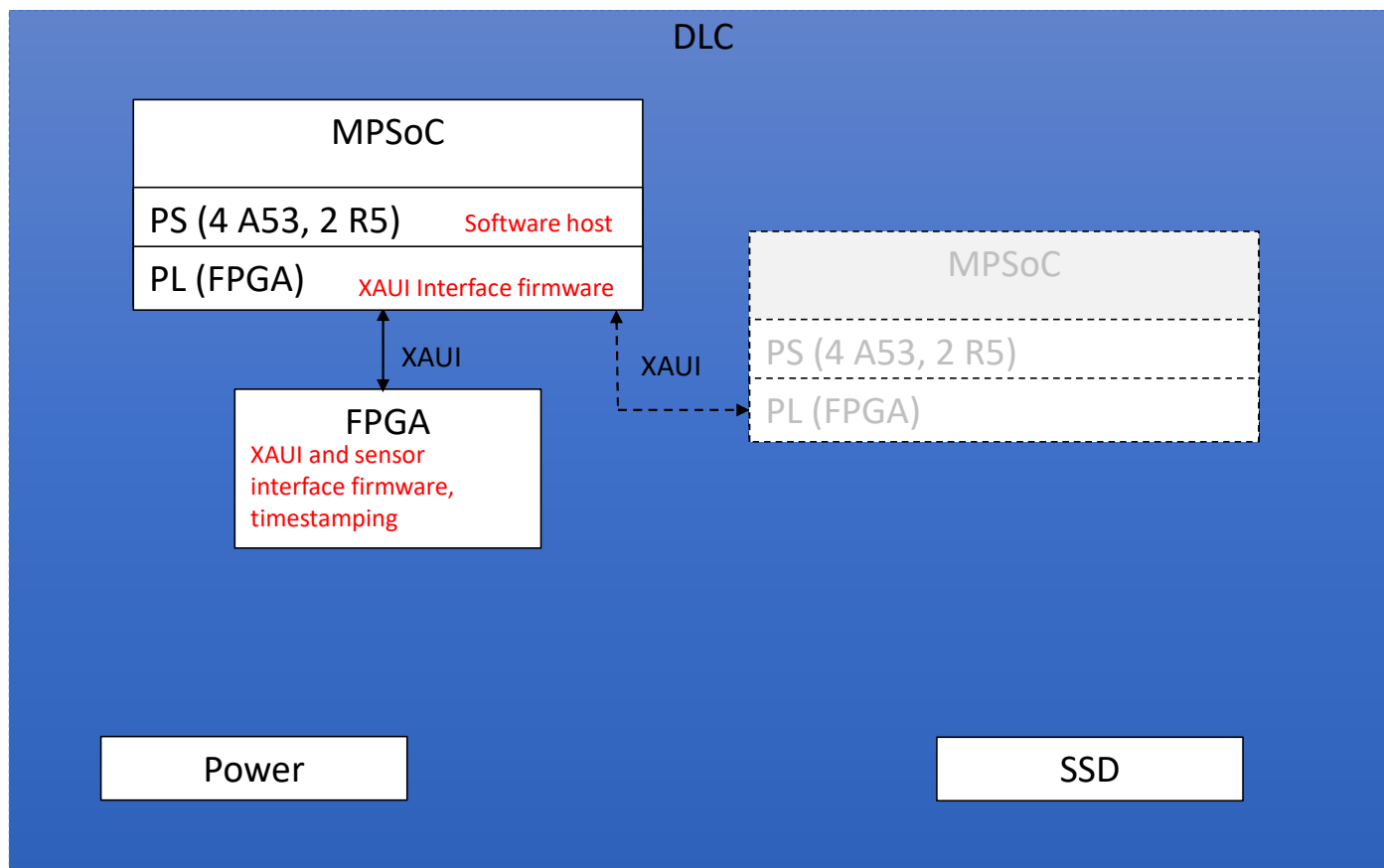
Portfolio of Current **PL&HA** Technologies

SMD/STMD/HEO/STMD/SMD/other Controlled (Soft) Landing Velocity and/or Range Sensing Navigation Doppler Lidar (NDL) TRL 5+ (6 in FY19) Line-of-site velocity of 200 m/s (± 1.7-cm/sec, 1σ) Line-of-site range of 4+ km (± 2.2m, 1σ) dev & test in ALHAT/Morpheus, COBALT, & SPLICE Long-range Laser Altimeter (LAlt) TRL 4 Range in vacuum, 50+ km (5 cm, 1σ) dev & tested in ALHAT/Morpheus Optical Velocimetry (many in development) TRL 3+ Estimates from image-based feature tracking and optical flow	SMD/STMD/HEO/STMD/SMD/other Precise Landing Terrain Relative Navigation (TRN) Passive-Optical/Camera-Based (requires illuminated terrain: applicable to most missions) • JPL Lander Vision System (LVS): camera + IMU + dedicated computing to be TRL 9 with Mars2020 • TRN solutions also available from APL, Draper & elsewhere in dev for multiple mission concepts • JPL Intelligent Lander System (ILS) in dev for Europa Lander concept Active/Lidar-based TRL 3-4 (dark/shadowed or illuminated terrain) dev & tested in ALHAT
SMD/STMD/HEO/STMD/SMD/other PL&HA Computing Descent & Landing Computer (DLC) HPSC (High Performance Spaceflight Computing) multicore A53 (extendable) + FPGAs (extendable) + PL&HA sensor interfaces TRL 3 (5 in FY2020) (in dev & test within SPLICE)	SMD/STMD/HEO/STMD/SMD/other Safe Landing Hazard Detection (HD) and Hazard Relative Nav (HRN) Hazard Detection System (HDS) prototype TRL 4 flash lidar + gimbal + dedicated IMU + dedicated computing Range, 1 km (± 8cm, 1σ). Generates 100mX100m map & safe landing sites within 10-12 sec dev & tested in ALHAT/Morpheus Hazard Detection Lidar (HDL) in dev & test within SPLICE TRL 4 (5 in FY2020) uses many flight heritage parts JPL Intelligent Lander System (ILS) in dev for Europa Lander concept

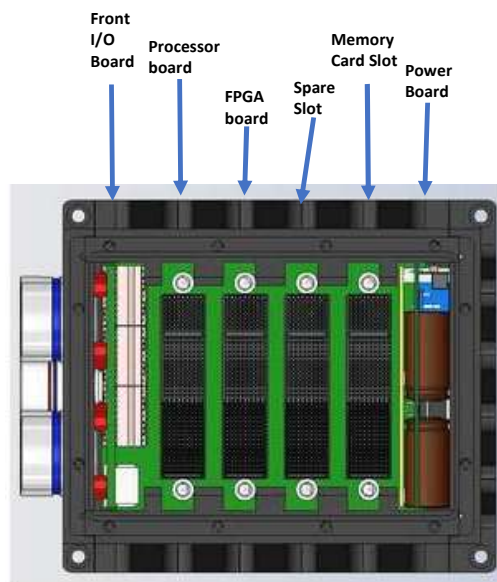
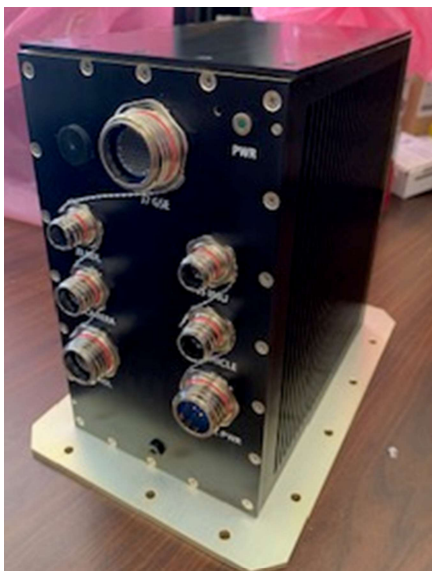
DLC (EDU) and Interfaces



DLC Structure and Function



SPLICE DLC EDU

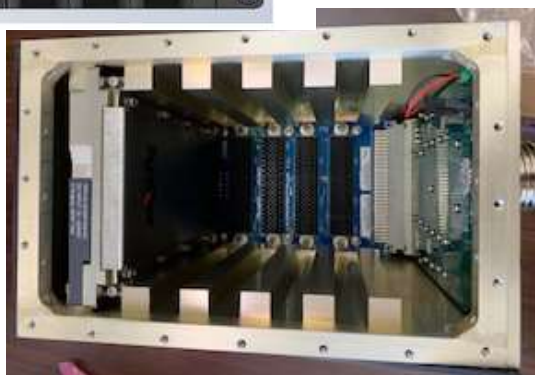


In-House Design & Development:

- Xilinx US+ MPSoC board
- Xilinx US Kintex FPGA board

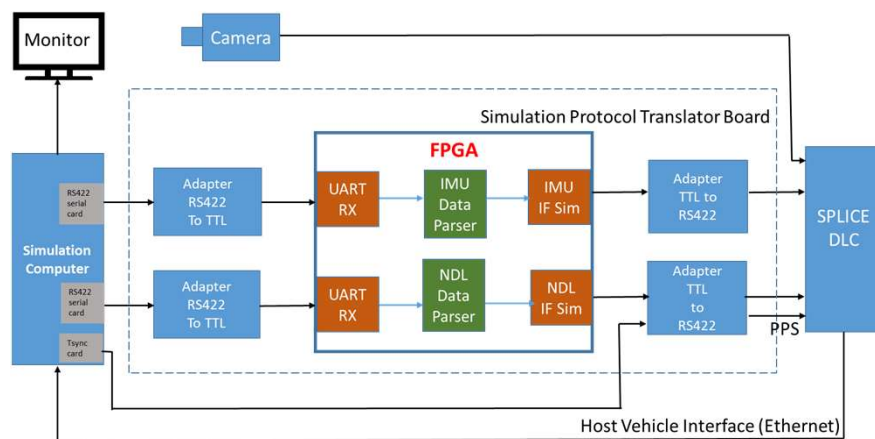
COTS 1/2 ATR Enclosure from PIXUS

- 4-slot OpenVPX backplane
- Syncor PSU
- I/O Card with Glenair 805 connectors
- COTS SSD Card from RedRock

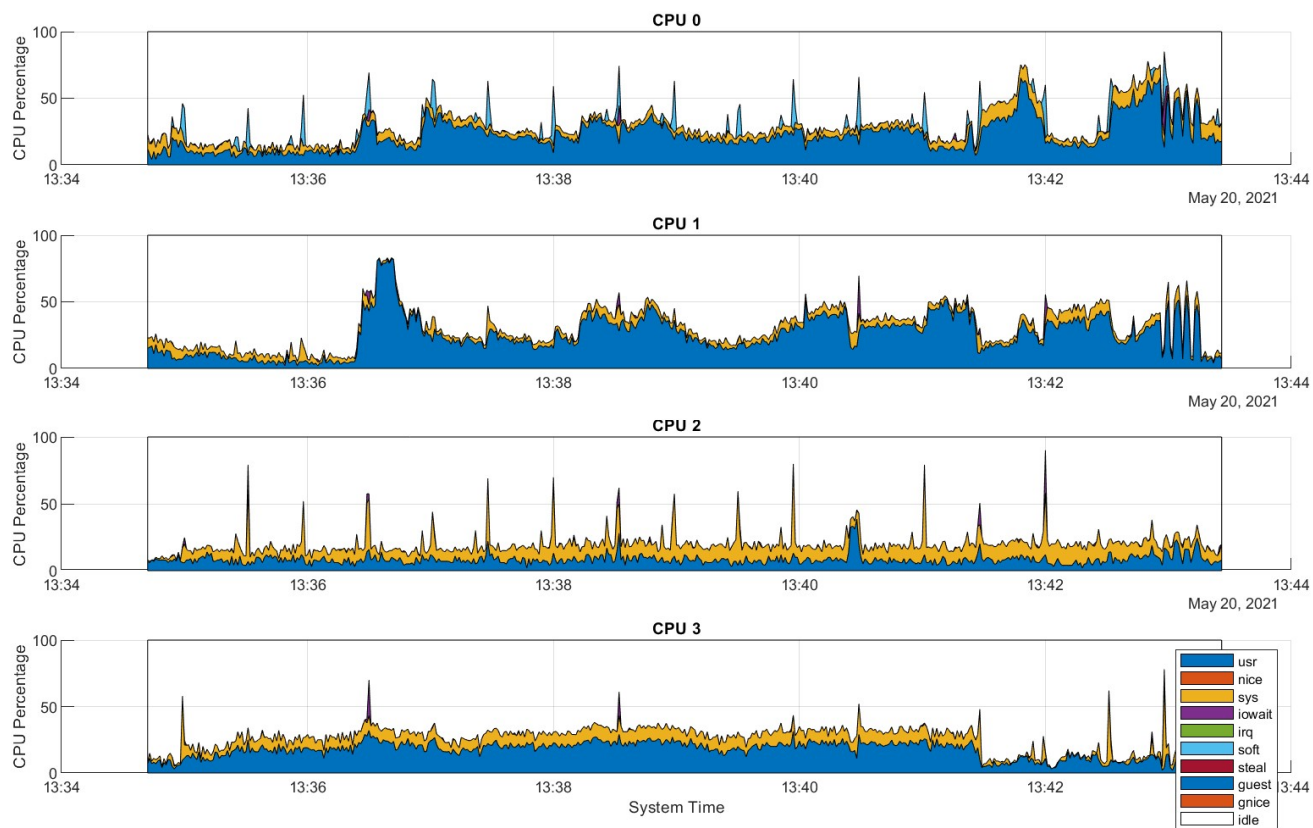


EDU Testing

- Suborbital flights on Blue Origin's New Shepherd rocket in 2020 and 2021
- HWIL simulation testing
- Workload performance measurements

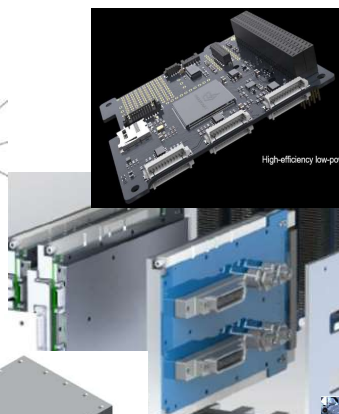
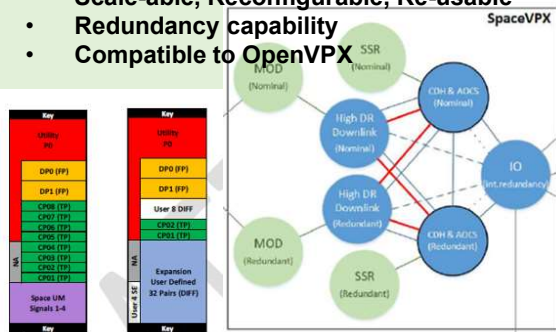


Performance Testing

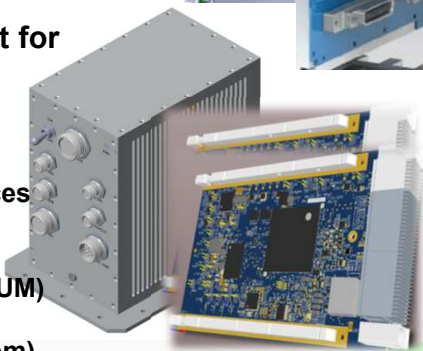


- **Develop an architecture with SpaceVPX Ecosystem**

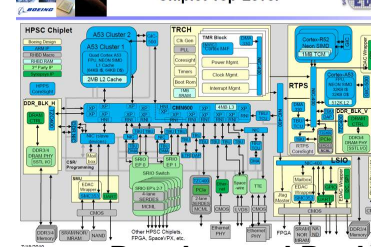
- **Scale-able, Reconfigurable, Re-usable**
- **Redundancy capability**
- **Compatible to OpenVPX**



- **Build a Computing Element for SPLICE for CLPS Missions**
 - ❖ **HPSC Surrogate SBC**
 - For high performance multicore computing and C&DH
 - ❖ **FPGA Module for sensor interfaces**
 - ❖ **Mass Memory Storage Module**
 - ❖ **Power Supply Module**
 - ❖ **SpaceVPX Utility Module (SpaceUM)**
 - ❖ **SpaceVPX Backplane**
 - ❖ **Flight Enclosure (COTS or Custom)**
- 



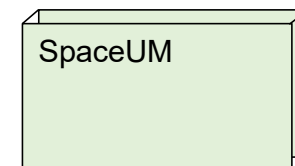
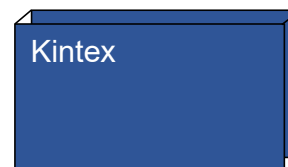
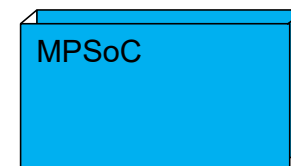
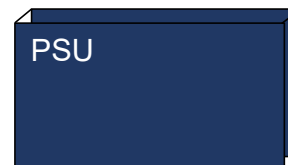
- **Radiation Tolerant Parts Selections and Procurement,**
- **Develop Circuit Designs for common core functions and interfaces**

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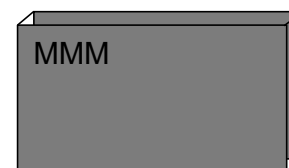
- **Develop and Design Ecosystem for HPSC SBC for future applications**

3U VPX Modules in Design Work

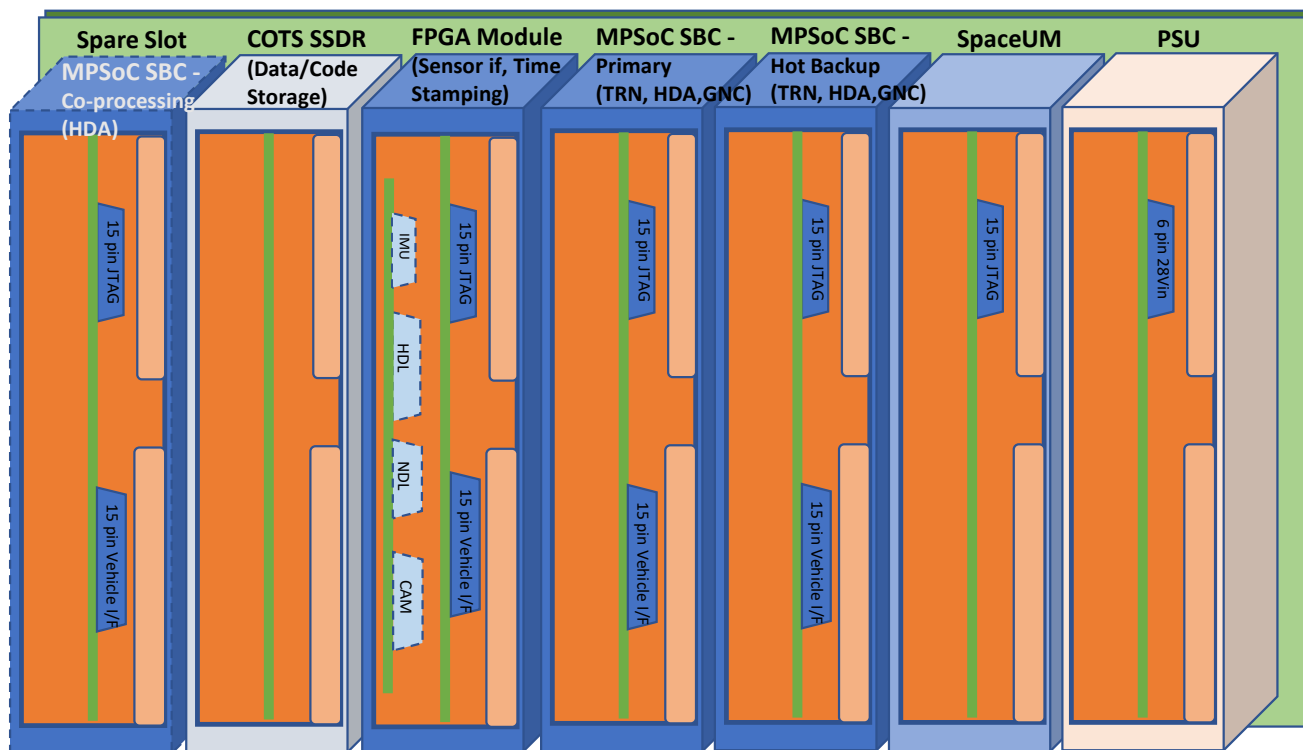
- RH Power Supply Unit (PSU)
 - @240Wmax for system, @40Wmax per slot
- RT Controller Module
 - w/ rugged military grade Zynq US+ MPSoC (XQZU9EG)
- RT Payload Module 1
 - w/ RT US Kintex FPGA (XQRKU060)
- RT Space Utility Module (SpaceUM)
 - Up to 5-Slot profile
- Custom Backplane



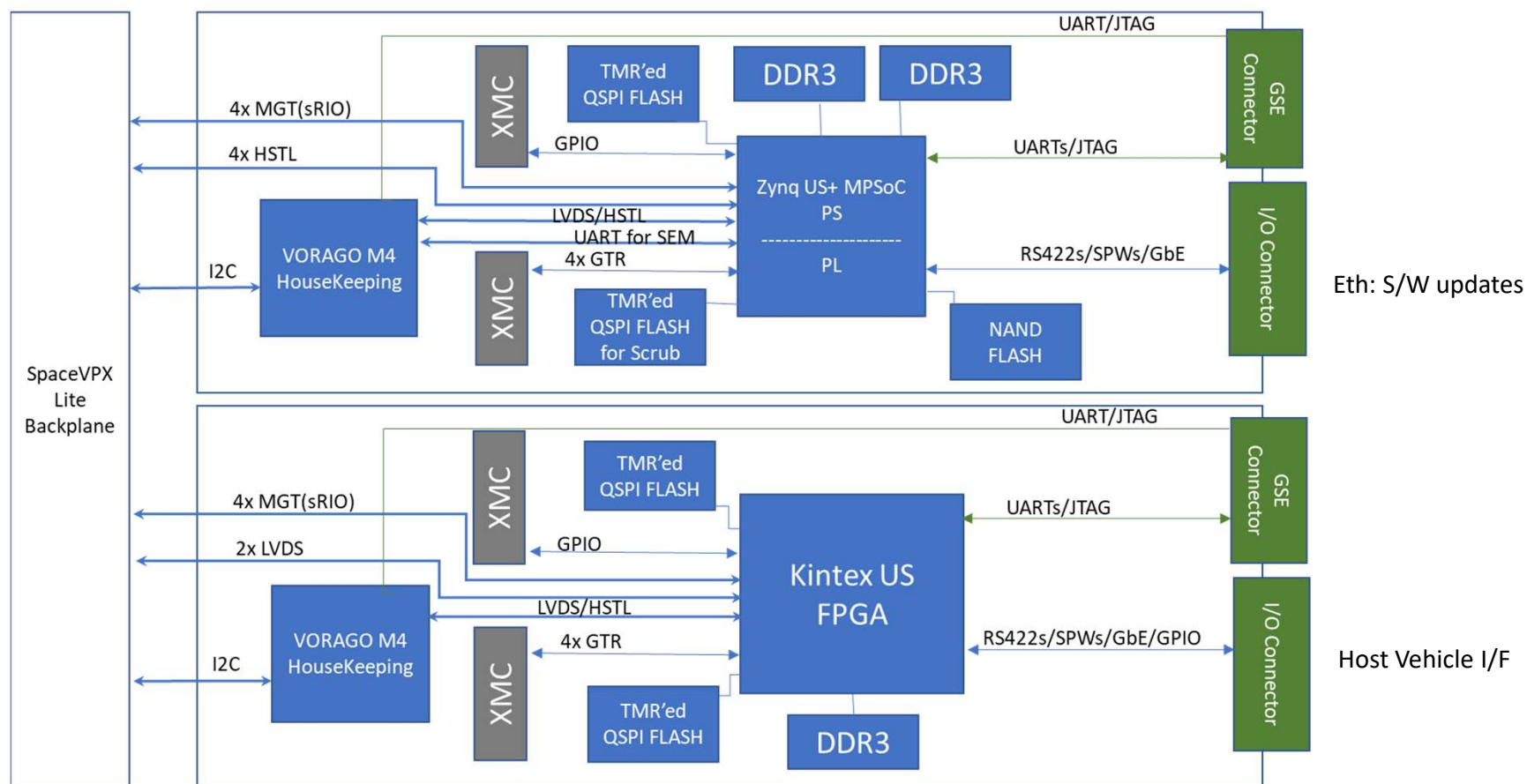
- RT XMC Mezzanine Card 1 – xx (Future Project requirement dependent)
 - TTE ASIC
 - Multi-port, high-speed ADC/DAC
 - Radio Module
- COTS SDR



SPLICE DLC Functional Allocation Example



Interconnects



Parts Selection Requirements

- To follow component specs, GFSC EEE-INST-002 Instructions for EEE Parts Selection, Screening, Qualification, and Derating
 - Radiation Harden/Radiation Tolerant (RH/RT) components that meet MIL-PRF-38535 level Q or V or MIL-PRF-38534 Class K for IC's
 - GSFC-S-311-P-4, Rectangular, space flight, electrical, connector.
 - GSFC-S-311-P-10, Subminiature, electrical and coaxial contact, electrical, connector.
 - MIL-C-55302, Printed circuit, electrical, connector, subassembly and accessories.
 - MIL-C-24308, Rectangular, miniature, polarized shell, crimp and solder contacts, electrical connector.
- Use Automotive (HighRel) or Industrial standards for all passive components that meet thermal requirement (-55 to +125 degC or better)
 - AEC-Q200



Radiation Mitigation Plan for SEL



- Over Current & Under Voltage Monitor, Detect, and Reset using RH M4 Microcontroller at each board
 - Slot-level Input Voltage & Current Monitoring at SpaceUM (VPX Vs3 = 5V)
 - Low-level Voltages and Currents Monitoring at each MPSoC board & each FPGA board
- Disable MPSoC's SysMon function.
- System-level radiation tolerance

Radiation Mitigation Plan for SEU

- 8-bit ECC on DDR3
- TMR'ed QSPI NOR Flash memory
- Boot Flash memory scrubbing
- FPGA Configuration Memory Scrubbing using SEM IP
- RH/RT parts for all memory: DDR3, QSPI Flash, NAND Flash
- TMR'ed Implementation in firmware IPs if needed



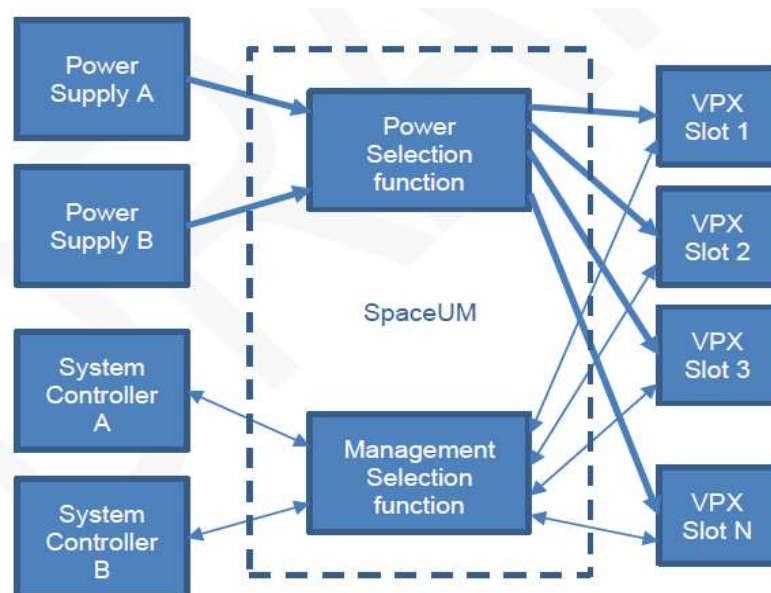
Chassis/Connector Requirements & Considerations



- Environmental Requirements are host vehicle dependent/location.
 - Thermal
 - Thermal Vac & Thermal Cycle
 - Vib & Shock
 - EMI
 - Power Quality
- Modular Chassis Design
 - Conductively Cooled
 - SpaceVPX Form Factor
 - 1.4" Pitch Slots (or Variable?) per VITA 78 Revision Rev.1.16 (unreleased)
 - 3U-220mm Length
 - 2 or more slot Enclosure design modification enabled (Custom or COTS)
 - I/O connector at the edge of each module
 - Nano D-Sub connectors from Glenair

SpaceUM

- The SpaceUM module combines the management selection and power selection functions into a single module.



- Power Sequencing
 - Controls the power up/down sequencing of Xilinx MPSoC or Kintex FPGA
 - Monitors power at all times
- Fault Detection
 - Monitors and detects fault conditions such as overcurrent, under-voltage, and missing power good signal, high temps.
 - Performs corrective actions by RESET or power cycling of MPSoC or Kintex FPGA
- Independent Operation
 - Power source for Sys Mon is separated
 - Can control RESETs or power cycling of MPSoC or Kintex FPGA without a complete system power cycle
- Scrubbing
 - Supports Xilinx SEM IP operations for error detection and correction.
 - Performs responsive actions based on status
- Health & Status Reporting
 - Performs Utility Management functions – ChMC & IPMC per VITA 46.11
 - ChMC identifies all modules
 - ChMC gathers health and status from all modules and reports to Telemetry path via MPSoC or Kintex FPGA - # of resets, currents, voltages, temps, heart-beat.

Future Work

- Continued development and testing on EDU in support of ETU
 - Early testing of new interfaces (High-speed serial, Spacewire, new sensors) and architecture upgrades (datapath bandwidth, timing, dual MPSoC configuration)
- ETU architecture development
 - DLC Engineering model (non-RT) version design and development
 - System Utility Management & Fault Management function development with VORAGO evaluation boards
- ETU integrated testing and HWIL simulated flights