National Aeronautics and Space Administration

NASA SpaceCube

Miniaturized Platform for Onboard Processing and Analysis

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SpaceCube

www.nasa.gov

Outline

- What is SpaceCube?
  - Approach / Technical Design
  - Performance
  - SpaceCube Family Overview
- How Can SpaceCube Help?
  - Application Hardware Acceleration
  - Rapid Hardware Prototyping
- How Can You Build SpaceCube Systems?
  - CubeSat Card Specification (CS^2)
  - Mission-Specific Mix-and-Match Boxes
  - Catalog of Designs
  - Cross-Cutting Concept
- Conclusion

What is SpaceCube?

NASA SpaceCube

A family of NASA developed space processors that established a hybrid-processing approach that provides a **blend of the best advantages** of both commercial and radiation-hardened technologies to yield unparalleled next-generation systems

Merits of approach recognized by peers with Award for **2020 NASA Government Invention of the Year Runner-Up** for SpaceCube v2.0

Flown 11 systems in space to date

Heritage

SpaceCube v1.0

STS-125, MISSE-7, STP-H4, STP-H5, STP-H6

SpaceCube v1.5

SMART (ORS)

SpaceCube v2.0-EM

STP-H4, STP-H5

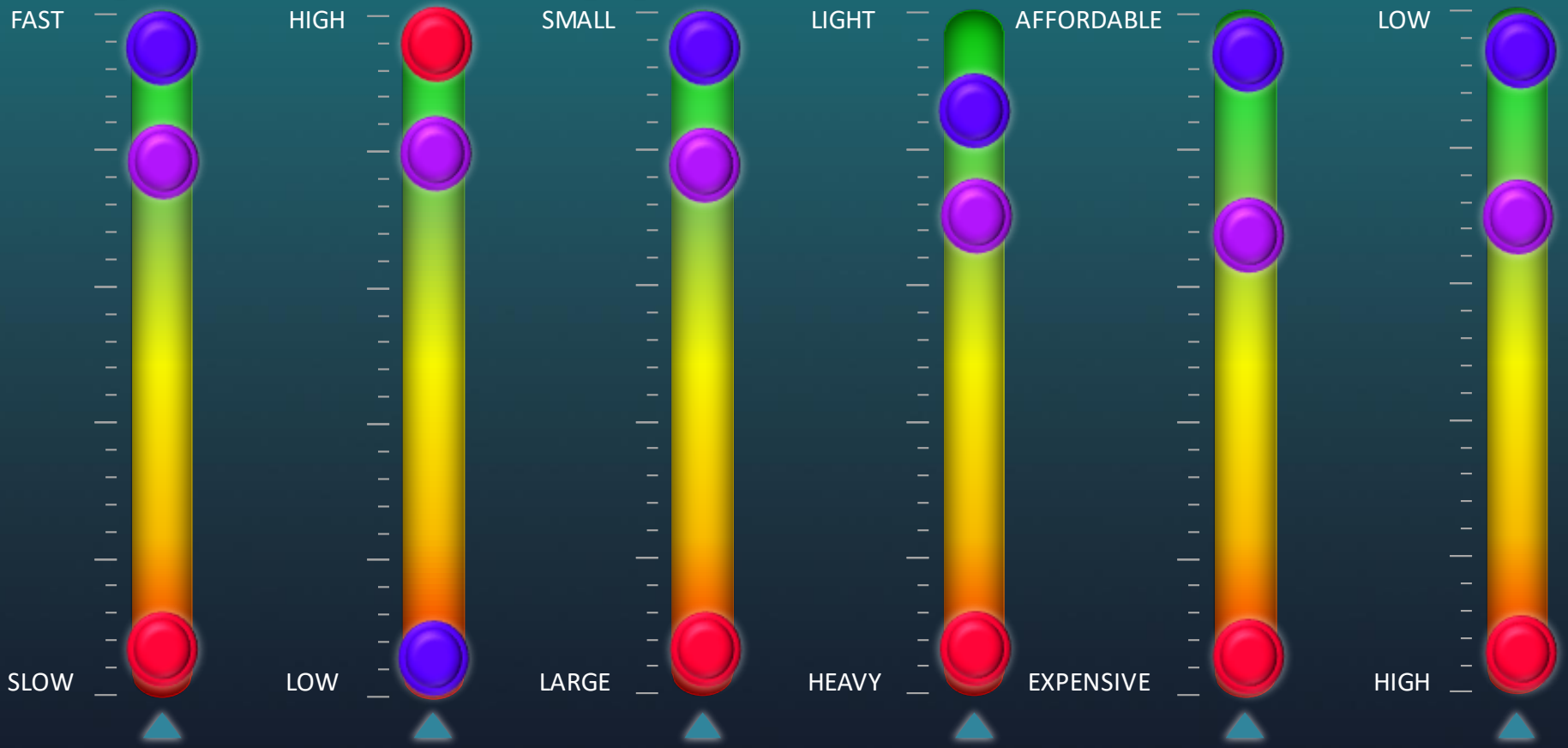
SpaceCube v2.0-FLT

RRM3, STP-H6 (NavCube)

SpaceCube v2.0 Mini

STP-H5, UVSC-GEO

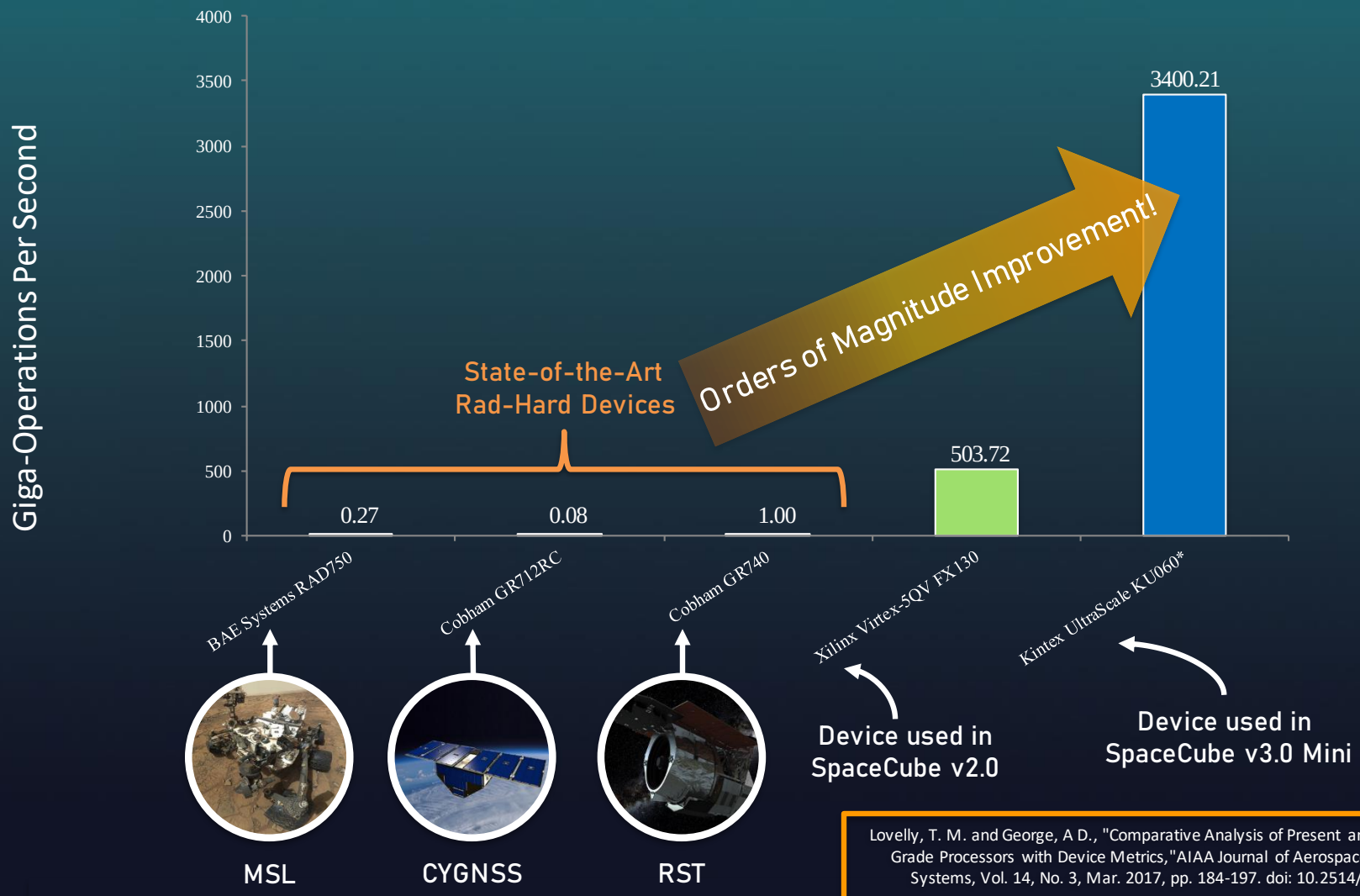
SpaceCube Approach



- COMMERCIAL/CONSUMER ELECTRONICS
- RADIATION-HARDENED ELECTRONICS
- SPACECUBE HYBRID SOLUTION

- Consumer electronics are fast and cheap, but unreliable
- Rad-Hard electronics are resilient, but expensive and large
- SpaceCube to provide **optimal balance** of key criteria

SpaceCube Performance

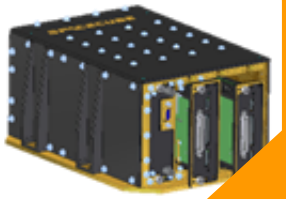


Lovelly, T. M. and George, A D., "Comparative Analysis of Present and Future Space-Grade Processors with Device Metrics,"AIAA Journal of Aerospace Information Systems, Vol. 14, No. 3, Mar. 2017, pp. 184-197. doi: 10.2514/ 1.I010472

8-Bit Integer Operaions
*UltraScale results are an estimate based off of existing data, new metrics are in progress but not currently available

SpaceCube for Many Missions!

Family of Options



SpaceCube v3.0

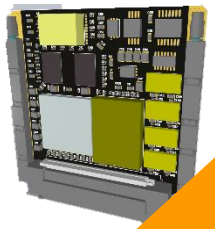
3U-SpaceVPX design with huge FPGA and SoC w/ lots of IO

SpaceCube v3.0 Mini

Miniaturized SmallSat design featuring huge FPGA and high-speed IO

SpaceCube Mini-Z/Z+

Miniaturized SmallSat design with FPGA+CPU SoC for low power



SpaceCube Mini-Z45

Miniaturized SmallSat design with FPGA+CPU SoC with high-speed IO

SpaceCube Family

Number of products with varying capabilities to support diverse set of mission-specific needs

SpaceCube v2.0

3U-cPCI design with extensive heritage for high-rel apps

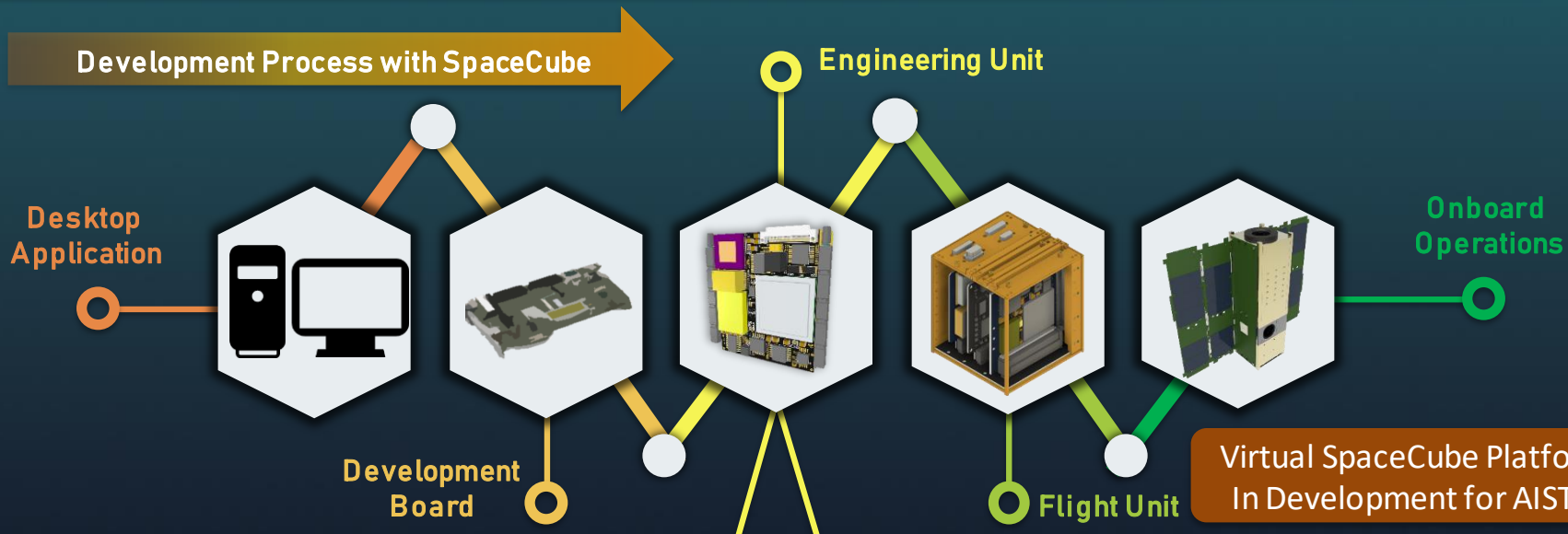
2020 NASA Government Invention of the Year Runner-Up

NASA SpaceCube

How Does SpaceCube Help?

SpaceCube helps scientists convert their applications from desktop to FLIGHT

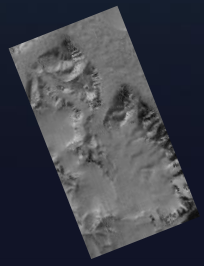
SpaceCube can hardware accelerate applications BEYOND embedded expectations



Virtual SpaceCube Platforms In Development for AIST18

Machine Learning App: Classification and Detection

Demonstrated massive **1733× speedup** over purely software baseline run on single processor



Lossless Compression: JPEG-LS

Demonstrated **61.68× speedup** on LandSat-8 Dataset over single processor (~2 hrs to 2 min)

Rapid Hardware Prototyping

FPGA-based Systems Suffer From Productivity Challenges:

- **Low-level design** and verification is tedious using hardware-description languages (HDLs)
- **Slow "build" compilation** on order of hours/days, as compared to software's secs/mins

High-Level Synthesis (HLS) Addresses FPGA Productivity Issues

- HLS generates low-level [1]RTL designs from **high-level languages** (commonly C/C++ subset)
- Enables faster design iterations through **fast algorithmic validation** in high-level languages instead of slow RTL simulations

HLS Has Been Used To Rapidly Hardware Accelerate Science Applications

- Rapid **design space exploration** of architectural parameters with different area/performance tradeoffs
- Swift prototyping of changes to science algorithms which would be **challenging or near impossible** for traditional hand-coded HDL

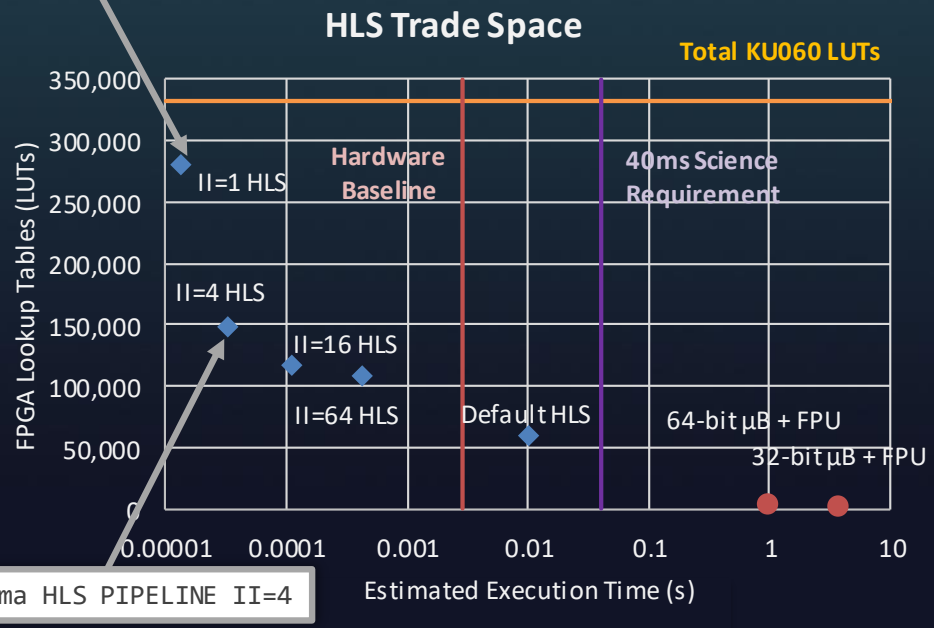
High-Level HLS C++ Code

```
// Precession/Nutation
Vector3f resultPN =
rotationPN * R;
Vector3f resultECEF =
rotationGAST * resultPN;
float scale[3] = {-1.0,
1.0, 0.0};
detectorLoop:
for (int i=0; i<NUM; i++){
  #pragma HLS PIPELINE II=1

  Matrix2<float,2,22> H =
    CalculateHMatrix(detect
```

HLS-Generated VHDL Code

```
...
stereoBit_sitofp_yd2_U284 :
 component
stereoBit_sitofp_yd2
    generic map (
        ID => 1,
        NUM_STAGE => 4,
        din0_WIDTH => 32,
        dout_WIDTH => 32)
    port map (
        clk => ap_clk,
        reset => ap_rst,
...
```



[1]**RTL**: Register-Transfer Level **II:** Initiation Interval **FPU:** Floating-Point Unit

Intelligent Multi-Purpose System (IMPS)

Custom Boxes Enabling Remote Sensing, Communication, and Navigation Missions

Goals

Develop system architecture to **mix-and-match** 1U CubeSat-sized cards to address needs of multiple computing domains

Demonstrate system-in-action with processing example

Motivations

New mission concepts demand vastly more processing for advanced applications and onboard processing

Need reusable, extendable architecture for **varying mission environments**

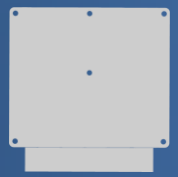
Challenges

Create reliable, **processing baseline** to support varying mission needs

Establish guidelines to enable reusability without imposing too stringent restrictions

[CS]^2

Learn 1U-Sized Specification



Design Compatible Cards

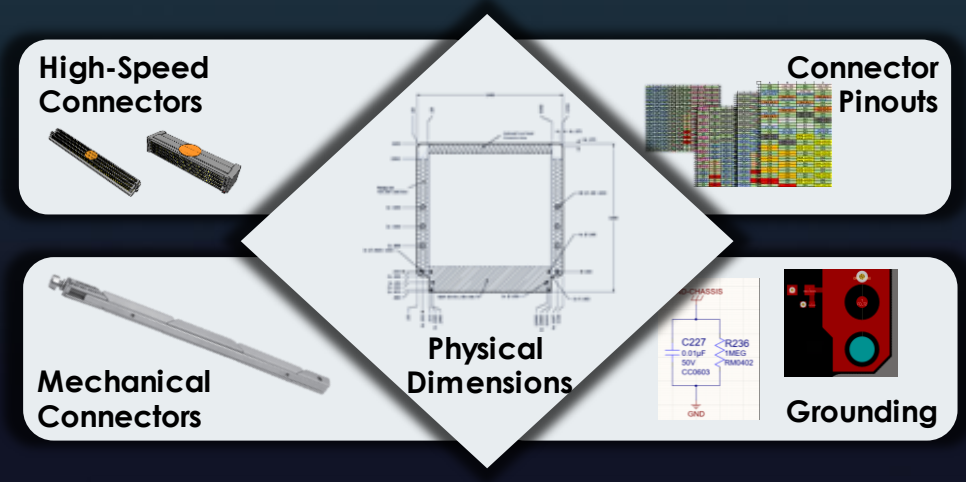
Build Future Systems

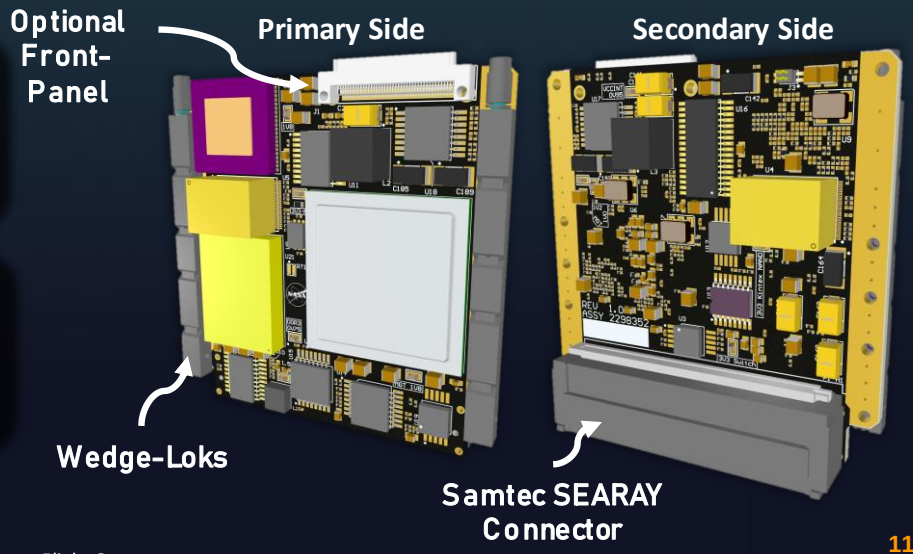
CubeSat Card Specification

[CS]²

Common Template To Build Compatible CubeSat-Sized 1U Cards

- Template needed for flexibility and interoperability of new designs to mix-and-match varying cards to construct new system
- Reduce constant mission-specific redesign of one-off cards, establish baseline configurations for compatible cards across multiple programs
- Provide convenient reference to integrate with numerous cards (and mechanical structures) supported by SpaceCube Family





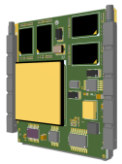
Additional CS² Benefits

Convert Heritage, Existing Designs into CS² Size

MUSTANG DSB

Heritage Goddard custom Data Storage Board (DSB) design

7.24" x 9.605" x 2" (chassis volume)



4" x 4" x 1" (chassis volume)

SpaceCube SSDR

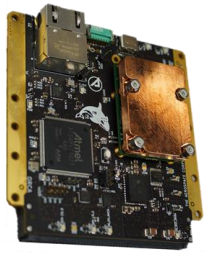
Miniaturized 1U Solid-State Data Recorder (SSDR)

Collaborate with Partners to Create New Compatible Designs!

CS² Template

Combine PCB board design experience with Specification

Myriad X Co-Processor



"Orca" Intel Myriad X Co-Processor developed by Aerospace Corp. for STP-H9 Mission

For more info for Myriad X card please contact:

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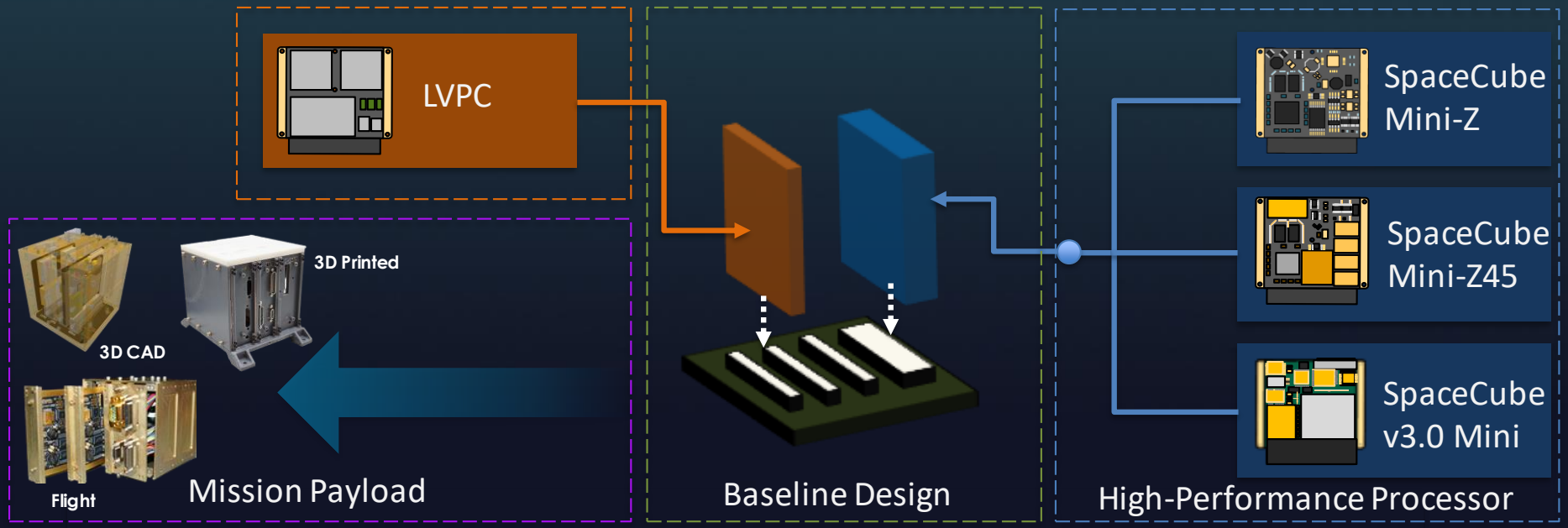
Building Systems & Payloads with SpaceCube

Diverse set of payloads can be realized with **same baseline infrastructure** of key reused cards and **simple addition** of one or two cards for mission-specific needs

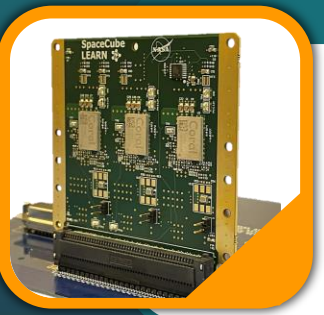
SpaceCube provides **high-performance computing** designs to be combined with added features from catalog of supporting cards

Designs are reusable and can be reconfigured for **multiple mission classes** (or varying orbits/environments) and science objectives



Catalog of CS2 Slices

SC-LEARN



SpaceCube Low-power Edge Artificial Intelligence Resilient Node

- Co-Processor for Advanced AI Apps
- Features three Google Coral Edge TPU Accelerator Modules
- Independent rad-hard load switches with current sense amplifiers

SC-DIC

SpaceCube Mini Digital IO Card

- Supports common interfaces originally designed as ISS interface
- Heritage design circuits from SC v1.0/2.0
- Includes 1553, Ethernet, LVDS/RS422 interface services, ADC and single-ended 5V output signals

SC-RAMS

SpaceCube Resilient Adaptable MIMO Software-Defined Radio (RAMS)

- Dual phase-synchronized Analog AD9361
- 4 × 4 MIMO configuration and simultaneous control of individual ch.
- 70 MHz to 6 GHz Operating Freq.
- 12-bit ADC and DACs

SC-SSDR

SpaceCube Solid-State Data Recorder

- 12 Tb capacity (1.5 TBytes)
- Two fully independent memory banks
- >400MB/s write, >600MB/s read
- 12-bit housekeeping ADC
- SERDES, SpaceWire, or LVDS interface
- 5-7W operating

SC-LVPC

SpaceCube Low-Voltage Power Converter

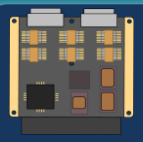
- 40W Output 18-40V/3.33A Input
  - 15W Output Variant
- 2x 8-ch 12-bit ADC monitoring
- 4x RS-422 UARTs
- 8x Switched Services
- Power-on-Reset

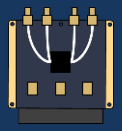
…And Many More In Development!

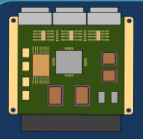
- Navigator GPS
- Versatile Analog Interface Card
- Miniaturized LIDAR
- Camera Interface ADC Readout

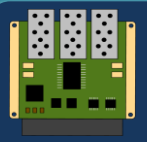
Configurable Slices

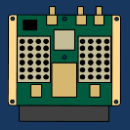

Low Voltage Power Converter


General Interface


Software Defined Radio


Lidar Interface

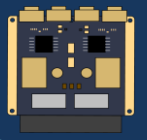

TTE / Ethernet Router


GPS

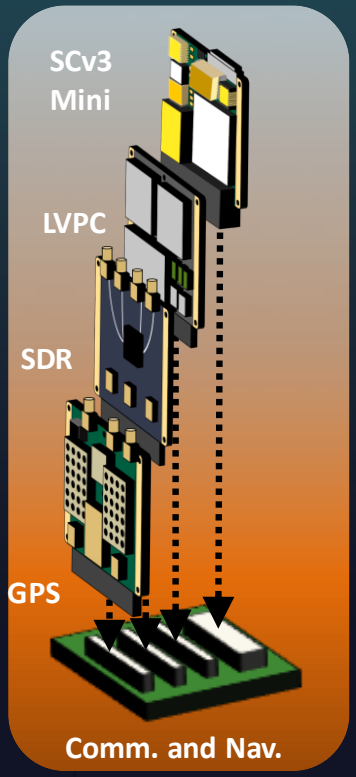

AI Accelerator

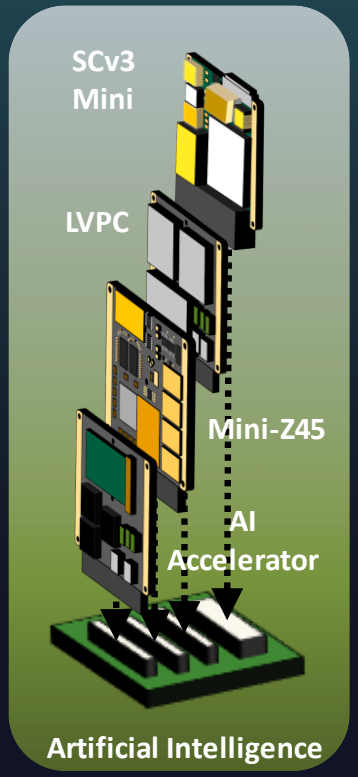

Solid-State Data Recorder

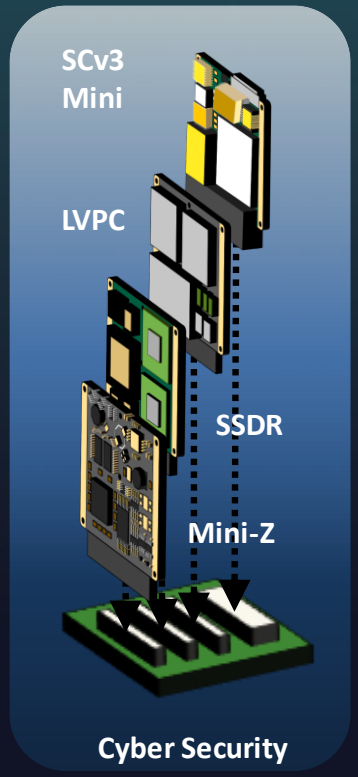

ADC Readout

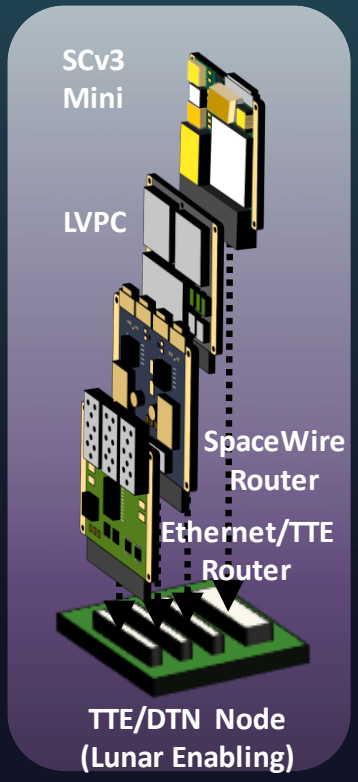

SpaceWire Router

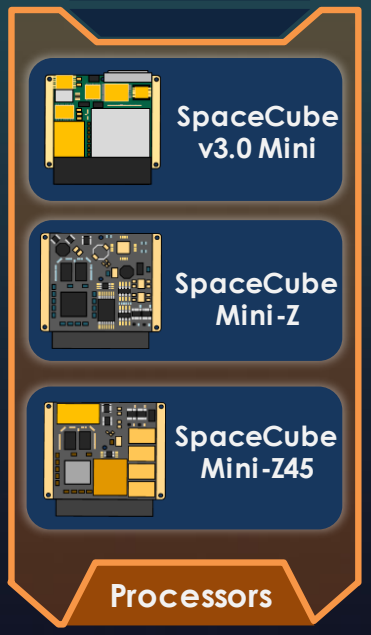
CS2 1U CubeSat Card Catalog





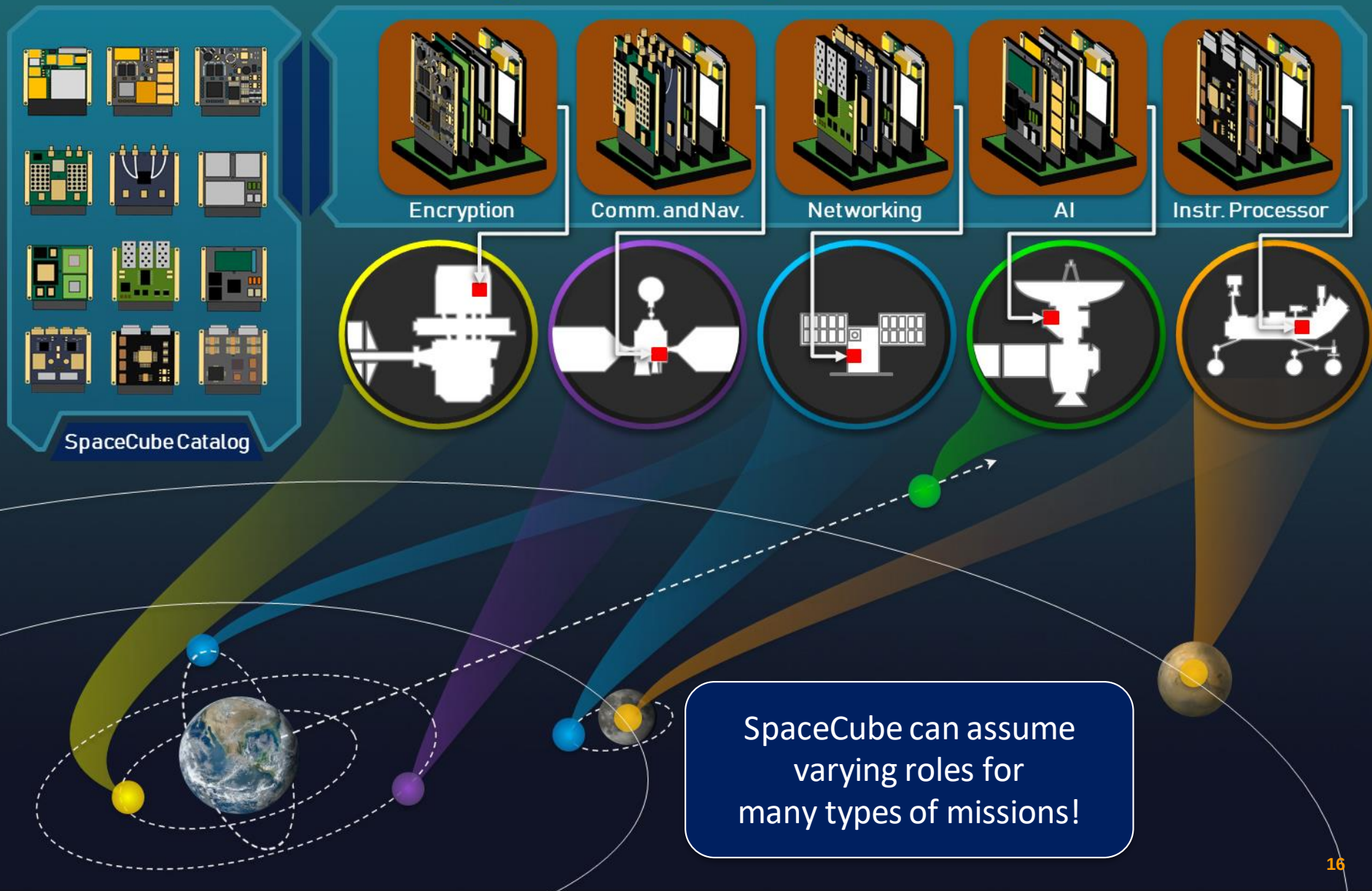






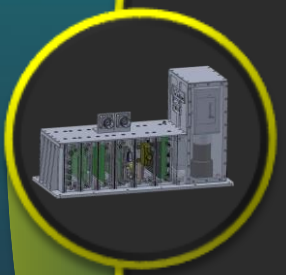
Multi-Purpose Box Configurations

Cross-Cutting Concept



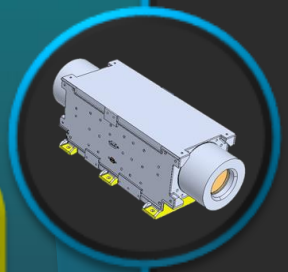
SpaceCube can assume varying roles for many types of missions!

Example Missions



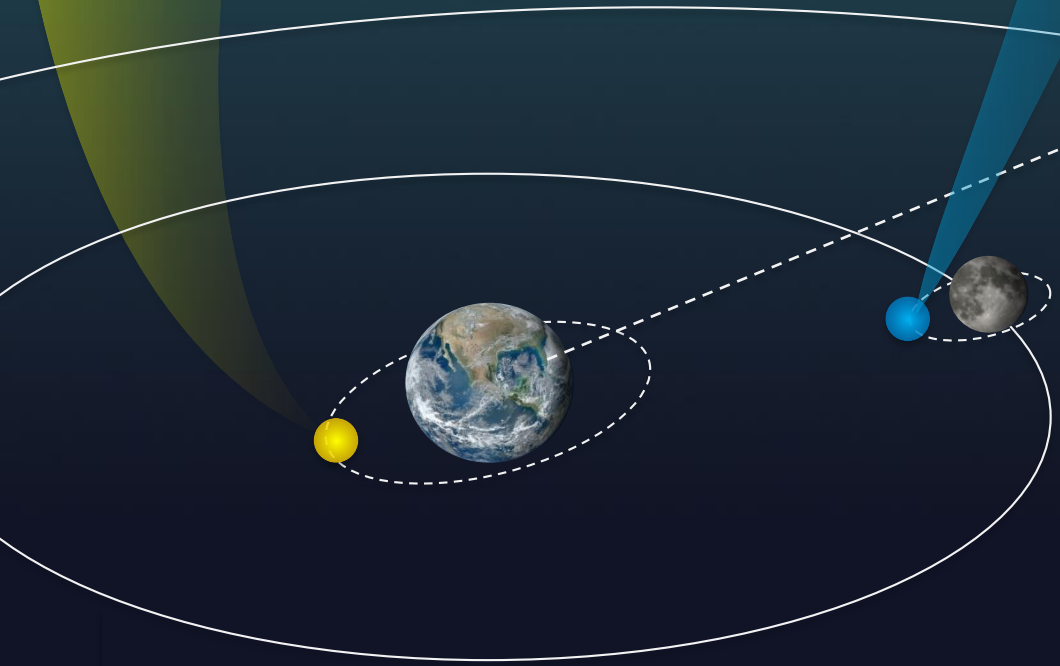
STP-H9 SCENIC

- Space Test Program – Houston 9 (STP-H9) SpaceCube Edge Node Intelligent Collaboration (SCENIC)
- ISS-based testbed to evaluate AI/machine learning technology on FPGA and custom AI microchip platforms in space
- Collaboration w/ AFRL & Aerospace Corp.
- SpaceCube v3.0 Mini, LVPC, RAMS (SDR), SC-LEARN (TPU), & Orca (Myriad X) Cards



HERMES/MERIT

- Heliophysics Environmental and Radiation Measurement Experiment Suite Miniaturized Electron pRoton Telescope (MERIT)
- Study processes in inner heliosphere for solar electrons, protons, and energetic electrons
- SpaceCube Mini-Z+ & Custom Front-End Electronics



DAVINCI+/CUVIS

- Deep Atmosphere Venus Investigation of Noble-gases, Chemistry and Imaging Compact Ultraviolet to Visible Imaging Spectrometer (CUVIS)
- CUVIS will employ advanced optical systems and innovative artificial intelligence/deep learning (AI/DL) hardware and software for on-board data processing for rapid identification of science results (Edge AI)
- SpaceCube v3.0 Mini, LVPC, SC-LEARN (TPU)

Conclusion

*SpaceCube is a **MISSION ENABLING** technology*

Delivers exceptional computing power in number of form factors

Cross-cutting technology for Communication & Navigation, Earth Science, Planetary Science, and Exploration missions

Being reconfigurable allows for extensive reuse

Exciting new demonstrations using these types of systems

Designs support AI applications for autonomy and analysis onboard

CS^2 allows mix-and-match of cards and enhances collaboration

Thank you! Questions?

Contact Us

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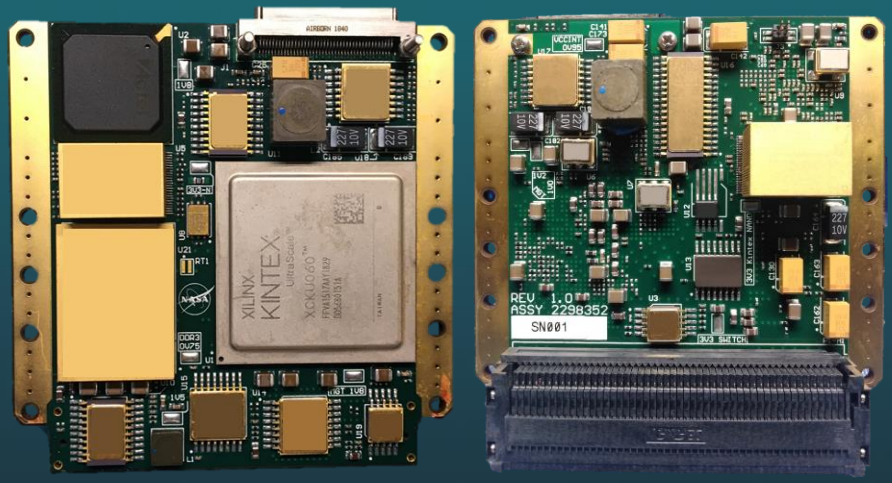
Javier Valle from Texas Instruments and Dylan Lang from Samtec

BACKUP

SpaceCube v3.0 Mini Specification

Overview

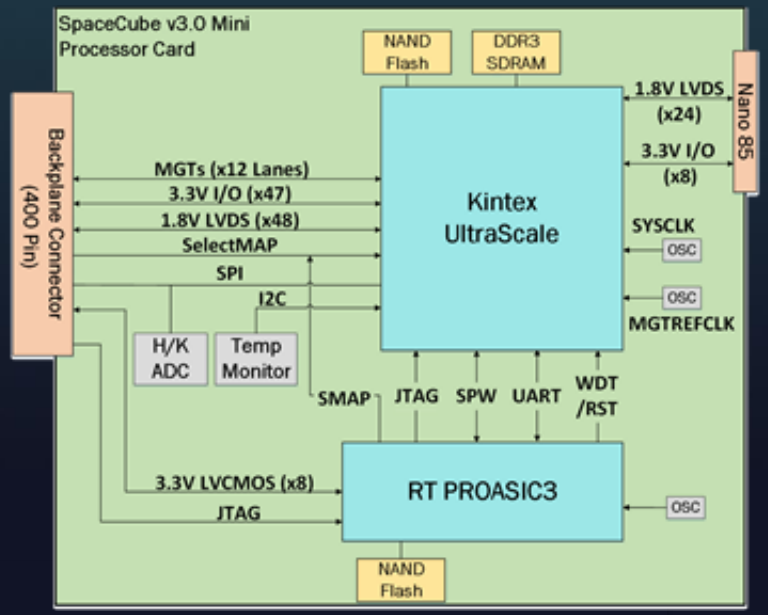
- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0
- High-performance processor of Goddard's modular CubeSat spacecraft bus MARES
- Evaluation board available with common interfaces for rapid prototyping and debug
- Conforms to CubeSat Card Specification (CS^2)



High-Level Specifications

Xilinx Kintex UltraScale

- 1x 2GB DDR3 SDRAM (x72 wide)
- 2x 16GB NAND Flash
- Radiation-Hardened Monitor
- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 48x 3.3V GPIO
  - SelectMAP Interface
  - (Front Panel) 24x LVDS pairs or 48x 1.8V single-ended I/O
  - (Front Panel) 8x 3.3V GPIO
- Debug Interfaces
  - 2x RS-422 UART (external transceivers)
  - JTAG



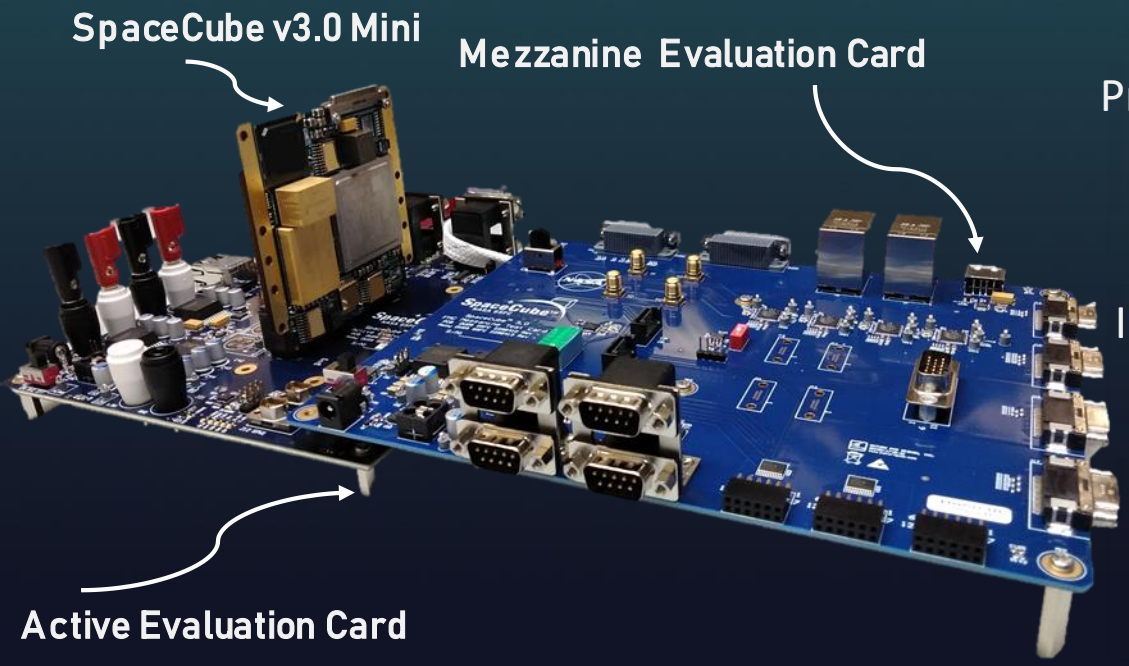
SpaceCube Mini Development Kit

Active Evaluation Card

- Gigabit Ethernet (RJ45/SGMII)
- USB Debug / JTAG
- JTAG headers (Xilinx and Microsemi)
- SelectMAP Header
- 2x SpaceWire ports
- 4x RS422 ports
- FMC+ Connector
  - 11 MGT lanes
  - 46x LVDS or 92x 1.8V GPIO
  - 22x 3.3V GPIO

Mezzanine Evaluation Card

- 3x SpaceWire Ports
- 4x RS-422 Ports
- 2x Gigabit Ethernet (RJ45-SGMII)
- 2x Camera Link (Base/Medium)
- 1x USB 2.0
- 1x SATA
- 1x CAN Bus
- 8x MGT lanes (1x SMA, 7x verSI)
- 9x LVDS
- 3x 3.3V GPIO



Provides **easy development platform** to support SpaceCube v3.0 Mini rapid prototyping and design

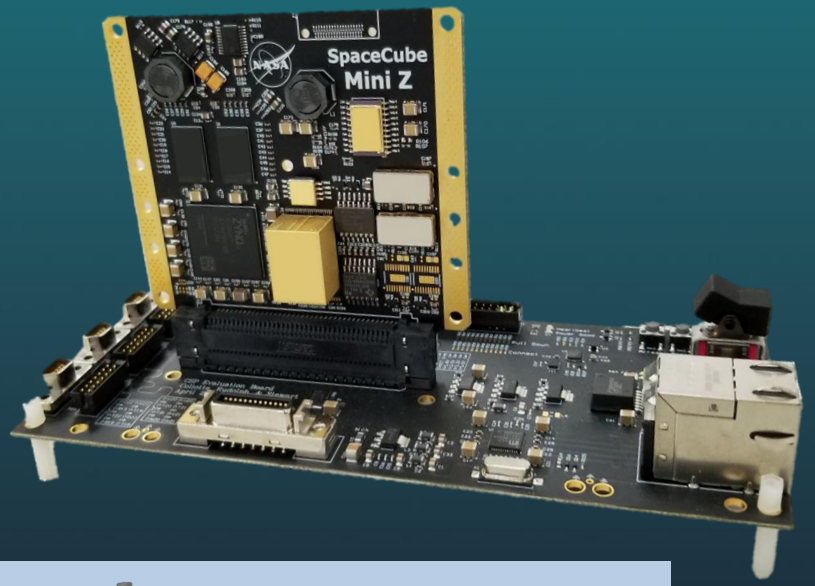
Includes several common interfaces for programming and debug

Incorporates FMC+ Connector to support future Mezzanine and commercial vendor designs

SpaceCube Mini-Z Specification

Overview

- **Re-envisioned and upgraded** version of popular CSPv1 design collaboratively developed between NASA GSFC and NSF CHREC
- Supports additional IO and form-factor changes to maintain compliance with MARES (GSFC's SmallSat bus) architecture



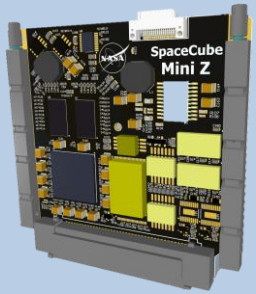
High-Level Specifications

Processing Capability

- Processing System (PS)
  - Xilinx Zynq-7020 SoC with Dual-Core ARM Cortex-A9 up to 667 MHz
  - 32KB I/D L1 Cache per core
  - 512KB L2 Cache
  - 256KB OCM
  - NEON SIMD Single/Double Floating Point Unit per core
- Programmable Logic (PL)
  - 85K Logic Cells
  - 53,200 LUTS /106,400 FF
  - 220 DSPs
  - 4.9Mb BRAM

Storage

- 1GB DDR3 SDRAM
- 4GB NAND Flash



IO

- MIO
  - 26 single-ended configurable IO into common interfaces such as UART, SPI, CAN, and I2C
- EMIO
  - 24 differential pairs and 12 single-ended IO
- Front Panel
  - 12 differential pairs

Dev. Tools

- CSP Evaluation Board
  - JTAG programming support
  - 10/100 Ethernet
  - MIO and EMIO breakout
  - 3 SpaceWire breakouts
  - Camera Link breakout
- USB-UART Board
  - USB to UART Converter

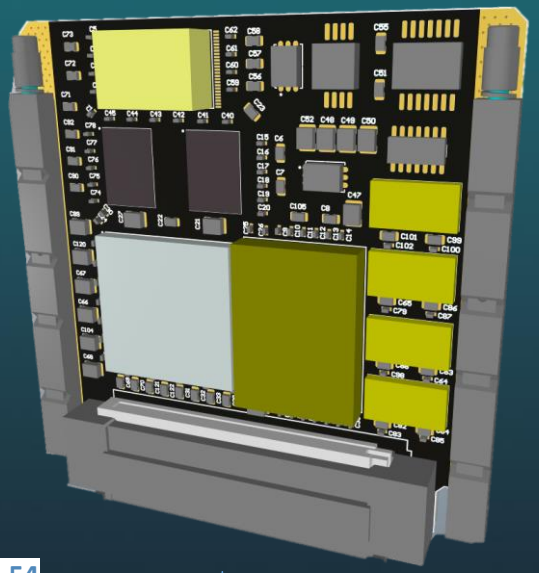
Physical Dimensions

- ~82g, 620 mil thick
- <1U CubeSat form factor
- 1.6-3.6W (FPGA load dependent)

SpaceCube Mini-Z45 Specification

Overview

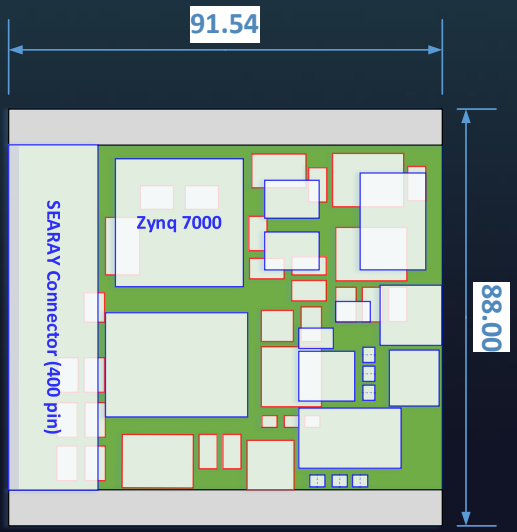
- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0 Mini and Mini-Z designs
- **Upgrade** capabilities of Mini-Z (CSPv1) to provide MGTs, more FPGA resources and more memory



High-Level Specifications

1x Xilinx Zynq 7000 System-on-Chip

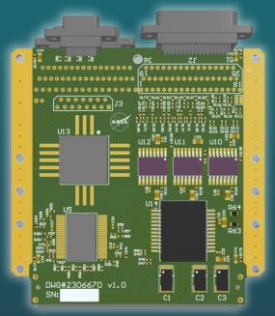
- 1GB DDR3 SDRAM for ARM Processors
- 2GB DDR3 SDRAM for Programmable Logic
- 16GB NAND Flash
- Radiation-Hardened Watchdog
- External Interfaces
  - 8x Multi-Gigabit Transceivers
  - 31x LVDS pairs or 62x single-ended I/O (voltage selectable)
  - 28x Single-ended PS MIO
- Debug Interfaces
  - 1x RS-422 UART (external transceivers)
  - JTAG

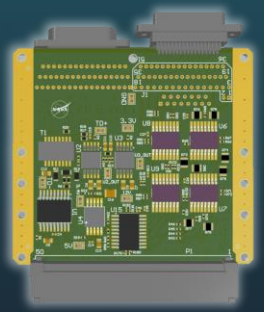


SpaceCube Mini Digital IO Card

Overview

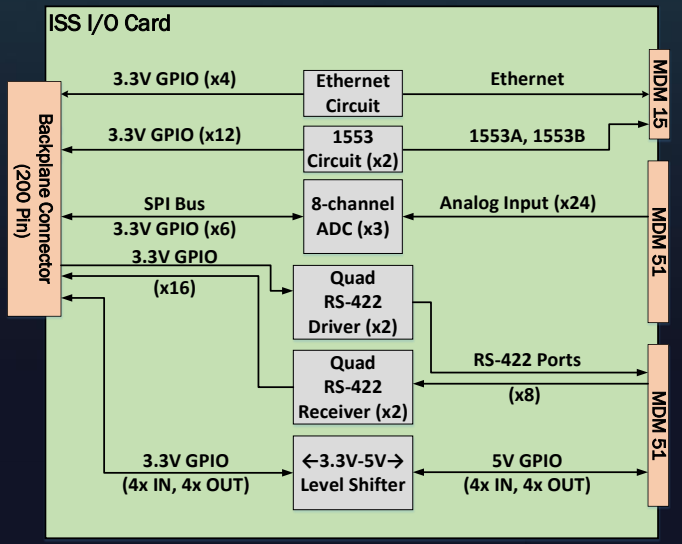
- Digital IO Card supporting common interfaces originally designed to support ISS interface for CODEX experiment
- Heritage design circuits from SpaceCube v1.0/2.0
- Includes 1553, Ethernet, LVDS/RS422 interface services, ADC and single-ended 5V output signals
- Compatibility with SpaceCube v3.0 Mini and conforms to CubeSat Card Specification (CS^2)





High-Level Specifications

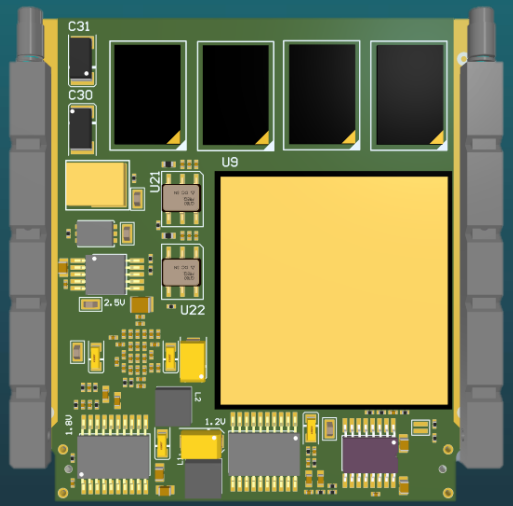
- 2x 1553 (A/B)
- 1x 10 Mbps Ethernet
- 4x Input 4x Output Discrete 5V GPIO
- 8x RS-422 UART
- 24x Analog input for thermistor readings
  - 3x 8-ch, 12-bit ADC, 1MSPS



Solid State Data Recorder (SSDR) Card

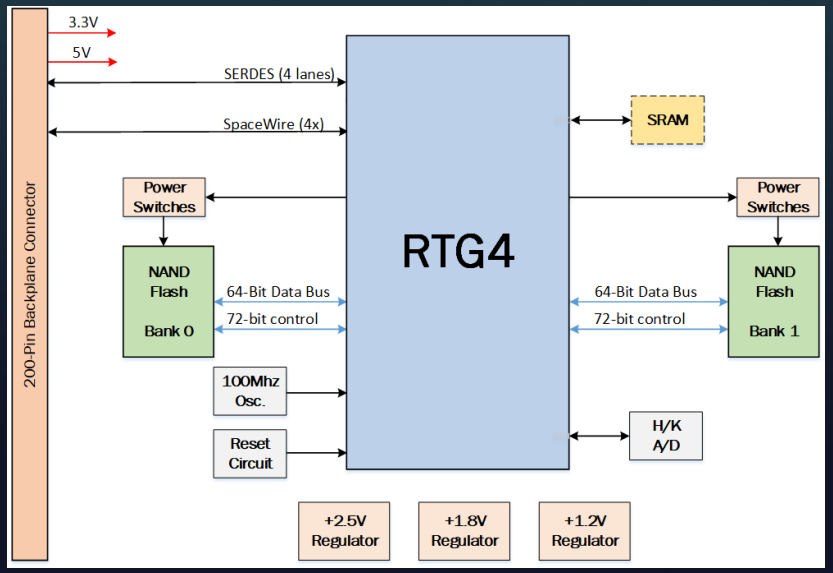
Overview

- Miniaturized, scalable, high-density, high-reliability SSDR
- Leverages heritage MUSTANG Data Storage Board
- On-board RTG4 manages memory interface (including ECC) and allows for multiple external interface types
- On-board SRAM for buffering high-speed transfers
- Conforms to CubeSat Card Specification (CS^2)



High-Level Specifications

- 12 Tb capacity (1.5 TBytes)
- Two fully independent memory banks
  - Can selectively populate or power cycle for SWAP-C savings
- Sustained memory rates (TBR):
  - >400MB/s write
  - >600MB/s read
- 12-bit housekeeping ADC
- SERDES, SpaceWire, or LVDS interface to system
- 5-7W (TBR) operating, with lower power "inactive" modes possible.

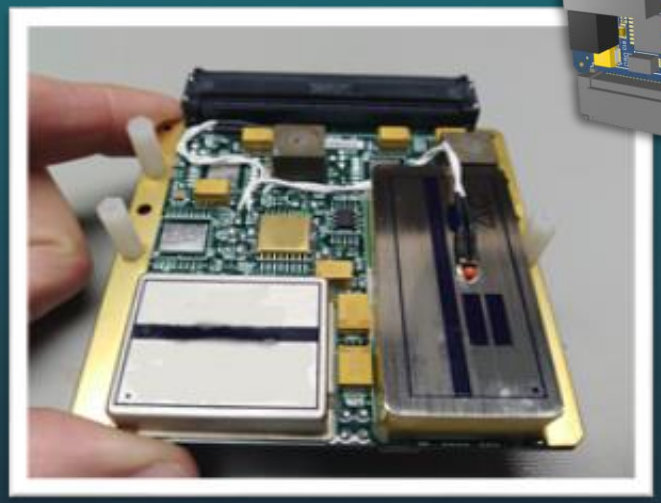


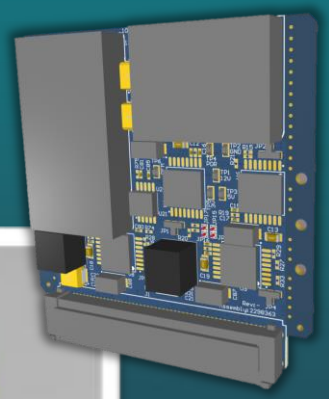
SpaceCube Mini LVPC

Overview

- Provides EMI filtering, 12V0, 5V0 and 3V3 secondary voltage rails for SpaceCube processors
- Heritage design from STP missions
- Optional switched services
- Includes RS-422 transceivers for SpaceCube Mini
- Compatibility with SpaceCube Mini/Mini-Z and conforms to CubeSat Card Specification (CS^2)

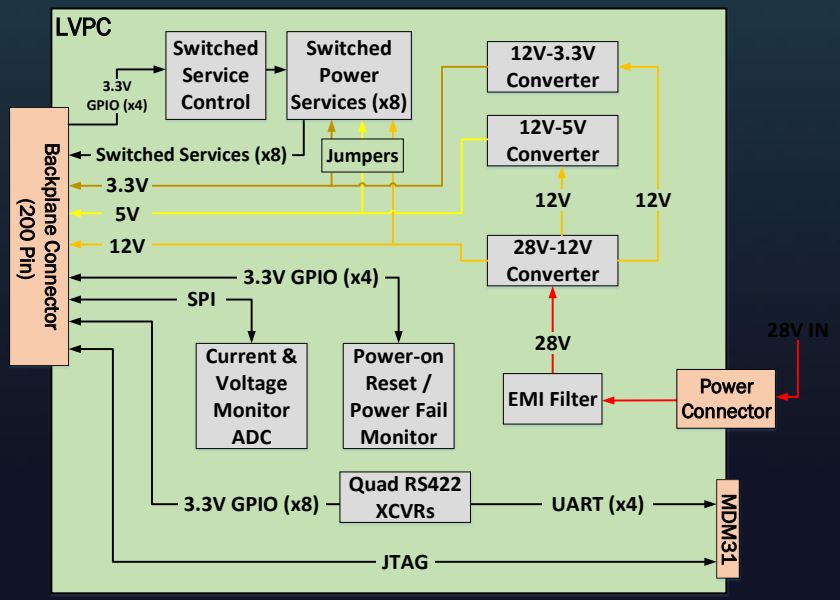
[CS]²





High-Level Specifications

- 40W Output 18-40V/3.33A Input
  - 15W Output in development
- 2x 8-ch 12-bit ADC monitoring
  - 12V, 5V, 3.3V voltage telemetry
  - 12V, 5V, 3.3V current telemetry
  - Two thermistor telemetry
  - SPI Interface
- 4x RS-422 UARTs
- 8x Switched Services
  - 4x 3.3V/5V @ 6A
  - 4x 5V/12V @ 3A
- POR



SpaceCube Low-power Edge Artificial Intelligence Resilient Node (SC-LEARN)

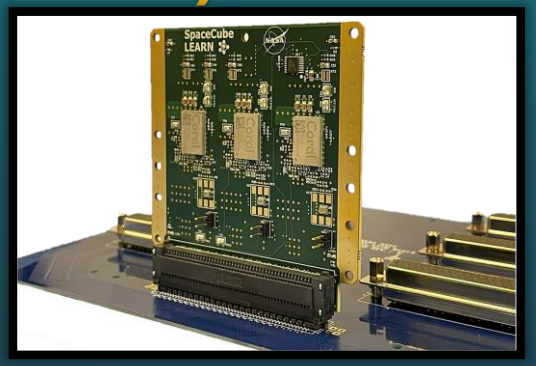
Overview

- Designed to act as Co-Processor for Advanced AI Applications
  - Compatible with SpaceCube Mini/Z/Z+
- Features **three Edge TPU** Accelerator Modules for multiple modes:
  - (1) High-performance parallel-processing
  - (2) Fault-tolerant mode for resilience
  - (3) Power-saving mode with cold spares
- Conforms to CubeSat Card Specification (CS^2) [CS]²

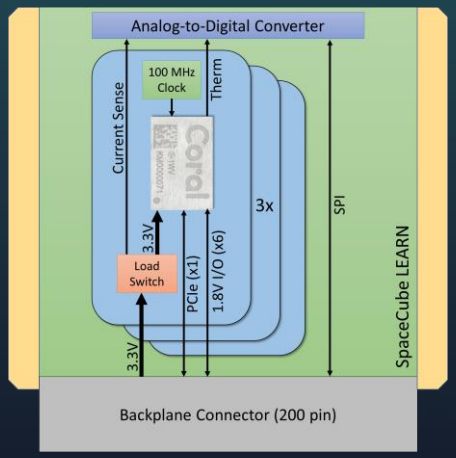
High-Level Specifications

Google Coral Edge TPU (3x)

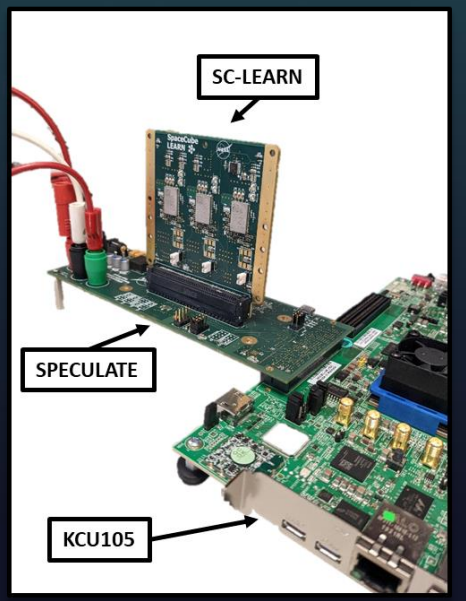
- External Interfaces
  - PCIe x1 / 1.8V LVCMOS I/O (x6) per Edge TPU
- Radiation-Hardened Load Switch per Edge TPU
  - Switches controlled by host
  - Integrated current sense amplifiers
- Analog-to-Digital Converter
  - 3x current sense outputs of load switches
  - 3x external thermistor connections
- SPECULATE (SPacE CUbe LeArn TEst board)
  - FPGA Mezzanine Card (FMC)



SC-LEARN in Electrical Test Card



Block Diagram



SPECULATE Evaluation Board

Versatile Analog / Digital InteRface (VADIR)

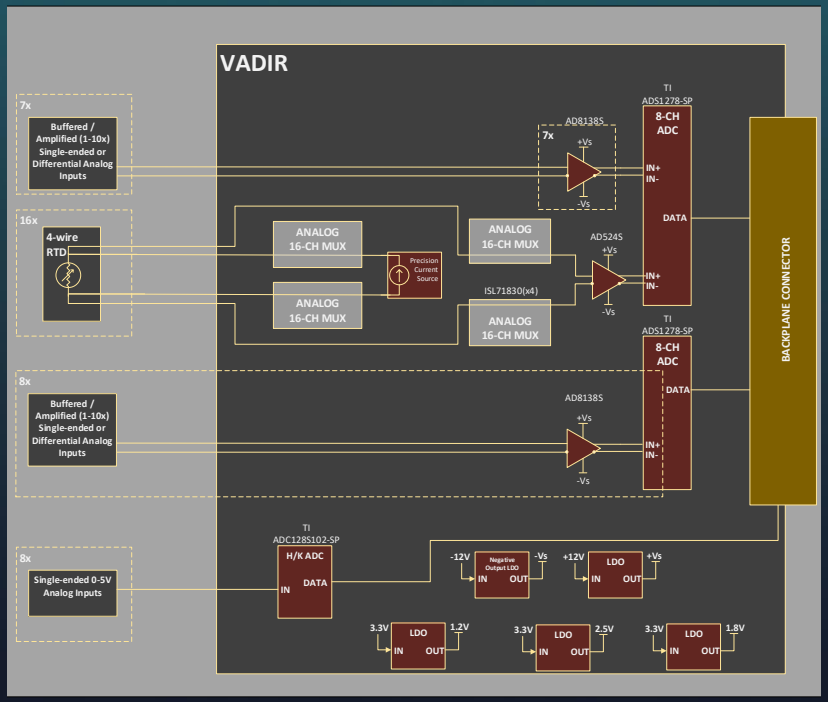
Overview

- Multiple configurable analog inputs in CubeSat form-factor
- Selective population enables SWAP-C savings depending on mission needs
- On-board level shifter allows for multiple control voltages
- Conforms to CubeSat Card Specification (CS^2)

[CS]²

High-Level Specifications

- 24-bit Science & Telemetry ADC
  - 2 independent ADCs, up to 52ksps each
  - 16x 4-wire RTD up to 45kΩ resistance
  - 15x Single-Ended or Differential Analog Inputs
- 12-bit Housekeeping ADC
  - 8x 0-5V Single-Ended Analog Inputs
- Bias Supplies
  - 2x LDO supplies, <1.5A, 1.2-3.3V
- Requires ±12V, +5V, and +3.3V
- Requires 16x I/O lines (1.8V or 3.3V)



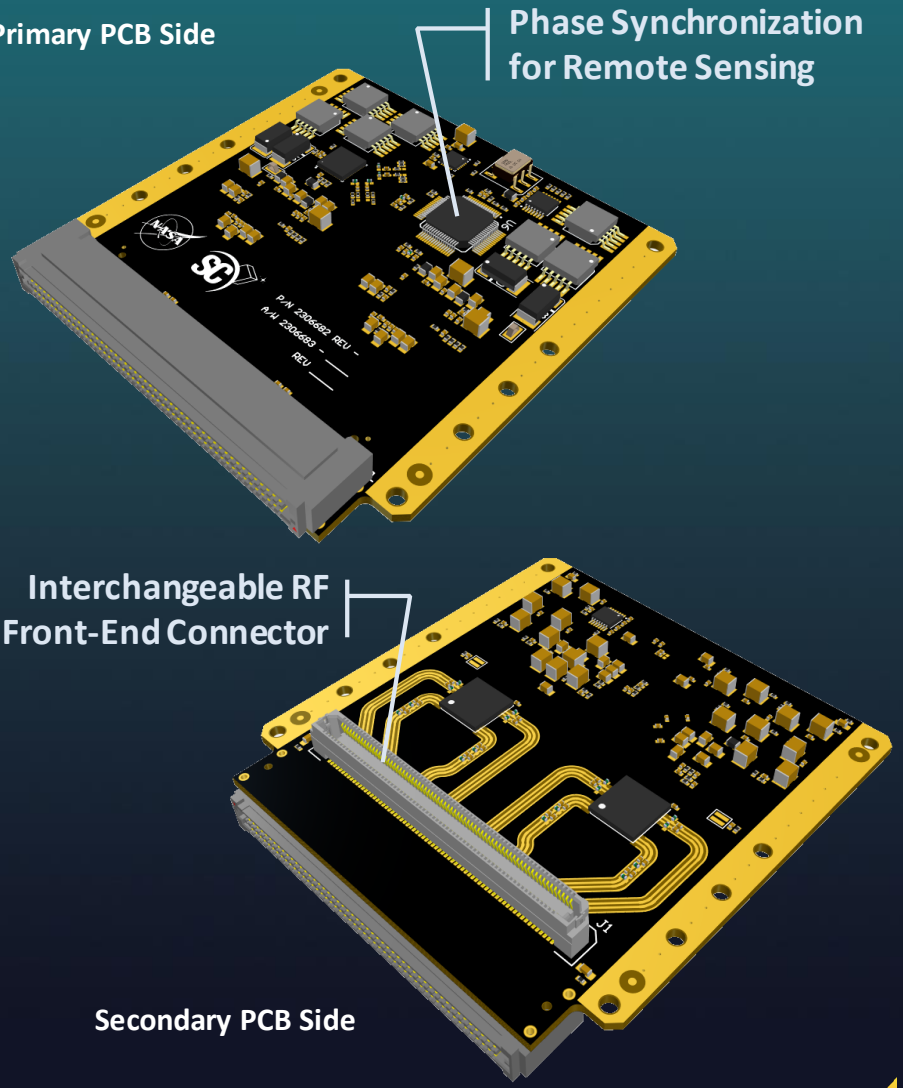
Resilient Adaptable MIMO Software-Defined Radio (RAMS)

Overview

- Dual phase-synchronized Analog AD9361
  - 4 × 4 MIMO configuration and simultaneous control of individual channels
- High-reliability component selection and extensive TID and SEL radiation testing
- Conforms to CubeSat Card Specification (CS^2) [CS]²

High-Level Specifications

- Internal, on-board, and external wideband fractional–N PLL synthesizer
- Interchangeable RF Front-End connector for varying operational modes
- Operating frequency from 70 MHz to 6 GHz
  - 12-bit ADC and DACs
  - Up to 56 MHz bandwidth per AD9361
- High-efficiency noise-optimized power system
  - Remote Sensing: 12W
  - Communication: 5W



SpaceCube v2.0 Processor Card

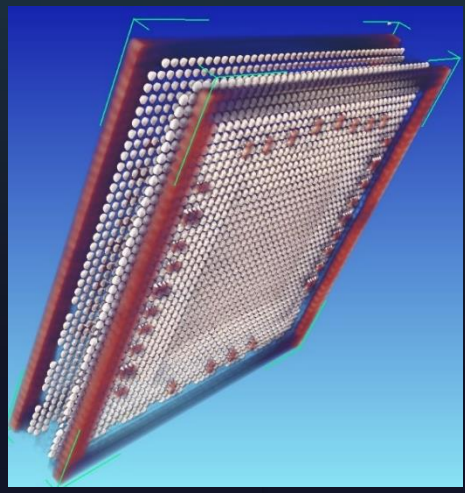
Overview

- TRL9 flight-proven processing system with unique Virtex **back-to-back** installed design methodology
- **3U cPCI** (190 mm × 100 mm) size
- Typical power draw: 8-10W
- 22-layer, via-in-pad, board design
- IPC 6012B Class 3/A compliant

High-Level Specifications

- 2x Xilinx Virtex-5 (QR) FX130T FPGAs (FX200T Compatible)
- 1x Aeroflex CCGA FPGA
  - Xilinx Configuration, Watchdog, Timers
  - Auxiliary Command/Telemetry port
- 4x 512 MB DDR SDRAM
- 2x 4GB NAND Flash
- 1x 128Mb PROM, contains initial Xilinx configuration files
- 1x 16MB SRAM, rad-hard with auto EDAC/scrub feature
- 16-channel Analog/Digital circuit for system health
- Mechanical support for heat pipes and stiffener for Xilinx devices
- External Interfaces
  - Gigabit interfaces: 4x external, 2x on backplane
  - 12x Full-Duplex dedicated differential channels
  - 88 GPIO/LVDS channels directly to Xilinx FPGAs
- Debug Interfaces
  - Optional 10/100 Ethernet interface

Back-to-Back FPGA Design

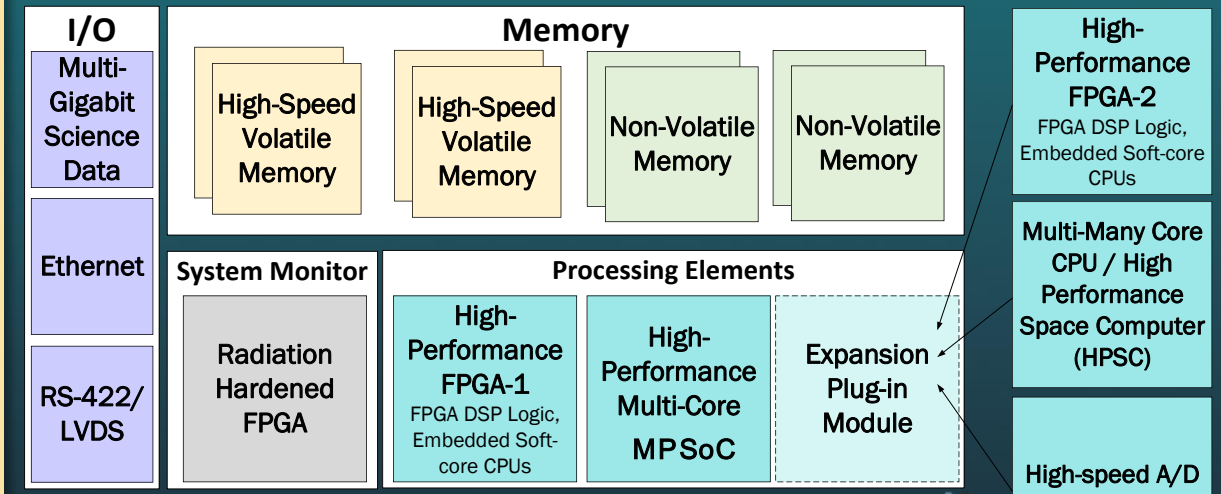


SpaceCube v3.0 Processor Card

Overview

- **Next-Generation** SpaceCube Design
- **3U SpaceVPX** Form-Factor
- Ultimate goal of using High-Performance Spaceflight Computing (**HPSC**) paired with the high-performance FPGA
  - HPSC will not be ready in time for the prototype design
  - Special FMC+ Expansion Slot

SpaceCube v3.0 Architecture



High-Level Specifications

1x Xilinx Kintex UltraScale

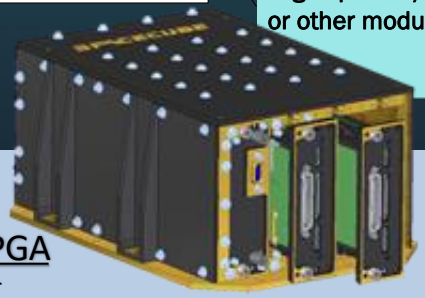
- 2x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - 24x Multi-Gigabit Transceivers
  - 75x LVDS pairs or 150x 1.8V single-ended I/O
  - 38x 3.3V single-ended I/O,
  - 4x RS-422/LVDS/SPW
- Debug Interfaces
  - 2x RS-422 UART / JTAG

1x Xilinx Zynq MPSoC

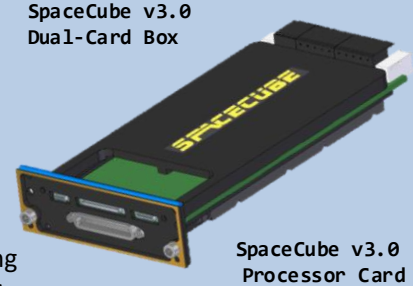
- Quad-core Arm Cortex-A53 processor (1.3GHz)
- Dual Arm R5 processor (533MHz)
- 1x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - I2C/CAN/GigE/SPIO/GPIO/SPW
  - 12x Multi-Gigabit Transceivers
- Debug Interfaces
  - 10/100/1000 Ethernet (non-flight)
  - 2x RS-422 UART / JTAG

Rad-Hard Monitor FPGA

- Internal SpaceWire router between Xilinx FPGAs
- 1x 16GB NAND Flash
- Scrubbing/configuration of Kintex FPGA
- Power sequencing
- External Interfaces
  - SpaceWire
- 2x 8-channel housekeeping A/D with current monitoring



SpaceCube v3.0 Dual-Card Box



SpaceCube v3.0 Processor Card