

LLISSE Accomplishments

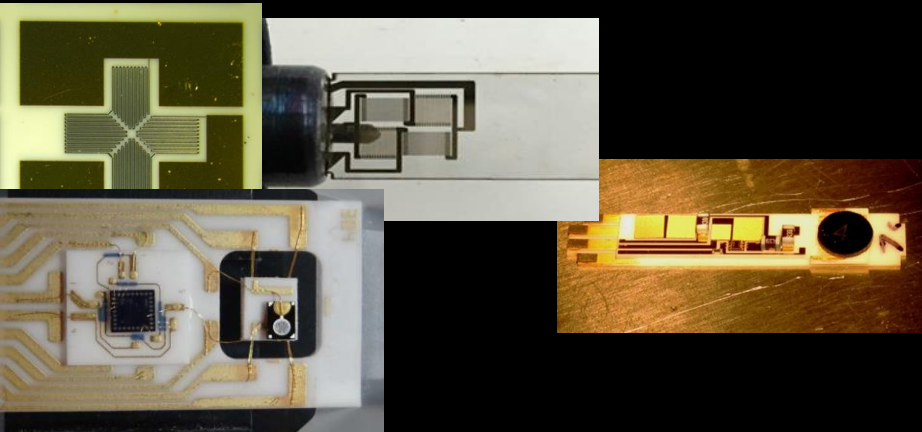
Compiled by Tibor Kremic 8/11/2021

Venus Surface Technology Advances Under LLISSE



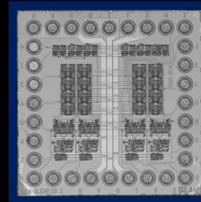
Communication:

- Conducted propagation and material tests
- Proof of concept of antenna developed
- First gen circuit designed and tested



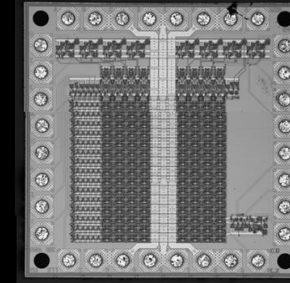
"IC Gen. 10" (2017)

(16-bit RAM, 195 SiC JFETs)
2 prototype 75 mm diameter SiC epi-wafers
3 mm x 3 mm, 32 I/O Bond Pads



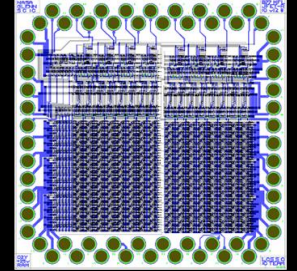
"IC Gen. 11" (2018)

(120-bit RAM, ~ 1000 SiC JFETs)
4 prototype 75 mm diameter SiC epi-wafers
4.65 mm x 4.65 mm, 32 I/O Bond Pads



"IC Gen. 12" (2021)

(248-bit RAM, ~ 2000 SiC JFETs)
6 prototype 100 mm diameter SiC epi-wafers
5 mm x 5 mm, 62 I/O Bond Pads

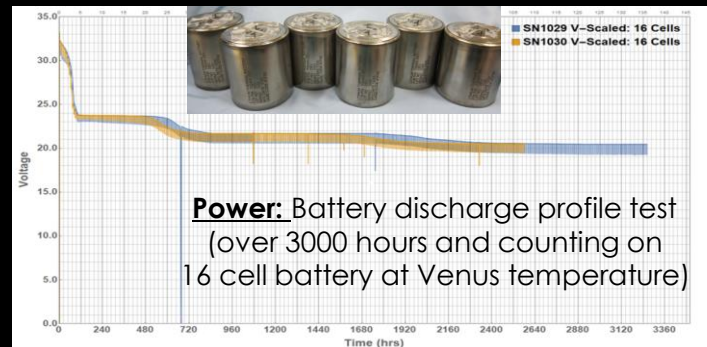


LLISSE Dramatically Increased the Level of SiC Electronics Complexity

- SiC electronics have demonstrated 1000's hours operation at 500C
- Electronics successfully operated during 60 day test in GEER (Venus surface conditions)
- Core electronics capability to operate LLISSE is in fabrication

Instrumentation / Sensors

- Material selection and first gen (or later) prototypes of all sensors completed
- *Most sensors have demonstrated successful extended operations in Venus conditions, some for the entire 60-day operations goal*
 - E.g. temperature, gas chemistry, wind, pressure
- Some sensors have demonstrated successful operation with driving background electronics as well – temperature, chemistry, pressure



LLISSE - An Approach to achieve a class of long-lived landers for Venus