DC Modeling of 4H-SiC nJFET Gate Length Reduction at 500 °C

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ABSTRACT: The development of robust, high-performance integrated circuits (ICs) will enable numerous potential NASA missions of current interest, including long-duration robotic missions exploring the 460 °C surface of Venus. Currently, NASA is looking towards SiC-based devices to provide such a solution. However, the current NASA silicon carbide (SiC) JFET device with a channel length of 6 µm (recently fabricated Gen. 11 ICs) limits mission-relevant circuit capabilities. In this study, we combined experiments with simulations to explore two straightforward fabrication strategies (shallow n^- and deep n^+) to reduce the SiC JFET channel length while maintaining turn-off behavior needed to realize 500 °C circuit operation. First, the material properties for 4H-SiC were implemented in COMSOL and the Poisson equation was solved for twelve 2D device designs. Then, based on the insights gained from the distribution of the electron concentration, electrostatic potential, and electric field for twelve designs (with three fabrication strategies), simulation for a 1 µm gate length nJFET with the turn-off performance comparable to the state-of-the-art.

1 INTRODUCTION

NASA is exploring Silicon Carbide, a wide-band-gap semiconductor material capable of operating at high-temperatures, based devices for the development of robust, high performance electronics to work under harsh environments (high radiation and high Venus surface temperatures). An elaborate and detailed discussion on the need for high-performance SiC electronics and the challenges faced with the current technologies can be found elsewhere (Neudeck et al. 2016, Neudeck et al. 2019). It is desired that current NASA silicon carbide (SiC) JFET device with a channel length of 6 µm, for recently fabricated Gen. 11 ICs (Neudeck et al. 2020), be improved upon by substantially shrinking the gate length towards 1 µm.

There are various strategies to reduce the gate length and feature size of a 4H-SiC JFET (Malhan et al. 2006). This paper presents a study on reducing the gate length of a lateral 4H-SiC nJFET by comparing and contrasting two fabrication strategies. The first fabrication strategy uses a shallow self-align nitrogen implant (Fig. 1a) along the device's top surface but not below the gate combined with a high-

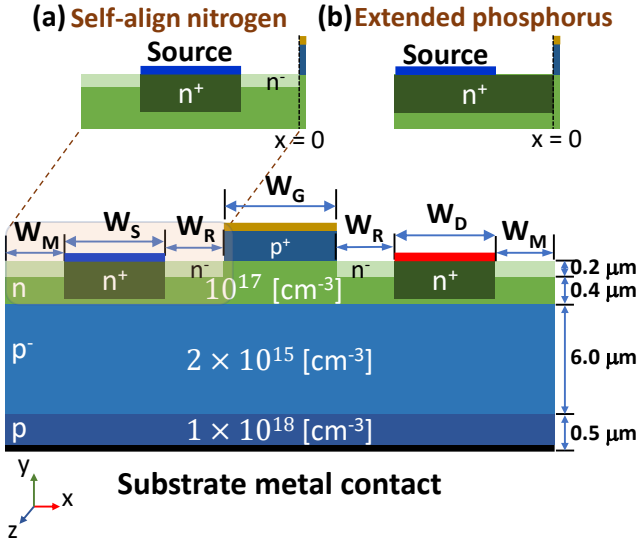

Figure 1: Schematic for the 4H-SiC nJFET device with two doping strategies: a) self-align nitrogen (SN) and b) extended phosphorous (EP). The different layers are p substrate (blue), p^- subchannel layer (light blue), n epitaxial layer (green), n^+ source and drain epilayer (dark green), n^- nitogen self-align implant (light green), and p^+ gate epilayer (dark blue).

dose phosphorous implant directly below the source and drain contacts, while the second fabrication strategy (Fig. 1b), the high-dose phosphorous implants extended from below the contacts all the way up to the gate edges. Two doping strategies are explored to reduce the gate length while maintaining or improving the turning-off response.

In this study, twelve variations of lateral epitaxial 4H-SiC nJFETs with different fabrication strategies and gate lengths were simulated in COMSOL. Since the COMSOL database does not have the material properties for 4H-SiC, these parameters were adopted from Ref. (Arvanitopoulos et al. 2017) and the model was validated with experiments conducted at NASA GRC. Finally, based on the insights (potential distribution below the gate and transfer characteristics) from twelve designs, results for a 1 µm device using both extended phosphorous and shallow self-align strategies with threshold voltages (V_{th}) similar to the current Gen. 11 device are presented.

2 METHODOLOGY

Experiment The first fabrication strategy uses a shallow self-align nitrogen implant (Figure 1a) along the device's top surface but not below the gate combined with a high-dose phosphorous implant directly below the source and drain contacts. This is consistent with experiments by NASA GRC in prototype IC generations 10 and 11 (Neudeck et al. 2020).

Finite-Element-Model The nJFET was simulated using commercial software, COMSOL Multiphysics v5.6 with the semiconductor module. The material parameters and the physical models used to simulate the electrical potential and carrier concentration profiles were taken from a published review (Arvanitopoulos et al. 2017). The models used to simulate the physics for nJFET were: Auger recombination, Shockley-Read-Hall (SRH) recombination, incomplete ionization, and low-field mobility. The device was simulated by solving Poisson's equation and the carrier continuity equations simultaneously.

The schematic cross-sections for the simulated 4H-SiC nJFETs is shown in Fig. 1. The n-channel JFET has device connections (source, gate, and drain) on the top and a substrate at the bottom. Note that it was important to include the p-substrate layer in the simulations to account for substrate body bias effect (Neudeck et al. 2016) and for the simulations to convergence. The implantation profiles for the high-dose phosphorous implant directly below the source, drain, and extended phosphorous implants, and the shallow self-align nitrogen implant are modeled using Gaussian distribution, with parameters listed in Table 1.

The following protocol was used to solve the Poisson equation in COMSOL for 4H-SiC nJFETs at

Table 1: Model parameters for Gaussian distribution used to fit the SIMS measurements for donor concentration.

Property	Value		Unit
	phosphorous	nitrogen	
N_{D0}	1×10^{20}	1.95×10^{18}	cm^{-3}
d_j^x	200	1	nm
d_j^y	200	120	nm
N_b	1×10^{17}	1×10^{17}	cm^3

460 °C (and 500 °C). Unfortunately, combining all the steps or rearranging the order did not lead to converged results. The convergence threshold paramter in COMSOL was set to 1×10^{-6}. The sequence of steps used to setup the simulation was important for the solution to converge. The sequence of steady-state simulations used to compute the transfer characteristics of the device was: first, the device was simulated at 25 °C with terminal voltages set to zero volt ($V_s = V_g = V_d = V_s = 0\,\mathrm{V}$) and without the generation and recombination models; second, the device was simulated with the generation and recombination models; third, the temperature of the device was changed from 25 °C to 460 °C (or 500 °C); fourth, the substrate voltage was changed to $V_s = -25\,\mathrm{V}$ (or $-15\,\mathrm{V}$); fifth, the drain voltage was increased to $V_d = 20\,\mathrm{V}$; Finally, the gate voltage was reduced from $0\,\mathrm{V}$ to $-15\,\mathrm{V}$ in $-0.5\,\mathrm{V}$ decrements. This simulation protocol was implemented in COMSOL as different study steps. The temperature and each terminal voltage are assigned using a separate study step, wherein the earlier solution is used as the initial condition for the current step.

3 RESULTS AND DISCUSSION

Before the gate optimization studies, the turn-off and transfer characteristics were validated with the measured data of a 4H-SiC nJFET with shallow self-align

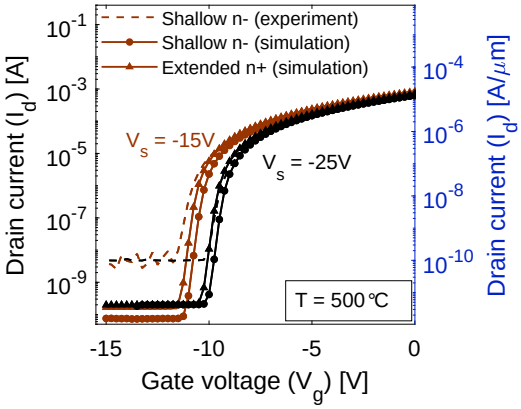

Figure 2: The transfer characteristics for a 6 µm gate length 4H-SiC nJFET with self-align N validated at 500 °C with measured experiments for two substrate biases, $-25\,\mathrm{V}$ (black) and $-15\,\mathrm{V}$ (brown). Left axis shows the total I_d (48 µm wide device) while the right axis shows normalized I_d. Note that measured current floor was limited by package leakage extrinsic to the device and was not simulated in the COMSOL (see text).

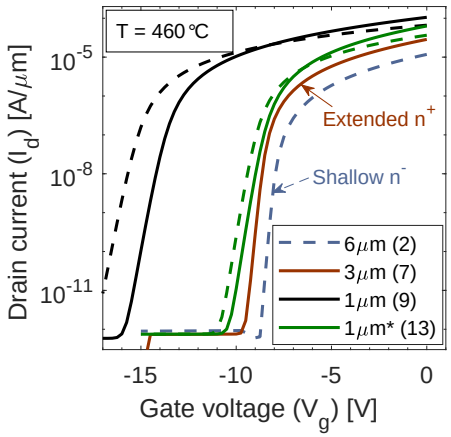

Figure 3: The simulated turn-off characteristics for selected designs from Table 2 (the device numbers are shown in brackets). Simulation results from the nitrogen self-align strategy are shown using dashed lines, while the extended phosphorous strategy results are shown using solid lines. Note that drain currents are normalized to the device width. Other simulation parameters were: $V_s = -25\,\text{V}$, $V_d = 20\,\text{V}$, and $T = 460\,°\text{C}$.

nitrogen implant at $500\,°\text{C}$ as shown in Fig. 2. The implantation profile (from SIMS measurements) of the self-aligned shallow nitrogen implant and phosphorous implants below the metal contacts were modeled (parameters listed in Table 1) using a uniform distribution with a Gaussian drop-off. The results of the transfer and output characteristics from the 4H-SiC JFET model and the simulation protocol implemented in COMSOL were validated with experiments. The device was simulated at $500\,°\text{C}$ with a $0.42\,\mu\text{m}$ n-epitaxial layer to match the experiments.

The threshold voltage for both the experiments and simulations is computed using the saturation extrapolation technique (Schroder 2005). The computed threshold voltage (V_g) for $V_s = -25\,\text{V}$ and $V_d = 20\,\text{V}$ shows a error of about 1% between measured ($V_g = -9.66\,\text{V}$) and simulation ($V_g = -9.83\,\text{V}$), while at higher substrate voltage ($V_s = -15\,\text{V}$), the error increased to 5% between experiment ($V_g = -10.68\,\text{V}$) and simulation ($V_g = -11.26\,\text{V}$). The high value of the turn-off current in the experiments was a result of the package leaking current (Neudeck et al. 2017), thus the model parameters were not modified to quantitatively match the experimentally measured turn-off current minimums, even though tuning the SRH recombination time could adjust the current floor (SRH recombination time lifetime for hole and electrons was held constant to $10\,\text{ns}$ throughout the study). The validated model was used to simulate the DC characteristics of the extended phosphorous strategy (Fig. 1b) and compare the performance against the self-align nitrogen doping strategy (Fig. 1a).

Note that since COMSOL limits the user to provide a single model for incomplete ionization (unless an explicit geometry is used and different material parameters are assigned to each geometry), the model parameters for phosphorous were used. We do not expect this change to affect the results significanly, since

Table 2: Transfer characteristics for thirteen 4H-SiC nJFET designs with two doping strategies simulated at $460\,°\text{C}$. The location of W_i listed in the table are shown in Fig. 1. The different types listed are self-align nitrogen (SAN), extended phosphorous (EP), and no strategy (NS). For the * cases, the n-epilayer thickness was reduced from $0.40\,\mu\text{m}$ to $0.34\,\mu\text{m}$.

#	Type	W_M μm	W_S μm	W_R μm	W_G μm	$-V_{th}$ V	I_{dss} A/m
1	SN	1.5	3.0	1.5	3.0	09.0	027.9
2	SN	3.0	6.0	3.0	6.0	08.2	011.8
3	SN	3.0	6.0	4.5	3.0	08.8	022.9
4	SN	3.0	3.0	4.5	3.0	10.0	028.5
5	SN	3.0	3.0	5.0	2.0	11.2	041.1
6	SN	3.0	3.0	5.5	1.0	15.8	066.3
7	EP	3.0	3.0	4.5	3.0	08.8	028.6
8	EP	3.0	3.0	5.0	2.0	09.7	046.0
9	EP	3.0	3.0	5.5	1.0	14.1	105.9
10	NS	1.5	3.0	1.5	3.0	10.0	028.0
11	NS	3.0	6.0	3.0	6.0	08.0	010.1
12	NS	3.0	6.0	4.5	3.0	10.0	019.0
13	EP*	3.0	3.0	5.5	1.0	08.8	063.2
14	SN*	3.0	3.0	5.5	1.0	09.4	036.6

the ionization energy are similar and impurities are completely ionized at higher temperature. The results show that the drain current for extended n^+ strategy is $\sim 14\%$ and $\sim 7\%$ higher than shallow n^- strategy for $V_s = -25\,\text{V}$ and $V_s = -15\,\text{V}$, respectively. The higher I_{dss} results from a deeper and higher concentration of dopants in the extended n^+ strategy. However, the change in the threshold voltage (V_{th}) is smaller, 2.5% and 2.7%, for substrate voltage $-25\,\text{V}$ and $-15\,\text{V}$ respectively.

Using this simulation framework, 14 devices were simulated (7 with shallow n^-, 4 extended n^+, and 3 without any doping strategy) and the results are presented in Table 2. As expected, increasing the gate length increases V_{th}. In contrast, reducing W_G ($6\,\mu\text{m}$ to $2\,\mu\text{m}$) lowers the threshold voltage. However, $1\,\mu\text{m}$ devices (#6) and (#9) with thicker nepi layer could not turn-off within the design constraints ($V_g \geq -15\,\text{V}$). By examining the potential, electron concentration (not shown), and electric-field (not shown) distributions inside the non-switching-off devices, the thickness of the nepi layer was reduced until the value of V_{th} was similar to the $6\,\mu\text{m}$ device. Reducing the nepi's thickness from $0.4\,\mu\text{m}$ to $0.34\,\mu\text{m}$, the threshold voltage was reduced to $-9.42\,\text{V}$ and $-8.9\,\text{V}$ for shallow n^- and extended n^+, respectively. The distribution of the maximum potential below the gate's surface and the Y-coordinate of the maximum potential are shown in Fig. 4) for the state-of-the-art device (a, d), and for the extended n^+ devices with gate length of $3\,\mu\text{m}$ (b, e) and $1\,\mu\text{m}$ (c, f). It is evident that as V_g decreases, the depth of the "potential well" increases and the device becomes "turned-off", which is not seen for the $1\,\mu\text{m}$ device (Fig. 4c) within $15\,\text{V}$.

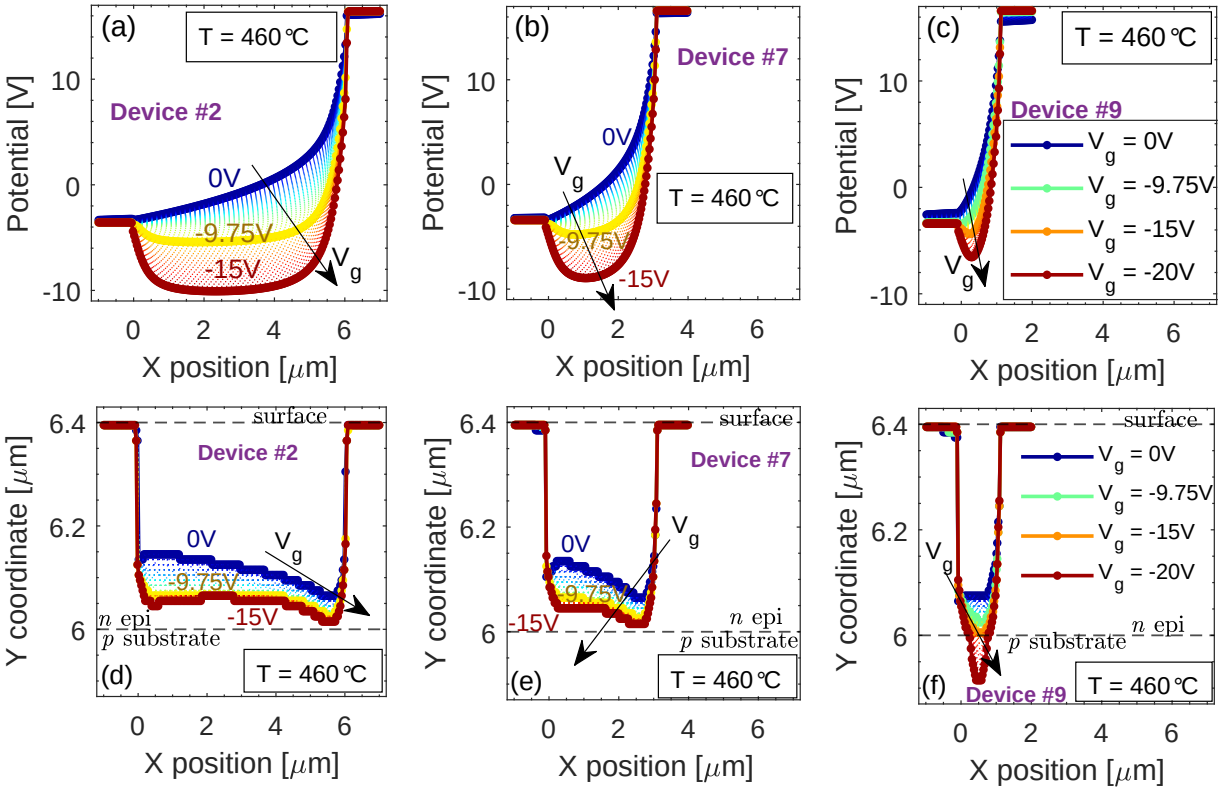

Figure 4: (a-c) The value of the maximum potential below the gate and (d-f) their Y-coordinate location (or depth) for the selected devices (2, 7, and 9) listed in Table 2. The substrate potential is held at -25 V. The devices were simulated at 460 °C.

4 CONCLUSIONS

In this paper, we explored design strategies to optimize the lateral-gate-length of a 4H-SiC JFET operating at 500 °C using COMSOL multiphysics. We compared the turn-off characteristics of two fabrication strategies, nitrogen self-align and extended phosphorous with gate length decreasing from $6\,\mu$m to $1\,\mu$m. The results show that the deeper and high concentration of phosphorous dopants lead to better turn-off response and provided a device with the gate reduced by 6X without compromising the turn-off performance when the gate is biased up to $V_g = -15$ V, while $V_s = -25$ V and $V_d = 20$ V.

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