SILICON VALLEY
AMES RESEARCH CENTER

DC Modeling of 4H-SiC nJFET Gate Length Reduction at 500°C

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Funded By

NASA Ames Research Center's Center Innovation Fund (ARC-CIF) and NASA Science Mission Directorate (SMD) under Long-Lived In-Situ Solar System Explorer (LLISSE)

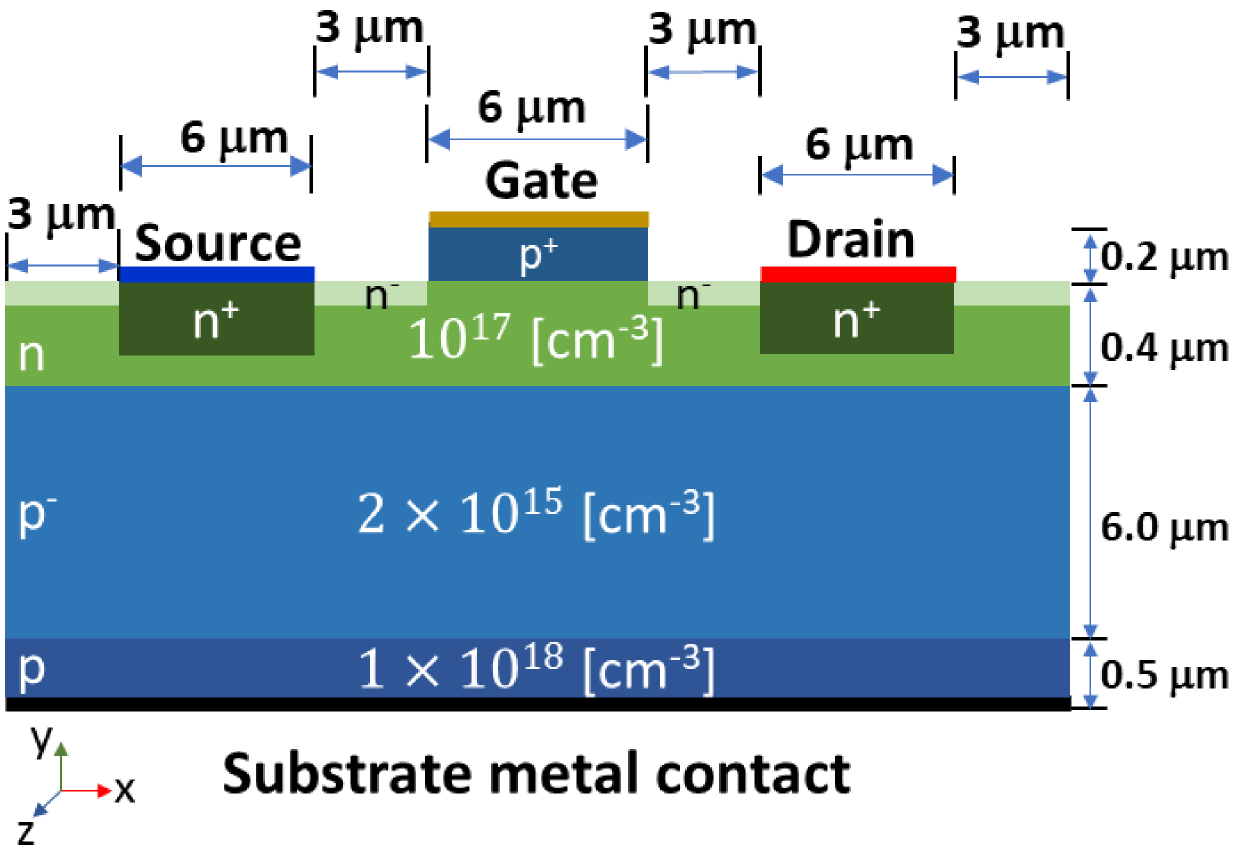
Presentation date: 10/28/2021

Outline

1. Introduction
2. 4H-SiC nJFET model in COMSOL
3. Validation of the 4H-SiC model
4. Results
5. Summary

500°C durable 4H-SiC nJFET structure

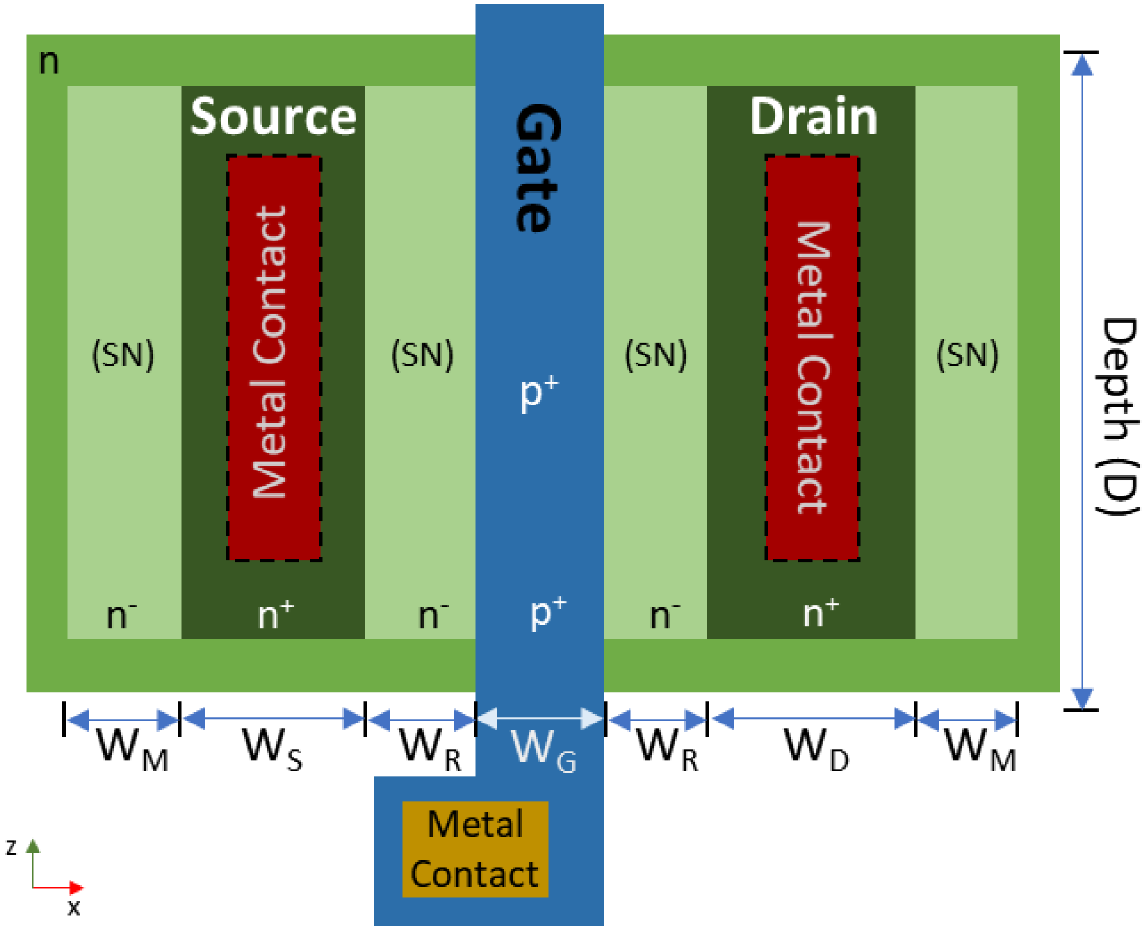
Cross-section



n^- -> Self-align nitrogen implant

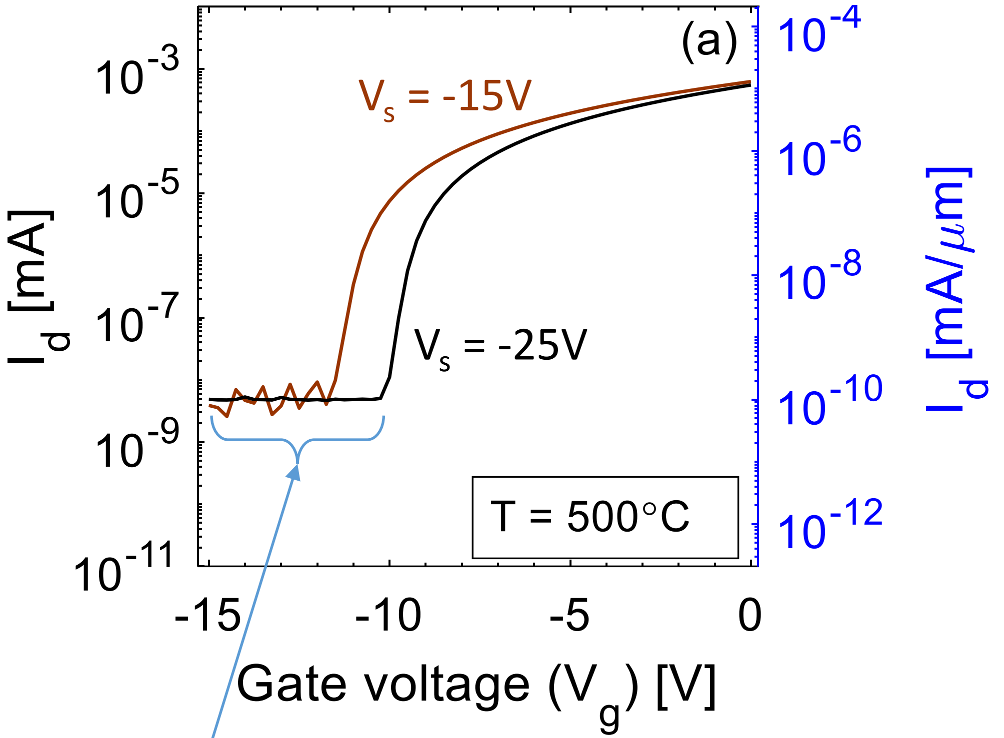
n^+ -> Phosphorous implant

Top view

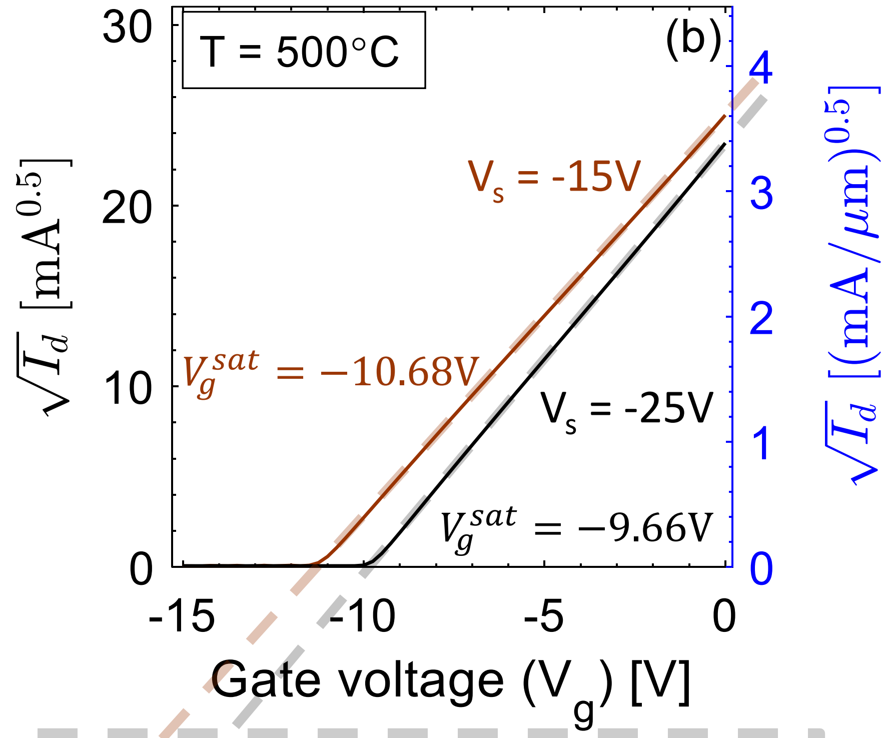


nJFET Turn-off for 6µm gate length

Measured IC Gen. 10 JFET I-V transfer characteristics



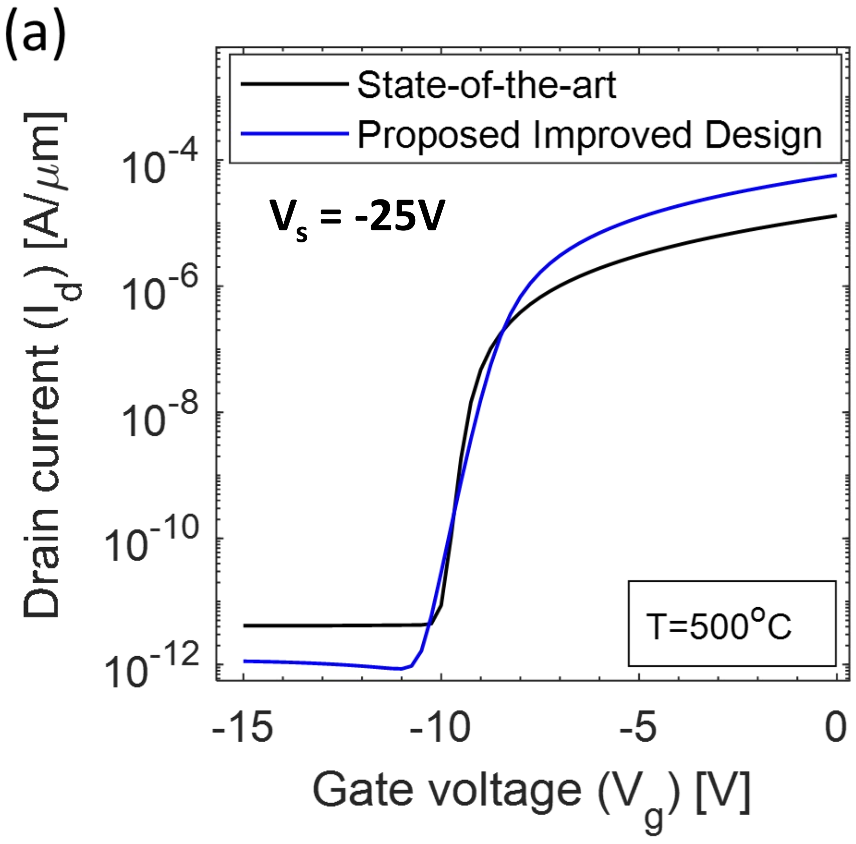
Measured off-state minimum current due to package leakage, not JFET [1]

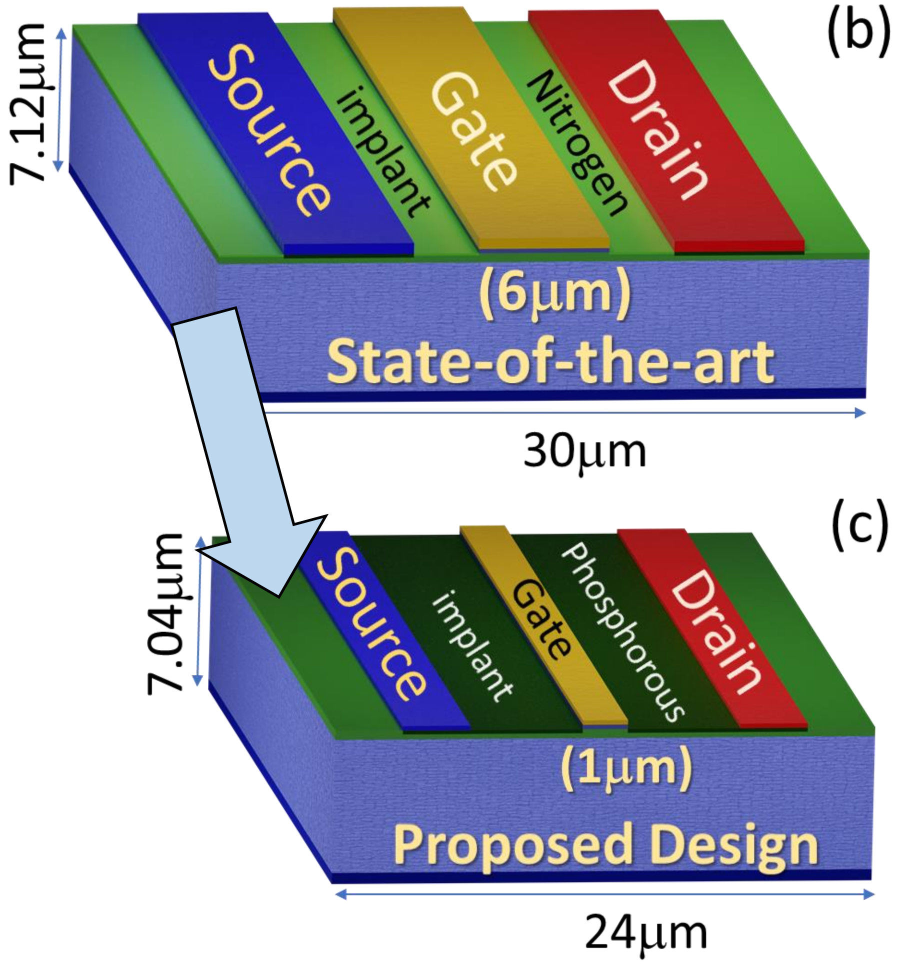


V_g^{sat} calculated from Saturation Extrapolation Technique

[1] P.G. Neudeck, D.J. Spry, L. Chen, N.F. Prokop, M.J. Krasowski, Demonstration of 4H-SiC Digital Integrated Circuits Above 800 °C, IEEE Electron Device Letters. 38 (2017) 1082–1085. https://doi.org/10.1109/LED.2017.2719280.

Goal of the Study





Understand quantitative design tradeoffs of reducing the gate length well below 6μm at 500 °C (and also 460 °C Venus surface temperature)

COMSOL Simulations

- Materials
  - SiC Antoniou (Cambridge) *(mat2)*
    - Basic *(def)*
    - Auger recombination *(Auger)*
    - Semiconductor material *(SemicondMaterial)*
    - Shockley-Read-Hall recombination *(SRH)*
    - Caughey-Thomas mobility model *(CaugheyThomasMobilityModel)*
    - Bandgap *(pg1)*
    - Jain-Roulston model *(JainRoulstonModel)*

4H-SiC Material Parameters

- Semiconductor *(semi)*
  - Semiconductor Material Model 1
  - Insulation 1
  - Zero Charge 1
  - Insulator Interface 1
  - Continuity/Heterojunction 1
  - Initial Values 1
  - p plus
  - n plus left
  - n self-align left
  - n plus right
  - n self-align right
  - n
  - p minus
  - p substrate
  - Source left
  - Drain right
  - Gate
  - Substrate
  - Trap-Assisted Recombination 1
  - Auger Recombination 1
  - Equation View

nJFET device implementation

Multi-study Simulation Protocol

- Simple Model (T=500degC)
  - Step 1: Step 1: Stationary Low Mesh
  - Solver Configurations
  - Job Configurations
- Complex Model (T=500degC)
  - Step 1: Step 1: Stationary Low Mesh
  - Solver Configurations
  - Job Configurations
- Change Vs=-25V
  - Step 1: Stationary Low Mesh 1
  - Solver Configurations
  - Job Configurations
- Change Vd=20V
  - Step 1: Stationary Low Mesh 1
  - Step 2: Stationary Low Mesh 1.1
  - Solver Configurations
  - Job Configurations
- Vg plot
  - Step 1: Vd=20V
  - Step 2: Vd=15V
  - Solver Configurations
  - Job Configurations
- All run
  - Simple Model (T=500degC)
  - Complex Model (T=500degC)
  - Change Vs=-25V
  - Change Vd=20V
  - Vg plot
  - Solver Configurations
  - Job Configurations

Equations

Low-field mobility

$$\mu_{\text{low}} = \mu_{\min} + \frac{(\mu_{\max} - \mu_{\min})}{1 + (N/N_{\text{ref}})^{\alpha}}$$

$$\mu_{\min/\max} = \mu^{0}_{\min/\max} \cdot (T/300\,\text{K})^{\gamma_{\min/\max}}$$

Auger recombination

$$R^{A}_{net} = (C_n n + C_p p)(np - n^2_{i,eff})$$

Incomplete Ionization

$$\frac{N_d^+}{N_d} = 0.5\left[1 + g_D \frac{n}{N_c} \exp\left(\frac{\Delta E_{D1}}{k_B T}\right)\right]^{-1} + 0.5\left[1 + g_D \frac{n}{N_c} \exp\left(\frac{\Delta E_{D2}}{k_B T}\right)\right]^{-1}$$

SRH recombination

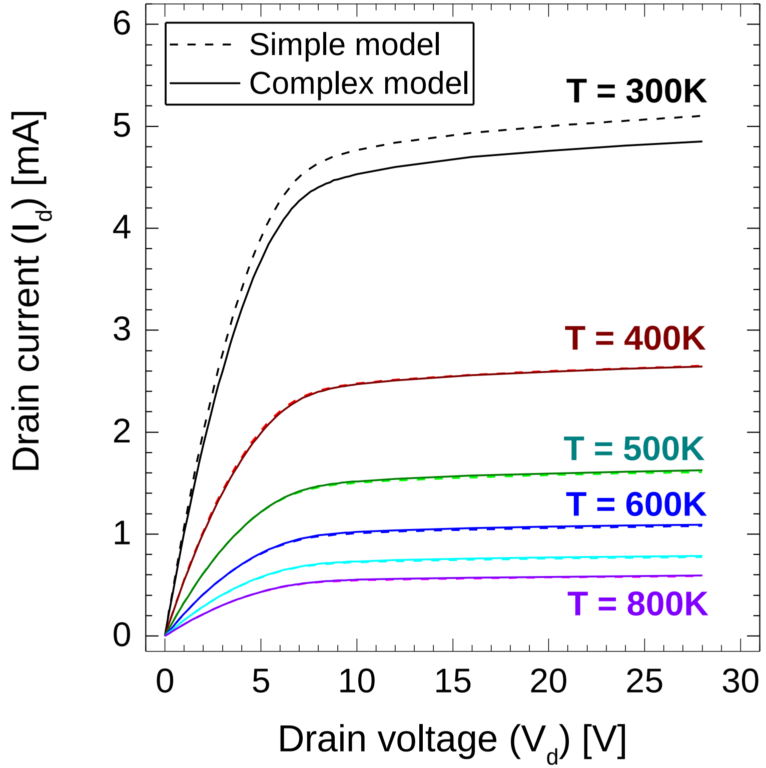
$$R^{\text{SRH}} = \frac{np - n_i^2}{\tau_p\,(n + n_1) + \tau_n\,(p + p_1)}$$

Arvanitopoulos, A., N. Lophitis, S. Perkins, K. N. Gyftakis, M. Belanche Guadas, and M. Antoniou. "Physical Parameterisation of 3C-Silicon Carbide (SiC) with Scope to Evaluate the Suitability of the Material for Power Diodes as an Alternative to 4H-SiC." In *2017 IEEE 11th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives (SDEMPED)*, 565–71, 2017. https://doi.org/10.1109/DEMPED.2017.8062411.

Influence of model complexity

Simple Model

- Low-field mobility



Complex Model

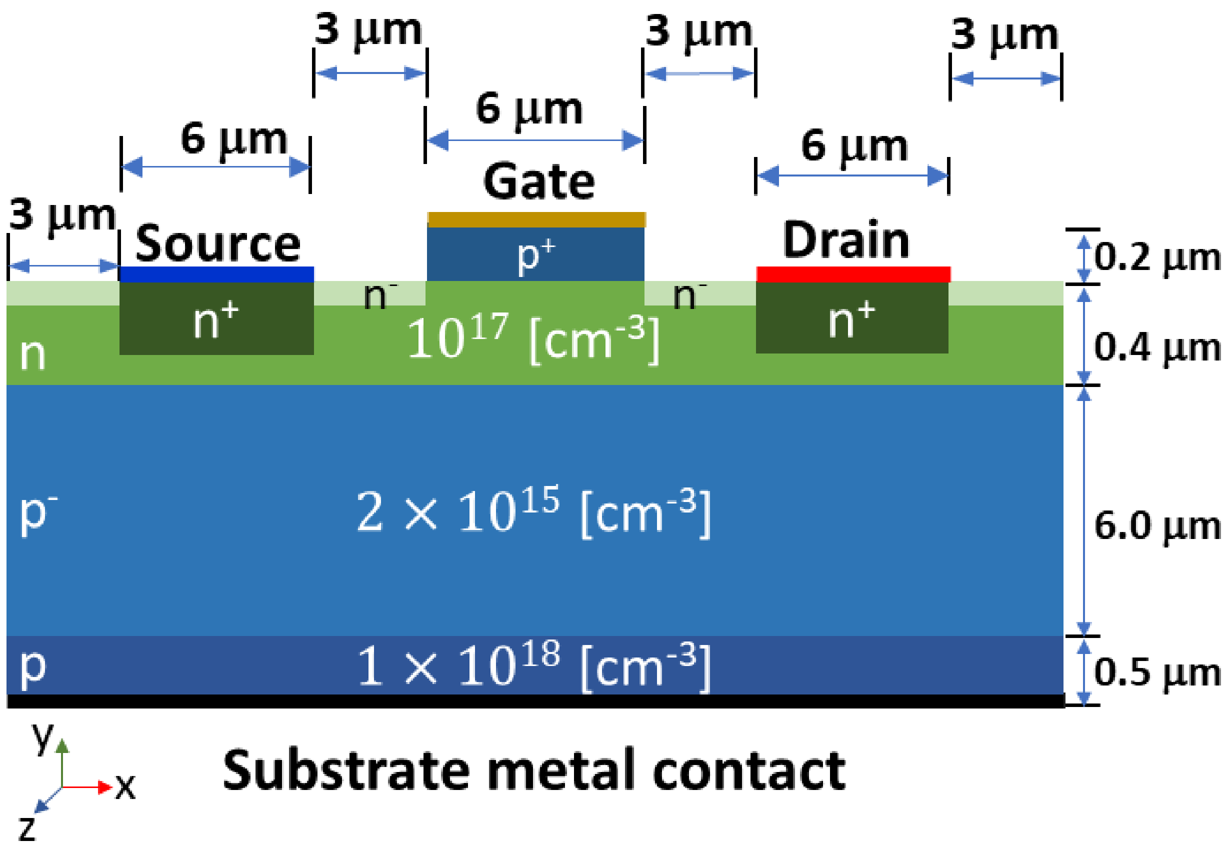
- Low-field mobility
- High-field mobility
- Incomplete ionization
- Auger recombination
- Impact ionization
- SRH recombination
- Band Gap narrowing

Higher operating temperature reduces the influence of the complex model

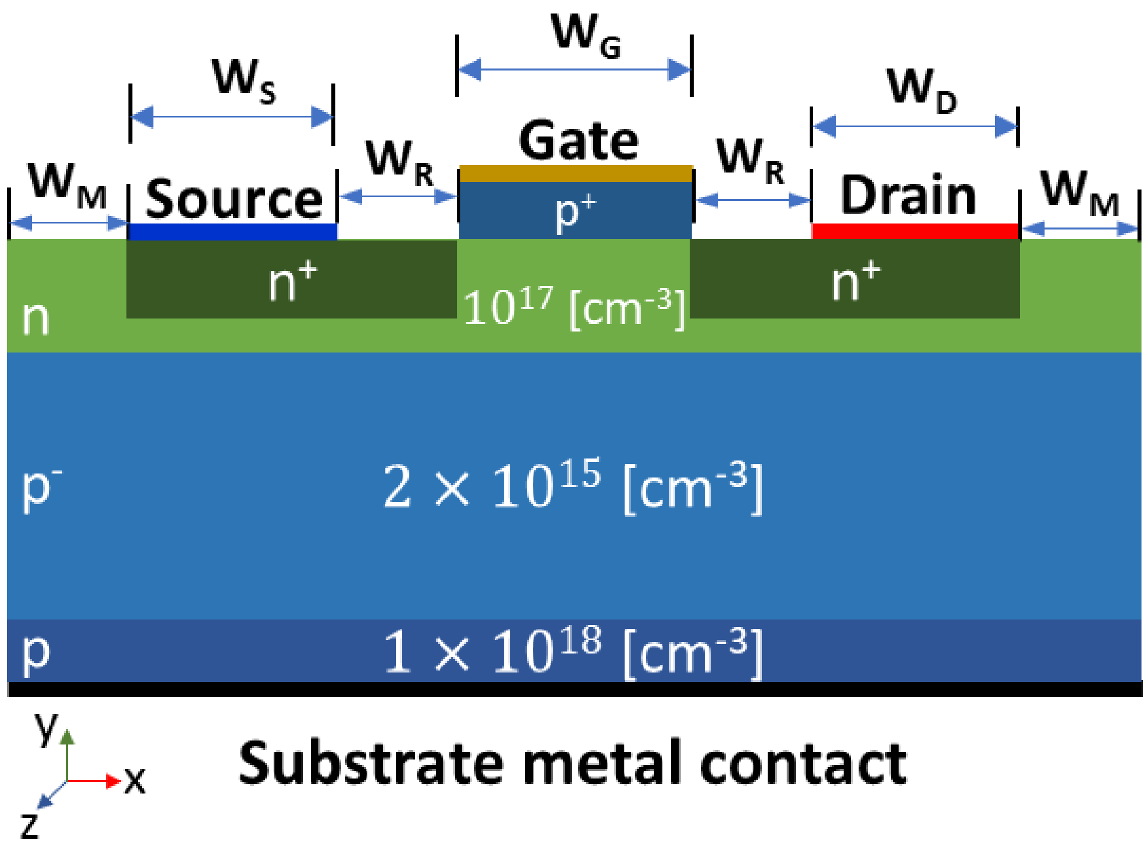
Schematic for Two Doping Strategy

Self-align nitrogen (SN; n^-)

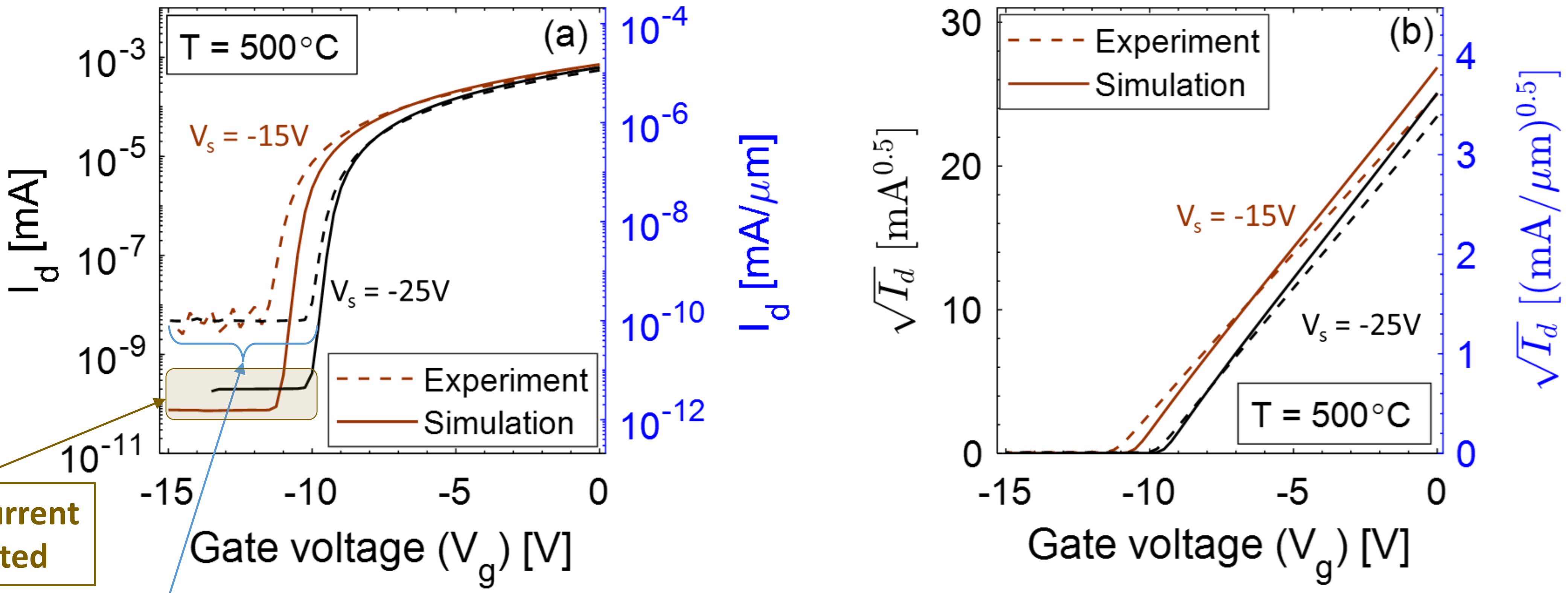
Experimentally realized IC Gen. 10 Device



Extended phosphorous (EP; n^+)



Validating simulation with experiment at 500°C

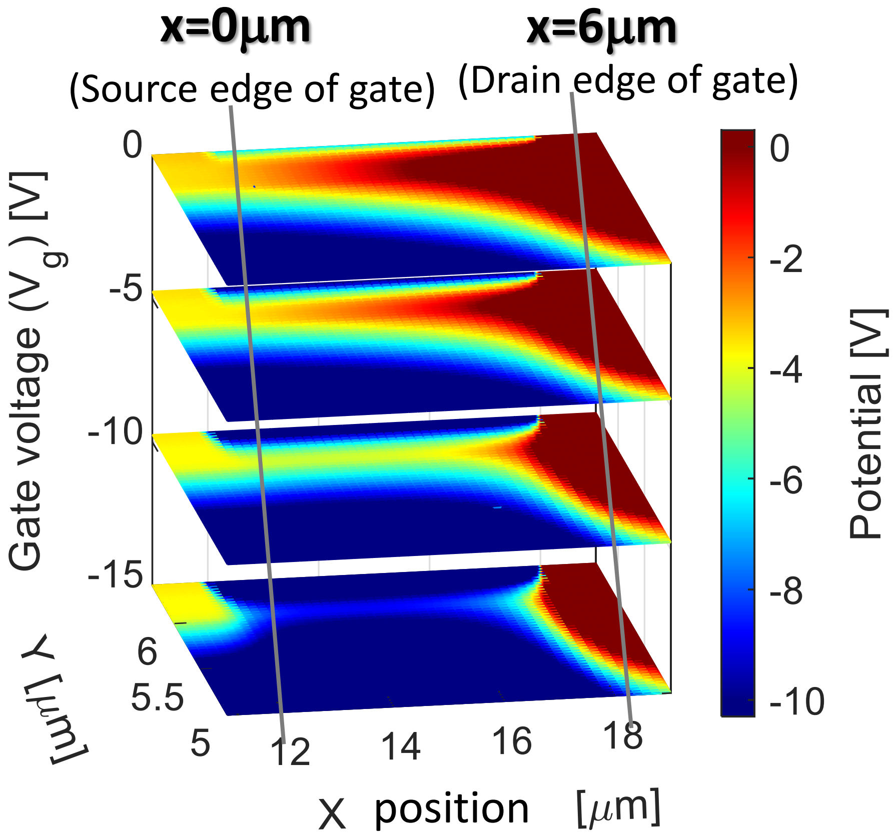


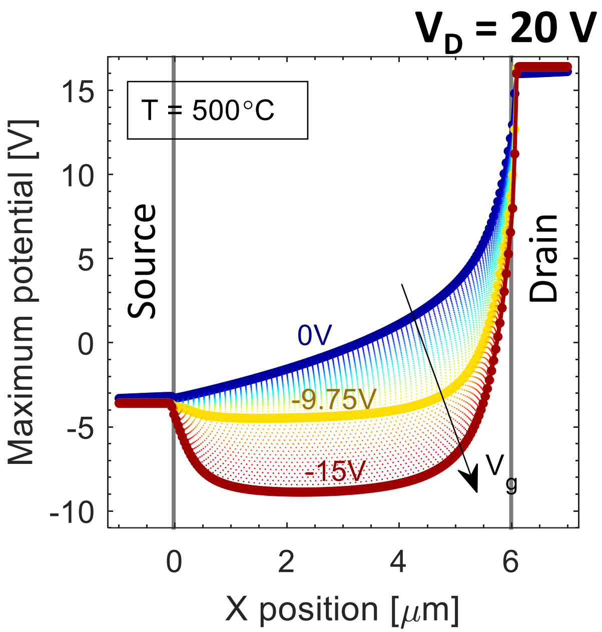
Leakage current not simulated

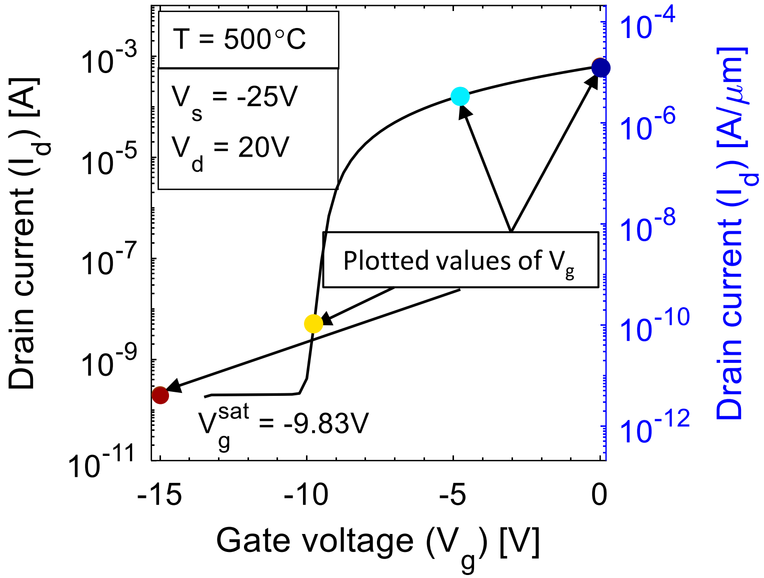
Experiment off-state minimum current due to package leakage, not JFET [1]

[1] P.G. Neudeck, D.J. Spry, L. Chen, N.F. Prokop, M.J. Krasowski, Demonstration of 4H-SiC Digital Integrated Circuits Above 800 °C, IEEE Electron Device Letters. 38 (2017) 1082–1085. https://doi.org/10.1109/LED.2017.2719280.

Long channel JFET potential profile





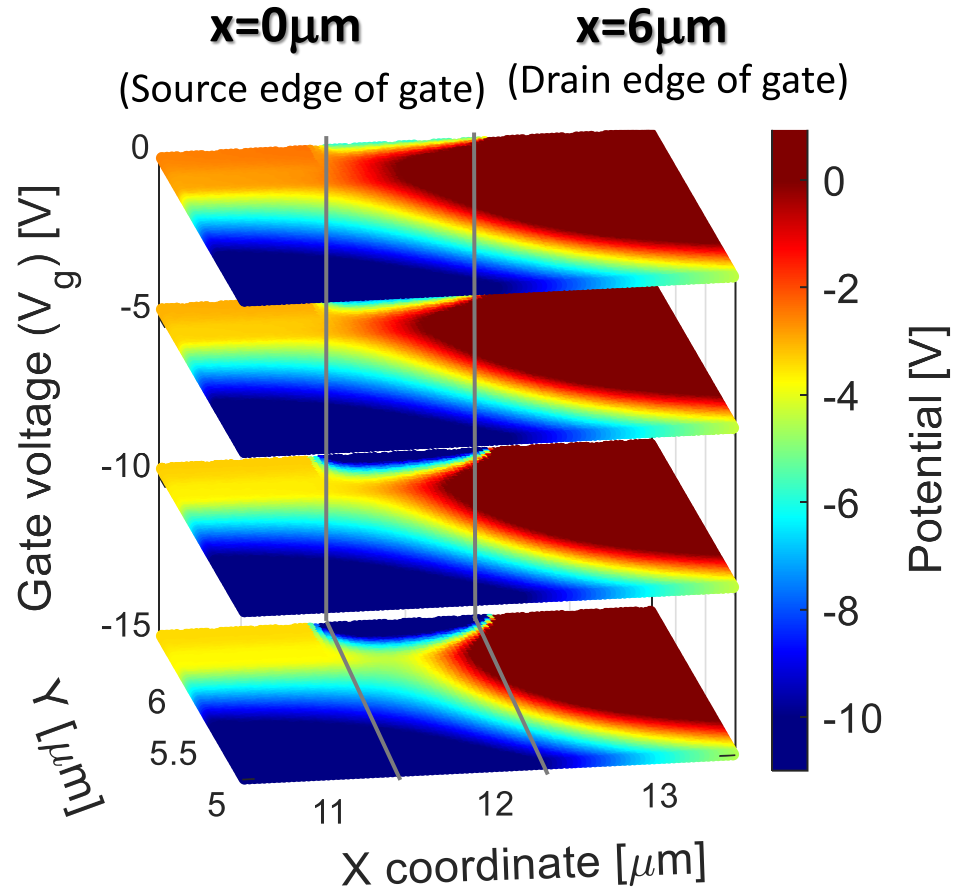


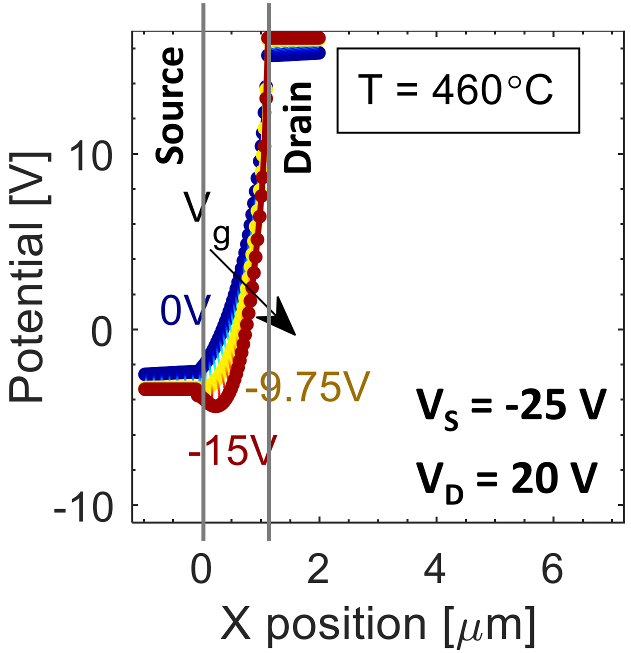
Device: 6 μm gate length SN JFET

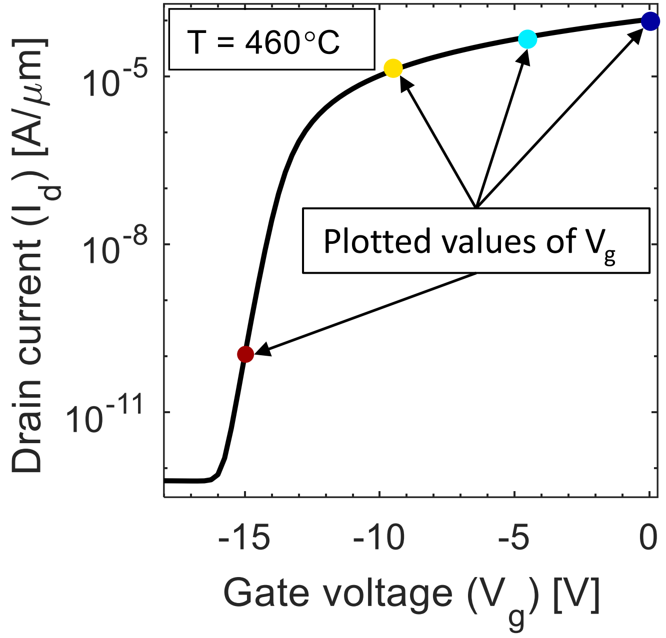
Simulation conditions: V_d = 20V
V_s = -25V
T = 500°C

- Electrons flow "uphill" towards positive bias drain terminal.
- No barrier to electron flow at V_G = 0 V (normally on device).
- Increasingly negative V_G creates potential barrier that exponentially cuts off electron flow from source to drain.
- Potential barrier is largest near middle x coordinate.
- Potential barrier is smallest near the bottom n-channel y coordinate, so this region controls off-state current flow.
- Drain bias has minimal influence on potential barrier and turn-off in long channel device.

Short channel JFET potential profile





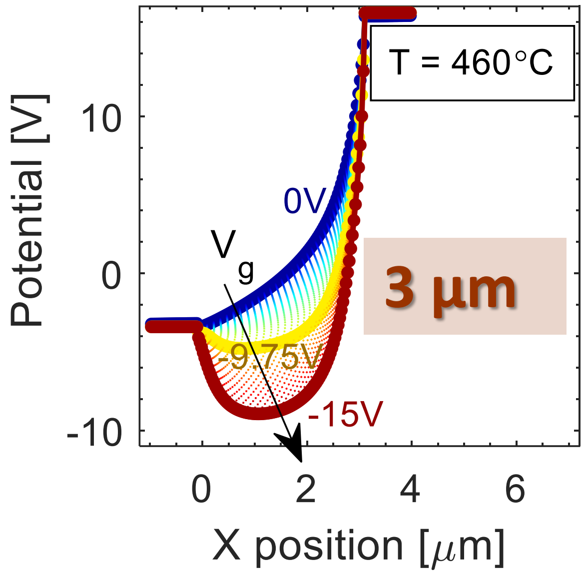


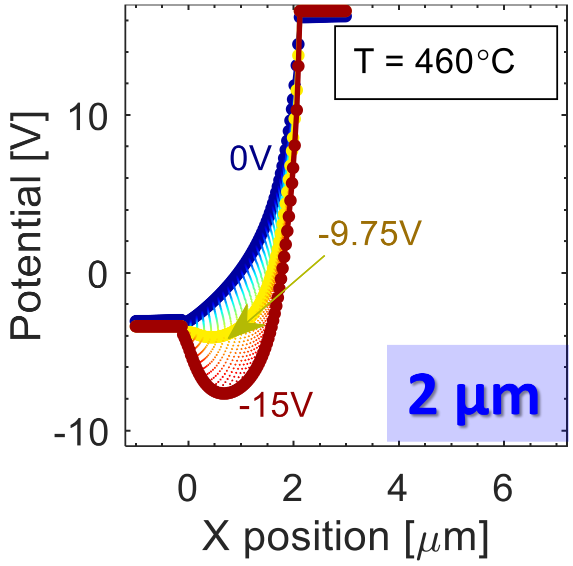
- "Short channel effects" significantly degrade turn-off properties.
- Drain bias has significant influence on potential barrier and turn-off in short channel device.
- Potential barrier maximum shifts to X-coordinate closer to the source terminal.
- Potential barriers are smaller than for long channel devices at comparable gate voltage

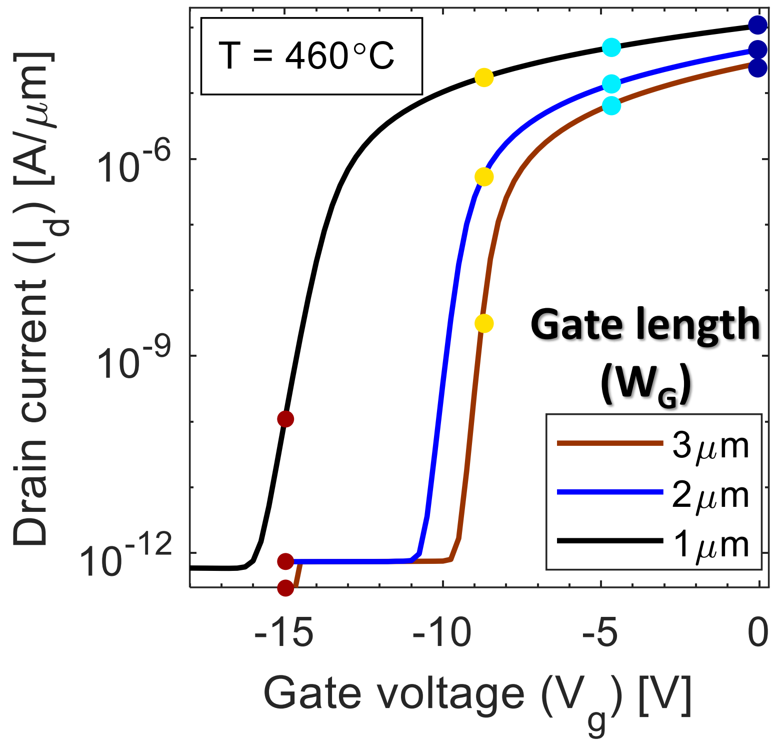
Device: 1 µm gate length EP nJFET
Simulation conditions: V_d = 20V
V_s = -25V
T = 460°C

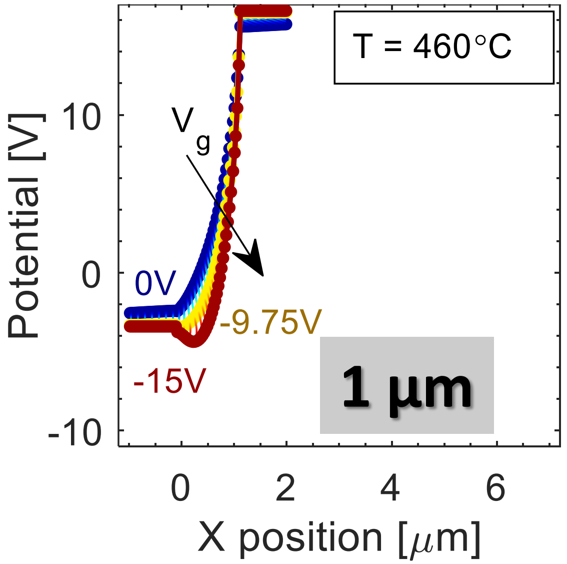
Shortening the gate length at 460°C

All plots are extended phosphorous (EP) device structure, n epi thickness 0.4 µm, V_d = 20 V, V_s = -25 V







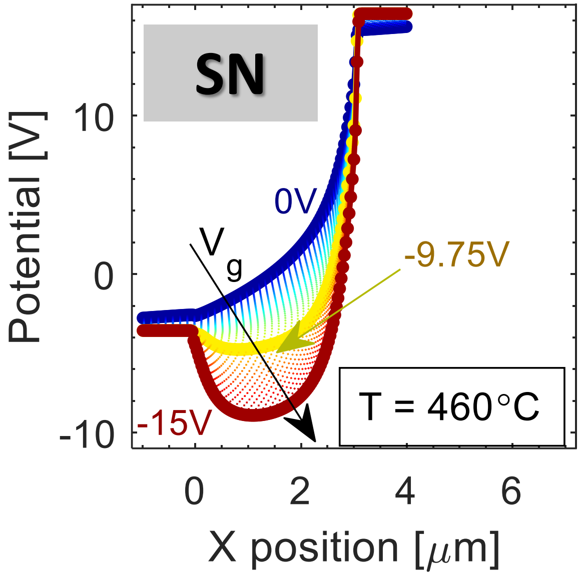


Shortening of gate length using EP implant strategy alone would not lead to a good turn-off performance

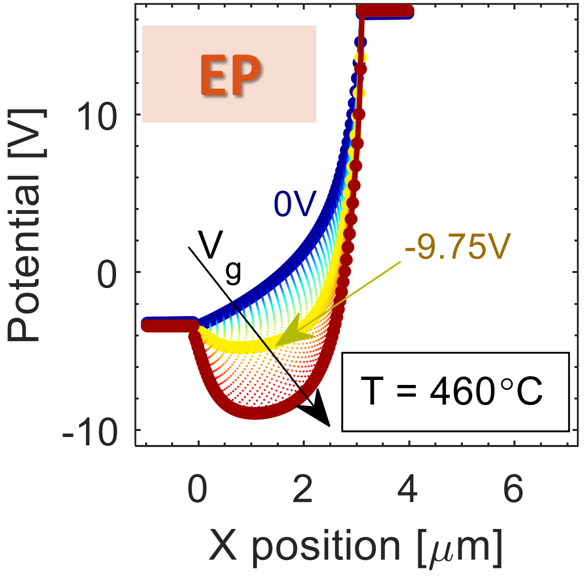
Implant Strategy at 460 °C

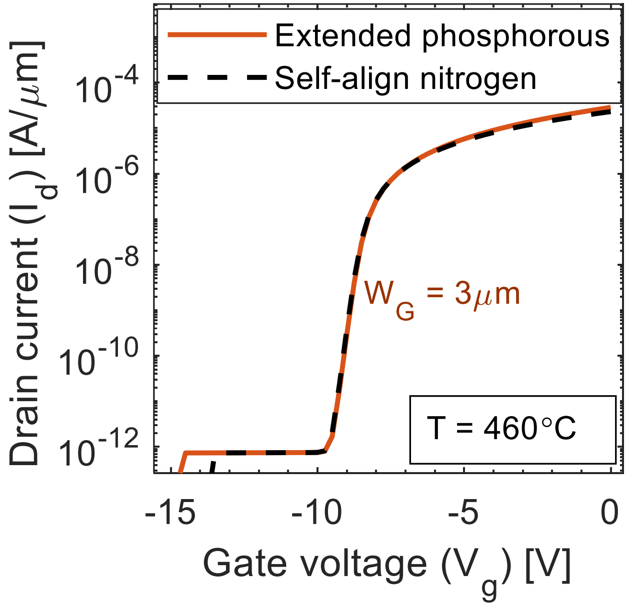
Gate length = 3 µm, N epi thickness, n epi thickness 0.4 µm, V_d = 20 V, V_s = -25 V

Self-aligned nitrogen



Extended phosphorous



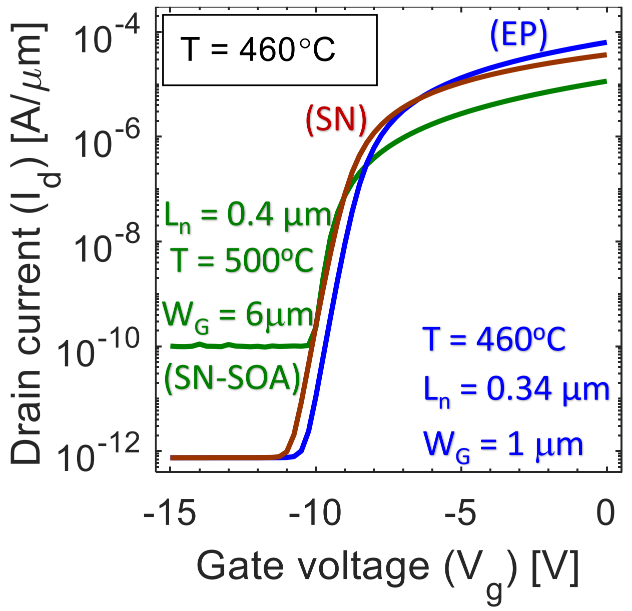


- Extended phosphorous strategy with its higher dose implant reduces parasitic source/drain resistance
- Increases ON-state I_{DSS} by about 20% without significantly changing JFET turn-off characteristics

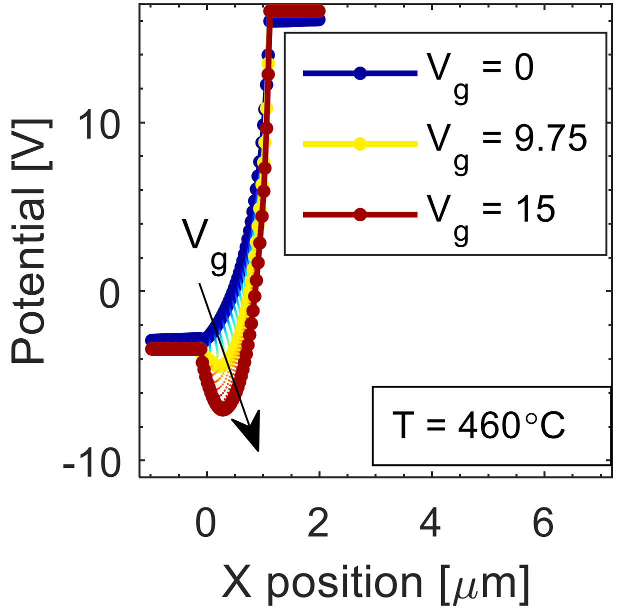
Thin-Epilayer Design

Reducing the n-epilayer thickness to 0.34 µm (from 0.4 µm) enables good turn-off in 1µm gate length device

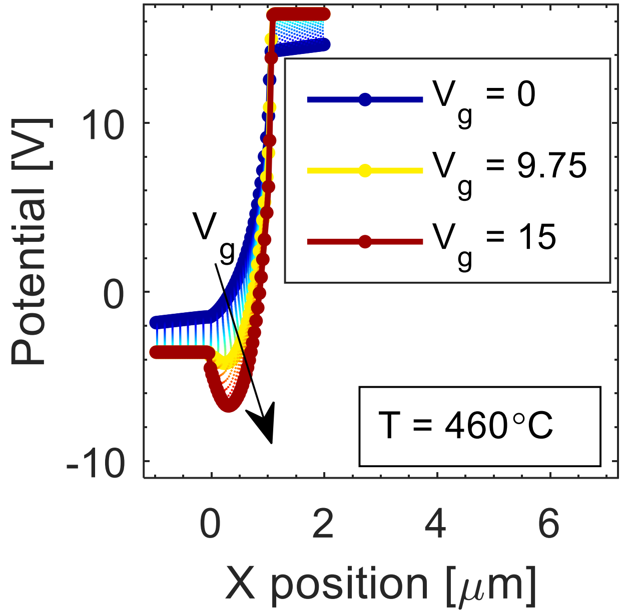
Simulation proposed designs



1 µm gate
Extended Phosphorous



1 µm gate
Self-aligned Nitrogen



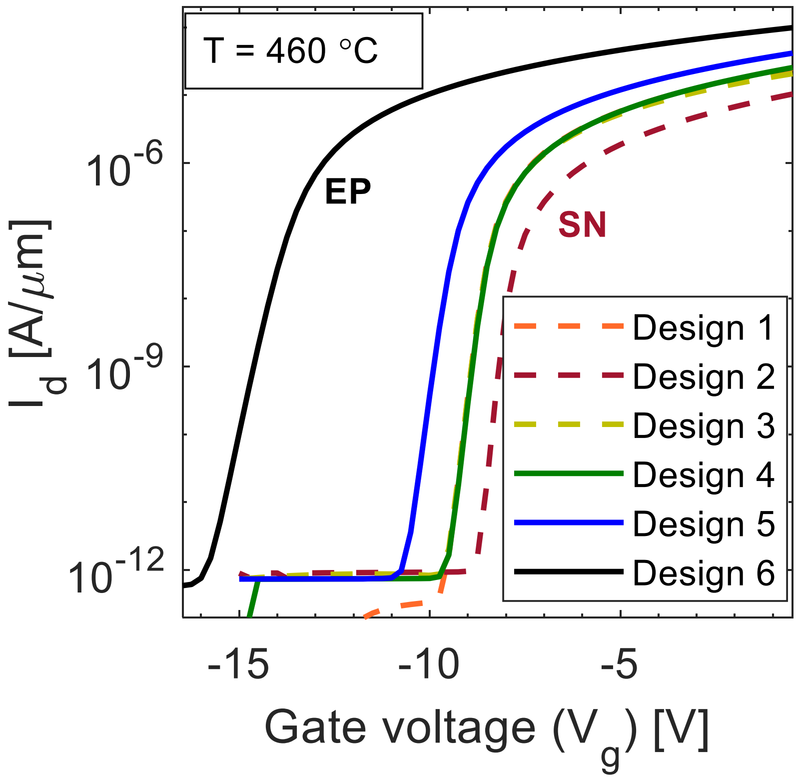
Thinner-channel approach significantly tightens the processing risk associated with SiC epilayer thickness tolerance/control as well as the gate finger etch depth.

Summary

- COMSOL simulation study of 4H-SiC JFET I-V characteristics at 500°C and 460°C
  - Verified agreement of simplified modeling with 6µm IC Gen. 10 measurements
  - 6 µm to 1 µm gate length
  - Self-aligned nitrogen and extended phosphorous source/drain implant geometries
  - 0.4 µm and 0.34 µm n-channel thickness
- Acceptable simulated performance at 500 °C for 1 µm gate length was obtained after the n-channel thickness was decreased from 0.4 µm to 0.34 µm

Back up Slides

Reducing W_G Through Simulations



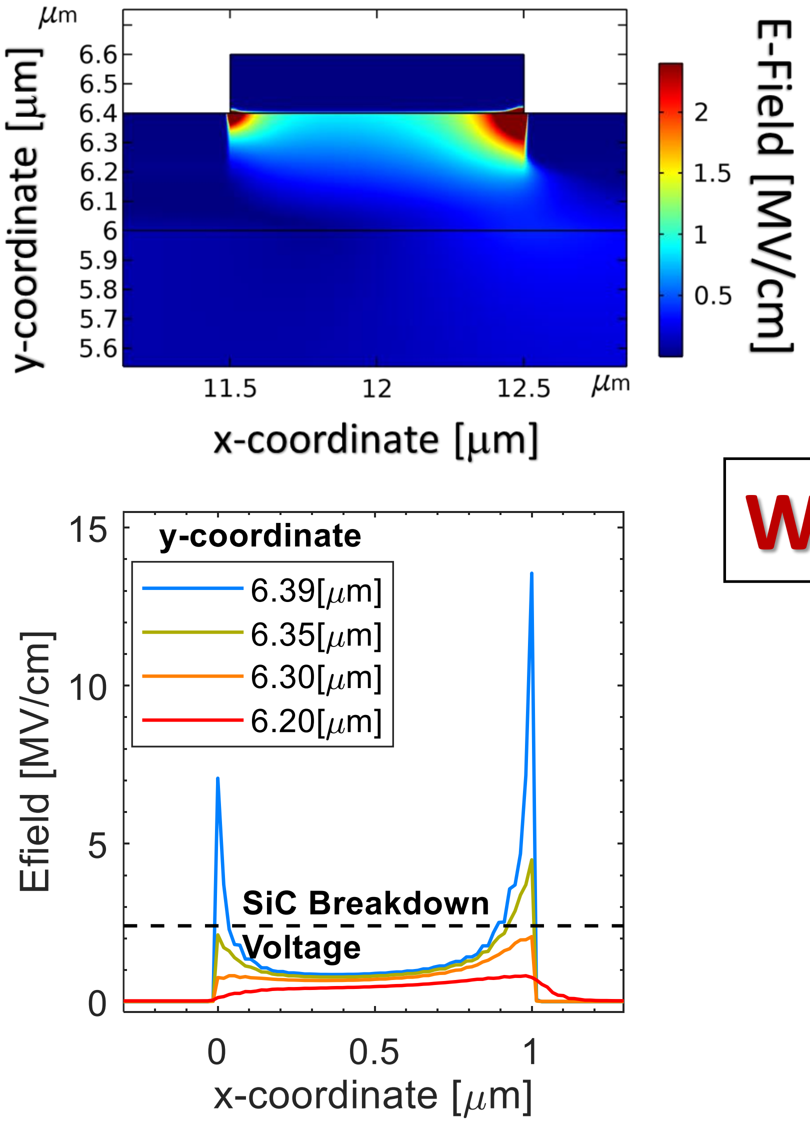
#	Dopant type	W_M [µm]	W_S [µm]	W_R [µm]	W_G [µm]	V_{th}[V]	I_{dss}[µA µm^{-1}]
1	Shallow n^-	1.5	3.0	1.5	3.0	-9	27.87
2	Shallow n^-	3.0	6.0	3.0	6.0	-8.2	11.79
3	Shallow n^-	3.0	6.0	4.5	3.0	-8.8	22.96
4	Extended n^+	3.0	3.0	4.5	3.0	-8.8	28.59
5	Extended n^+	3.0	3.0	5.0	2.0	-9.74	46
6	Extended n^+	3.0	3.0	5.5	1.0	-14.1	105.9

- Simulations use thicker *n* epilayer: 0.4µm
- Using a shallow n^- implantation strategy leads to **higher** V_g^{sat} and **lower** I_d^{sat}
- A total of 12 designs were explored

Either implantation strategy alone cannot lead to a thinner gate with the required turn-off performance

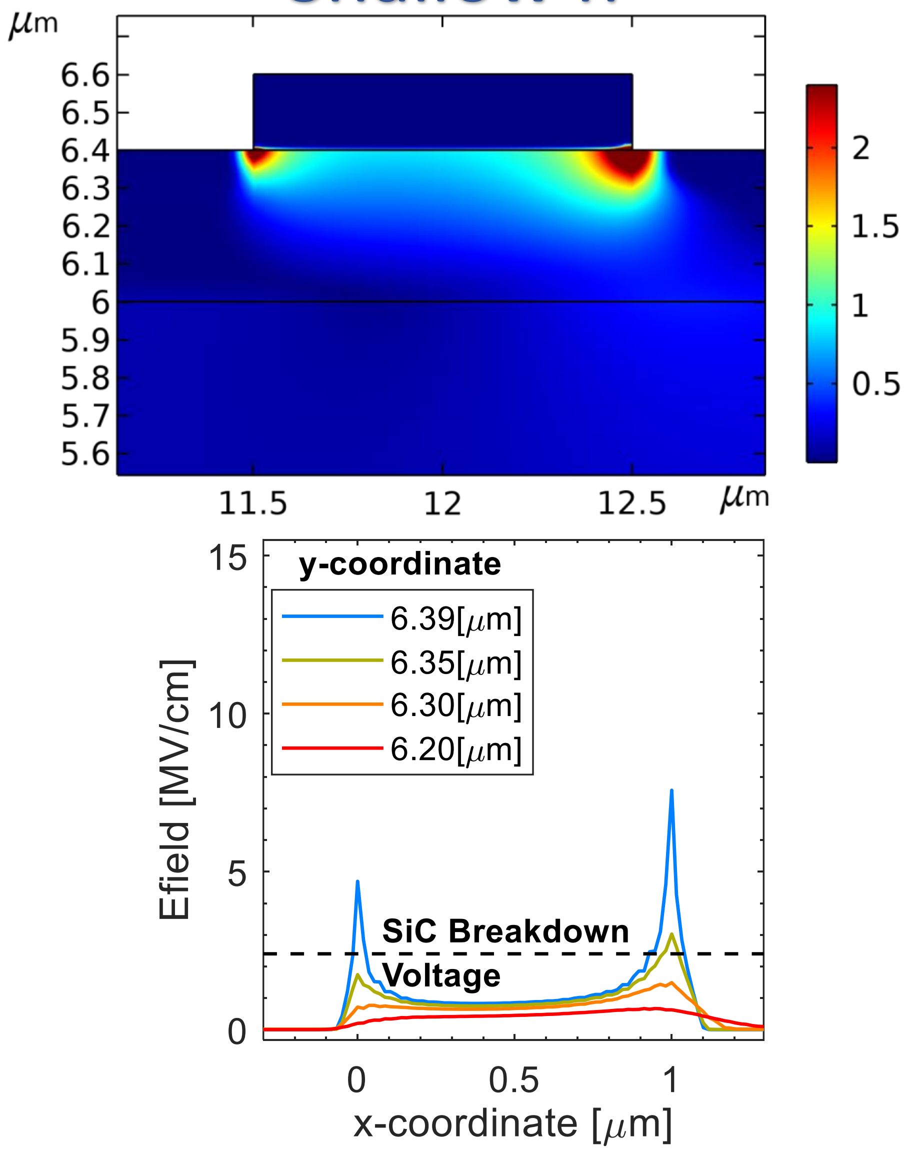
Electrical Field Distribution

Extended n^+

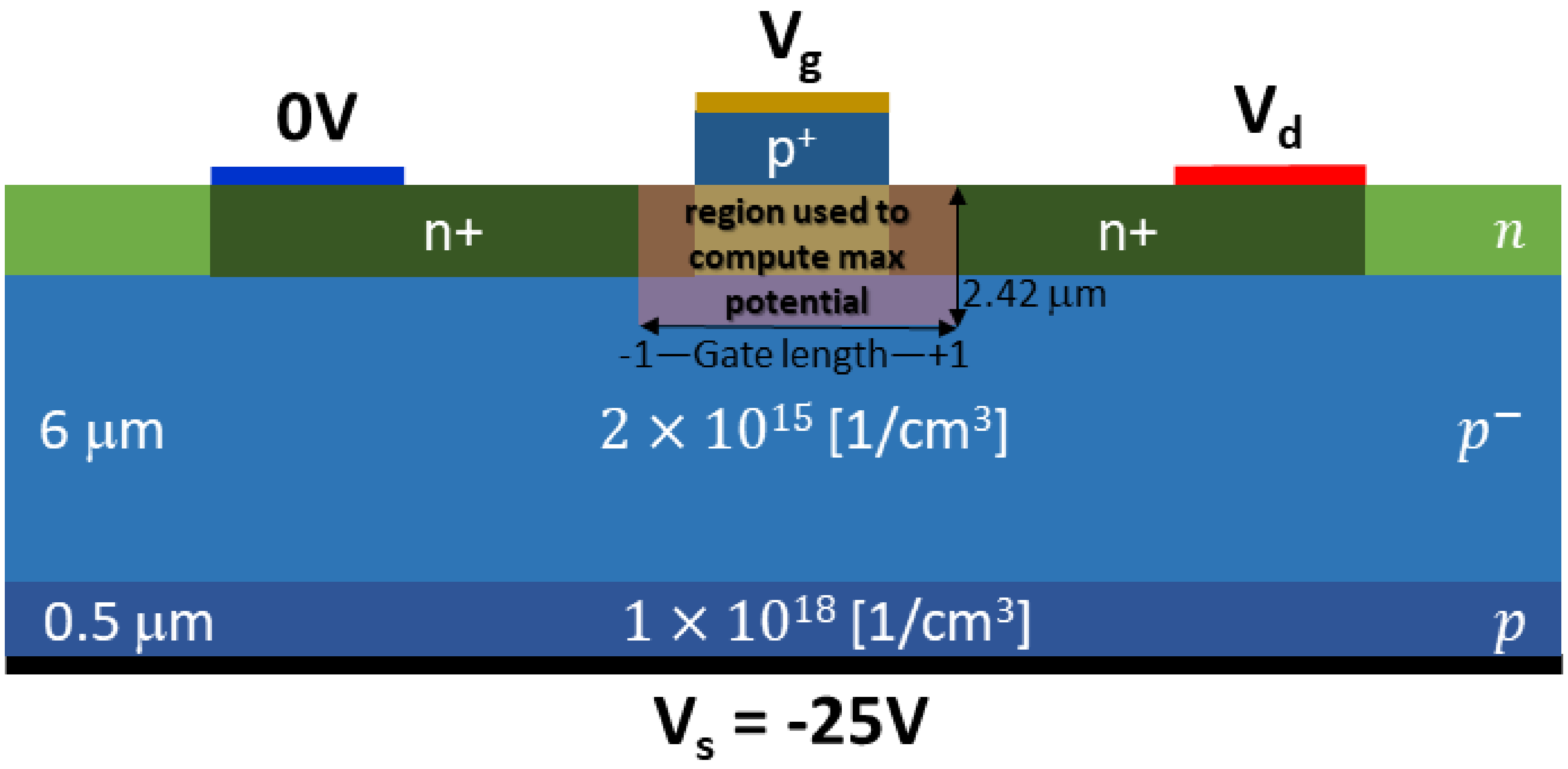


W_G = 1μm

Shallow n^-



Computation of the Max potential below the gate

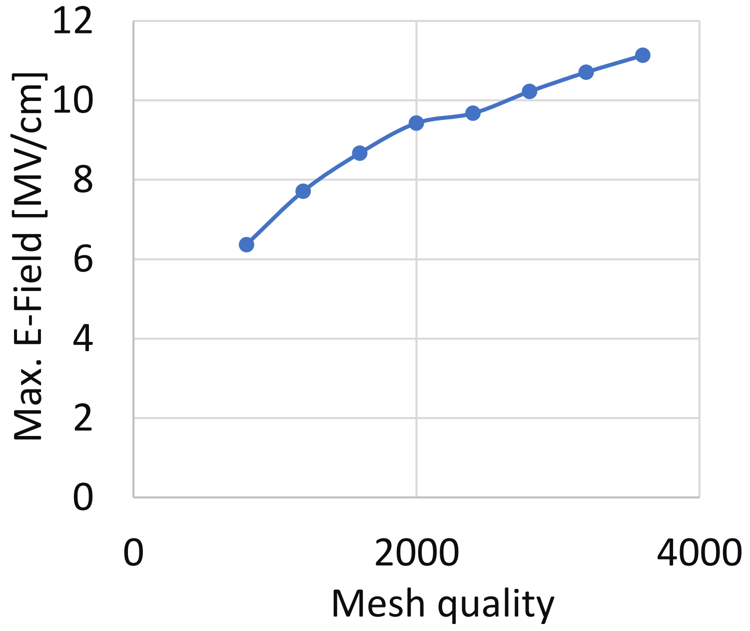


Meshing Effect on Electrical Field

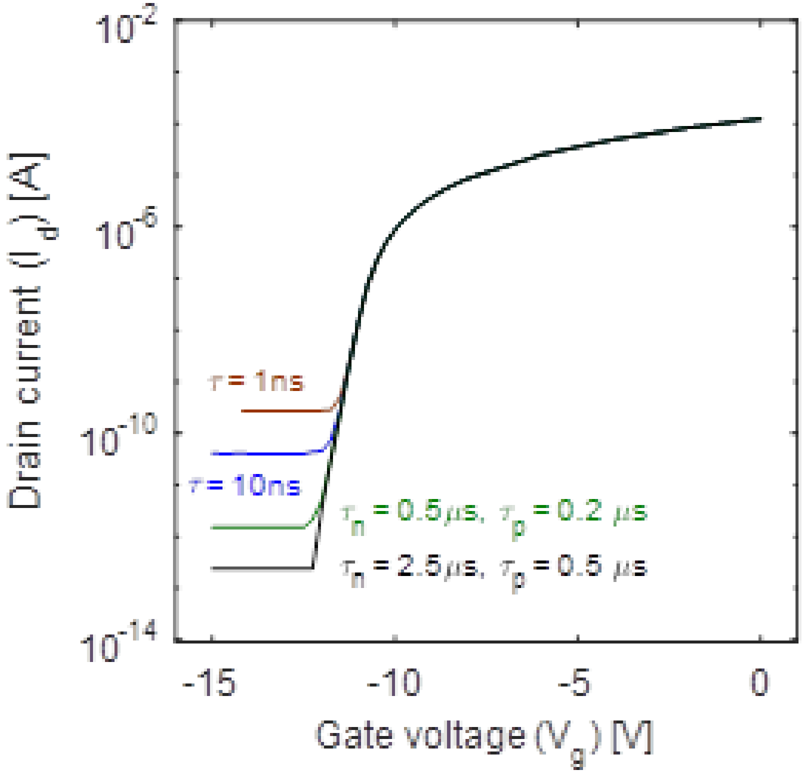
Extended n^+ (W_G: 1μm)

Fine Grid	Max. Efield (MV/cm)	I_d (A)
800	6.4	1.96E-10
1200	7.7	1.96E-10
1600	8.7	1.96E-10
2000	9.4	1.96E-10
2400	9.7	1.96E-10
2800	10.2	1.96E-10
3200	10.7	1.96E-10
3600	11.1	1.96E-10

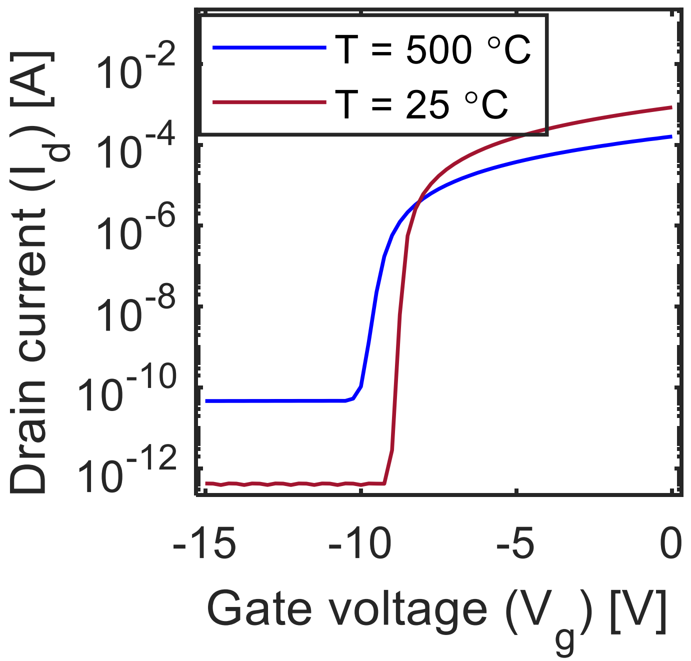
V_g = -15V, V_d = 20V, V_s = -25V



The "mesh quality" affects the maximum value of the electric field but not the drain current (I_d)

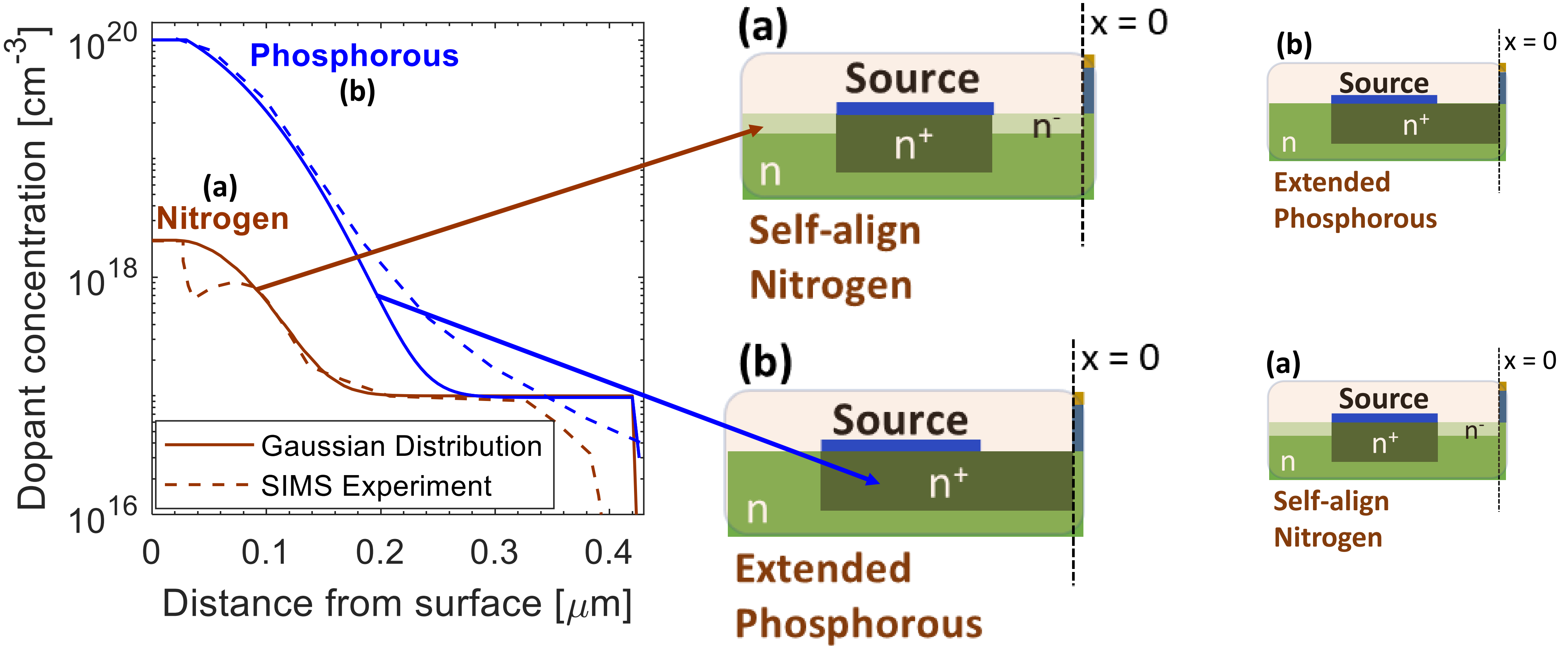


Drain current (I_d) [A]
Gate voltage (V_g) [V]
10^{-2}
10^{-6}
10^{-10}
10^{-14}
-15
-10
-5
0
τ = 1ns
τ = 10ns
τ_n = 0.5μs, τ_p = 0.2 μs
τ_n = 2.5μs, τ_p = 0.5 μs



T = 500 °C
T = 25 °C
Drain current (I_d) [A]
Gate voltage (V_g) [V]
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
-15
-10
-5
0

Dopant Implant Profile



Parameters

Low-field mobility

Parameter	p	n
μ^0_{max}	$125\,cm^2\,V\,s$	$950\,cm^2\,V\,s$
γ_{max}	-2.15	-2.4
μ^0_{min}	$15.9\,cm^2\,V\,s$	$40\,cm^2\,V\,s$
γ_{min}	-0.57	-1.536
N_{ref}	$1.76 \times 10^{19}\,cm^{-3}$	$1.94 \times 10^{19}\,cm^{-3}$
α	0.34	0.61

Auger recombination

Property	value	units
C_n	5×10^{-31}	cm^6/s
C_p	2×10^{-31}	cm^6/s

Incomplete Ionization

Property	value	unit
g_D	4	1
ΔE_{D1}	60.7	meV
ΔE_{D2}	120	meV
g_A	4	1
ΔE_A	198	meV

SRH recombination

Property	value	units
τ_n	10	ns
τ_p	10	ns
ΔE_t	0	V