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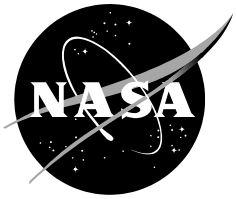

ISSI IS46DR16640B-25DBA25 DDR2 SDRAM Heavy Ion Single-Event Upset Test Report

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February 2022

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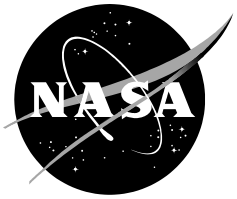

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Test Date: 10/2/2017
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1. Introduction

The purpose of this testing was to obtain heavy ion-induced single event upset (SEU) cross sections and error rates for the Integrated Silicon Solutions, Inc. (ISSI) IS46DR16640B-25DBA25. The test was conducted at Texas A&M University's Cyclotron Institute. Testing occurred on October 2, 2017.

2. Test Samples

The IS46DR16640B-25DBA25 is a DDR2 SDRAM from ISSI with a 64Mx16 (8Mx16x8 banks) configuration. Five (5) parts from two Lot Date Codes (LDC) for the ISSI IS46DR16640B-25DBA25 were provided for testing: 1504 and 1510. The datasheet was the March 2015 version. More information can be found in Tables 1 – 3.

Table 1: Part Identification Information

Qty	Part Number	LDC	REAG Identifier	Package
8	IS46DR16640B-25DBA25	1504	16-011	BGA-84
8	IS46DR16640B-25DBA25	1510	16-012	BGA-84

Table 2: SDRAM Address Table

Parameter	Addresses	Total
Row Addressing	A0-A12	13
Column Addressing	A0-A9	10
Bank Addressing	BA0-BA2	3
Pre-charge Addressing	A10	1

Table 3: Clock Cycle Timing

Parameter	-25D	Units
Speed Grade	DDR2-800D	
CL-tRCD-tRP	5-5-5	tCK
tCK(CL=3)	5	ns
tCK(CL=4)	3.75	ns
tCK(CL=5)	2.5	ns
tCK(CL=6)	2.5	ns
tCK(CL=7)	2.5	ns
Frequency (max)	400	MHz

3. Test Facility

Facility:	Texas A&M University Cyclotron Institute
Ions (Energies MeV/amu):	Ne, Kr, Xe, Ar
Angles	0°, 30°, 60°
LETs (MeV-cm^2/mg):	1.9 – 55.5
In Vacuum (y/n):	No

4. Test Conditions and Error Modes

Test Temperature:	Room temperature
Power Supply Voltages:	1.8 V_{DC}
Run Type	Static, Dynamic, Random
Error Modes:	SEUs, SEFIs, Bursts of errors independent of SEFIs

5. Test Methods

Equipment necessary:

A project-developed test setup by Jackson & Tull (J&T) contractors was used for testing. The DDR2 die was mounted on SODIMMs and then tested using a Xilinx ML507 evaluation board with the external power supply connector attached to an Agilent N6702B for external power. The 1.8V power supply for the DUT was isolated by disabling the regulator on the evaluation board and connecting a laboratory DC supply; both were controlled via LabView. The DDR2 die was thinned to 100 µm for testing. Figure 1 shows an image of the evaluation board used.

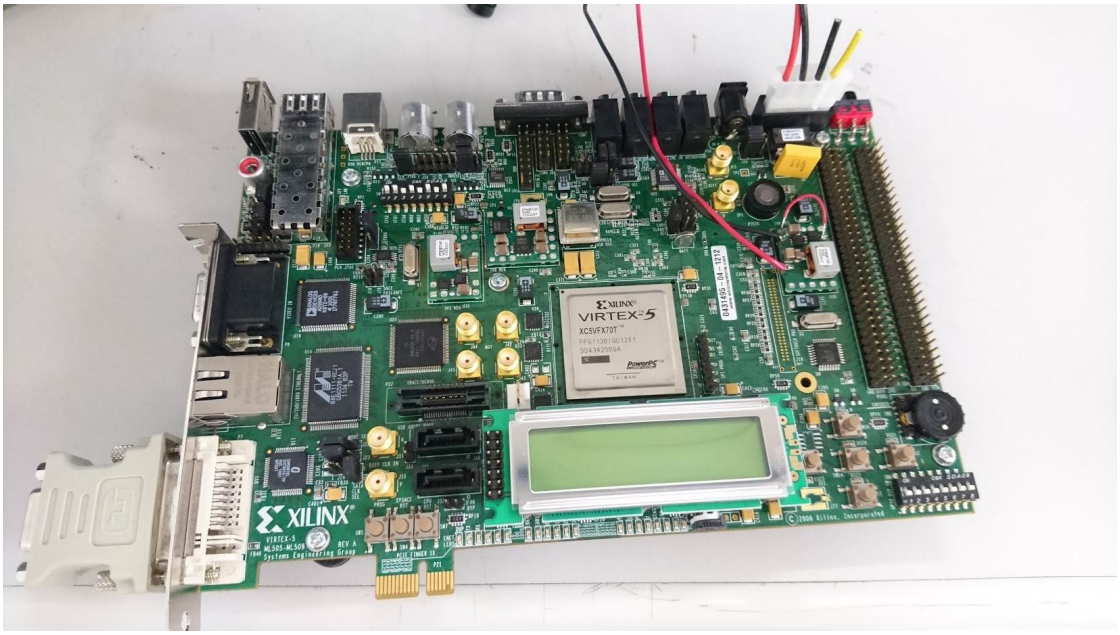

Figure 1. Evaluation board used for SEE testing of DDR2.

Test Performance

The test was performed by Ted Wilcox (GSFC-561), Michael Campola (GSFC-561), Madhu Kadari (J&T), and Seshagiri Nadendla (J&T).

Test Sequence:

Testing was done using a broadbeam ion beam whose diameter is larger than the device, so every part of the device was equally likely to be struck by an ion. Testing was done on five (5) devices, all biased at a nominal operating voltage of 1.8 V. Table 5, on the following 3 pages, lays out the test sequence; the full run log can be found in Section 7 – Run Log.

Table 5: Test Execution Sequence

Run #	Device	Thickness (µm)	LDC	RunType	Memory Space (bits)	Ion	MeV/amu	Eff, LET (MeV-cm^2/mg)	Angle (°)	Avg Flux (s^{-1}cm^{-2})	Fluence (cm^{-2})	Live Time (s)
1	1	133	1510	static	1073741824	Ne	21.5	1.9	0	1.00E+04	5.00E+05	51.4
2	1	133	1510	static	1073741824	Ne	21.5	1.9	0	1.00E+04	1.00E+06	130.5
3	1	133	1510	static	1073741824	Ne	18.7	4.3	60	1.00E+04	1.00E+06	192.1
4	1	133	1510	dynamic	33554432	Ne	18.7	4.3	60	1.00E+04	1.00E+06	216.9
5	1	133	1510	dynamic	33554432	Ne	18.7	4.3	60	1.00E+04	1.00E+06	-
6	1	133	1510	static	1073741824	Kr	14.5	25.8	0	1.00E+04	1.00E+06	92.3
7	1	133	1510	static	1073741824	Kr	14.5	25.8	0	1.00E+04	1.00E+06	71
8	1	133	1510	dynamic	33554432	Kr	14.5	25.8	0	1.00E+04	1.00E+06	72.6
9	1	133	1510	random	1073741824	Kr	14.5	25.8	0	1.00E+04	1.00E+06	71
10	8	138	1504	static	1073741824	Kr	14.5	25.8	0	1.60E+04	1.00E+06	67
11	8	138	1504	static	1073741824	Kr	14.5	25.8	0	1.60E+04	1.00E+06	54
12	8	138	1504	dynamic	33554432	Kr	14.5	25.8	0	1.60E+04	1.00E+06	62
13	8	138	1504	dynamic	33554432	Kr	14.5	25.8	0	1.60E+04	1.00E+06	54
14	8	138	1504	random	1073741824	Kr	14.5	25.8	0	1.00E+04	1.00E+06	95
15	8	138	1504	static	1073741824	Kr	14.5	31.4	30	1.00E+04	8.50E+05	102
16	8	138	1504	static	1073741824	Kr	14.5	31.4	30	1.00E+04	1.00E+06	102
17	8	138	1504	dynamic	33554432	Kr	14.5	31.4	30	1.00E+04	1.00E+06	82
18	8	138	1504	dynamic	33554432	Kr	14.5	31.4	30	1.40E+04	1.00E+06	80
19	8	138	1504	dynamic	33554432	Kr	14.5	31.4	30	1.40E+04	1.00E+06	82
20	8	138	1504	random	1073741824	Kr	14.5	31.4	30	1.50E+04	1.00E+06	82
21	9	87	1504	static	1073741824	Kr	16.7	27.8	30	1.00E+04	1.00E+06	113
22	9	87	1504	static	1073741824	Kr	16.7	23.4	0	0.00E+00	0.00E+00	0
23	9	87	1504	static	1073741824	Kr	16.7	23.4	0	1.00E+04	4.46E+04	0
24	9	87	1504	static	1073741824	Kr	16.7	23.4	0	1.00E+04	1.00E+06	81
25	9	87	1504	static	1073741824	Xe	15.5	46.7	0	5.00E+03	1.00E+05	18

Run #	Device	Thickness (µm)	LDC	RunType	Memory Space (bits)	Ion	MeV/amu	Eff, LET (MeV-cm^2/mg)	Angle (°)	Avg Flux ($s^{-1}cm^{-2}$)	Fluence (cm^{-2})	Live Time (s)
26	9	87	1504	static	1073741824	Xe	15.5	46.7	0	5.00E+03	1.00E+05	25
27	9	87	1504	dynamic	33554432	Xe	15.5	46.7	0	5.00E+03	1.00E+05	28
28	9	87	1504	dynamic	33554432	Xe	15.5	46.7	0	5.00E+03	5.00E+05	124
29	9	87	1504	random	1073741824	Xe	15.5	46.7	0	3.00E+04	1.00E+07	350
30	9	87	1504	static	1073741824	Xe	15.5	55.5	30	3.00E+04	1.00E+06	40
31	9	87	1504	static	1073741824	Xe	15.5	55.5	30	3.00E+04	5.00E+05	56
32	9	87	1504	dynamic	33554432	Xe	14.4	55.5	30	1.00E+04	5.00E+05	50
33	9	87	1504	dynamic	33554432	Xe	14.4	55.5	30	1.00E+04	5.00E+05	50
34	9	87	1504	random	1073741824	Xe	15.5	55.5	30	3.00E+04	1.00E+07	480
35	9	87	1504	random edit	1073741824	Xe	15.5	55.5	30	2.00E+04	7.00E+06	394
36	9	87	1504	random edit	1073741824	Xe	15.5	46.7	0	2.00E+04	1.12E+06	36
37	9	87	1504	random edit	1073741824	Xe	15.5	46.7	0	2.00E+04	2.81E+06	107
38	9	87	1504	random edit	1073741824	Xe	15.5	46.7	0	2.00E+04	1.24E+06	46
39	9	87	1504	random edit	1073741824	Xe	15.5	55.5	30	2.00E+04	4.41E+05	25
40	9	87	1504	random edit	1073741824	Ar	20.2	7.3	30	1.00E+04	5.00E+06	493
41	9	87	1504	random edit	1073741824	Ar	20.2	7.3	30	5.00E+04	5.00E+06	118
42	2	132	1510	static	1073741824	Ar	18.1	7.8	30	5.00E+04	1.00E+06	22
43	2	132	1510	static	1073741824	Ar	18.1	7.8	30	5.00E+04	5.00E+06	120
44	2	132	1510	dynamic	33554432	Ar	18.1	7.8	30	5.00E+04	5.00E+06	120
45	2	132	1510	dynamic	33554432	Ar	18.1	7.8	30	5.00E+04	5.00E+06	130
46	2	132	1510	random edit	1073741824	Ar	18.1	7.8	30	5.00E+04	5.00E+06	130
47	2	132	1510	random edit	1073741824	Ar	13.2	16.7	60	5.00E+04	6.14E+05	26
48	2	132	1510	random edit	1073741824	Ar	13.2	16.7	60	5.00E+04	5.00E+06	195
49	2	132	1510	static	1073741824	Ar	13.2	16.7	60	5.00E+04	5.00E+06	195
50	2	132	1510	static	1073741824	Ar	13.2	16.7	60	1.00E+04	1.00E+05	20
51	2	132	1510	static	1073741824	Ar	13.2	16.7	60	1.00E+04	5.00E+05	97

Run #	Device	Thickness (µm)	LDC	RunType	Memory Space (bits)	Ion	MeV/amu	Eff, LET (MeV-cm^2/mg)	Angle (°)	Avg Flux ($s^{-1}cm^{-2}$)	Fluence (cm^{-2})	Live Time (s)
52	2	132	1510	static	1073741824	Ar	18.9	6.6	0	1.00E+04	5.00E+05	53
53	2	132	1510	random edit	1073741824	Ar	18.9	6.6	0	1.00E+04	1.00E+06	130
54	2	132	1510	random edit	1073741824	Ar	18.9	6.6	0	1.00E+04	7.26E+04	7
55	2	132	1510	random edit	1073741824	Ar	18.9	6.6	0	1.00E+04	4.00E+06	347
56	2	132	1510	random edit	1073741824	Ar	13.2	16.7	0	1.00E+04	5.00E+06	825
57	3	99	1510	random edit	1073741824	Ar	16.3	14.6	60	1.30E+04	4.41E+06	703
58	3	99	1510	static	1073741824	Ar	16.3	14.6	60	1.30E+04	1.00E+06	184
59	3	99	1510	static	1073741824	Ar	20.2	6.3	0	1.30E+04	2.00E+06	132
60	3	99	1510	random edit	1073741824	Ar	20.2	6.3	0	1.30E+04	4.23E+06	278
61	3	99	1510	random edit	1073741824	Ar	20.2	6.3	0	1.30E+04	1.33E+06	91
62	3	99	1510	random edit	1073741824	Ar	20.2	6.3	0	1.30E+04	4.61E+06	307
63	3	99	1510	random edit	1073741824	Ne	22.2	1.9	0	3.00E+04	4.65E+06	137

6. Results

Three sets of cross-section conditions were obtained from testing: SEUs during static operation, SEUs during dynamic operation, and SEFI/Burst events. Figures 2 – 4 show the cross-section curves for the different categories, along with the associated Weibull curves; the Weibull parameters are provided in Table 6.

Table 6: Weibull Parameters

SEU Condition	LET_{th} (MeV·cm²/mg)	Width (MeV·cm²/mg)	Exponent	Limiting Cross-Section (cm²)
Static	2.0	80.00	3.500	5.00e-11
Dynamic	2.0	150.0	3.000	1.00E-09
SEFI/Burst	4.3	170.8	0.582	3.00E-06

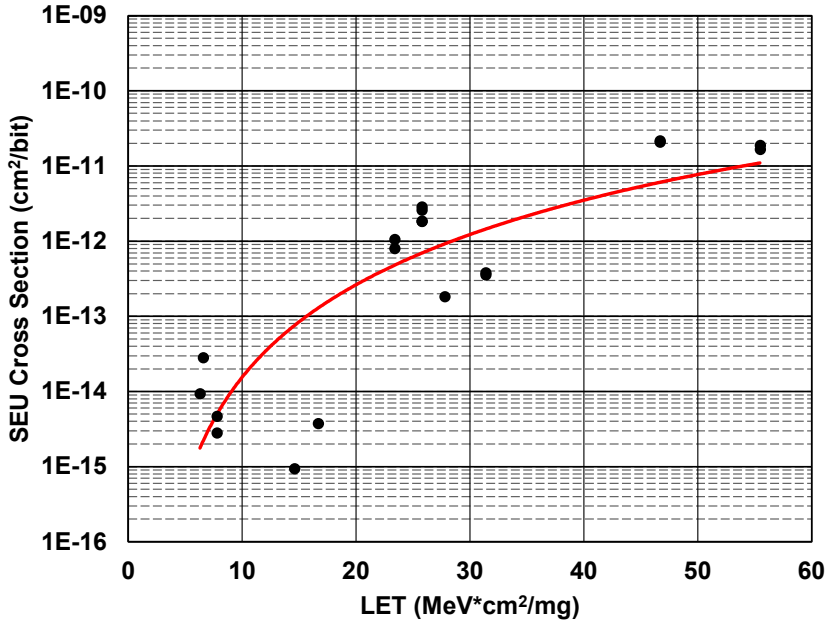

Figure 2. Cross-section vs LET for SEUs during static operation. Weibull fit shown in red.

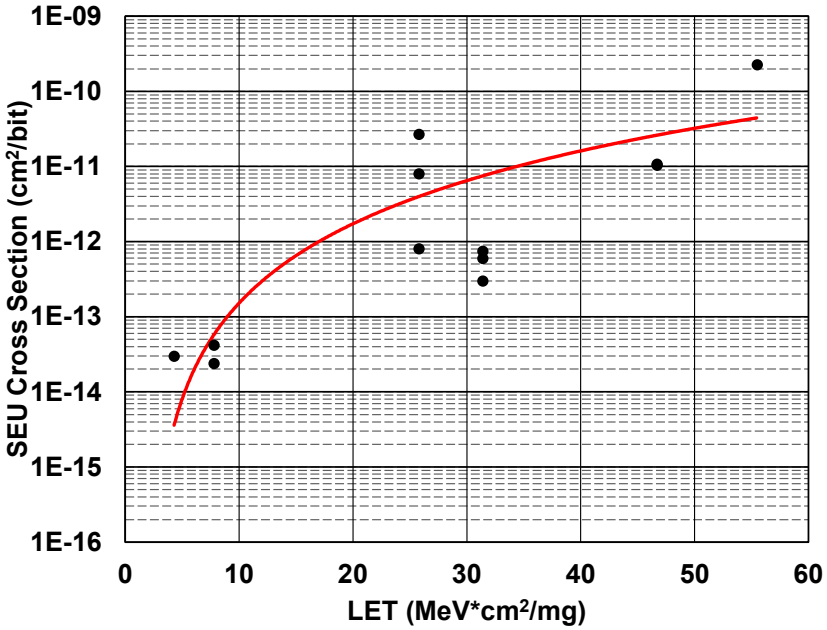

Figure 3. Cross-section vs LET for SEUs during dynamic operation. Weibull fit shown in red.

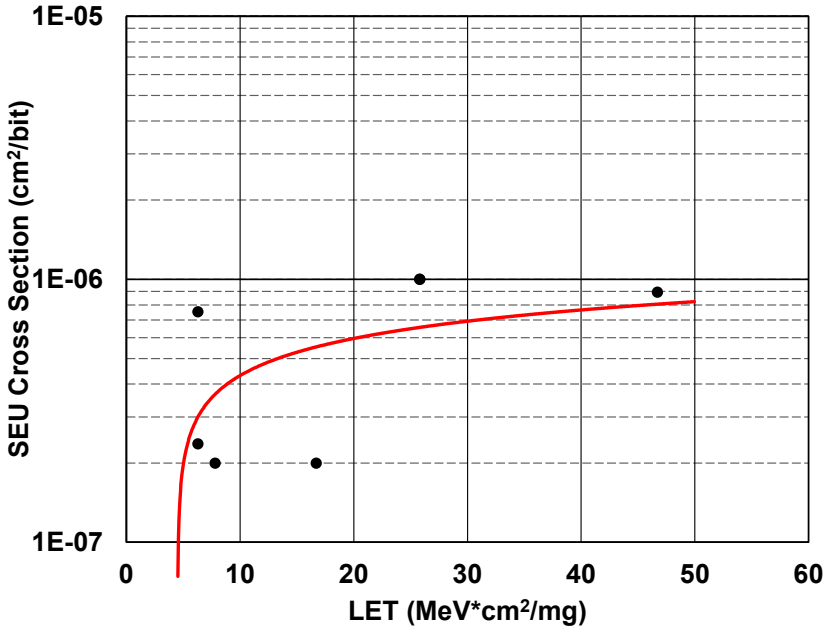

Figure 4. Cross-section vs LET for SEFIs and Burst events. Weibull fit shown in red. SEFI cross-section dominates the response.

7. Run Log

Run Info														Errors			Cross Sections				
RUN	Device	Thickness (um)	LDC	Runtype	Memory Space (bits)	Ion	MeV/amu	Eff LET	Angle	Avg Flux	Fluence	Live Time	pre-run errors	Error Count	Total SEFI	Row Errors/Burst	SEU CS	Dynamic SEU CS	SEFI CS	Burst CS	Notes
1	1	133	1510	static	1073741824	Ne	21.5	1.9	0	1.00E+04	5.00E+05	51.4	0	0			0.00E+00	0.00E+00	0.00E+00	0.00E+00	nada
2	1	133	1510	static	1073741824	Ne	21.5	1.9	0	1.00E+04	1.00E+06	130.5	0	0			0.00E+00	0.00E+00	0.00E+00	0.00E+00	nada
3	1	133	1510	static	1073741824	Ne	18.7	4.3	60	1.00E+04	1.00E+06	192.1	0	0			0.00E+00	0.00E+00	0.00E+00	0.00E+00	increased angle for LET higher than 2.3 based off of 3D plus testing
4	1	133	1510	dynamic	33554432	Ne	18.7	4.3	60	1.00E+04	1.00E+06	216.9	0	1	0	0	0.00E+00	2.98E-14	0.00E+00	0.00E+00	static test after to reveal if there was a stuck bit address, none. No permanently stuck bit.
5	1	133	1510	dynamic	33554432	Ne	18.7	4.3	60	1.00E+04	1.00E+06	-	0	0	0	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	
6	1	133	1510	static	1073741824	Kr	14.5	25.8	0	1.00E+04	1.00E+06	92.3	0	2749			2.56E-12	0.00E+00	0.00E+00	0.00E+00	Good error count from random addresses
7	1	133	1510	static	1073741824	Kr	14.5	25.8	0	1.00E+04	1.00E+06	71	0	3052			2.84E-12	0.00E+00	0.00E+00	0.00E+00	
8	1	133	1510	dynamic	33554432	Kr	14.5	25.8	0	1.00E+04	1.00E+06	72.6	0	897	0	1	0.00E+00	2.67E-11	0.00E+00	1.00E-06	844 of errors were in the burst
9	1	133	1510	random	1073741824	Kr	14.5	25.8	0	1.00E+04	1.00E+06	71	0		0		0.00E+00	0.00E+00	0.00E+00	0.00E+00	
10	8	138	1504	static	1073741824	Kr	14.5	25.8	0	1.60E+04	1.00E+06	67	0	1956			1.82E-12	0.00E+00	0.00E+00	0.00E+00	
11	8	138	1504	static	1073741824	Kr	14.5	25.8	0	1.60E+04	1.00E+06	54	0	1961			1.83E-12	0.00E+00	0.00E+00	0.00E+00	
12	8	138	1504	dynamic	33554432	Kr	14.5	25.8	0	1.60E+04	1.00E+06	62	0	27	0	0	0.00E+00	8.05E-13	0.00E+00	0.00E+00	
13	8	138	1504	dynamic	33554432	Kr	14.5	25.8	0	1.60E+04	1.00E+06	54	0	268	0	1	0.00E+00	7.99E-12	0.00E+00	1.00E-06	235 from one count, burst
14	8	138	1504	random	1073741824	Kr	14.5	25.8	0	1.00E+04	1.00E+06	95	0		0		0.00E+00	0.00E+00	0.00E+00	0.00E+00	
15	8	138	1504	static	1073741824	Kr	14.5	31.4	30	1.00E+04	8.50E+05	102	0	322			3.53E-13	0.00E+00	0.00E+00	0.00E+00	
16	8	138	1504	static	1073741824	Kr	14.5	31.4	30	1.00E+04	1.00E+06	102	0	405			3.77E-13	0.00E+00	0.00E+00	0.00E+00	
17	8	138	1504	dynamic	33554432	Kr	14.5	31.4	30	1.00E+04	1.00E+06	82	0	25	0	0	0.00E+00	7.45E-13	0.00E+00	0.00E+00	
18	8	138	1504	dynamic	33554432	Kr	14.5	31.4	30	1.40E+04	1.00E+06	80	0	10	0	0	0.00E+00	2.98E-13	0.00E+00	0.00E+00	
19	8	138	1504	dynamic	33554432	Kr	14.5	31.4	30	1.40E+04	1.00E+06	82	0	20	0	0	0.00E+00	5.96E-13	0.00E+00	0.00E+00	
20	8	138	1504	random	1073741824	Kr	14.5	31.4	30	1.50E+04	1.00E+06	82	0		0		0.00E+00	0.00E+00	0.00E+00	0.00E+00	
21	9	87	1504	static	1073741824	Kr	16.7	27.8	30	1.00E+04	1.00E+06	113	0	194			1.81E-13	0.00E+00	0.00E+00	0.00E+00	
22	9	87	1504	static	1073741824	Kr	16.7	23.4	0	0.00E+00	0.00E+00	0	0	0			#DIV/0!	0.00E+00	#DIV/0!	#DIV/0!	no beam
23	9	87	1504	static	1073741824	Kr	16.7	23.4	0	1.00E+04	4.46E+04	0	0	38			7.94E-13	0.00E+00	0.00E+00	0.00E+00	
24	9	87	1504	static	1073741824	Kr	16.7	23.4	0	1.00E+04	1.00E+06	81	0	1123			1.05E-12	0.00E+00	0.00E+00	0.00E+00	
25	9	87	1504	static	1073741824	Xe	15.5	46.7	0	5.00E+03	1.00E+05	18	1	2300			2.14E-11	0.00E+00	0.00E+00	0.00E+00	one error pre-run
26	9	87	1504	static	1073741824	Xe	15.5	46.7	0	5.00E+03	1.00E+05	25	1	2220			2.07E-11	0.00E+00	0.00E+00	0.00E+00	
27	9	87	1504	dynamic	33554432	Xe	15.5	46.7	0	5.00E+03	1.00E+05	28	0	36	0	0	0.00E+00	1.07E-11	0.00E+00	0.00E+00	
28	9	87	1504	dynamic	33554432	Xe	15.5	46.7	0	5.00E+03	5.00E+05	124	0	174	0	0	0.00E+00	1.04E-11	0.00E+00	0.00E+00	
29	9	87	1504	random	1073741824	Xe	15.5	46.7	0	3.00E+04	1.00E+07	350	0		0		0.00E+00	0.00E+00	0.00E+00	0.00E+00	
30	9	87	1504	static	1073741824	Xe	15.5	55.5	30	3.00E+04	1.00E+06	40	15	17726			1.65E-11	0.00E+00	0.00E+00	0.00E+00	
31	9	87	1504	static	1073741824	Xe	15.5	55.5	30	3.00E+04	5.00E+05	56	28	10090			1.87E-11	0.00E+00	0.00E+00	0.00E+00	
32	9	87	1504	dynamic	33554432	Xe	14.4	55.5	30	1.00E+04	5.00E+05	50			1	0	0.00E+00	0.00E+00	2.00E-06	0.00E+00	each cycle had 2097152, some kind of SEFI different than row, 29360291, rewrite did not fix, p
33	9	87	1504	dynamic	33554432	Xe	14.4	55.5	30	1.00E+04	5.00E+05	50	23	3782	0	0	0.00E+00	2.25E-10	0.00E+00	0.00E+00	
34	9	87	1504	random	1073741824	Xe	15.5	55.5	30	3.00E+04	1.00E+07	480			0	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	67108302, all zeroes, 19773474, all ones? SEFI maybe happened but random test isn't picking i
35	9	87	1504	random edit	1073741824	Xe	15.5	55.5	30	2.00E+04	7.00E+06	394			0	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	
36	9	87	1504	random edit	1073741824	Xe	15.5	46.7	0	2.00E+04	1.12E+06	36			0	1	0.00E+00	0.00E+00	0.00E+00	8.93E-07	edited random program printed too many errors
37	9	87	1504	random edit	1073741824	Xe	15.5	46.7	0	2.00E+04	2.81E+06	107			1	0	0.00E+00	0.00E+00	3.56E-07	0.00E+00	4718926 errors, cannot write to part
38	9	87	1504	random edit	1073741824	Xe	15.5	46.7	0	2.00E+04	1.24E+06	46	81		1	0	0.00E+00	0.00E+00	8.06E-07	0.00E+00	not stuck 0, stuck HI, some blocks have alternate patterns, power cycle clears
39	9	87	1504	random edit	1073741824	Xe	15.5	55.5	30	2.00E+04	4.41E+05	25	98		1	0	0.00E+00	0.00E+00	2.27E-06	0.00E+00	stuck low
40	9	87	1504	random edit	1073741824	Ar	20.2	7.3	30	1.00E+04	5.00E+06	493			0	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	
41	9	87	1504	random edit	1073741824	Ar	20.2	7.3	30	5.00E+04	5.00E+06	118			0	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	
42	2	132	1510	static	1073741824	Ar	18.1	7.8	30	5.00E+04	1.00E+06	22		5			4.66E-15	0.00E+00	0.00E+00	0.00E+00	
43	2	132	1510	static	1073741824	Ar	18.1	7.8	30	5.00E+04	5.00E+06	120		15			2.79E-15	0.00E+00	0.00E+00	0.00E+00	
44	2	132	1510	dynamic	33554432	Ar	18.1	7.8	30	5.00E+04	5.00E+06	120		7	0	0	0.00E+00	4.17E-14	0.00E+00	0.00E+00	
45	2	132	1510	dynamic	33554432	Ar	18.1	7.8	30	5.00E+04	5.00E+06	130		4	0	0	0.00E+00	2.38E-14	0.00E+00	0.00E+00	
46	2	132	1510	random edit	1073741824	Ar	18.1	7.8	30	5.00E+04	5.00E+06	130			0	1	0.00E+00	0.00E+00	0.00E+00	2.00E-07	burst was possibly something preventing a write, very small group of errors 120 or so do not p
47	2	132	1510	random edit	1073741824	Ar	13.2	16.7	60	5.00E+04	6.14E+05	26			1	0	0.00E+00	0.00E+00	1.63E-06	0.00E+00	everthing cleared with power cycle. But necessary
48	2	132	1510	random edit	1073741824	Ar	13.2	16.7	60	5.00E+04	5.00E+06	195			0	1	0.00E+00	0.00E+00	0.00E+00	2.00E-07	876, 864 came from burst, did not require power cycle.
49	2	132	1510	static	1073741824	Ar	13.2	16.7	60	5.00E+04	5.00E+06	195			1	0	0.00E+00	0.00E+00	2.00E-07	0.00E+00	error prevents SEU numbers, stuck low
50	2	132	1510	static	1073741824	Ar	13.2	16.7	60	1.00E+04	1.00E+05	20	2	2	0	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	
51	2	132	1510	static	1073741824	Ar	13.2	16.7	60	1.00E+04	5.00E+05	97	2	4	0	0	3.73E-15	0.00E+00	0.00E+00	0.00E+00	
52	2	132	1510	static	1073741824	Ar	18.9	6.6	0	1.00E+04	5.00E+05	53	1	16	0	0	2.79E-14	0.00E+00	0.00E+00	0.00E+00	
53	2	132	1510	random edit	1073741824	Ar	18.9	6.6	0	1.00E+04	1.00E+06	130		0	0	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	
54	2	132	1510	random edit	1073741824	Ar	18.9	6.6	0	1.00E+04	7.26E+04	7		0	0	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	bunk run
55	2	132	1510	random edit	1073741824	Ar	18.9	6.6	0	1.00E+04	4.00E+06	347		1	0	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	
56	2	132	1510	random edit	1073741824	Ar	13.2	16.7	0	1.00E+04	5.00E+06	825		18	0	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	
57	3	99	1510	random edit	1073741824	Ar	16.3	14.6	60	1.30E+04	4.41E+06	703		2	1	0	0.00E+00	0.00E+00	2.27E-07	0.00E+00	power cycle brings it back, able to read from, but not write the area
58	3	99	1510	static	1073741824	Ar	16.3	14.6	60	1.30E+04	1.00E+06	184		1	0	0	9.31E-16	0.00E+00	0.00E+00	0.00E+00	
59	3	99	1510	static	1073741824	Ar	20.2	6.3	0	1.30E+04	2.00E+06	132		20	0	0	9.31E-15	0.00E+00	0.00E+00	0.00E+00	
60	3	99	1510	random edit	1073741824	Ar	20.2	6.3	0	1.30E+04	4.23E+06	278		971	0	1	0.00E+00	0.00E+00	0.00E+00	2.36E-07	
61	3	99	1510	random edit	1073741824	Ar	20.2	6.3	0	1.30E+04	1.33E+06	91		746	0	1	0.00E+00	0.00E+00	0.00E+00	7.52E-07	
62	3	99	1510	random edit	1073741824	Ar	20.2	6.3	0	1.30E+04	4.61E+06	307			1	0	0.00E+00	0.00E+00	2.17E-07	0.00E+00	only writing AA pattern is a problem, power cycle to fix
63	3	99	1510	random edit	1073741824	Ne	22.2	1.9	0	3.00E+04	4.65E+06	137			0	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	
64	3	99	1510	random edit	1073741824	Ne	22.2	1.9	0	3.00E+04	5.00E+06	112			0	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	