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July 2022

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Review of Controllers for Low-Power Free-Piston Stirling Convertors

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Abstract

This work provides a complete review of controller strategies for free-piston Stirling convertors (FPSCs) and design recommendations for future controller development efforts. First, basic operating principles for the control of FPSCs and design variables for the FPSC controllers are described. Next, past controller approaches are reviewed and categorized based on the design variables. State-of-the-art controllers are also summarized by their key features, which are then hypothetically extended to flight designs to compare their critical metrics such as the estimated size, weight, and power with cost (SWaP-C) and reliability. Finally, design recommendations are suggested to improve the state-of-the-art controllers for future flight development projects. Along with the maturation of FPSC technologies for radioisotope power systems over the last three decades, various controllers for FPSCs have been proposed, among which a couple of those controllers were developed to the Engineering Model (EM) for a flight development project. Further improvements of the controllers have been made recently at the NASA Glenn Research Center (GRC) and the improvements will continue for future flight development projects.

Nomenclature

A_d	displacer area [m^2]
A_p	piston area [m^2]
A_r	displacer rod area [m^2]
C_t	capacitance of the tuning capacitor [Farads]
C_p	piston damping [N/(m/s)]
I_{alt}	alternator current [Amps]
K_d	displacer spring constant [N/m]
K_e	back emf constant [Volts/(m/s)]
K_i	magnetic force constant [N/Amp]
K_p	piston spring constant [N/m]
L_{alt}	inductance of the alternator in a Stirling convertor [Henries]
M_d	displacer mass [kg]
M_p	piston mass [kg]
P_d	displacer pressure factor [Pa/m]
P_p	piston pressure factor [Pa/m]
ΔP_d	delta displacer pressure factor [Pa/(m/s)]
ΔP_p	delta piston pressure factor [Pa/(m/s)]
R_{alt}	parasitic resistance of the alternator in a Stirling convertor [Ω]
R_L	load resistance [Ω]
V_c	rms of a controller output voltage [V]

X_d displacer displacement [m]

$\dot{X}_d$ displacer velocity [m/s]

X_p piston displacement [m]

$\dot{X}_p$ piston velocity [m/s]

Introduction

Since the first Systems for Nuclear Auxiliary Power (SNAP)-3B generators launched in 1961, radioisotope thermoelectric generators (RTGs) have been used as power sources for NASA's various missions including Apollo, Viking, Voyager, Cassini, New Horizons, and Mars 2020 (Refs. 1 to 4). Starting from the first 2.7 W RTG, designs of the thermoelectric devices have improved significantly to the current multi-mission radioisotope thermoelectric generators (MMRTGs) where each MMRTG produced 110 W (Ref. 5). While both the RTGs and MMRTGs have successfully demonstrated long-term reliable operation throughout all the aforementioned missions, they have low thermal-to-electrical conversion efficiency, which is approximately 6 percent. To improve these, there have been many studies including enhanced MMRTG (eMMRTG), Next Generation RTG (NGRTG) (Refs. 6 to 8), and Dynamic Radioisotope Power System (DRPS). The DRPS, which is the focus of this paper, uses external combustion engines, such as free-piston Stirling convertors (FPSCs), to convert thermal energy to electrical energy, and this has been extensively studied for the last three decades. Efficiency greater than 20 percent and long lifetime estimated through long-term laboratory demonstrations over the last 14 years have been demonstrated for the FPSCs (Refs. 9 to 11). Given the limited supply of Pu-238 in the United States (~1.5 kg/yr) and high power requirements for near-future flight missions (several hundreds of Watts to Kilowatts), the FPSC technology would make a well-suited power system for future deep-space missions (Refs. 12 to 14).

Because the FPSC involves moving parts for the conversion—a displacer and a piston—and the piston stroke in the FPSC is inherently unstable, a controller is required to stabilize and constrain the piston stroke so that physical collision between the piston and the convertor itself can be avoided. While many books and papers have discussed technical details and operating principles of FPSCs, only a few papers have discussed the theory of operation for FPSC controllers to the best of the author's knowledge and even those papers are very sparse. Therefore, in this paper, basic operating principles of the controllers and design variables that determine important metrics of the controllers such as size, weight, and power with cost (SWaP-C) and reliability, will be discussed, followed by a review of various FPSC controllers that have been developed to date. Finally, qualitative comparison analysis among the state-of-the-art controllers will be conducted and potential design recommendations will be presented.

Operating Principles and Design Variables

A simplified block diagram of the FPSC controller is shown in Figure 1. In general, the power factor (PF) of the FPSC, which will be discussed later in the section, is quite low and this needs to be improved by using a power factor correction (PFC) circuit. After that, the corrected power is rectified and converted to intermediate DC voltage, which is then converted to the 28 VDC spacecraft voltage. Simultaneously, the piston stroke of the FPSC needs to be controlled for long-term stable operation. In order to implement these four main features of the FPSC controller, the following main design variables have been historically considered: active/passive PFC and rectification, self/forced-oscillation, analog/digital implementation, resistive-dissipating/power-converting, and direct piston motion sensor/indirect piston motion indicator. In this section, the operating principles of the FPSC controller and details about each design variable will be discussed.

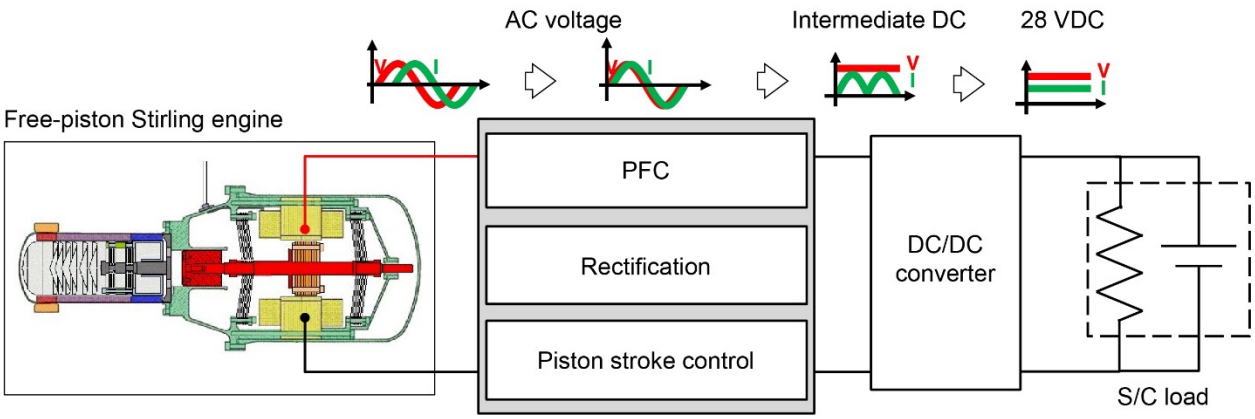


Figure 1.—A simplified block diagram of the FPSC controller.

Passive/Active Power Factor Correction and Rectification

In the FPSC-based Radioisotope Power System (RPS), AC power generated from the FPSC is converted to DC and delivered to the 28 VDC spacecraft load, and the amount of power delivered to the spacecraft is largely determined by the phase difference between the back-EMF and alternator current waveforms from the FPSC and shapes of those waveforms. This is normally quantified using the power factor (PF). The PF quantifies how much of power generated by a power plant (i.e., the FPSC) is delivered to the load to perform actual work, and is defined as a ratio of the power dissipated by a load, which is an average of the product of the back-EMF and alternator current (i.e., real power), to the product of root mean square (RMS) of the back-EMF and the RMS of the alternator current (i.e., apparent power), as (Ref. 15):

$$\mathrm{PF} = \frac{P}{S} = \frac{\langle V_{emf} \cdot I_{alt} \rangle}{V_{emf,rms} \cdot I_{alt,rms}} \tag{1}$$

where P is real power in Watts (W), S is apparent power in volt-amperes (VA), $\langle\ \rangle$ is the average, V_{emf} is the back-EMF, I_{alt} is the alternator current, and $V_{emf,\,rms}$ and $I_{alt,\,rms}$ are the RMS values of the back-EMF and the alternator current, respectively. Qualitatively, a higher PF indicates that more power generated by the FPSC is delivered to the load. Therefore, a higher PF is desirable for higher efficiency and this can be accomplished through the power factor correction (PFC). Depending on the load type—linear or non-linear—different mechanisms will affect the PF and thus, it is important to understand those mechanisms.

A linear load is a type of load that maintains the sinusoidal shapes of voltage and current waveforms, and only the phase difference between those waveforms can be changed by the load. Typical examples of a linear load include passive components, such as a resistor, capacitor, and inductor. When a linear load is connected to the FPSC, the PF is merely determined by the phase difference between the back-EMF and the alternator current. It should be noted that as shown in Figure 2(a), due to the nature of the alternator, the "actual" load seen from the back-EMF of the Stirling convertor is the sum of alternator resistance, alternator inductance, and the linear load. If the "actual" load connected to the back-EMF is purely resistive, then the back-EMF and the alternator current will be in phase and the product of those two AC signals will always result in positive power. Therefore, the real power will be equal to the apparent power, and thus the PF will be equal to 1 (Figure 2(b)). On the other hand, if the "actual" load is purely inductive (i.e., the back-EMF leads the alternator current by 90°), the exact amount of power dissipated by the load will be returned to the FPSC throughout a full cycle, resulting in a net-zero power dissipation at the load

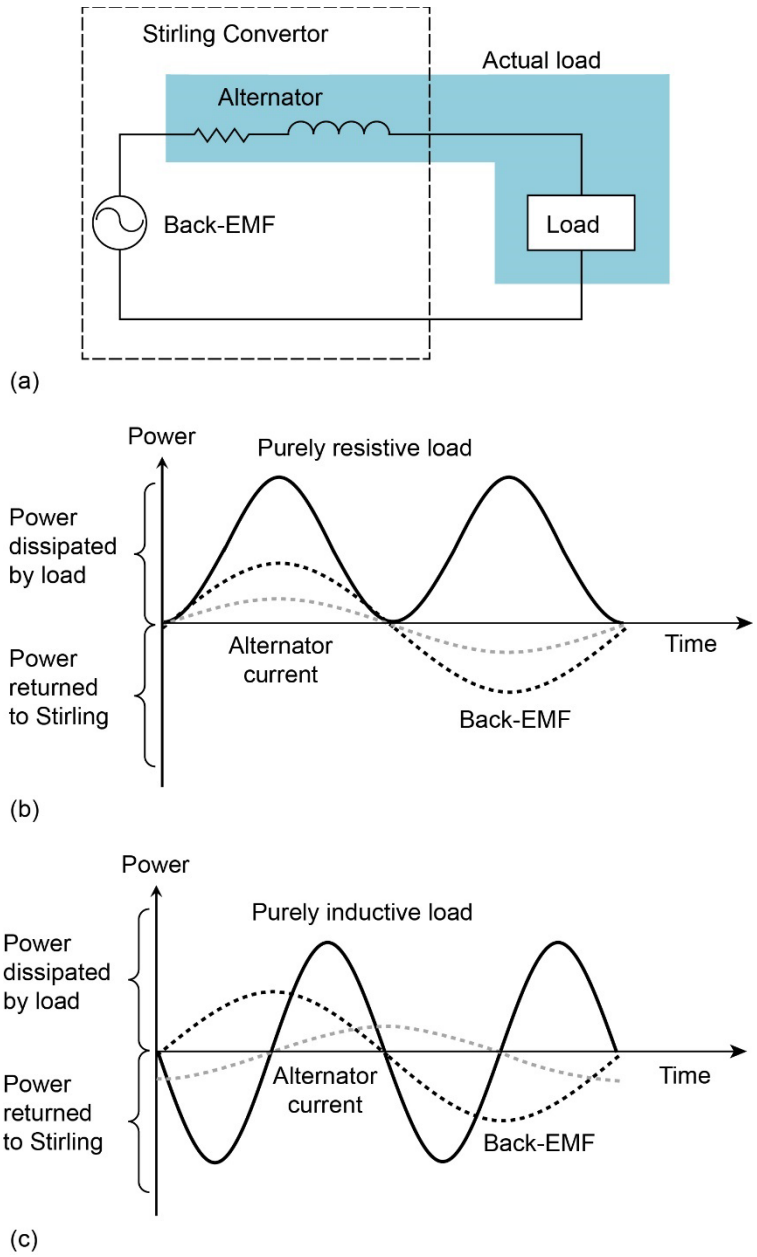


Figure 2.—PF illustration for a linear load: (a) Simplified schematic, (b) the power waveform when the actual load is purely resistive, and (c) the power waveform when the actual load is purely inductive.

(Figure 2(c)), and therefore the PF is 0 (Ref. 15). This type of power is called the reactive power and in this case, the reactive power is equal to the apparent power. Likewise, if the "actual" load is purely capacitive, the PF will be also zero. When the load is a combination of those three elements, R, L, and C, then some portion of the power will be dissipated at the load while the rest will be returned to the FPSC, resulting in the PF between 0 and 1. Therefore, the PF for a linear load can be simply calculated as:

$$\mathrm{PF}_{disp} = \cos(\theta_{PF}) \tag{2}$$

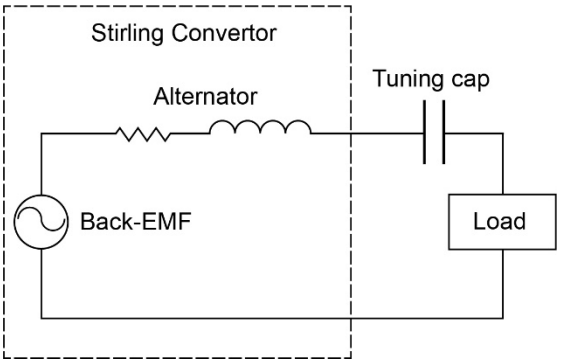


Figure 3.—A passive PFC using a series tuning capacitor.

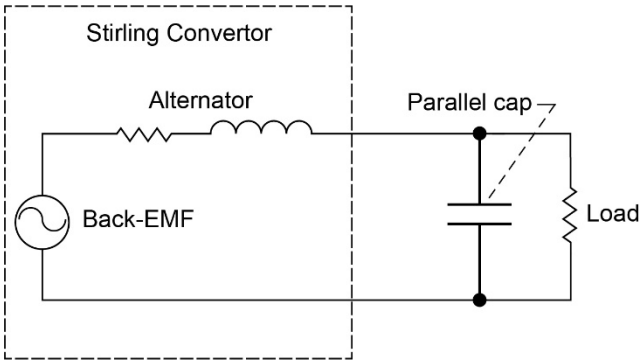


Figure 4.—A parallel PFC capacitor for the FPSC.

and this is known as the displacement PF (Ref. 15). In order to correct the displacement PF, the most widely used approach for the FPSC is the passive PFC where a capacitor is simply placed in series with the alternator as shown in Figure 3. This capacitor is called a tuning capacitor because it "tunes" into the resonant frequency of the FPSC by canceling the reactance of the alternator inductor. The series tuning capacitance can be calculated as:

$$C_t = \frac{1}{\omega^2 \cdot L_{alt}} \tag{3}$$

where ω is the angular frequency of the piston in the FPSC and L_{alt} is the alternator inductance. It should be noted that because the alternator inductor is not separable from the back-EMF by the nature of the linear alternator, a parallel capacitor, which is a common industry practice, cannot be used in this application. In other words, if the PFC capacitor is connected in parallel as shown in Figure 4 where a resistive load is assumed for simplicity, the output impedance looking from the alternator will be

$$Z = \frac{R}{1+(\omega RC)^2} - j\frac{\omega R^2 C}{1+(\omega RC)^2} \tag{4}$$

where ω is the angular frequency of the FPSC, R is the load resistance, and C is the capacitance of the parallel capacitor. As shown in Equation (4), the reactance of the impedance will be highly dependent on the load resistance, which is not desirable. Furthermore, if the load resistance approaches zero, the reactance term will also approach zero, and thus the parallel capacitor cannot correct the PF.

On the other hand, a non-linear load is a type of load through which sinusoidal voltage and current waveforms are altered to non-sinusoidal waveforms, and a typical example is a passive full-bridge diode rectifier as shown in Figure 5(a). As it rectifies the AC voltage generated from the FPSC and converts it to DC voltage, it can distort the sinusoidal alternator current waveform (Refs. 16 to 18). This distortion is called the total harmonic distortion (THD), and it is defined as the ratio of the RMS value of the harmonics in the alternator current except for the RMS at the operating frequency of the FPSC to the RMS value of the alternator current at the operating frequency, as (Ref. 19):

$$\mathrm{THD} = \frac{\sqrt{I_{alt2}^2 + I_{alt3}^2 + I_{alt4}^2 + \cdots}}{I_{alt1}} \tag{5}$$

where I_{alt1} is the magnitude of the alternator current at the operating frequency in Amps (A), and I_{alt2}, I_{alt3}, and I_{alt4}, are magnitudes of the alternator current at the second, third, and fourth harmonics in Amps (A). Furthermore, the PF due to the THD can be calculated as (Ref. 16),

$$\mathrm{PF}_{dist} = \frac{1}{\sqrt{1+\mathrm{THD}^2}} \tag{6}$$

and this is called the distortion PF. As a common practice in the industry, an inductor can be inserted in the power path or active switches can be used to improve the distortion PF (Ref. 20). Fortunately, depending on the alternator inductance, the alternator inductor can suppress the distortion greatly without additional circuits, as shown in Figure 5. When the alternator inductance is relatively low (i.e., 0.3 mH),

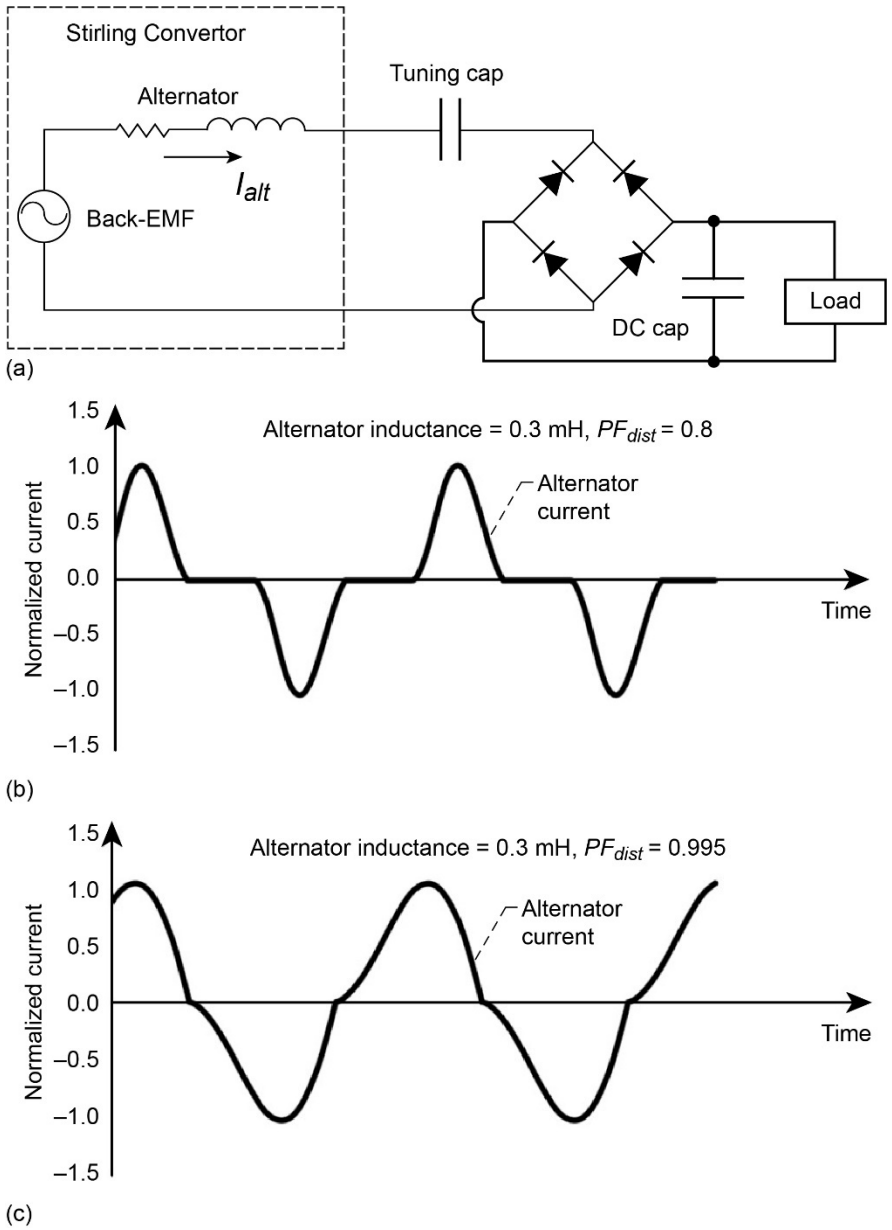


Figure 5.—PF illustration with a non-linear load: (a) a simplified schematic. Alternator current waveform when the alternator inductance is (b) 0.3 mH and (c) 3 mH. Note that the current amplitude was normalized to –1 to 1 A.

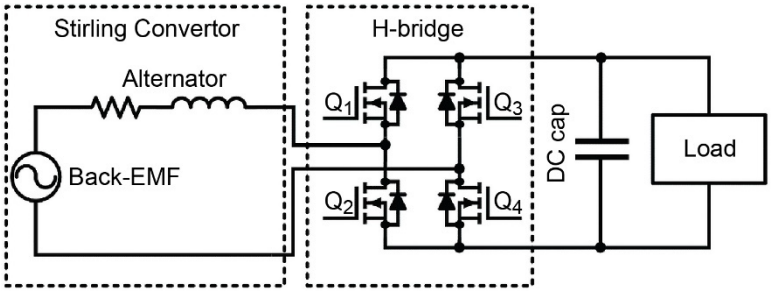


Figure 6.—An active PFC for the FPSC.

then the distortion is quite severe and the distortion PF is approximately 0.8. On the other hand, when the inductance is increased by a factor of ten (i.e., 3.0 mH), the distortion is significantly suppressed and the distortion PF is very close to 1. In most low-power FPSCs that have been developed to date, the alternator inductance normally ranges from a few mH (Advanced Stirling Convertors—ASCs) to hundreds of mH (Technology Demonstration Convertors—TDCs). Therefore, correcting the distortion PF is often ignored and the displacement PF alone is normally corrected in the controllers.

On the other hand, depending on the alternator inductance, the required tuning capacitance could range from tens of μF to a few mF. Given that the voltage and power levels of the system are relatively high, the size and weight of the tuning capacitor are usually very large and heavy. As an example, among the currently available flight-qualified AC capacitors according to EEE-INST-002, one of the best AC capacitors is MIL-PRF-83421/2 due to its relatively high energy density (Refs. 21 and 22). If the alternator inductance is 3 mH and the operating frequency is 100 Hz, then according to Equation (4), the required tuning capacitance would be 844 μF. Assuming that 60 Vrms capacitors are good enough, the maximum unit capacitance would be 25 μF, which means that at least 34 capacitors will be needed to build a tuning capacitor bank. Given that the diameter, length, and mass of the capacitor are 1 in., 2.44 in., 19 g (estimated), respectively, the size and weight of the 34 capacitors alone will be approximately 67 in^3 and 0.64 kg, respectively. If they are laid out on a PCB, the size will become 2 to 3 times larger than the size of the capacitors. If redundancy is required or multiple convertors need to be controlled, then the size and weight will proportionally increase. It should be noted that while FPSCs with higher alternator inductance will need much lower tuning capacitance, the overall size of the tuning capacitor would still be large because energy density over voltage stays roughly constant for typical flight capacitors. In order to address the size and weight concerns, some studies have been conducted to increase the energy density of capacitors to reduce the overall size and weight of the tuning capacitor (Ref. 23). As an alternative approach, active PFC controllers have been widely studied and developed to reduce the size and weight of the PFC circuit (Refs. 24 to 29). One of the most popular active PFC controllers is the H-bridge circuit shown in Figure 6 (Ref. 25). This circuit can actively control the alternator current waveform or the alternator voltage waveform to correct the PF, and detailed operating principles will be discussed later.

Finally, voltage rectifiers can be implemented passively or actively. A passive rectifier would be normally implemented using a full-bridge diode rectifier, and an active rectifier using active semiconductor switches such as MOSFETs. Historically, most FPSC controllers have been using a passive rectifier with a passive PFC circuit or an active rectifier with an active PFC circuit. On the other hand, other variations are possible to improve certain aspects of the FPSC controllers and two examples are shown in Figure 7 and Figure 8. A kilowatt-level Stirling convertor controller is shown in Figure 7 and it corrects the PF using a passive PFC capacitor to simplify the design while it rectifies the AC voltage using an active full-bridge totem pole rectifier to reduce the power loss (Ref. 23). Also, a typical example of an active PFC circuit with a passive rectifier is shown in Figure 8 where a passive diode

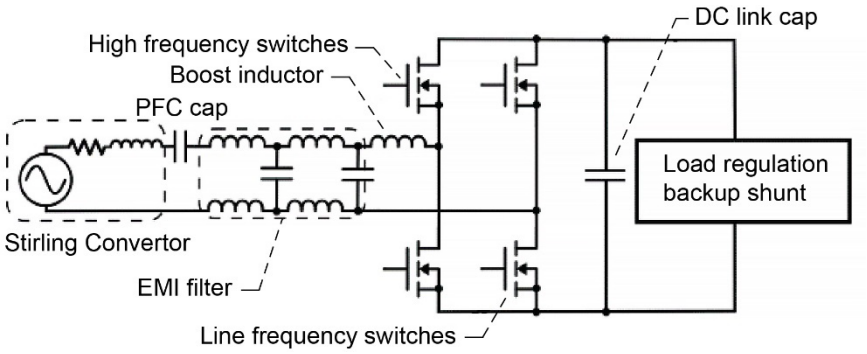


Figure 7.—A passive PFC with an active rectifier for a kilowatt-level FPSC controller (Ref. 23).

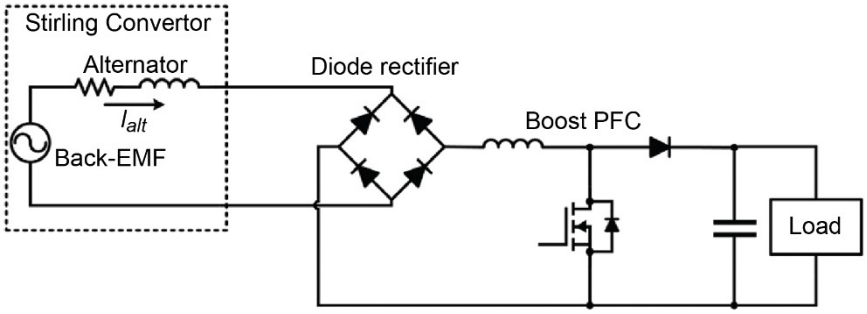


Figure 8.—A typical active PFC with a passive rectifier.

rectifier and an active boost PFC circuit are used, and this may reduce the overall control complexity of an active PFC circuit with an active rectifier. In this paper, however, those two historical topologies in low-power FPSC controllers, a passive rectifier with a passive PFC and an active rectifier with an active PFC, will be considered for simplicity, and they will be referred to as the active PFC and the passive PFC, respectively.

Self-Oscillation and Forced-Oscillation

The FPSC can be linearized and modeled as impedance with negative resistance, and thus the entire system with the controller can be considered as an oscillator system (Ref. 30). The negative resistance indicates that the FPSC generates power rather than dissipates power, and the negative resistance concept has been quite extensively used in oscillator systems (Ref. 31). Because the FPSC is inherently unstable, once the piston starts oscillating, the piston amplitude will grow until it strikes the convertor case if a controller does not restrict the piston stroke. Since the FPSC is inherently a non-linear system, just like general oscillators, many studies have been conducted to linearize the FPSC at its operating conditions to enable the use of many useful classical stability analysis tools, such as pole/zero analysis, root locus, bode plot, and Nyquist stability criterion (Refs. 30 to 35). State-space representation of the linearized FPSC can be expressed as (Ref. 30).

$$\begin{aligned} \dot{x}(t) &= Ax(t) + BI_{alt}(t) \\ V_b(t) &= C^T x(t) \end{aligned} \tag{7}$$

or

$$\begin{bmatrix} \dot{X}_d \\ \ddot{X}_d \\ \dot{X}_p \\ \ddot{X}_p \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ -\dfrac{K_d + A_r P_d}{M_d} & \dfrac{A_d \Delta P_d}{M_d} & -\dfrac{A_r + P_p}{M_d} & \dfrac{A_d \Delta P_p}{M_d} \\ 0 & 0 & 0 & 1 \\ -\dfrac{A_p P_d}{M_p} & 0 & -\dfrac{K_p + A_p P_p}{M_p} & -\dfrac{C_p}{M_p} \end{bmatrix} \begin{bmatrix} X_d \\ \dot{X}_d \\ X_p \\ \dot{X}_p \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ K_i / M_p \end{bmatrix} I_{alt} \tag{8}$$

$$V_b = \begin{bmatrix} 0 & 0 & 0 & K_e \end{bmatrix} \begin{bmatrix} X_d & \dot{X}_d & X_p & \dot{X}_p \end{bmatrix}^T$$

As can be seen from Equations (7) and (8), the input is the alternator current and the output is the back-EMF, which is the definition of impedance (Ref. 30). Furthermore, in order to understand the stability of the FPSC from Equation (8), locations of poles need to be identified by calculating eigenvalues of the A-matrix. In most FPSCs, poles are located in the right-half plane of the S-plane at operating conditions, because they are inherently unstable. Essentially, the goal here is to stabilize the piston stroke and sustain the oscillation. In doing so, two fundamentally different approaches exist and they are self-oscillation and forced-oscillation approaches depending on how the piston operating frequency is determined.

Self-Oscillation

A basic self-oscillation controller is shown in Figure 9 where the alternator is connected to a tuning capacitor and a resistor load, and state-space representation of the controller and a linearized FPSC model can be expressed as (Ref. 30):

$$\begin{bmatrix} \dot{X}_d \\ \ddot{X}_d \\ \dot{X}_p \\ \ddot{X}_p \\ \dot{I}_a \\ \dot{V}_c \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 \\ -\dfrac{K_d + A_r P_d}{M_d} & \dfrac{A_d \Delta P_d}{M_d} & -\dfrac{A_r P_p}{M_d} & \dfrac{A_d \Delta P_p}{M_d} & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ -\dfrac{A_p P_d}{M_p} & 0 & -\dfrac{K_p + A_p P_p}{M_p} & -\dfrac{C_p}{M_p} & \dfrac{K_i}{M_p} & 0 \\ 0 & 0 & 0 & -\dfrac{K_e}{L_{alt}} & -\dfrac{(R_{alt} + R_L)}{L_{alt}} & -\dfrac{1}{L_{alt}} \\ 0 & 0 & 0 & 0 & \dfrac{1}{C_t} & 0 \end{bmatrix} \begin{bmatrix} X_d \\ \dot{X}_d \\ X_p \\ \dot{X}_p \\ I_{alt} \\ V_c \end{bmatrix} \tag{9}$$

$$V_b = \begin{bmatrix} 0 & 0 & 0 & K_e & R_L & 0 \end{bmatrix} \begin{bmatrix} X_d & \dot{X}_d & X_p & \dot{X}_p & I_{alt} & V_c \end{bmatrix}^T$$

This system is very similar to a self-sustaining oscillator, where poles are located at RHP at the startup and the poles move to the $j\omega$-axis to sustain the oscillation by reducing the trans-conductance of the oscillator system (Ref. 31). In other words, under conditions where the net heat input and the hot-end temperature of the FPSC are variable, the piston amplitude grows during the startup and the increased piston amplitude will, in turn, change the hot-end temperature, pressure factors (P_p, P_d) and pressure drops (ΔP_p, ΔP_d) in Equation (9). As a result, poles of the system, which are initially located at RHP, will

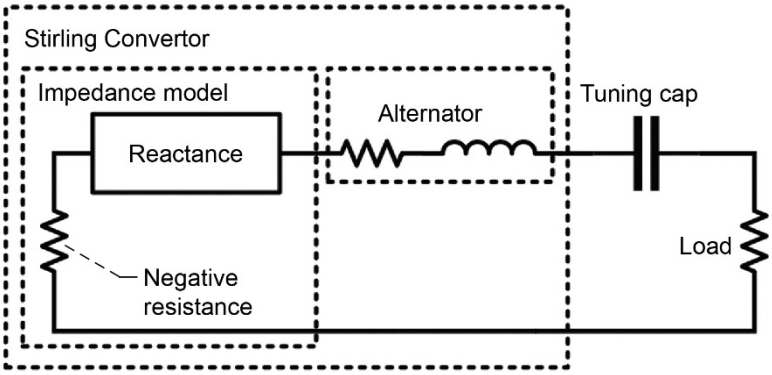


Figure 9.—An oscillation system with a FPSC impedance model. Note that the resistance of the FPSC is negative to produce power.

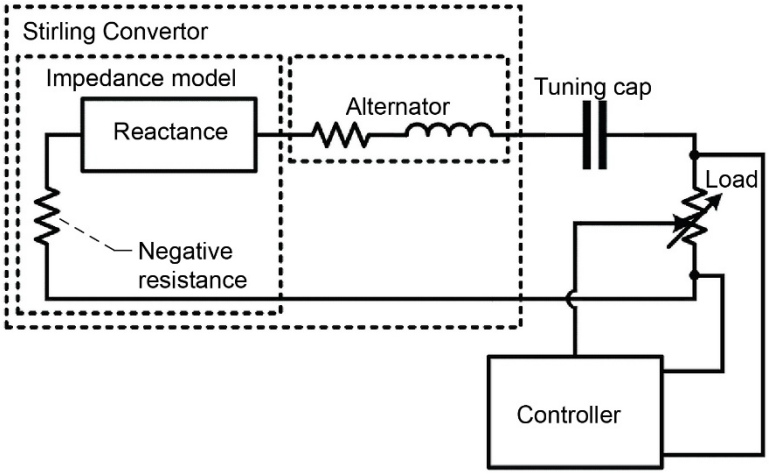


Figure 10.—Voltage across the AC load is controlled to sustain oscillation.

move to the imaginary axis to sustain the oscillation (Ref. 30). This results in a sustained oscillation and the piston amplitude will be determined by various factors. On the other hand, if the hot-end temperature is controlled to a constant value, which is the most likely case in flight missions, then the same self-sustaining mechanism will not work because no inherent parameters in Equation (9) will be changed to sustain the oscillation. Therefore, a very accurate load resistance needs to be selected to dissipate the exact power generated from the FPSC, or the oscillation amplitude will either decay or grow indefinitely.

Assuming that a proper value of the tuning capacitor is selected and thus the PFC is operated at its natural frequency, the reactance components in the circuit system in Figure 9 will become zero. As a result, only the resistance components will remain at the operating frequency. In order to sustain the oscillation, therefore, the load resistance should meet the following criterion so that all generated power from the FPSC can be dissipated in the alternator resistor and the load (Ref. 31):

$$R_L + R_{FPSC} + R_{alt} = 0 \tag{10}$$

where R_L is the load resistance, R_{FPSC} is the negative resistance of the FPSC impedance model, and R_{alt} is the alternator resistance. In practical situations where the hot-end temperature is controlled to a constant value, the FPSC impedance would be nearly constant that a very precise value for the load resistance will have to be selected to sustain oscillation, which is not quite practical. Alternatively, controlling the voltage across the load resistor can meet Equation (10) as shown in Figure 10. Assuming the alternator resistance is much smaller than the magnitude of the resistance of the FPSC (i.e., $|R_{alt}| \ll |R_{FPSC}|$), the

controlled voltage across the load resistor will force the voltage across the negative resistance of the FPSC to the same voltage, because reactance will be canceled at the natural frequency. Furthermore, because those two resistors are connected in series, the current flowing through them will be the same. As a result, the magnitude of the load resistance will be made the same as the FPSC resistance with opposite signs (i.e., one generating power and the other dissipating the exact amount of power). Therefore, poles will be located on the $j\omega$-axis and the oscillation will be sustained.

Forced-Oscillation

Also, simply connecting a sinusoidal signal (i.e., AC bus) after the tuning capacitor will control the FPSC as shown in Figure 11, assuming that the AC bus dissipates all power generated from the FPSC. As in the self-oscillation circuit, the voltage across the negative resistance in the FPSC will be made almost identical to the AC bus voltage. On the other hand, poles of the system will have to be located in LHP to suppress self-oscillation of the FPSC so that the AC bus can control the piston amplitude and frequency, and this is referred to as "forced-oscillation". The state-space representation of this system can be expressed as (Ref. 30):

$$\begin{bmatrix} \dot{X}_d \\ \ddot{X}_d \\ \dot{X}_p \\ \ddot{X}_p \\ \dot{I}_a \\ \dot{V}_c \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 \\ -\dfrac{K_d + A_r P_d}{M_d} & \dfrac{Ad\Delta P_d}{M_d} & -\dfrac{A_r P_p}{M_d} & \dfrac{A_d \Delta P_p}{M_d} & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ -\dfrac{A_p P_d}{M_p} & 0 & -\dfrac{K_p + A_p P_p}{M_p} & -\dfrac{C_p}{M_p} & \dfrac{K_i}{M_p} & 0 \\ 0 & 0 & 0 & -\dfrac{K_e}{L_a} & -\dfrac{R_a}{L_a} & -\dfrac{1}{L_a} \\ 0 & 0 & 0 & 0 & \dfrac{1}{C_t} & 0 \end{bmatrix} \begin{bmatrix} X_d \\ \dot{X}_d \\ X_p \\ \dot{X}_p \\ I_a \\ V_c \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ -1/L_a \\ 0 \end{bmatrix} V_{ac} \tag{11}$$

$$I_a = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} X_d & \dot{X}_d & X_p & \dot{X}_p & I_a & V_c \end{bmatrix}^T$$

In this system, the input signal is the AC bus, and eigenvalues of the 6×6 A-matrix will have to be located in LHP for stable operation. Furthermore, the frequency of the AC bus will have to be carefully selected so that it is as close to the natural frequency of the FPSC as possible for a high PF (Ref. 30).

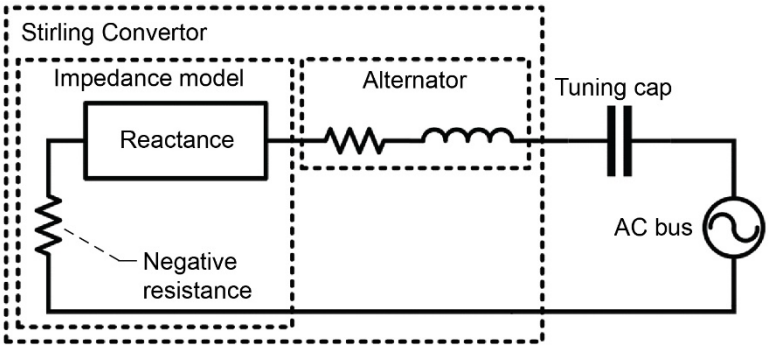


Figure 11.—A fixed-frequency controller using an AC bus.

While the forced-oscillation approach has higher controllability because both frequency and amplitude of the piston are actively controlled, the forced-oscillation approach tends to have a stability concern during a switchover where a backup controller in a redundant architecture takes over the control from the primary controller upon failure events, because a finite switching time from the primary to the backup controller causes a phase difference between the AC bus of the backup controller and the velocity of the piston, leading to unstable transition (Ref. 30). As a result, a complex algorithm needs to be designed to make the system stable. On the other hand, the self-oscillation approach would not have the same issue, and thus it will be inherently more reliable.

Analog and Digital Implementations

Implementing the FPSC controller in analog or digital is also an important factor for the controller design. In this paper, the analog implementation indicates that the controller is implemented using multiple discrete components such as integrated circuit (IC) chips and passive components, while in the digital implementation, a single digital processing unit such as a field-programmable gate array (FPGA), a microprocessor, or a single board computer (SBC) is used to implement the controller. The main power-path (i.e., orange blocks in Figure 12) generally require discrete components, such as power MOSFETs and diodes, for both analog and digital implementations. On the other hand, the sub-controller blocks (i.e., green blocks in Figure 12) can be implemented either using analog discrete components or a digital FPGA or processor, while both implementation approaches will compute the same control algorithms.

Assuming that all parts are space-qualified, the analog approach is likely to have a larger size and heavier weight because the analog approach requires more component counts than the digital approach does, and the size and weight of an FPGA, microprocessor, or SBC are quite small and light. On the other hand, the cost of the digital approach is likely to be higher than that of the analog approach. The other factors, power consumption and reliability, are highly dependent on the design complexity and component selections.

Other Design Variables

Additionally, depending on how the piston amplitude is regulated, the controllers can be “resistive-dissipating” or “power-converting”. In many FPSC controllers, the intermediate DC bus power (i.e., *intermediate DC voltage* in Figure 12) is always dissipated by internal load resistors to regulate the DC bus voltage and the piston amplitude, and this is often referred to as a resistive-dissipating controller to

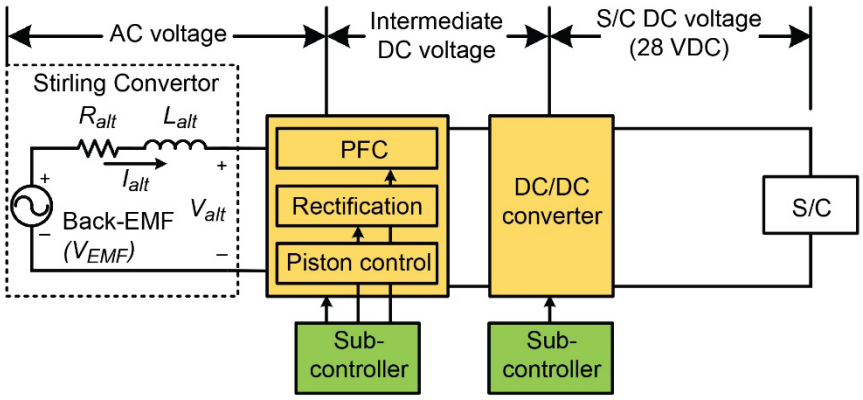


Figure 12.—A basic FPSC controller block diagram: orange boxes indicate general power-path components and the green boxes sub-controller blocks.

emphasize the dissipation by the internal resistors for the piston regulation. Because the regulated DC bus voltage is not the same as the 28 VDC spacecraft voltage, it will need to be converted to 28 VDC. In contrast, a power-converting controller controls the intermediate DC bus voltage through power conversion circuits without any internal dissipation mechanisms and converts to 28 VDC for the spacecraft. As a result, most power will be delivered to and dissipated in the spacecraft rather than being dissipated internally. Therefore, the power-converting controller will be much more efficient and would be suitable for flight designs while the resistive-dissipating controller is likely to be limited to the lab demonstrations.

Finally, some controllers may control the piston amplitude through direct piston motion measurements using a piston motion sensor, while the other controllers control the piston amplitude through indirect piston motion indicators such as the alternator voltage. Since no piston sensor has been demonstrated to operate for more than 17 years of the mission requirement and controllers with a piston sensor require a more complex circuit design than controllers without a piston sensor do, the piston amplitude control approach using indirect piston motion indicators is generally preferred.

FPSC Controller Classification and Review

While all criteria discussed in the previous section are important in the FPSC controller design, the passive/active PFC and self/forced-oscillation criteria would be historically the most common and distinctive design variables for the FPSC controllers. Therefore, in this section, all FPSC controllers will be classified into the following four categories—self-oscillation passive (SOP), forced-oscillation passive (FOP), self-oscillation active (SOA), and forced-oscillation active (FOA)—while other design variables will be described in each controller approach in those categories. Furthermore, controllers in each category will be reviewed and their detailed operating principles will be discussed.

Self-Oscillation Passive Controller

A self-oscillation passive (SOP) controller was first developed in the 1990s for the Space Power Research Engine (SPRE) project, which was then advanced for the Stirling Radioisotope Generator (SRG) and the Advanced Stirling Radioisotope Generator (ASRG) flight projects (Refs. 33 and 40). Even after the ASRG flight project ended, more effective SOP controllers have been actively designed and developed at the NASA Glenn Research Center (GRC), and some of them have been extensively used to control flexure-based Stirling convertors such as TDCs for the last 14 years (Refs. 11 and 39). On the other hand, because most SOP controllers developed to date are resistive-dissipating controllers, they have been mostly used as means for validating the operation of Stirling convertors operating in the laboratory. Also, because all SOP controllers that have been developed for low-power FPSCs to date use a tuning capacitor for PFC and a diode rectifier, this review will focus on the differences in the implementation of their DC bus regulation stage.

Reference 40 is a digital SOP controller and it uses an analog synthesized variable linear load (ASVLL) as shown in Figure 13. As mentioned previously, after the PF of the alternator voltage is corrected by a tuning capacitor, the corrected voltage is rectified by a diode rectifier, and this is referred to as *Rectified voltage* in Figure 13. A metal-oxide-semiconductor field-effect transistor (MOSFET) is operated in the ohmic region to control the rectified DC bus voltage (V_{DC}) to a constant value by adjusting the current flow (I) through the resistors (R_L) (Ref. 41). This controller has redundant load resistors and although not shown, each resistor can be controlled by an individual MOSFET for redundancy, if needed (i.e., four MOSFETs with four load resistors). Because the two inputs of the operational amplifier

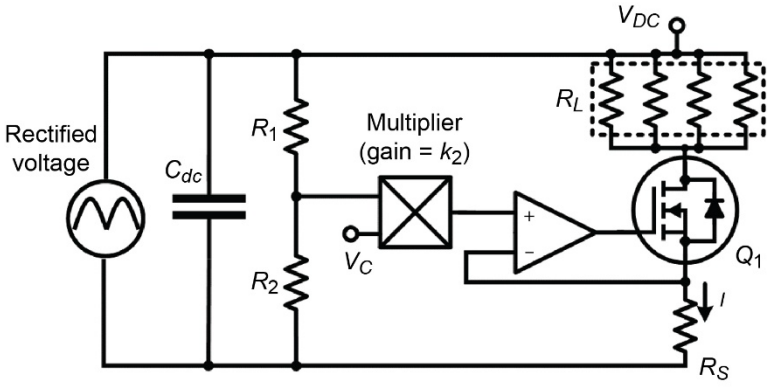


Figure 13.—An ASVLL DC load controller (Ref. 40).

(op-amp) will be forced to be equal due to the virtual short characteristic of the op-amp, the following equation can be derived (Refs. 40 and 41):

$$IR_s = k_1 k_2 V_c V_r \tag{12}$$

where I is the current flowing through a sensing resistor (R_s), k_1 is a voltage divider factor by R_1 and R_2, k_2 is a multiplier gain constant, V_c is the control set voltage determined by a controller, and V_{DC} is the DC bus voltage. The effective load resistance at the DC bus voltage then can be calculated as follows (Refs. 40 and 41):

$$R_{\mathrm{DC}} = \frac{V}{I} = \frac{R_s}{k_1 k_2 V_c} \tag{13}$$

According to Equation (13), the effective load resistance at the DC bus voltage node is a linear load directly controlled by the control voltage, and is independent of the load resistors, R_L. The control set voltage is determined in the digital engine controller (DEC) and it is used to control the DC bus voltage using a multiplier (i.e., a proportional (P) controller) such that the piston amplitude is regulated to the desired value based on the linear relationship between the piston amplitude and the DC bus voltage. It should be noted that while this controller does not require a piston sensor, it is a resistive-dissipating controller, and therefore, this controller is likely to be limited to laboratory exercise.

GRC 1st and 2nd Generation Digital Controllers, which were used for several years during the SPRE project and afterward, are digital SOP controllers and use a voltage-controlled resistive load to control the root mean square (RMS) value of the AC voltage across the load, as shown in Figure 14 (Refs. 40 and 42). These controllers sense AC voltage after the tuning capacitor and control relays connected to a resistor array to vary the total load resistance and regulate the RMS value of the AC voltage across the array and the piston amplitude. The 1st Generation controller uses an analog-to-digital converter (ADC), which is in Controller in Figure 14, to synthesize the load resistance based on the sensed voltage across the resistive array, while the 2nd Generation controller uses the ADC to compute the relative change that needs to be reflected in the load resistance based on the difference between the sensed voltage and the setpoint voltage and a P controller. As a result, the AC voltage across the resistor array will be regulated to a reference set point to regulate the piston amplitude based on their linear relationship.

Reference 37 is an analog SOP controller and it uses a linear AC regulator to regulate the DC load voltage, as shown in Figure 15. In this design, a pair of convertors in dual-opposed are connected with isolated electrical systems (Ref. 43). This means that each convertor is connected to a separate tuning capacitor for the PFC, after which they are connected in parallel to share the same DC bus. The PF-

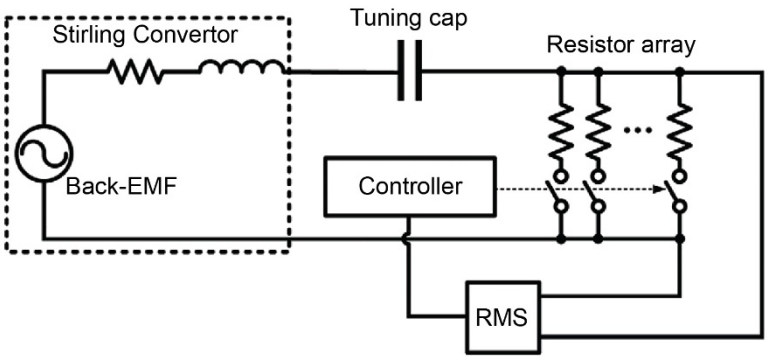


Figure 14.—A brief circuit diagram of the AC load controller in GRC 1st Generation Digital Controller and GRC 2nd Generation Digital Controller (Refs. 40 and 42).

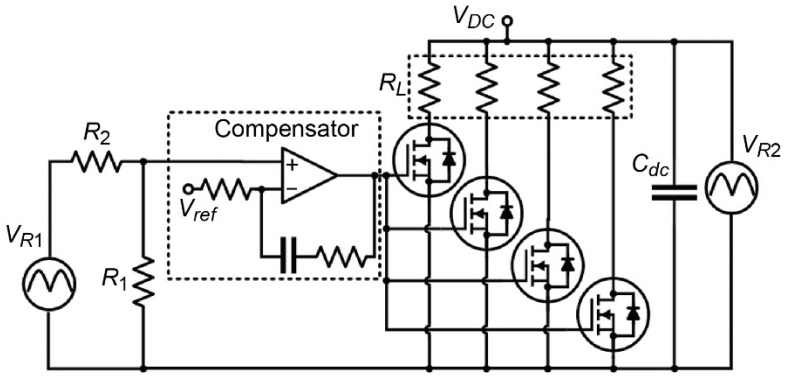


Figure 15.—The DC load controller in the linear AC regulator controller (Ref. 37).

corrected AC signal is then rectified by two diode rectifiers, resulting in V_{R1} and V_{R2} in Figure 15. V_{R1} is scaled by a voltage divider consisting of R_1 and R_2, which is then controlled to V_{ref} by a proportional-integral (PI) compensator, four MOSFETs, and four load resistors. On the other hand, V_{R2} is converted to a DC voltage by an energy buffer capacitor (C_{dc}) and this is the power path to transfer the AC power generated from the FPSC to the output DC bus. In this circuit, the MOSFET operates in the ohmic region for a linear load: if the output voltage of the voltage divider goes above V_{ref}, then the gate-source voltages of the MOSFETs will increase, which will in turn decrease the resistance of the MOSFETs. As a result, more current will flow through the load resistors and MOSFETs to dissipate more power to decrease V_{DC}. Likewise, if the output voltage of the voltage divider goes below V_{ref}, the compensator will increase V_{DC}. Therefore, the DC bus voltage will be actively controlled to constrain the piston amplitude based on the linear relationship between the DC bus voltage and the piston amplitude.

References 42 and 44 is an analog SOP controller and it uses an adjustable Zener shunt regulator (Z_1) to control the DC bus voltage, as shown in Figure 16. This controller is often referred to as the Zener diode controller (ZDC). The rectified voltage (V_R) is converted to DC voltage by an energy storage capacitor (C_{dc}) and the anode of the shunt regulator (i.e., the negative node of $V_{in,ref}$) is controlled to the reference voltage (V_{ref}) by op-amps and MOSFETs, while $V_{in,ref}$ and V_{DC} are regulated by the Zener shunt regulator, R_1, and R_2. The op-amps operate as comparators and MOSFETs operate in the saturation region (i.e., on-off switches) to form a bang-bang controller. The inputs to the positive nodes of the four op-amps are made slightly different by a voltage ladder consisting of three R_4 and one R_5 resistors, and R_5 is normally much greater than R_4 (i.e., $R_5 \gg R_4$). Because the positive input voltage of M_1 is higher than

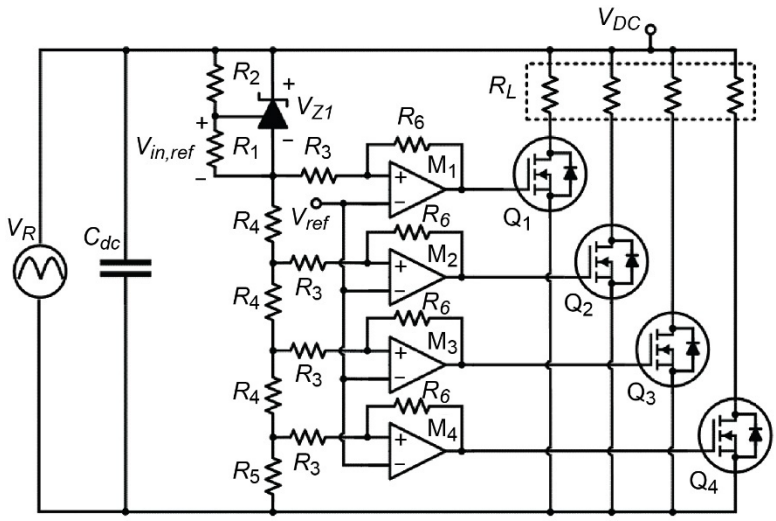


Figure 16.—The DC load controller in the ZDC (Refs. 42 and 44).

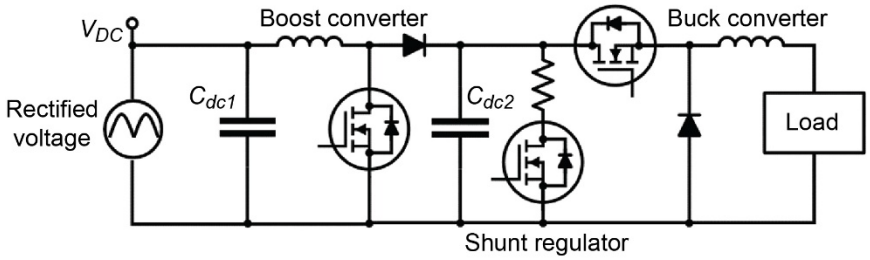


Figure 17.—The DC load controller in the NAC.

the other three op-amps, Q_1 and its series-connected resistor load will start dissipating power to regulate the DC bus voltage, while Q_2 to Q_4 will not until Q_1 alone cannot dissipate enough power to regulate the positive input voltage to V_{ref}. At this point, Q_2 will turn on and its load resistor will start dissipating power, while Q_3 to Q_4 will remain off, and so on. The input voltage differences should be made large enough that only a minimum number of the MOSFETs and load resistors will dissipate power for higher reliability of the system, while the differences should be made small enough for a low-ripple bus control. The input reference voltage of the Zener shunt regulator ($V_{in,ref}$) is normally determined by the manufacturer, and the regulating voltage across the Zener shunt regulator (V_z) can be calculated according to the following equation:

$$V_Z = \left(1 + \frac{R_2}{R_1}\right) V_{in,ref} \tag{14}$$

Therefore, the DC bus voltage will be controlled to

$$V = V_{ref} + V_Z = V_{ref} + \left(1 + \frac{R_2}{R_1}\right) V_{in,ref} \tag{15}$$

and the piston amplitude is indirectly regulated by controlling the DC bus voltage.

Each of these SOP controllers discussed focused on providing a simple mechanism for the validation of Stirling convertor hardware and are not ideal designs to transmit energy onto a spacecraft bus. The NASA Analog Controller (NAC), as shown in Figure 17, uses the series connection of a boost and buck

converter with an intermediate dc link to maintain effective convertor loading while efficiently transmitting power to the spacecraft bus. In this controller, the rectified output voltage is converted to DC voltage by an energy storage capacitor and regulated by a boost converter. Unlike a conventional boost converter, which regulates the output voltage, the boost converter in this controller controls the input voltage and the piston amplitude, and this is known as the input-controlled boost converter (Ref. 45). The boost converter can also correct the distortion PF, if necessary. The input-controlled boost converter is then followed by an input-controlled buck converter. This output buck converter seeks to regulate the C_{dc2} DC link instead of the load voltage and presents itself as a current source to the spacecraft load. Although not shown in this schematic, the voltage across the spacecraft load is normally regulated at around 28 VDC by a spacecraft voltage controller. Finally, a shunt regulator located between the boost and the buck converters will dissipate power in the case where the spacecraft load does not dissipate all power generated by the FPSC. It should be noted that this controller is the only power-converting SOP controller to date and a good candidate for flight projects.

Forced-Oscillation Passive Controller

As discussed earlier, the forced-oscillation passive (FOP) control strategy uses tuning capacitors and an AC bus signal. References 46 and 47 use tuning capacitors, a digital signal processor (DSP)-based AC power supply, and a resistor load to control a pair of FPSCs in a dual-opposed configuration (Figure 18). Since the particular AC power supply used cannot dissipate power, a resistor load is connected to the AC bus signal in parallel to dissipate the power. Resistance of the resistive load should be low enough so that it not only dissipates power generated from FPSCs but also dissipates any extra power supplied by the AC power supply to ensure that the AC power supply does not supply power to the FPSCs. This control strategy has been extensively used for laboratory testing of ASCs for more than a decade at NASA GRC due to its very simple and easy test setup. However, this control strategy is limited to the laboratory due to its resistive-dissipating nature.

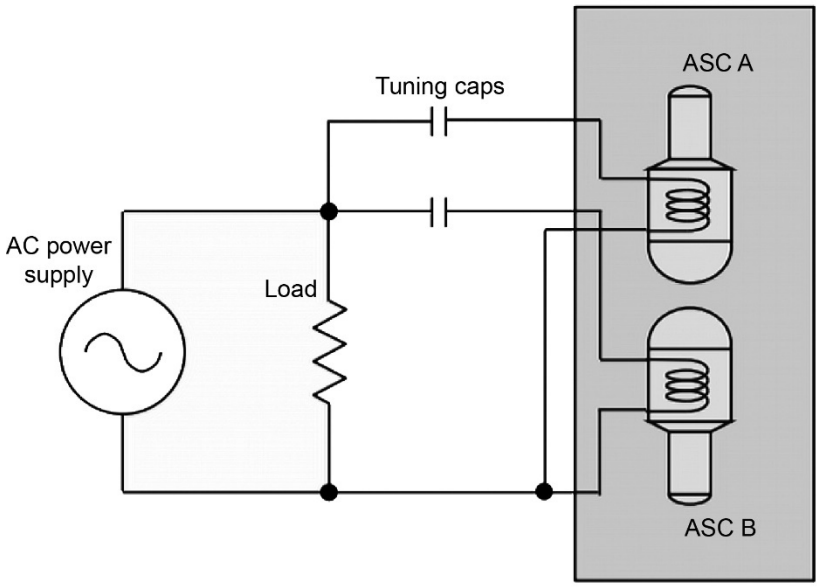


Figure 18.—An AC bus controller (Ref. 46).

Self-Oscillation Active Controller

The self-oscillation active (SOA) controller uses the active PFC approach and the operating frequency is primarily determined by the FPSC through self-oscillation. In principle, active PFC circuits in the SOA controller can be implemented by various circuit topologies (Refs. 24 to 29, and 48).

Reference 49 is a digital SOA controller and uses a bi-directional rectifier based on Reference 25 for the active PFC, as shown in Figure 19. In this design, six MOSFETs and two capacitors are used to generate five different voltage levels at the alternator terminals and this is often referred to as the five-level switching according to the definition in Reference 50. The controller first measures the piston motion (X_p) using a piston sensor to calculate the back-EMF (V_{emf}) and the reference current (I_{ref}) as follows:

$$V_{emf} = -K_e \frac{dX_p}{dt} \tag{16}$$

and

$$I_{ref,rms} = \frac{P_{out}}{V_{emf,rms}} \tag{17}$$

where K_e is the back-EMF constant in V/(m/s), X_P is the piston motion in m, and P_{out} is the power output set point in Watts. In the Reference Current Generator in Figure 19, the RMS value of the back-EMF is computed and a power setpoint value is divided by the RMS value to calculate an appropriate amplitude for the reference current. The back-EMF signal is then normalized between 1 and –1 and multiplied by the calculated amplitude to generate the reference current. This way, the reference current signal will be in phase with the back-EMF and have an appropriate amplitude to dissipate all power generated from the FPSC. Furthermore, oscillation of the piston stroke will be sustained as though there is a variable parasitic load (Ref. 42). Simultaneously, the alternator current (I_{alt}) is also measured by a current sensor and is forced to follow the reference current by switching the six MOSFETs to apply five different control voltage levels, V_{DC}, $V_{DC}/2$, 0, $V_{DC}/2$, and $-V_{DC}$, assuming that capacitance values of the two capacitors (C_1 and C_2) are the same. The switching sequence is shown in Table I and only the case when the polarity of the back-EMF is positive will be discussed because the same principle can be applied to the case when the

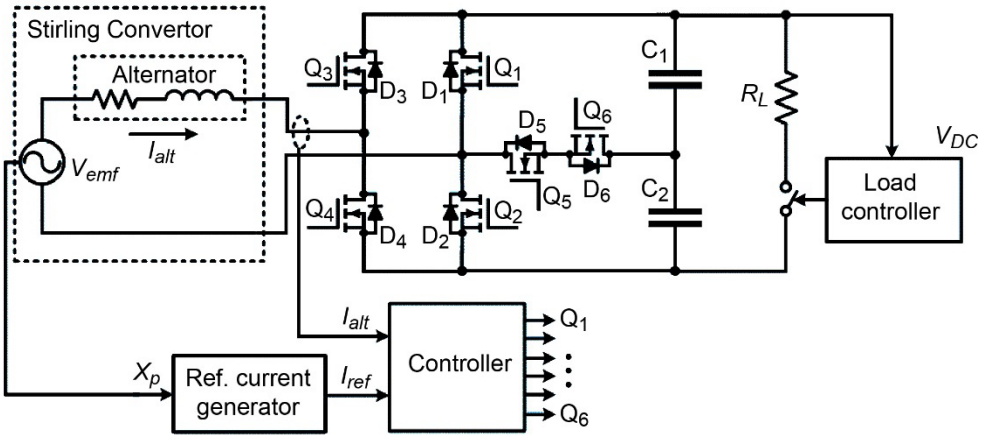


Figure 19.—A schematic of the GRC APFC controller (Ref. 49).

TABLE I.—SWITCHING SEQUENCE FOR FIVE-LEVEL SWITCHING (REF. 49)

V_{emf} polarity	MOSFET/ Diode on	V_{alt}	I_{alt} effect
+	D_2, D_3	V_{DC}	Fast decrease
+	D_3, D_5, Q_6	$V_{DC}/2$	Slow decrease
+	D_2, Q_4	0	Slow increase
+	Q_4, D_5, Q_6	$-V_{DC}/2$	Increase
+	Q_1, Q_4	$-V_{DC}$	Fast increase
−	Q_2, Q_3	V_{DC}	Fast increase
−	Q_3, Q_5, D_6	$V_{DC}/2$	Increase
−	D_1, Q_3	0	Slow increase
−	D_4, Q_5, D_6	$-V_{DC}/2$	Slow decrease
−	D_1, D_4	$-V_{DC}$	Fast decrease

polarity is negative. When no switch is turned on, the alternator current flowing in the positive direction will conduct the body diodes of Q_3 and Q_2 (D_3 and D_2, respectively) and the alternator voltage (V_{alt}) will be the sum of the voltage across C_1 and the voltage across C_2, or V_{DC}. Because V_{DC} is normally larger than the amplitude of the back-EMF, the voltage across the alternator inductor becomes negative, resulting in the decrease in the alternator current. If Q_6 is turned on, then the body diodes of Q_5 and Q_3 (D_5 and D_3, respectively,) will conduct and the alternator voltage will become $V_{DC}/2$, which is higher than the back-EMF for most times. Therefore, the alternator current will decrease but rather more slowly than the first sequence. If Q_4 is turned on, then the body diode of Q_2 (D_2) will conduct to make the voltage across the alternator zero. Because the back-EMF is positive, the voltage across the inductor will be also positive to increase the alternator current. If Q_4 and Q_6 are turned on, then the current will flow through C_2 and the alternator voltage will become—$V_{DC}/2$ to make the alternator current increase steeper. Finally, if Q_1 and Q_4 are turned on, then the alternator voltage will become $-V_{DC}$, resulting in a very fast increase in the alternator current. The piston amplitude is controlled by adjusting the amplitude of the reference current. With compared to the conventional H-bridge circuit where four MOSFETs are controlled, this circuit requires a more complex controller design as well as more MOSFETs and driving circuits. On the other hand, due to the higher resolution of the alternator current, THD and potentially electromagnetic interference (EMI) can be reduced (Ref. 49). Although this approach does not convert to 28 VDC tolerance band algorithm for the active PFC and AC-DC conversion, as shown in Figure 20. A reference current waveform (I_{ref}) is generated in the Reference Current Generator in the same manner as Reference 49 according to Equation (17), and the alternator current (I_{alt}) is measured using a current sensor. The measured alternator current is then subtracted from the reference current to compute an error current signal (I_{err}). Finally, the tolerance band algorithm will determine if the alternator current should be increased or decreased based on the error current signal and switch the four MOSFETs accordingly (Ref. 51). In order to switch the MOSFETs properly, they proposed the two most typical switching schemes: two-MOSFET switching and one-MOSFET switching, which generate two alternator voltage levels and three alternator voltage levels, respectively. These are often referred to as two-level switching and three-level switching, respectively (Ref. 50). The two-level switching turns on two diagonally-positioned MOSFETs simultaneously to increase the alternator current depending on the polarity of the alternator voltage, while it turns all MOSFETs off to decrease the alternator current. The switching sequence is shown in Table II (Ref. 17). If Q_2 and Q_3 are turned on, then the alternator voltage will

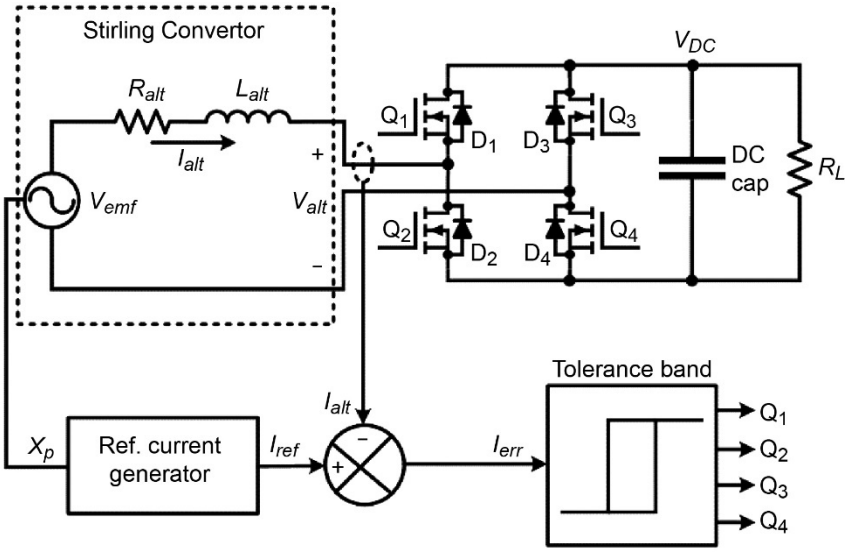


Figure 20.—An APFC controller using an H-bridge circuit (Ref. 17).

TABLE II.—SWITCHING SEQUENCE FOR TWO-LEVEL SWITCHING (REF. 17)

V_{emf} polarity	MOSFET/ Diode on	V_{alt}	I_{alt} effect
+	Q_2, Q_3	$-V_{DC}$	Increase
+	D_1, D_4	V_{DC}	Decrease
–	Q_1, Q_4	V_{DC}	Increase
–	D_2, D_3	$-V_{DC}$	Decrease

TABLE III.—SWITCHING SEQUENCE FOR THREE-LEVEL SWITCHING (REF. 17)

V_{emf} polarity	MOSFET/ Diode on	V_{alt}	I_{alt} effect
+	Q_2, D_4	0	Increase
+	D_1, D_4	V_{DC}	Decrease
+	Q_3, D_1	0	Increase
–	Q_1, D_3	0	Increase
–	D_2, D_3	$-V_{DC}$	Decrease
–	Q_4, D_2	0	Increase

become $-V_{DC}$. As a result, the voltage across the alternator inductor becomes positive and the alternator current will be increased. On the other hand, if all MOSFETs are turned off, then D_1 and D_4 will conduct and the alternator voltage will become V_{DC}. Because V_{DC} is generally greater than the back-EMF (V_{emf}), the voltage across the alternator inductor will become negative, and the alternator current will be decreased. The case when the polarity of the back-EMF is negative is very similar. In the three-level switching scheme, only one MOSFET is turned on at a time to increase the alternator current, while all MOSFETs are turned off to decrease the alternator current. The switching sequence of the three-level switching scheme is shown in Table III (Ref. 17). If Q_2 is turned on, then D_4 will conduct to make the alternator voltage zero. Since the back-EMF is positive, the voltage across the inductor will be positive,

and the alternator current will be increased. If all MOSFETs are turned off, then D_1 and D_4 will conduct and the alternator voltage will become V_{DC}. Therefore, the voltage across the inductor will become negative, and the alternator current will be decreased. Finally, if Q_3 is turned on, then D_1 will start conducting and the alternator voltage will become zero. As a result, the voltage across the inductor will become positive and the alternator current will increase. The case when the polarity of the back-EMF is negative can be analyzed in the same manner. The two-level switching scheme is suitable for the FPSC with high alternator inductance where higher voltage and current drawings are required, while the three-level switching scheme is suitable for the FPSC with low alternator inductance because relatively low voltage and current drawings are sufficient to force the alternator current to follow the reference current waveform (Ref. 17). Although the algorithms of this controller are practical and this has a potential for flight projects, only the simulation results were reported and no hardware was developed.

Forced-Oscillation Active Controller

Like the FOP controller, the forced-oscillation active (FOA) controller forces system poles into the LHP, and like the SOA, it uses active PFC circuits to perform PFC and AC-DC conversion. Since its first development by Sunpower in 2006, the FOA controller has been extensively developed by Lockheed Martin Space Systems (LMSS), Applied Physics Laboratory (APL), and NASA Glenn Research Center (GRC). In particular, this type of controller was designed for flight missions and Engineering Models (EMs) were developed. As discussed earlier, many different active PFC topologies are available to implement the FOA controller (Refs. 24 to 29).

Reference 52 is a digital FOA controller and uses an H-bridge circuit to implement an algorithm called a “virtual tuning capacitor”. The virtual tuning capacitor algorithm integrates current flowing into the controller and calculates the voltage which would be present across a capacitor and an AC bus as shown in Figure 21. The controller then enforces that voltage on the alternator using an H-bridge. The reference voltage can be calculated as:

$$V_{ref} = V_{ac} + V_t \tag{18}$$

where V_{ac} is the AC bus voltage and V_t is the voltage across the virtual tuning capacitor. Because V_t can be calculated as

$$V_t = \frac{1}{C_t}\int I_{alt}\, dt \tag{19}$$

V_{ref} will then become

$$V_{ref} = V_{ac} + \frac{1}{C_t}\int I_{alt}\, dt \tag{20}$$

While this controller uses an H-bridge circuit like a digital SOA in Reference 17, the H-bridge circuit in this controller works as an inverter that inverts the DC bus voltage (V_{DC}) to the reference AC voltage (V_{ref}) in the direction opposite to the power transmission path. Just like the two-level switching in the previous section, two diagonally-located MOSFETs will be switched on and off simultaneously to produce either $+V_{DC}$ or $-V_{DC}$ across the alternator. Figure 22 and Table IV show one typical example of implementing the two-level switching modulation. A triangle waveform (V_{tri}) with a much higher frequency than the frequency of the reference voltage and an amplitude higher than that of the reference voltage signal will be compared with the reference voltage signal to generate a modulated signal as shown

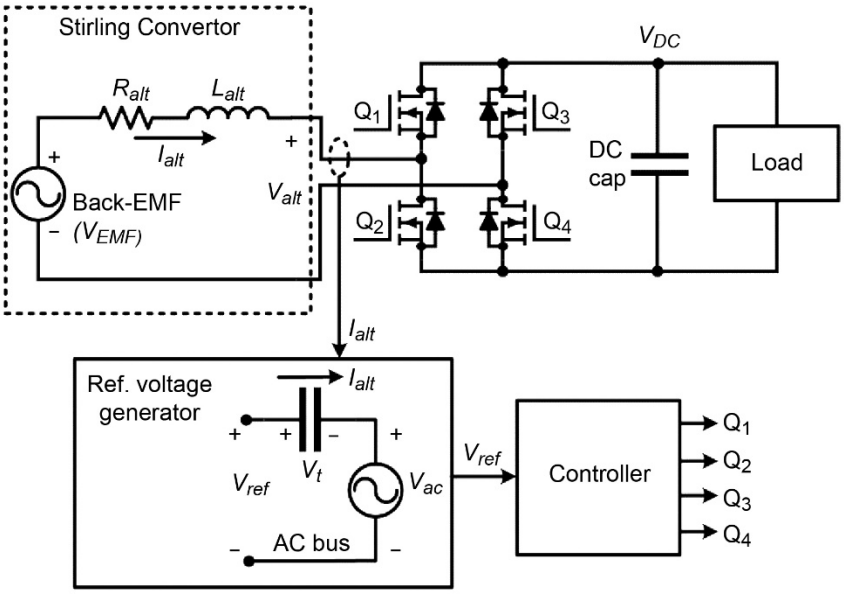


Figure 21.—A digital FOA controller (a virtual tuning capacitor) developed by Sunpower (Ref. 52).

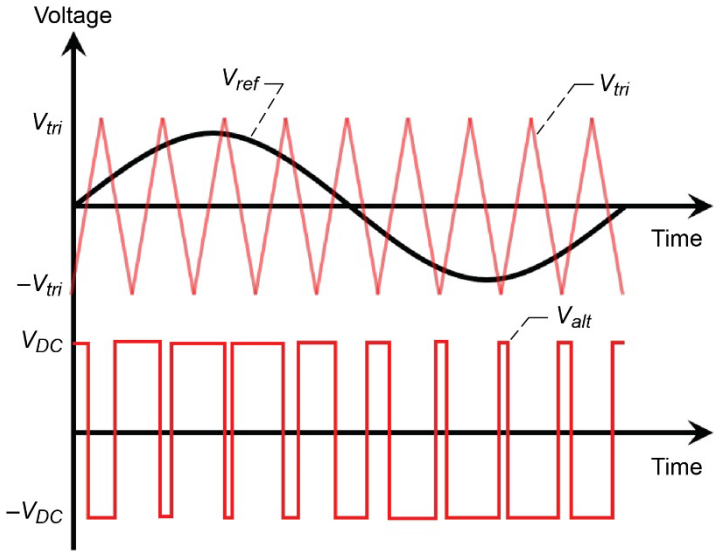


Figure 22.—Two-level switching waveform.

TABLE IV.—SWITCHING SEQUENCE FOR TWO-LEVEL SWITCHING FOR AN INVERTER

Condition	PWM polarity	MOSFET/ Diode on	V_{alt}
$V_{sine} > V_{tri}$	+	Q_1, Q_4	V_{DC}
$V_{sine} < V_{tri}$	–	Q_2, Q_3	$-V_{DC}$

in the V_{alt} waveform in Figure 22. If the instantaneous reference voltage is higher than the instantaneous triangle voltage, then the PWM signal will become V_{DC}. Likewise, if the instantaneous reference voltage is lower than the instantaneous triangle voltage, then the PWM signal will become $-V_{DC}$. A set of produced two-level voltage pulses will then be filtered by the alternator inductor to produce desired sinusoidal waveform for the back-EMF.

On the other hand, LMSS, APL, and NASA GRC have introduced the three-level switching scheme to potentially improve power efficiency, reduce EMI, and waveform distortion, by adding one more voltage level: $+V_{DC}$, 0, $-V_{DC}$. One common example of the three-level switching scheme is shown in Figure 23 and the switching sequence is shown in Table V. In this switching scheme, a triangle waveform (V_{tri}) and its inverted signal ($-V_{tri}$) are used. If $V_{ref} > V_{tri}$ and $V_{ref} > -V_{tri}$ then Q_1 and Q_4 will turn on and the alternator voltage will become V_{DC}. If $V_{ref} > V_{tri}$ and $V_{ref} < -V_{tri}$ or $V_{ref} < V_{tri}$ and $V_{ref} > -V_{tri}$, then the alternator voltage will become zero. Finally, if $V_{ref} < V_{tri}$ and $V_{ref} < -V_{tri}$, then Q_2 and Q_3 will start conducting and the alternator voltage will become $-V_{DC}$.

Advanced Stirling Convertor Controller Unit (ACU), developed by LMSS and NASA GRC, uses the same virtual tuning capacitor algorithm as Reference 52 and the overall schematic is shown in Figure 24 (Ref. 53). Like Reference 52, the H-bridge circuit operates as an inverter in the reverse direction to invert the H-bridge DC output voltage (V_{local}) to a reference AC voltage according to Equation (20). An intermediate DC-DC power converter (buck) then converts the H-bridge DC output voltage to 28 VDC spacecraft bus voltage, and it regulates the H-bridge output voltage to be always several volts higher than the spacecraft bus voltage to ensure that the H-bridge output voltage is higher than the amplitude of the alternator voltage for a proper operation of the H-bridge as an inverter. The buck converter has an outer

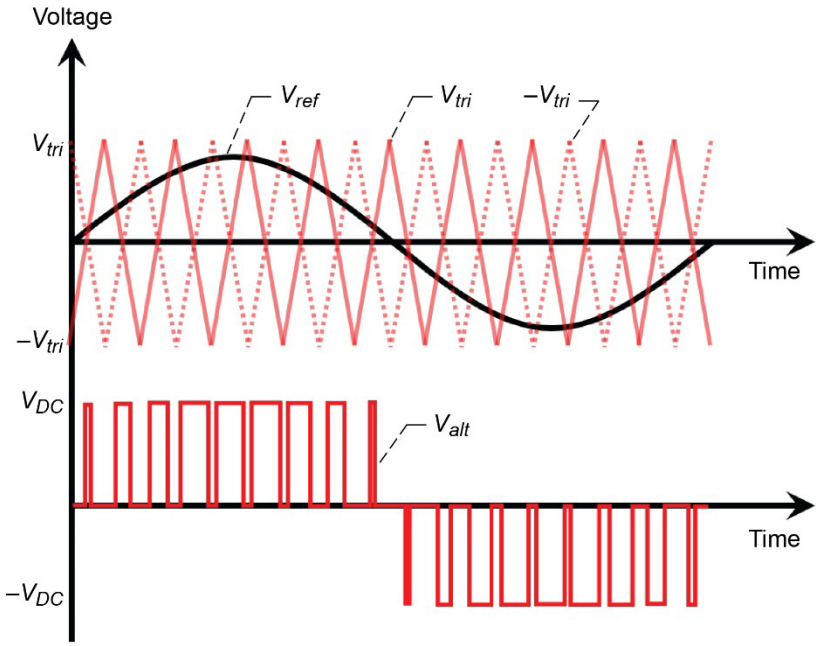


Figure 23.—Three-level switching waveform.

TABLE V.—SWITCHING SEQUENCE FOR THREE-LEVEL SWITCHING FOR AN INVERTER

Condition	MOSFET/ Diode on	V_{alt}
$V_{ref} > V_{tri}, V_{ref} > -V_{tri}$	Q_1, Q_4	V_{DC}
$V_{ref} > V_{tri}, V_{ref} < -V_{tri}$	Q_1, Q_3	0
$V_{ref} < V_{tri}, V_{ref} > -V_{tri}$	Q_2, Q_4	0
$V_{ref} < V_{tri}, V_{ref} < -V_{tri}$	Q_2, Q_3	$-V_{DC}$

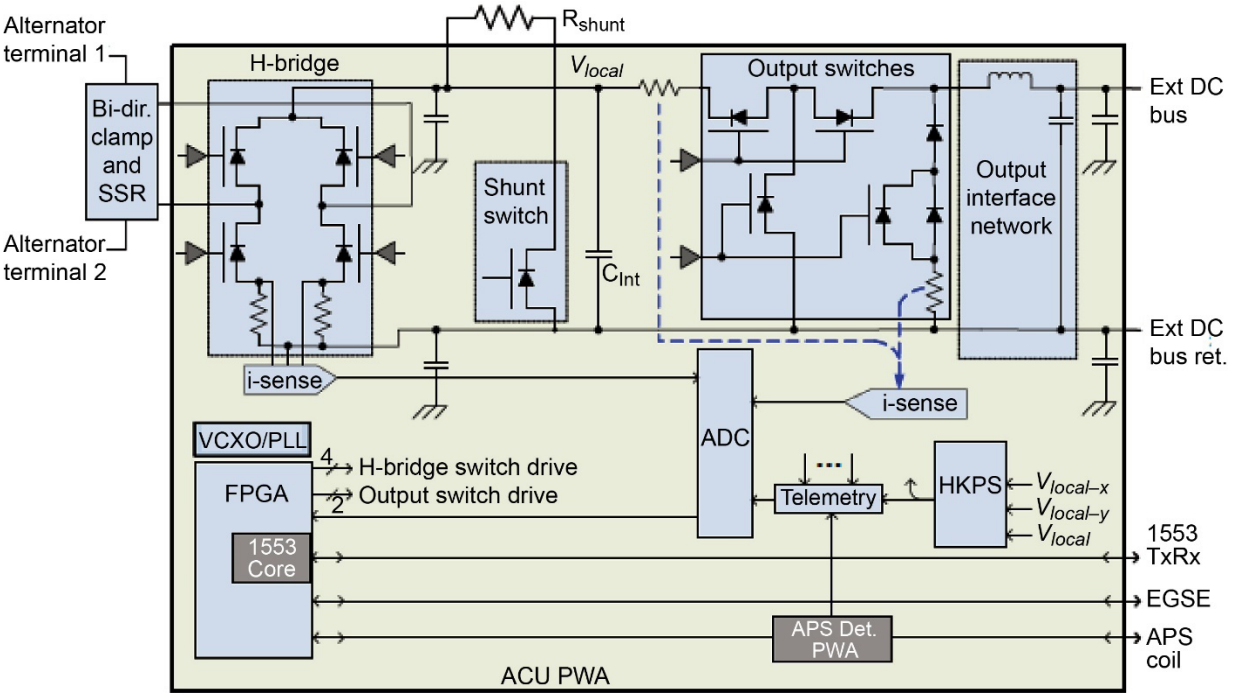


Figure 24.—ACU developed by LMSS and NASA GRC (Ref. 53).

current control loop (CCL), in addition to the inner voltage control loop (VCL), to provide DC current to the spacecraft. Furthermore, if the H-bridge voltage goes above 40 VDC, then a shunt switch will be activated to dissipate power and lower the voltage back down below 40 VDC. All control algorithms are implemented in an FPGA, Engineering Models (EMs) were developed for the ASRG flight project, and the operation was verified through testing with ASCs. Finally, two identical controllers controlled a pair of ASCs in the dual-opposed configuration with one backup controller in case of failure events (N+1 redundancy architecture).

The Single Convertor Controller (SCC) and Dual Convertor Controller (DCC), developed by APL and NASA GRC, also uses the same virtual tuning capacitor algorithm as Reference 52 (Refs. 30, 44, and 54). The basic schematic is shown in Figure 25. The H-bridge controls the alternator voltage to the reference voltage according to Equation (20) and a buck converter stage regulates the DC link voltage ($V_{out}(t)$) at a value higher than the amplitude of the alternator voltage. More specifically, the buck converter is regulated in the average current mode (ACM) to produce DC current output to the spacecraft and its current setpoint is adjusted by the difference between the H-bridge output voltage and the voltage set point. If the DC link voltage goes above the setpoint, then the buck converter will increase the current setpoint to dissipate more power and decrease the DC link voltage. Likewise, if the DC link voltage goes below the voltage setpoint, then the current setpoint will be decreased to dissipate less power and increase the DC link voltage. Also, an emergency shunt is placed at the DC link to prevent it from increasing above a limit to cause any damages on electronics by dissipating any remaining power that the spacecraft could not use. All controller algorithms are implemented in an FPGA. Engineering Models (EM) were developed and the extended operation has been demonstrated at NASA GRC (Ref. 44). Finally, two identical primary controllers control a pair of ASCs in the dual-opposed configuration, each of which has a backup controller in case of failure events, and this is called a 2N redundancy architecture. The primary controllers and the backup controllers are located in separate controller chassis, which will allow repair work on the primary controllers to be attempted upon fault events while the secondary controllers control the FPSCs.

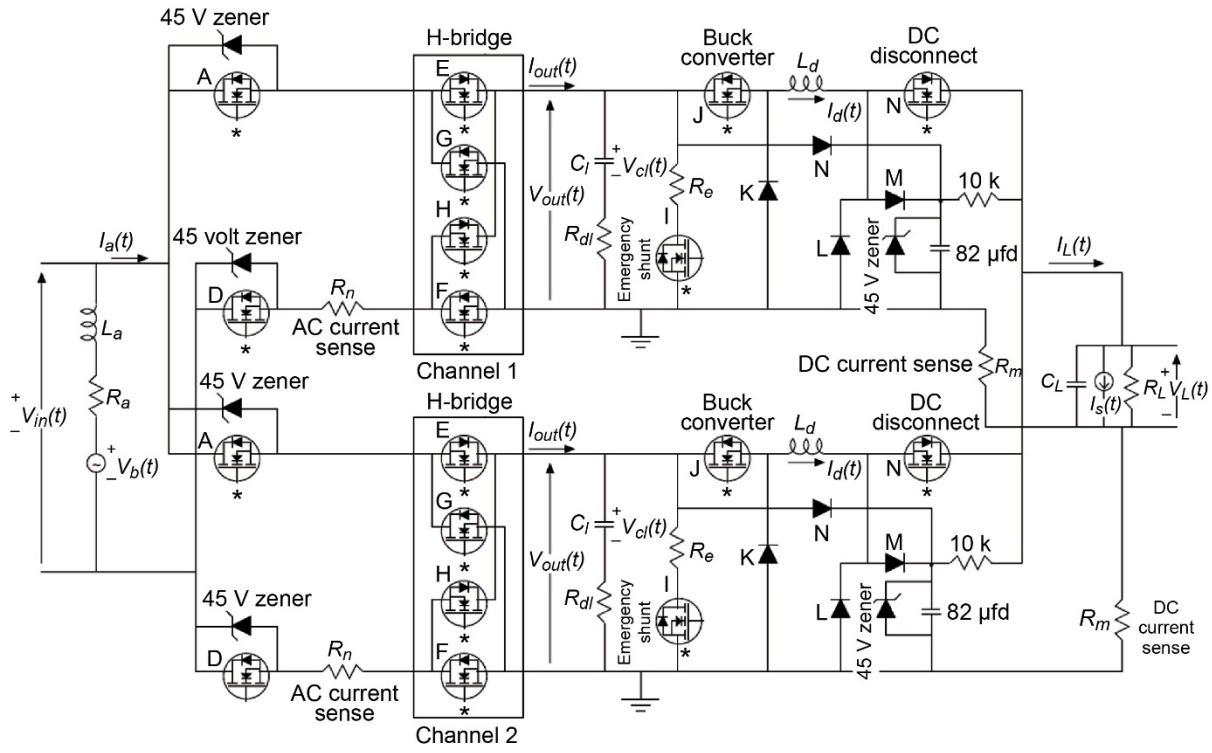


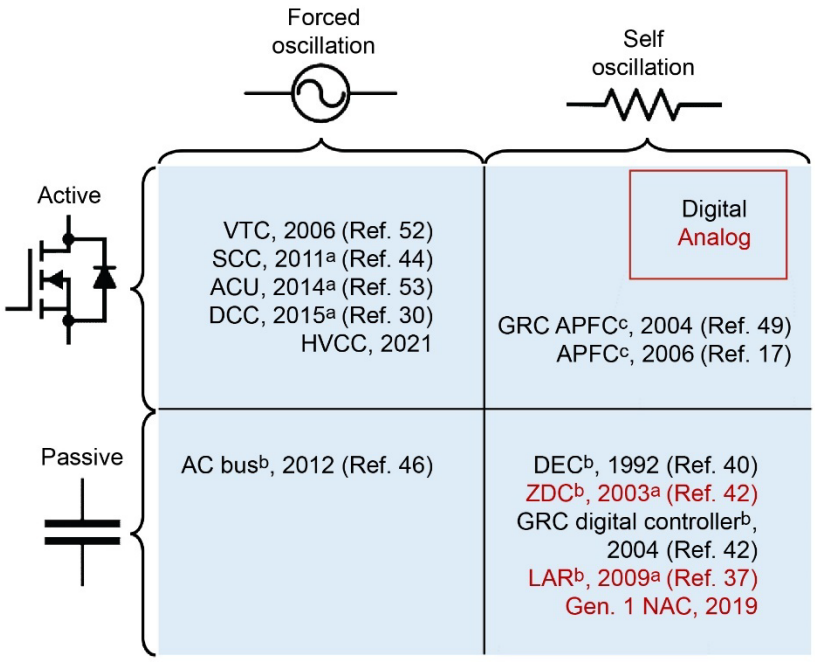
Figure 25.—The 2-channel SCC developed by APL and NASA GRC (Ref. 30).

High-Voltage Convertor Controller (HVCC), although not reported, is currently being developed by APL and NASA GRC, and the control algorithm and basic operating principles are almost identical to the SCC/DCC except the HVCC is designed for FPSCs with higher alternator voltage such as the Flexure-Isotope Stirling Convertor (FISC).

Finally, both ACU and SCC/DCC reported that the controller tends to show some instability issue when the backup controller takes over the control from the primary controller upon failure, or a switchover (Refs. 30 and 53). This is because a few milliseconds of switching time during the switchover can create a small phase difference between the AC bus signal in the backup controller and the piston velocity, and the phase difference leads to a momentary instability issue. This can be problematic because pistons can be damaged due to the instability during the switchover. In order to mitigate this issue, an algorithm was developed by APL where a virtual resistive load or an SOA controller is momentarily used during the switchover until the piston is stabilized, after which it is transitioned back to an FOA controller. While this was successfully demonstrated using ASCs, this indicates that the self-oscillation type controllers would be inherently more stable and reliable than the forced-oscillation type controllers.

FPSC Controllers Comparisons

Figure 26 and Figure 27 show the FPSC controllers according to the categories and in chronological order, respectively. The FOA controller and the SOP controller have been the most popular design choices for the last three decades, while the FOP controller hasn't been actively developed since its first development and has been only used in laboratory testing. Also, a couple of efforts have been made to develop the SOA controller during the SRG-110 flight development project, after which this approach hasn't been pursued further. Furthermore, most FOA, FOP, and SOA controllers have been developed in



[a]This is an actual delivery date and may be different from the report date.
[b]Resistive-dissipating controllers.
[c]Piston sensor required.

Figure 26.—A summarized classification of FPSC controllers. This is an actual/estimated delivery date and may be different from the report date.

*Resistive-dissipating controllers to exercise the FPSC operation.
†Piston sensor required.

Figure 27.—FPSC Controllers in the chronological order.

digital, while most SOP controllers in analog. As shown in Figure 27, nearly 10 new FPSC controllers were designed and/or developed during the two flight development projects, SRG-110 and ASRG. It should be noted that the DCC and ACU, which were delivered to GRC after the ASRG project was terminated, were also designed and developed during the ASRG project. It is also worth noting that during the SRG-110 project, where TDC units were used, self-oscillation type controllers were actively developed, while during the ASRG project where ASC units were used, forced-oscillation type controllers were actively developed. After those two flight development projects, the main choices have been FOA and SOP controllers.

Detailed comparisons of the state-of-the-art FPSC controllers are shown in Table VI. Resistive-dissipating controllers are excluded from the table due to their limitations. Since SCC/DCC and ACU are the only controllers that were developed to Engineering Models (EMs), the SWaP numbers for those controllers are specified, and relative estimations of the other controllers with respect to the SCC/DCC and ACU are made based on assumptions that the other controllers are implemented using flight-equivalent COTS parts. It should be noted that while designs and basic layouts of the EMs of the SCC/DCC and ACU are mostly compatible with space-qualified parts, the actual SWaP numbers of the flight units would be larger than those numbers of the EMs. Furthermore, in this comparison, the SCC was excluded because it is the predecessor of the DCC.

For the size and weight estimations, the most contributing factor would be the presence of the physical tuning capacitor. The size and weight of a passive PFC controller, which requires a physical tuning capacitor, would be normally heavier and larger than those of an active PFC controller. Additionally, although it will not be as a significant contributor as the physical tuning capacitor, the size and weight of analog controllers would be slightly larger and heavier than those of digital controllers, given the complexity of the controllers where many op-amps, other semiconductor devices, and passive components would be required in the analog implementation. Also, for the power loss estimation, the rectification method will be the most dominating factor: a passive diode rectifier would normally dissipate much more power than an active rectifier would due to high forward voltage drops of space-qualified

TABLE VI.—DETAILED COMPARISONS OF STATE-OF-THE-ART LOW-POWER FPSC CONTROLLERS

Reference	NAC	(Ref. 49)	(Ref. 30)	(Ref. 53)	HVCC
Other name	NAC	GRC APFC	DCC	ACU	HVCC
Frequency control	Self-oscillate	Self-oscillate	Forced-oscillate	Forced-oscillate	Forced-oscillate
PFC	Passive	Active	Active	Active	Active
Rectification	Passive	Active	Active	Active	Active
Analog/Digital	Analog	Digital	Digital (RTAX-2000S)	Digital (RTAX-4000S)	Digital
Switching scheme	----------	5-level	2-level /3-level	2-level /3-level	TBD
Flight project	Future flight project	SRG-110	Future flight project	ASRG	Future flight project
Flight units	----------	----------	EM	EM	----------
Redundancy	----------	----------	2N	N+1	----------
Piston sensor required	No	Yes	No	No	No
Estimate reliability[a]	High	Low	Moderate	Moderate	Moderate
Estimate size[b]	Large	Small	Small (561 in^3)[c]	Small (687 in^3) [c]	Small
Estimate weight[b]	Heavy	Light	Light (3.8 kg)[c]	Light (6.9 kg)[c]	Light
Estimate power loss[b]	High	Low	Low (10 to 15%) [c]	Low (10 to 15%) [c]	Low
Estimate cost[b]	Low	High	High	High	High

[a]Reliability is based on the design complexity of each controller approach. No component-level reliability analysis is conducted in this paper.
[b]SWaP-C are based on controllers for two FPSCs with redundancy controllers using flight parts or their COTS equivalent parts.
[c]These numbers are based on flight-equivalent COTS parts and actual numbers using flight parts may be larger.

power diodes (~1 V). Other factors would be quite insignificant. For the cost estimation, the digital implementation, which would normally require a space-qualified FPGA, would cost significantly higher than the analog implementation, while the cost difference due to other factors would be quite insignificant. Finally, reliability was estimated. While analog approaches (i.e., discrete IC components) or Application-Specific Integrated Circuits (ASIC) have been considered more reliable than FPGAs, due to significant technology advancement, FPGAs seem to be as reliable as other means or some even claim that FPGAs are more reliable due to the computational overhead (Refs. 56 and 57). Therefore, in this paper, it is assumed that digital and analog approaches are equally reliable and the reliability is merely determined by the complexity of the controller design. The complexity is dominantly determined by the frequency control method and the PFC and rectification algorithms. Depending on whether the FPSC is self-oscillated or forced-oscillated, the switchover algorithm can become very complex, because the forced-oscillation type controller forcibly controls the phase and the frequency of the piston velocity to those of the AC bus signal, which can potentially cause instability from a small phase difference between the piston velocity and the AC bus signal during the switchover transition (Ref. 30). On the other hand, since the operating frequency is mostly determined by the FPSC in the self-oscillation type controller, these controllers will not have the instability issue during the switchover, and thus a very simple switchover algorithm should suffice. Also, rectification circuits using MOSFETs, such as an H-bridge circuit, require much more complex algorithms than diode rectifier circuits do. Furthermore, unlike other approaches, GRC APFC, which is an SOA controller, requires a piston sensor to perform the PFC and this can introduce higher complexity and lower reliability since no piston sensor has been demonstrated reliable operation for 17 years to date.

Based on the SWaP-C and reliability analysis of the state-of-the-art FPSC controllers, it is clear that the NAC, an analog SOP controller, is suitable for applications that require low-cost and high-reliability, while GRC APFC, DCC, ACU, and HVCC (digital SOA and digital FOA controllers) are suitable for applications that require small-size, light-weight, and high-efficiency. For future flight designs, further improvements in these state-of-the-art controllers can be made in terms of the SWaP-C and reliability. For example, for the NAC, a diode rectifier and a boost converter can be replaced with active switches to reduce power loss, the controller for the active switches can be controlled in the discontinuous conduction mode (DCM) to improve reliability, and the current tuning capacitors can be replaced with tuning capacitors with higher energy density as in a kilowatt-level controller (Ref. 23). Also, the GRC APFC may be implemented without a piston sensor to improve reliability. Finally, the cost of the GRC APFC, DCC, ACU, and HVCC can be reduced by developing their analog versions, while the size and weight may be slightly increased.

Conclusion

This paper presented a brief review of the FPSC controller approaches that have been developed for low-power radioisotope power systems and suggested design recommendations for state-of-the-art FPSC controllers. First, the basic operating principles and design variables of the FPSC controllers were discussed. After that, all FPSC controller approaches were classified into four different categories based on the two most common design variables. Next, a review of the FPSC controller approaches in each category was conducted and those approaches were plotted according to the categories and in chronological order. Finally, important metrics of the state-of-the-art FPSC controllers, such as SWaP-C and reliability, were summarized and compared, and their design recommendations for future flight projects were suggested.

The five main design variables for the FPSC controllers were first discussed: active/passive PFC and rectification, self/forced-oscillation, analog/digital implementation, resistive-dissipating/power-converting, and direct piston motion sensor/indirect piston motion indicator. It was found that the PFC is a critical step to maximize the power transfer from the FPSC to the spacecraft and two different approaches—passive PFC and active PFC—were available. The passive PFC was more reliable than the active PFC, while the active PFC was smaller in size and lighter in weight than the passive PFC. Next, self-oscillation and forced-oscillation approaches were discussed using an impedance model of the FPSC and an oscillation system analysis method. The self-oscillation approach was operated by locating poles of the system on the $j\omega$-axis while in the forced-oscillation approach, poles were moved to the LHP to force the FPSC to oscillate at the frequency of an electrical AC bus. It was also found that the self-oscillation approach was more reliable than the forced-oscillation approach due to the simpler switchover algorithm. After that, analog and digital implementation approaches were discussed. The digital implementation was estimated to be smaller in size and lighter in weight than the analog implementation, while the cost of the analog implementation was estimated to be much lower than that of the digital implementation. Finally, the other two design variables, resistive-dissipating/power-converting and direct piston motion sensor/indirect piston motion indicator, were discussed. It was found that the power-converting approach would consume much less power than the resistive-dissipating and a controller using an indirect piston motion indicator would be more reliable than a controller using a direct motion sensor.

Because active/passive PFC and self/forced-oscillation were found to be the most commonly discussed and distinctive design variables, all FPSC controllers were classified into the following four categories and the other three design variables were discussed in the review of each category: (1) self-oscillation passive (SOP) controller, (2) forced-oscillation passive (FOP) controller, (3) self-oscillation active (SOA) controller, and (4) forced-oscillation active (FOA) controller. Among the controllers that have been developed over the last three decades, the SOP and FOA controllers were the most popular design choices and most SOP controllers and all FOA controllers were implemented in analog and digital, respectively. On the other hand, FOP controllers were limited to laboratory demonstrations, and SOA controllers were designed for the SRG-110 flight project about 15 years ago but no further development efforts have been made since then. Furthermore, most power-converting FPSC controllers—NAC, GRC APFC, DCC, ACU, and HVCC—were selected as the state-of-the-art FPSC controllers and they were compared in terms of their important metrics including SWaP-C and reliability. Finally, design recommendations were suggested for each state-of-the-art controller. The large size and heavyweight of the NAC can be improved by adopting new capacitor technologies with higher energy density, the low reliability of the GRC APFC can be improved by designing an SOA controller with an indirect piston motion indicator, and the high cost of the GRC APFC, DCC, ACU, and HVCC can be reduced by implementing them using analog components.

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