Radiation Effects and Analysis Lessons: a Scientist's Field Instruction to Explain Radiation Testing

March 2022 Version

(REAL SciFI ExpRT 22)

This presentation was compiled for
The NASA Electronic Parts and Packaging (NEPP) Program by:

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Acronyms

3D	3-Dimensional (3D)
AI	Artificial Intelligence (AI)
AKA	Also Known As (AKA)
ARC	Ames Research Center (ARC)
Arms	Root Mean Square Current in Amps (Arms)
BGA	Ball Grid Array (BGA)
BOK	Body of Knowledge (BOK)
Caps, C	Capacitor (Caps, C)
CMOS	Complimentary Metal-Oxide Semiconductor (CMOS)
COTS	Commercial Off the Shelf (COTS)
CREME-96	Cosmic Ray Effects on Micro-Electronics 1996 Revision (CRÈME-96)
DDD	Displacement Damage Dose (DDD)
DFN	Dual Flat-Pack No-Leads (DFN)
DSEE	Destructive Single Event Effects (DSEE)
DUT	Device Under Test (DUT)
ECC	Error Correcting Code (ECC)
EMPC	Experimental & Mathematical Physics Consultants (EMPC)
ESD	Electrostatic Discharge (ESD)
FET	Field Effect Transistor (FET)
FTP	File Transfer Protocol (FTP)
FWHM	Fixed Width at Half Maximum power (FWHM)
GCR	Galactic Cosmic rays (GCR)
GEO	Geosynchronous Orbit (GEO)
GPIO	General Purpose Input Output (GPIO)
GPU	Graphics Processing Unit (GPU)
GSFC	Goddard Space Flight Center (GSFC)
HDPE	High Density Polyethylene (HDPE)
HPC	High Performance Computing (HPC)
I, V, P	Current, Voltage, Power (I, V, P)
ID	Identifier (ID)
IP	Intellectual Property (IP)
JEDEC	Joint Electron Device Engineering Council (JEDEC)
JESD	JEDEC Standards (JESD)
JPL	Jet Propulsion Lab (JPL)
JSC	Johnson Space Center (JSC)
KVM	Keyboard Video Mouse (KVM)
L	Inductor (L)
LDC	Lot Date Code (LDC)
LET	Linear Energy Transfer (LET)
LPDDR4	Low-Power Dual Data Rate Random Access Memory, Generation 4 (LPDDR4)
MAPLD	Military and Aerospace Programmable Logic Devices (MAPLD)
ML	Machine Learning (ML)
MOSFET	Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
NASA	The National Aeronautics and Space Administration (NASA)
NDSEE	Non-Destructive Single Event Effects (NDSEE)
NEPP	NASA Electronic Part and Packaging (NEPP) Program
NRL	Naval Research Laboratory (NRL)
NSRL	NASA Space Radiation Laboratory (NSRL)
PCB	Printed Circuit Board (PCB)
PCBA	Printed Circuit Board Assembly (PCBA)
PMIC	Power Management Integrated Circuit (PMIC)
PoP	Package-On-Package (PoP)
RAM	Random Access Memory (RAM) - AKA system memory
REAG	Radiation Effects and Analysis Group (REAG)
RIC	Radiation-Induced Conductivity (RIC)
ROM	Read Only Memory (ROM) - AKA program memory
SBC	Single Board Computer (SBC)
SEB	Single Event Burnout (SEB)
SEFIs	Single Event Functional Interrupts (SEFIs)
SEGR	Single Event Gate Rupture (SEGR)
SEL	Single Event Latchup (SEL)
SET	Single Event Effect induced transients (SET)
SEU	Single Event Upsets (SEU)
SI	International System of Units (SI)
SiP	System-In-Package (SiP)
SoC	System-on-Chip (SoC)
SOI	Silicon on Insulator (SOI)
SOTA	State of the Art (SOTA)
SPE	Solar Proton Events (SPE)
SRIM	Stopping and Range of Ions in Matter (SRIM)
SSAI	Science Systems and Applications, Inc. (SSAI)
TAMU	Texas Agricultural & Mechanical University (TAMU)
TID	Total Ionizing Dose (TID)
TM	Technical Memorandum (TM)
TPA	Two-Photon Laser absorption (TPA)
TPU	Tensor Processing Unit (TPU)
TSV	Through Silicon Via (TSV)
VDD	Drain Voltage (VDD)
VSS	Source/Sink Voltage (VSS)

Radiation Assurance Requires Synchronous Integration

This is why radiation engineers tend to answer with "it depends…"

Image credits: NASA and other government sources

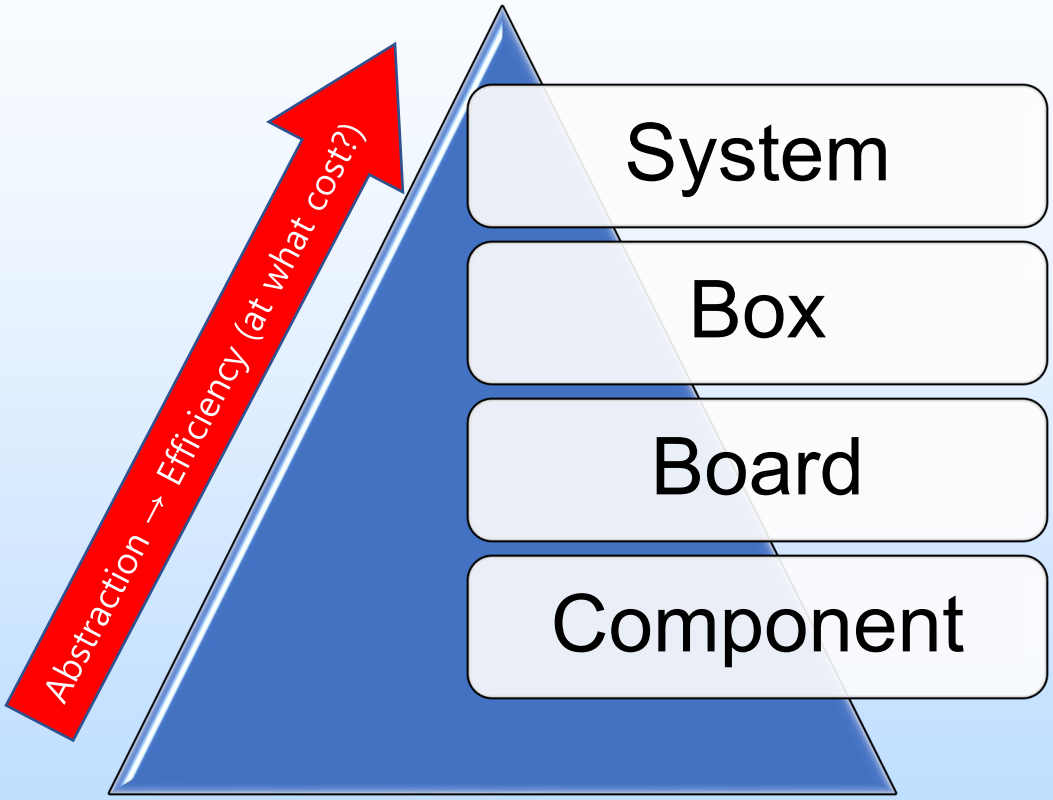
- Considerations summarized in these elements allow designers to effectively choose parts for their best performance for a given architecture
- Comprehension requires a complete synchronous picture of how technologies are to be used effectively
- Emphasizing one of these elements without understanding the others can compromise the integrity and performance of the parts and mission success

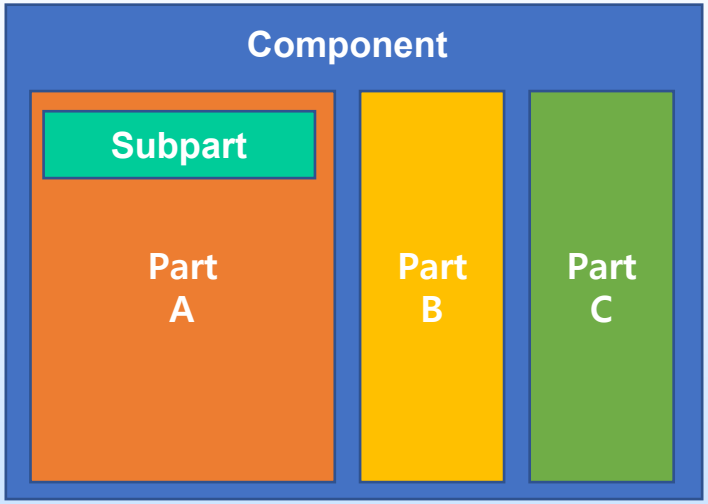
Adapted from Edward Wyrwas' presentation from the 12th Space Computing Conference in Pasadena, CA. July 30 – August 1, 2019. STI DAA number 20190028690

NEPP Processor Enclave

- State of the Art (SOTA) computational devices exist as individual semiconductor components yet require other devices to operate in a realistic system.
- The **Processor Enclave** is intended to be better nomenclature to categorize these types of compute devices, including compute devices that are System-In-Package (SiP), Package-On-Package (PoP), or monolithic devices which employ SOTA heterogeneous process integration to achieve a system within one device package.
- While Graphics Processor Units (GPUs) are the primary technology being characterized in this NEPP subtask, the GPU is a general-purpose compute component, and its **relevant technology competitors need to be evaluated** such as Systems on Chip (SoC), microprocessors and artificial intelligence (AI) capable devices.
- In these slides we provide a glimpse into the challenges associated with performing radiation testing on High Performance Computing (HPC) and Neuromorphic Computing devices.
- **These slides provide a high-level overview for an approximation of our radiation assurance process.**

Design Characterization & Qualification Trade Space





Based on ISO 26262-11:2018(E)
Figure 2. "A semiconductor, its parts and subparts"

The higher we go in abstraction,
the farther we are from the Device Under Test (DUT)

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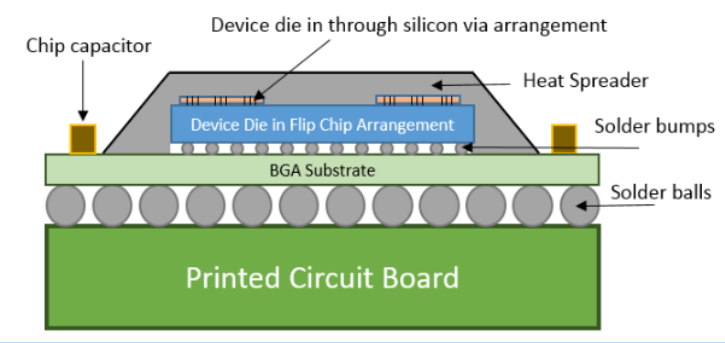
Miniaturization Trends

- The trend in microelectronics has always been toward miniaturization, improvements in transistor density (quantity per μm^3), and power efficiency.
- Because we need our electronics to do more things, state of the art technologies aim to heterogeneously integrate many capabilities into small discrete components with ever increasing quantities of input and output signals.
- To accomplish this feat, component package configurations must evolve in at least the same velocity leveraging all 3 dimensions. This has permitted computers to shrink from room-sized to palm-sized in just a few decades while their complexities and capabilities have increased tremendously from basic calculations to running most of the modern world.
- Moore's Law has historically been the colloquial term associated with scaling technology smaller as time moves forward. Gordon Moore (co-founder of Intel) spoke about an observation he made in 1965 that "the number of transistors on a microchip would double about every two years, while the cost of computers is halved" because of improvements in manufacturing technology.

Component Packaging Technology

- Coinciding with Moore's Law have been developments in two adjacent industries which impact how the semiconductor devices are physically used. The semiconductor device is called the **die**, as it **is diced from a larger wafer of material**.
  - The circuit board industry has developed multiple substrate material options (e.g., epoxy, glass, polyimide) to reduce size (notably thickness) and increase functionality such as flexibility
  - Device integrators have invented interconnect systems (e.g., bond wires, solder bumps) which connect the miniature metallization to the circuit boards and have reduced the overburden (e.g., over-mold, encapsulant, passivation coatings) that provides thermal relief, fire retardants, and protection from environmental stressors such as moisture and chemicals. The latter is called the component package, and in some cases, there isn't one (i.e., chip-on-board).
- To address the needs of converging commercial market segments, component packaging technology has developed in favor of modular, multifunctional system blocks that ease integration, shorten product design cycles, and permit automated assembly (aka attaching the devices to the circuit board).

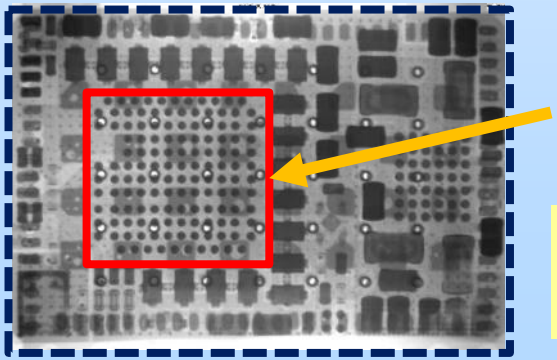


What is a DUT Really?

- The Device Under Test (DUT), or electronic item we intend to test, is the transistor layers of the semiconductor die. We call these layers (which typically extend to nearly the edges of the die) and their corresponding thickness the sensitive volume of a device.
- The die is often embedded in plastic molding compound, ceramic cavities, or found on organic (small chain polymer) substrates, sometimes with a metal lid over top of it.
- A Neuromorphic Computing example is the Google Coral Tensor Processing Unit (TPU) module which is used for tensorflow-lite inferences.
  - Organic substrate module circuit board with a backfilled lid cavity and copper heat spreader. The backfill is plastic molding compound that fills the entire cavity. Not only is there a 5x5mm TPU die inside the package, but also a power management die, a crystal oscillator, and at least a dozen passive components.

10mm

15mm



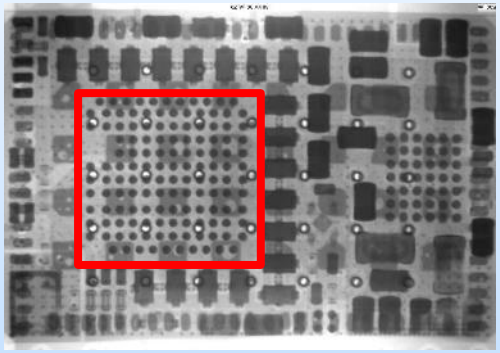
DUT is found within the 5mmx5mm die, outlined here

Left: Photo
Right: X-ray

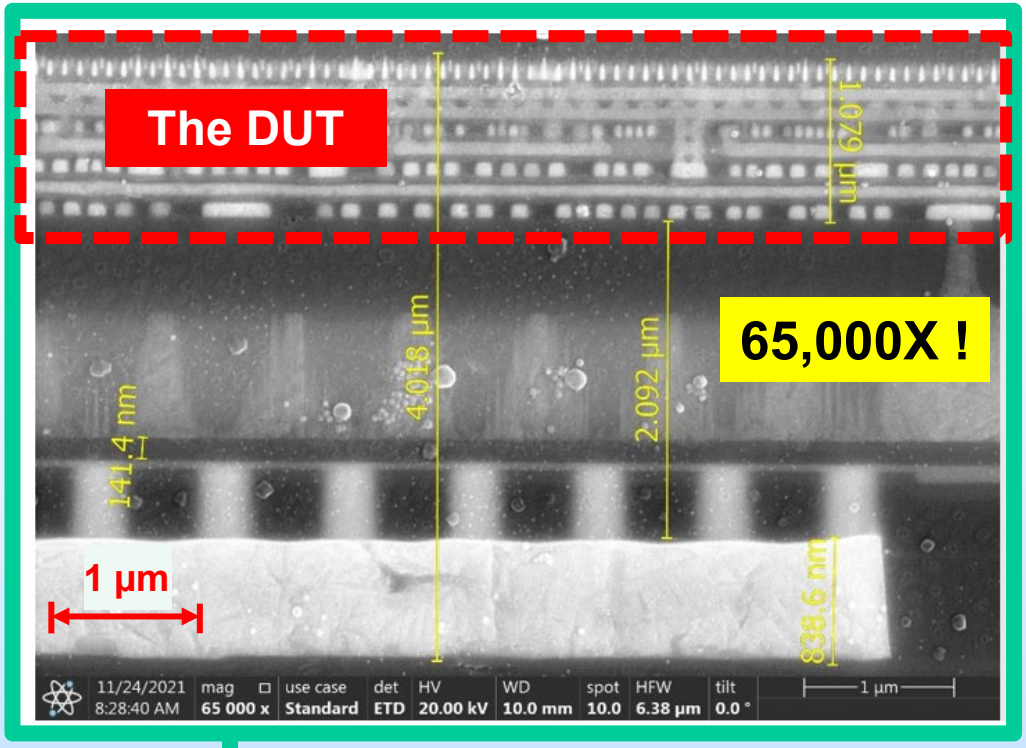
Images courtesy of NEPP

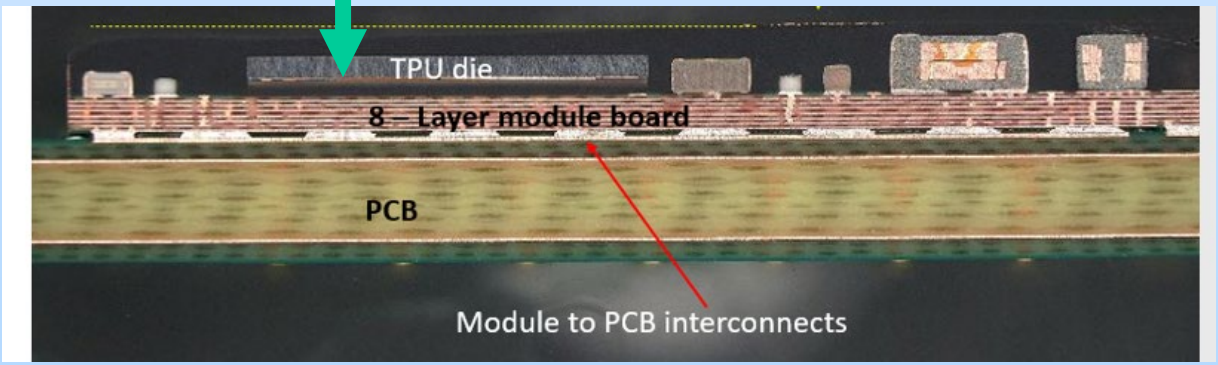
Component Packaging vs Sensitive Volume

We had to design and fabricate a PCB to use the component



Component of interest (TPU die) is a 5x5mm flip-chip (aka upside down die with underside metallization) within the plastic encapsulant, ~500um beneath a copper foil at the top of the packaging lid.

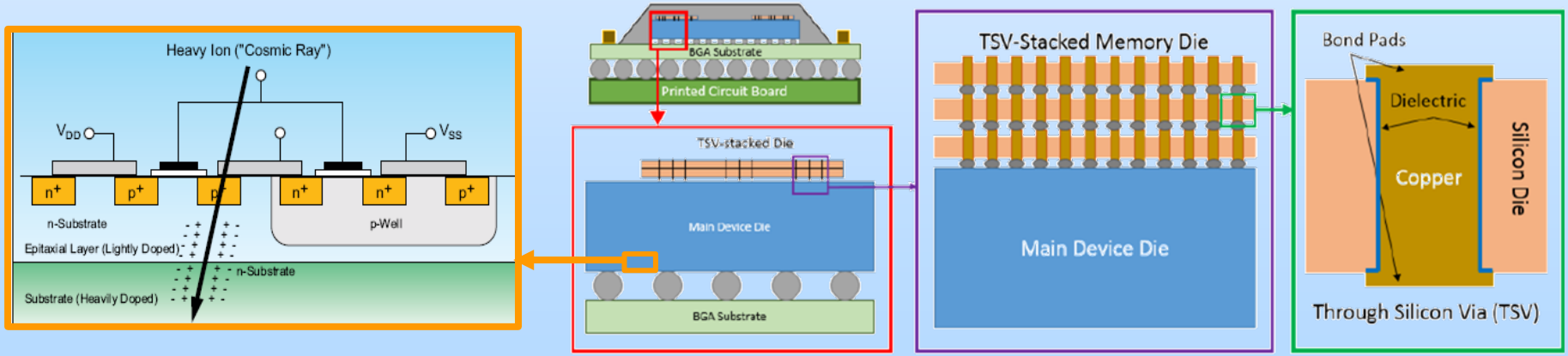




Images courtesy of NEPP

SOTA Packaging

- State of the Art (SOTA) packaging, while it permits higher performance computing, it introduces significant challenges in the techniques and methodologies used by radiation test designers.
- Metallization layers are a higher density barrier in the line-of-sight to reach the sensitive volumes.
  - Sometimes we can remove some layers, but we risk the integrity of the device
- Heatsinks, heat spreaders, and lidded components create additional challenges and prevent radiation from reaching the sensitive volume.
- These overlays prevent us from testing at common ground-based test facilities and <u>do not</u> stop radiation in space.



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“Fault Tolerant Schemes” (1/2)

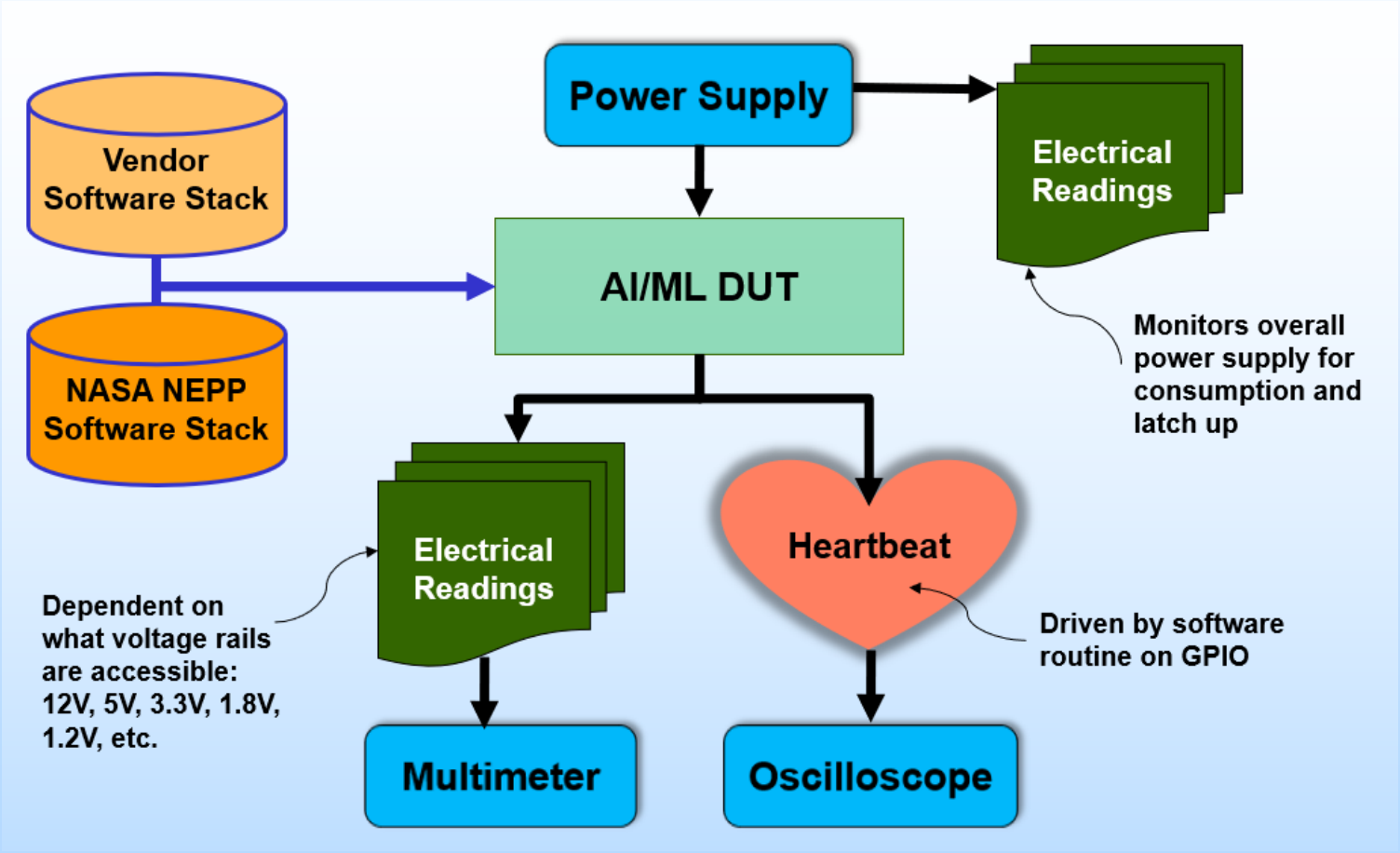
- High Performance Computing (HPC) Commercial Off The Shelf (COTS) devices are extremely complex. Therefore, we map out system redundancies, and any features which promote error correction or parity.
- We have to ask questions:
  - Fault tolerance schemes; are they employed correctly? Are they used correctly/overloaded?
  - Does Error Correcting Code (ECC) improve or hurt radiation performance?
  - Will we have the ability to test with and without the mitigation in place?
  - What software frameworks and libraries must also run in the background in addition to their test software or scientific payload? Are any of these systemwide services prone to faults?

“Fault Tolerant Schemes” (2/2)

- Upset tolerance is important. Mitigation schemes need to restore the system to a good state.
- It is important to understand when the mission-critical systems need to be available. There are many discrete time windows which exist during the mission, with different requirements. It is not appropriate to assume a complex device will be in the same computational state when radiation effects happen.
- Not all fault modes caused by radiation effects can be "injected" or mimicked easily. Charge spreading and diffusion to regions you can't control tend to reign supreme.
- It is hard or impossible to fully exercise the state-space to verify the tolerance. There are more ways to break something than we can usually test.

Electrical Monitoring

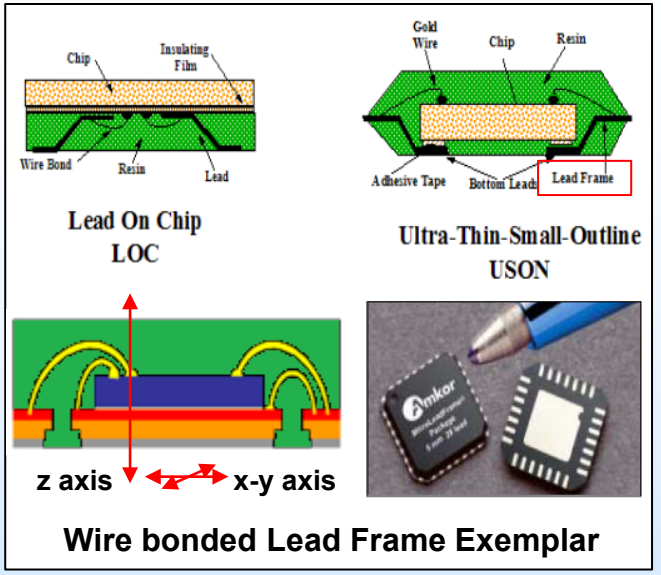
- In addition to monitoring the outbound data from the device (e.g., accuracy, error, results), we try to monitor electrical and thermal readings from a variety of points within the test system



Adapted from Edward Wyrwas' presentation from the NEPP Electronic Technology Workshop (ETW), Greenbelt, MD, June 15-18, 2020

Single Event Latch-Up (1/3)

- The consideration for Single Event Latch-up (SEL) is its impact on system availability.
  - Does the device have a recovery rate as compared to the mission?
  - Can it sustain an upset and a reboot during the mission? What about during the critical time window where science should be happening?
  - Is the latch-up recoverable at all? If so, does it cause latent damage?



Wire bonded Lead Frame Exemplar

- Underlying problem:
  - "COTS are not intended to experience space related latch-up. They are able to receive Electrostatic Discharge (ESD) related latch-up through their packaging lead frame (x-y axis latch-up) and are tested for this. They are not tested for z-axis latch-up, which is what radiation does. It's fault injection within the transistors, which are otherwise not accessible from outside its package." (E. Kawam, Microchip, paraphrased from NEPP Processor Enclave teleconference 1/21/2022)
  - COTS devices are not designed for SEL tolerance or immunity. Limited latch-up mitigation is usually implemented to protect against terrestrial concerns like power supply over voltage or ESD. High energy particles in space cause SEL by depositing charge vertically in a transistor → a different concern. (T. Wilcox. GSFC)

Image adapted R. Ghaffarian, Body of Knowledge (BOK) for Leadless Quad Flat No-Lead/Bottom Termination Components (QFN/BTC) Package Trends and Reliability. STI number 20160001774

Single Event Latch-Up (2/3)

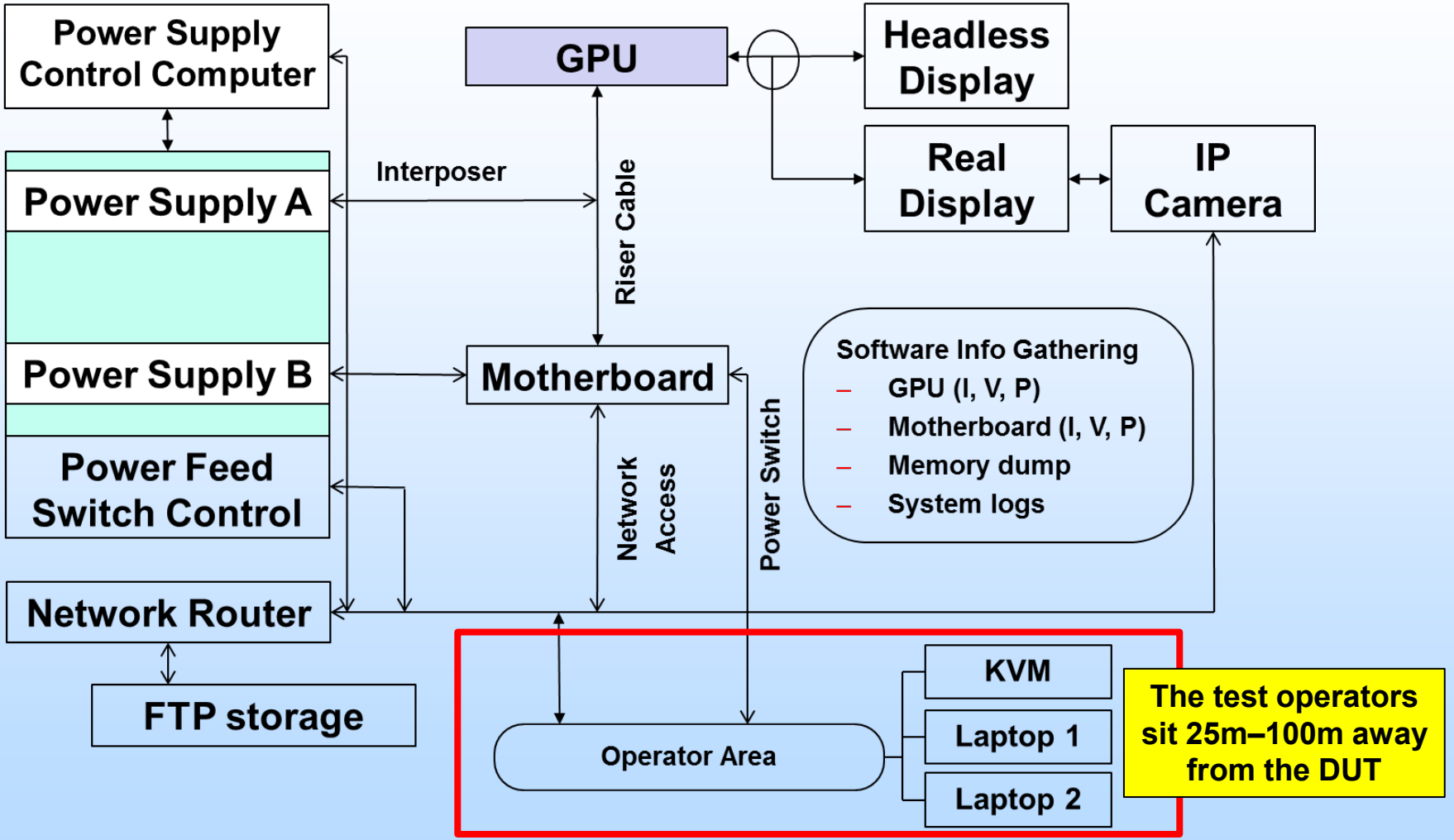
- COTS vendors may report total ionizing dose data for a part that is adequate for the mission, but this carries no meaning to SEE response or is even a guarantee for TID
- Where SEL data is published, care must be taken to evaluate the linear energy transfer (LET) threshold in the broader context of reliability and availability requirements. In many cases, immunity of an underlying technology is used in lieu of test data for COTS (e.g., bipolar-only or dielectrically isolated processes).
- Shielding in a space environment only has a practical reduction to TID and DDD. While minimal, it can reduce SEE rates up to a factor of 2 depending on sensitivity and mission orbit. Additional secondary particles can also be cascaded if the shield is close to the die or cause dose enhancement effects*.
- GCRs are not shieldable, hence the focus on avoiding SEL susceptibility entirely.
- **Testing is the only way to assure a mission can be met**.

S. H. Crain, J. E. Mazur, R. B. Katz, R. Koga, M. D. Looper and K. R. Lorentzen, "Analog and digital single-event effects experiments in space," in IEEE Transactions on Nuclear Science, vol. 48, no. 6, pp. 1841-1848, Dec. 2001, doi: 10.1109/23.983140.

Single Event Latch-Up (3/3)

- SEL doesn't have a test standard. JESD57 helps but doesn't fit the bill for devices with a lot of overburden (i.e., plastic encapsulant). Classical latch-up in a radiation terminology is “often” destructive. In many tests, determining the root cause of SEL-like events is very difficult and potentially costly, and classifying as a non-destructive SEL vs a high-current SEFI not caused by physical latch-up requires serious analysis.
  - JEDEC JESD57: Test procedure for the management of single-event effects in semiconductor devices from heavy ion irradiation
  - This test standard is valid when using a cyclotron or Van de Graaff accelerator. Microcircuits under test must be delidded. The ions used at the facilities have an atomic number Z > 2. It does not apply to SEE testing that uses protons, neutrons, or other lighter particles.
- Hypothetical approximation for statistical relevance for SEL:
  - Let’s hypothesize that it takes 10M ions to hit each state of a single transistor: On/Off/Transition State
  - If we have a device with 1B transistors, how many ions do we need to hit all the transistor states? Is this even enough ions to accomplish this feat? Do we have enough time to do this?
- Single Event Latch-up testing will help to determine **how the device will fail**
  - A common level for broad statistical sampling with heavy ions is 1x10^7/cm^2 but even that does not guarantee whole die coverage.

No Human Presence While the Beam is Engaged



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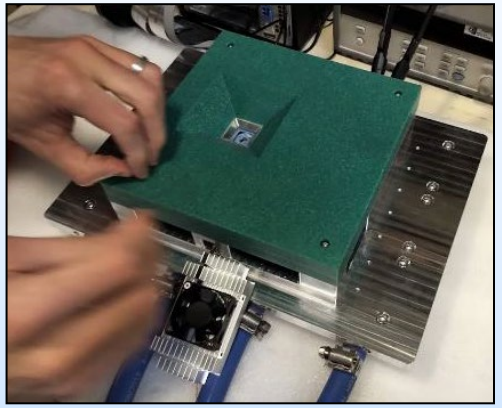
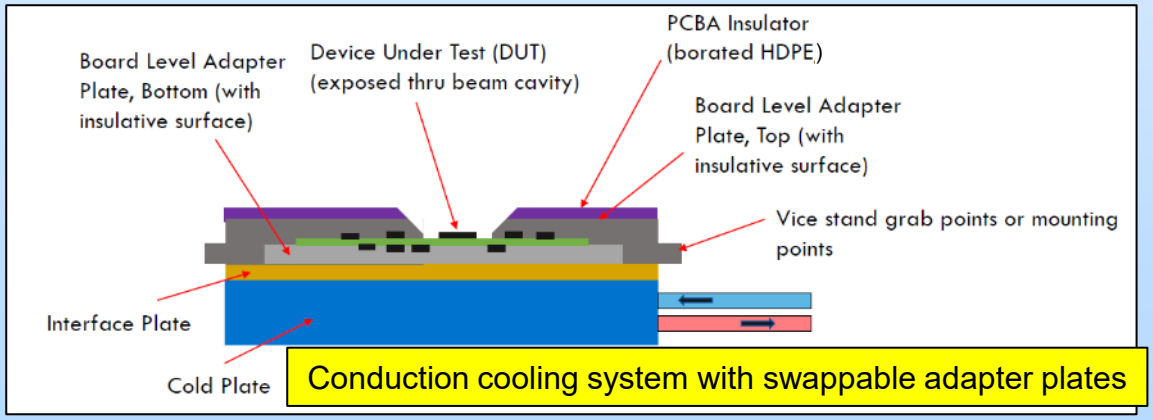
What About Software?

- A single board computer (SBC) has firmware, a boot loader, operating system, drivers, libraries, etc.
  - We try to control as many variables as possible; cross compiling code from a single code base or version-locking libraries and other supporting software
- While the usual “test as you fly” concept is applicable to simple devices (i.e., operational amplifier), the more complex the device (i.e., GPU), the more challenging it becomes to design an appropriate test design (and build a reliable tester).
  - This is due to the accelerated nature of the SEE test versus space particle rates – actual flight designs might not be appropriate to gather sufficient information, nor to cover sufficient application state-space, nor to statistically cover all the functional blocks during short beam test run times.
  - It is important to note that due to the huge number of application options that modern complex devices are capable of, most SEU testing is geared to provide application-specific information.
  - Interpreting this data is challenging, at best, for other applications.
- “Test as you fly” may not be possible with higher complexity devices; Therefore, we focus on simpler IP blocks with simple algorithms
  - If the software routine is too complex, then we cannot capture the error taking place. The system simply crashes.
  - Ultimately, a project must reduce expectations for amounts of resources available on a flight system; an HPC cluster is not same as a flight board. There is less RAM, less ROM, slower clock speeds, and therefore slower throughput compared to COTS counterparts

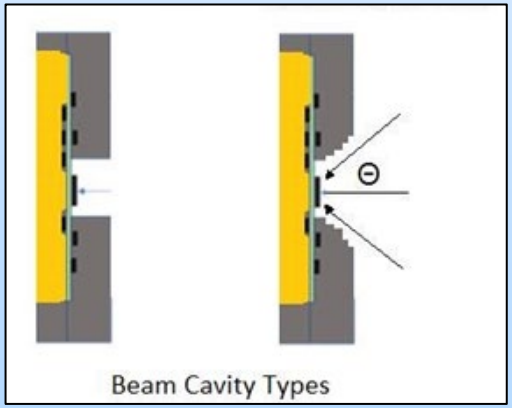
Thermal Control

- Some facilities have compressed dry nitrogen that can be used to actively cool a component.
- Some facilities operate the device in a vacuum, which means there is no air present to cool the device. Thermal conduction is the only solution using a chiller on location.
- Because HPC COTS are typically rated for room temperature conditions, the HPC device must operate well within its nominal thermal specification as modified.
  - Spare parts are often required to fine tune the cooling solutions.
  - A fine-tuned system also allows for testing at the HPC's rated temperature limit; decreasing the cooling until the desired temperature is achieved
- It is worth noting that non-HPC components are tested at its maximum rated junction temperature (85°c or 125°c) when conducting SEL testing.





Conduction cooling system with swappable adapter plates



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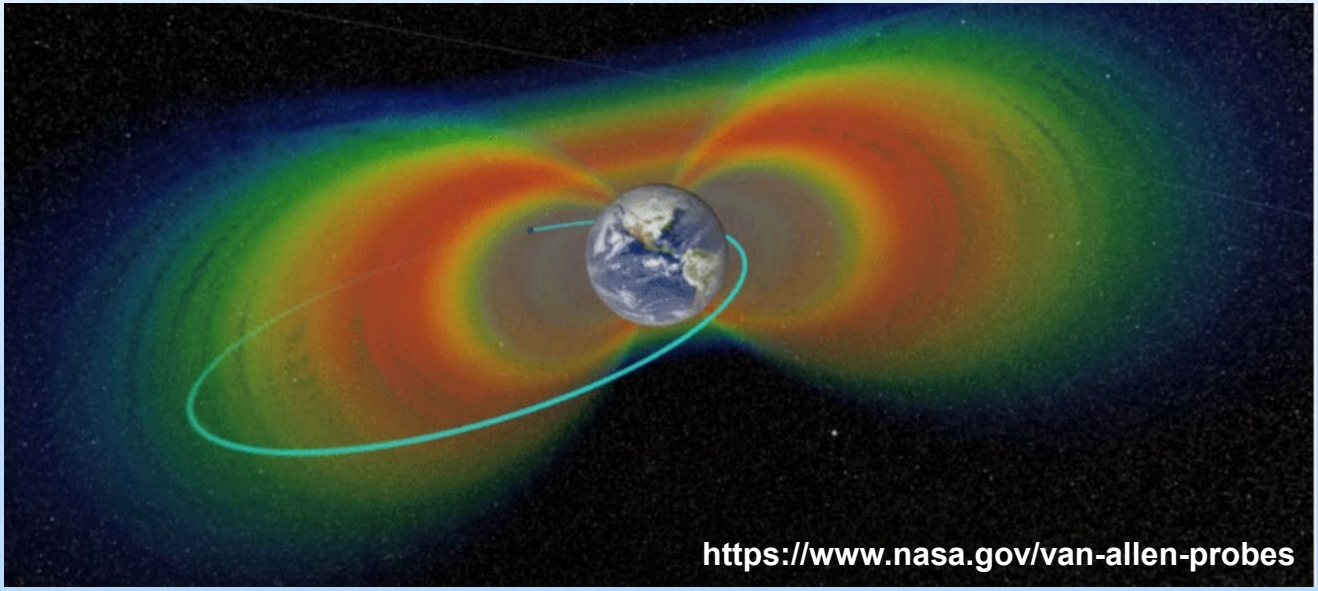
Terrestrial Effects – Energetic Particle Sources

- High-energy particles impact Earth's atmosphere and create air showers that generate a variety of particles (e.g., neutrons etc.) that reach ground level – fluxes are anisotropic
- Depends on latitude/longitude, atmospheric depth, and solar activity
- Process contamination in wafer fab materials
- Trace elements in packaging and in metallic (e.g., Pb) bumps
- ^{232}Th and ^{238}U are relatively abundant in terrestrial materials used in electronics processing and active enough to be a radiation effects concern



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Cosmic Rays

- Galactic Cosmic rays (GCR) are the most difficult to simulate on earth. GCR can have energies up to 1,020 eV, with a flux maximum at around 1 GeV/nucleon. For reasons of cost effectiveness and availability, the qualification tests on earth are done at accelerators with much lower energies, usually in the 10 MeV/nucleon range.
- In space, we tend to see a fall-off of particle energies over 30 MeVcm^2/mg (supernova limit), and as such tend to use this as a threshold for testing. However, heavy ion facilities can go much higher than this.
- Cosmic rays have enough energy in space to penetrate an entire satellite, but at ground testing we are often range limited to hundreds of microns.

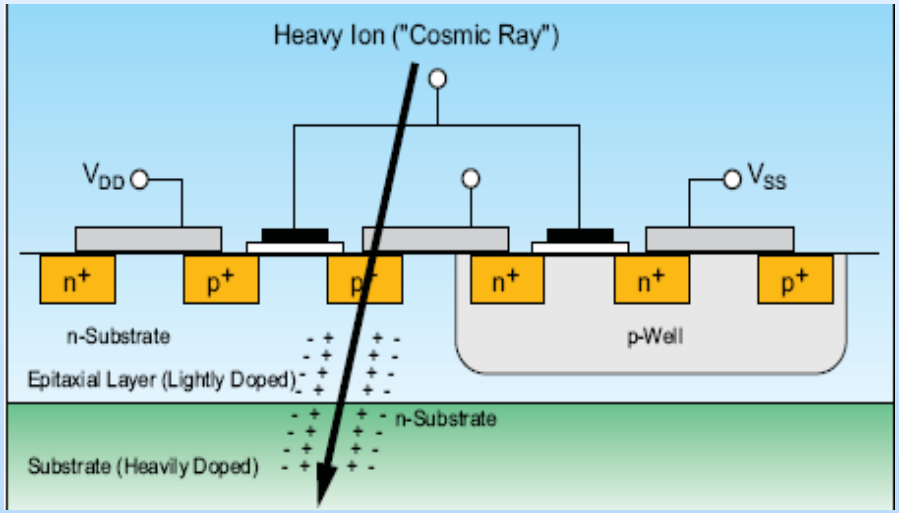
Linear Energy Transfer (LET)

- LET characterizes the deposition of charged particles
- LET is based on average energy loss per unit path length (stopping power)
- Density is used to normalize LET to the target material
- LET is the average energy deposited per unit path length
- We often use terms like charge column or charge cone to describe the particle path and results

$$LET = \frac{1}{\rho}\frac{dE}{dx} \qquad \left(MeV\frac{cm^2}{mg}\right)$$

Density of target material

Units



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Characterizing Single Event Upsets (SEU)

SEU Cross Sections (σ_{seu}) characterize how many upsets will occur based on ionizing particle exposure.

Cross Section at saturation measured LET (σ_{sat}) (cm^2/device, unless specified as cm^2/bit).

$$\sigma_{seu} = \frac{\#errors}{fluence}$$

Terminology:

- Flux (rate): Particles/(sec·cm^2)
- Fluence: Particles/cm^2
- σ_{seu} is calculated at several LET values

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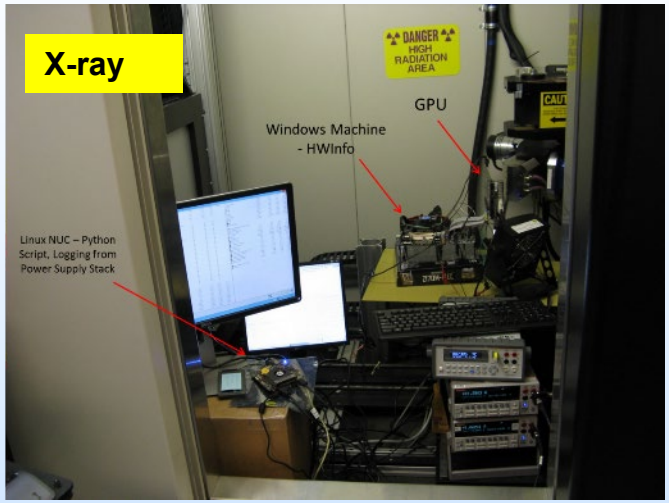
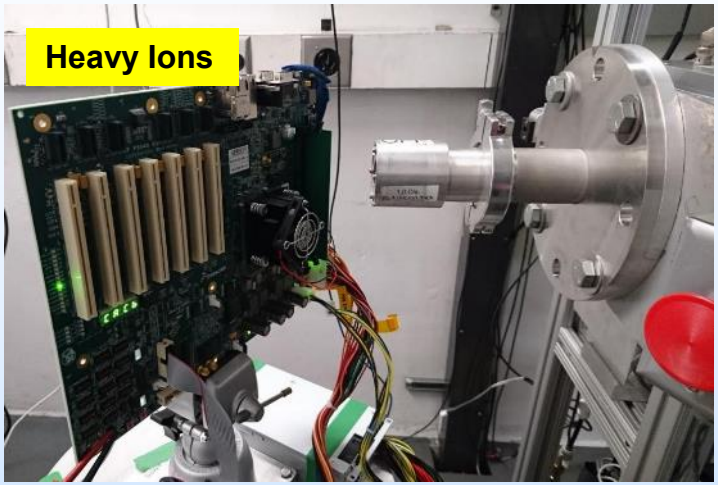
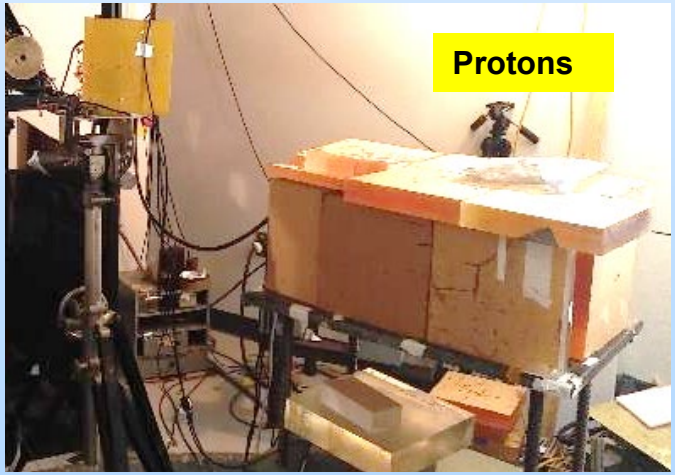
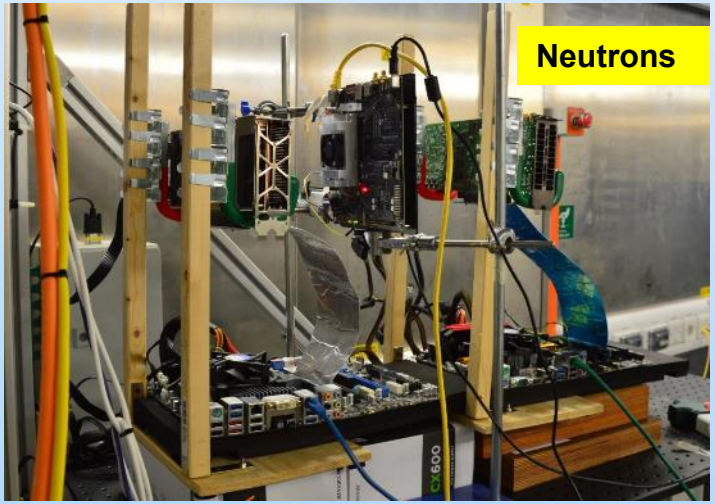
Facility Types

- X-ray, Heavy Ions, Neutrons, Protons
- Not shown: Electrons, Gamma, Two-Photon Laser absorption (TPA)









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Main Types of Radiation Tests

Heavy-ion testing

- Determine effects of different energy levels (Linear Energy Transfer, LET)
- If effects are apparent below 20 MeV•cm^2/mg, proton testing may be necessary
- Heavy Ion is good for SEU, SET, SEFI, SEL, SEGR, SEB

Proton testing

- Evaluates Single Event Effect (SEE) induced transients, Single Event Functional Interrupts (SEFIs), and accessible device power-states
- 200MeV protons generate secondary nuclear products with short range. Similar effects and energy deposition from 200MeV to 500MeV.
- Proton testing does not provide significant information on SEL or SEGR/SEB

Total Ionizing Dose (TID)

- X-ray Irradiators and Cobalt-60 gamma-rays are used as an analogous test source for simulating ~1 MeV protons and electrons.
- Characterizes parametric variations (step stress or in real time), and the long-term radiation effects on the device. Determines whether dose-rate sensitivity exists.

2-Photon Laser Testing

- Conventional setup at NRL for 1260 nm wavelengths have a Full Width at Half Maximum power (FWHM) spot size of ~1 micron.
- Pulsed laser testing could be useful for fault injection, but we can't correlate that to LET so it would be an auxiliary test.
- Identify any extra-sensitive areas in the active area such that the characteristics of any events can be later evaluated against those results.

Adapted from Edward Wyrwas' presentation from the 12th Space Computing Conference in Pasadena, CA. July 30 – August 1, 2019. STI DAA number 20190028690

Pros and Cons of Facility Types

Heavy-ion testing

- Requires decapsulation, often die thinning, and thermal relief (for HPC components)
- High LET, good range (<1mm), good coverage
- Best comparison to on-orbit performance

Proton testing

- Broad beam (~400cm^2) or collimated ~1-2cm^2
- Limited LET (<1 MeVcm^2/mg), dependent on secondary interactions up to 15 MeVcm^2/mg, but a broad distribution and limited amount at the high LET
- High accumulated dose, activation of test setup – especially metal heat sinks
- Simplest test preparation – protons can be focused through a few cm of material

Total Ionizing Dose (TID)

- Hard to isolate a single component
- Often requires large sample size, potentially lot and wafer dependent
- Dose rate is facility dependent but can be as low as a few mrad(Si)/second to many krad(Si)/second

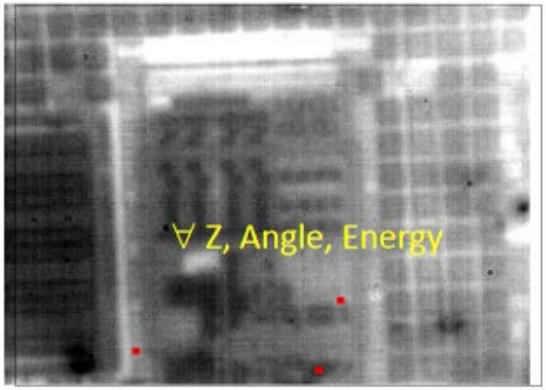
2-Photon Laser Testing

- Requires decapsulation, thinning and polishing
- Hard to draw direct comparisons to on-orbit performance
- Very focused energy deposition (1 micron) & visual localization of events

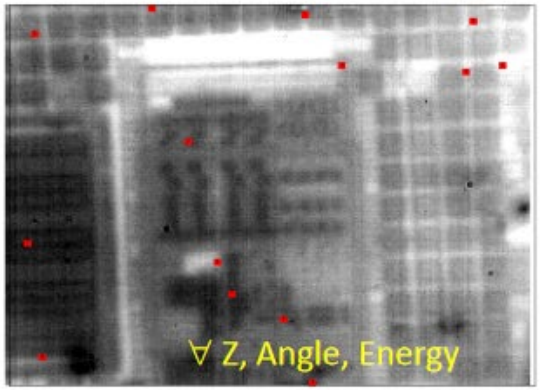
Adapted from Edward Wyrwas' presentation from the 12th Space Computing Conference in Pasadena, CA. July 30 – August 1, 2019. STI DAA number 20190028690

Coverage of Secondaries versus Heavy Ions

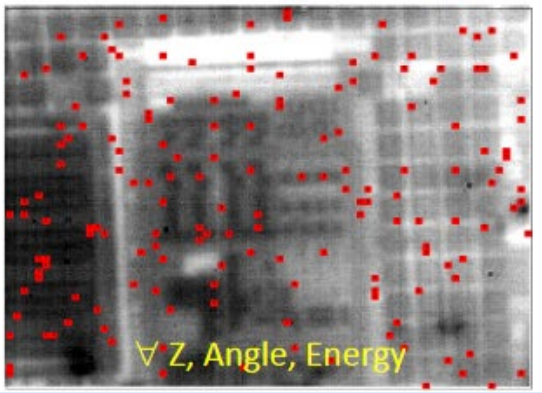
1E10 200 MeV protons/cm^2

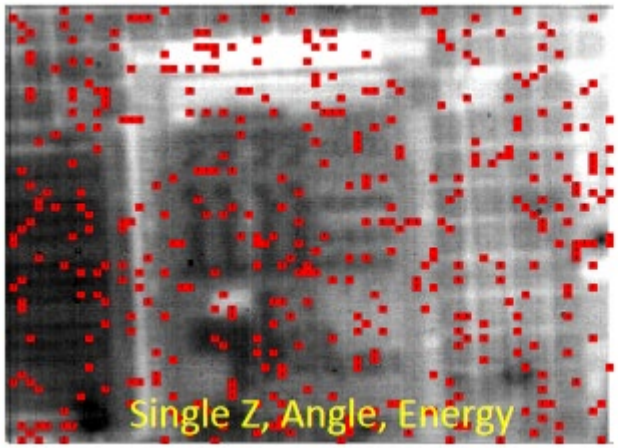


1E11 200 MeV protons/cm^2



1E12 200 MeV protons/cm^2





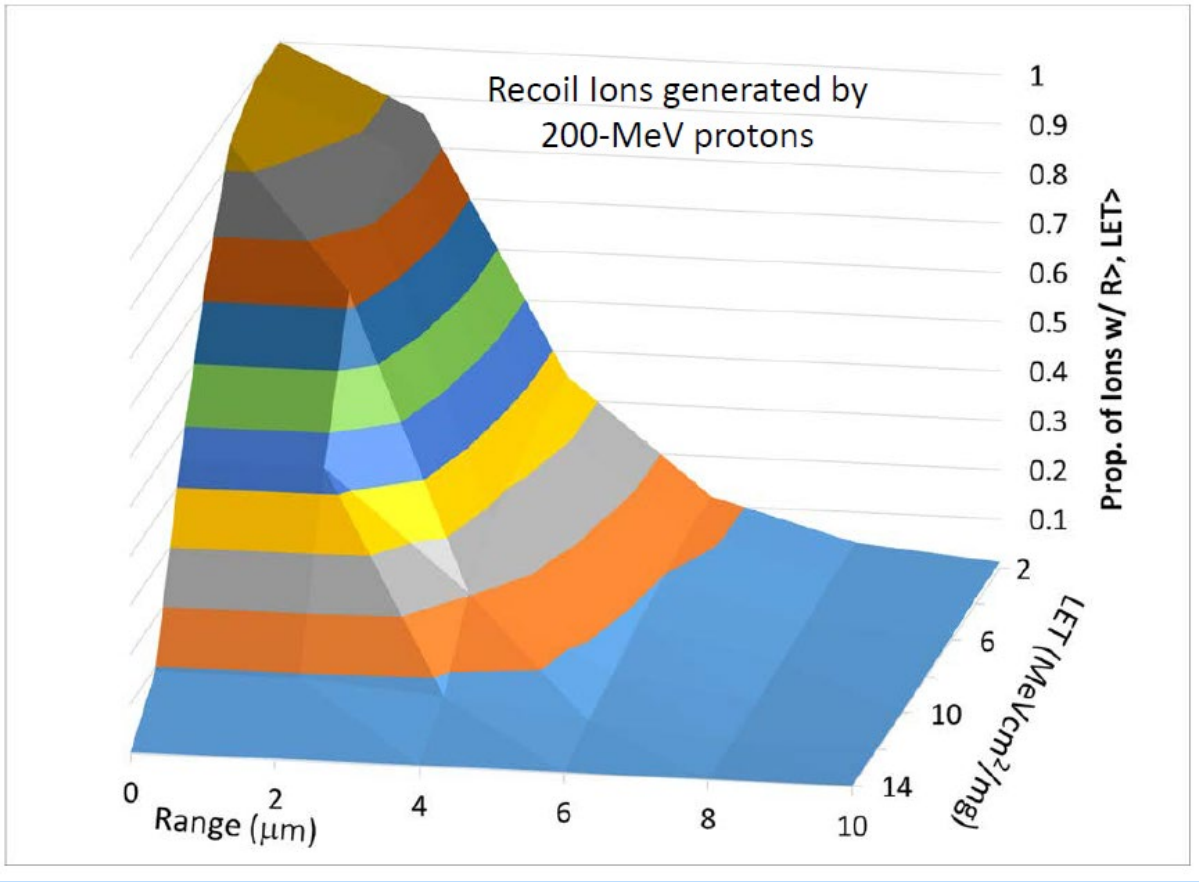
Coverage from 1E7 ions/cm^2 Heavy Ions

The takeaway here:

- Protons must induce secondary fission reactions within the materials in the die to cause a proper upset. For the same probability or quantity of upsets, it takes much fewer heavy ions than protons.
- While heavy ions cost more, they take less time to cause an error to occur. In testing, we want to induce errors – and capture that electrical behavior.

Another Perspective on Interactions

Prime Proton SEE Mechanism



Reaction of protons interacting with semiconductor materials causes secondary recoil ions – Indirect Ionization
Secondaries have various LETs and penetration ranges
Courtesy Ladbury/NASA

Radiation Effects, Literally

Radiation Effect	Displacement Damage Dose (DDD)	Total Ionizing Dose (TID)	Non-Destructive Single Event Effects (NDSEE)	Destructive Single Event Effects (DSEE)
Technologies Dominated by the Effect	Opto-electronics, Bipolar	Analog, CMOS, MOSFETs	All	All (e.g., CMOS→SEL, MOSFETs→SEB & SEGR)
Type of Effect	Cumulative (total particle fluences)	Cumulative (total particle fluences)	Instantaneous (one particle)	Instantaneous (one particle)
Why?	Damage cascades, disruption of the semiconductor lattice	Charge trapping (oxide/passivation/interface trapping especially)	Transient conditions: recombination and drift of charge carriers. Upsets that are persistent. Charge collection.	Semiconductor tolerances exceeded internally (current density, electric field strength, etc.)
What does that lead to?	Photonics and transparent material degradation	Threshold voltage shifts, leakage current	System and functionality drop-outs, some may require power cycle or reset	System and functionality failure
Radiation Source that Exhibits the Effects in an Isolated Fashion	Mid-energy protons (50-63 MeV p+)	Gamma source to create electron-hole pairs uniformly throughout the DUT	High energy protons or heavy ions for sufficient local charge deposition	Heavy ions
Other Sources that can also create the effect	Neutrons (difficult to count) or other energy protons (competing Coulombic interactions)	Protons, electrons, x-rays, heavy ions (physical coverage uniformity in question)	Protons, pulsed laser	Protons (competing with dose effects)

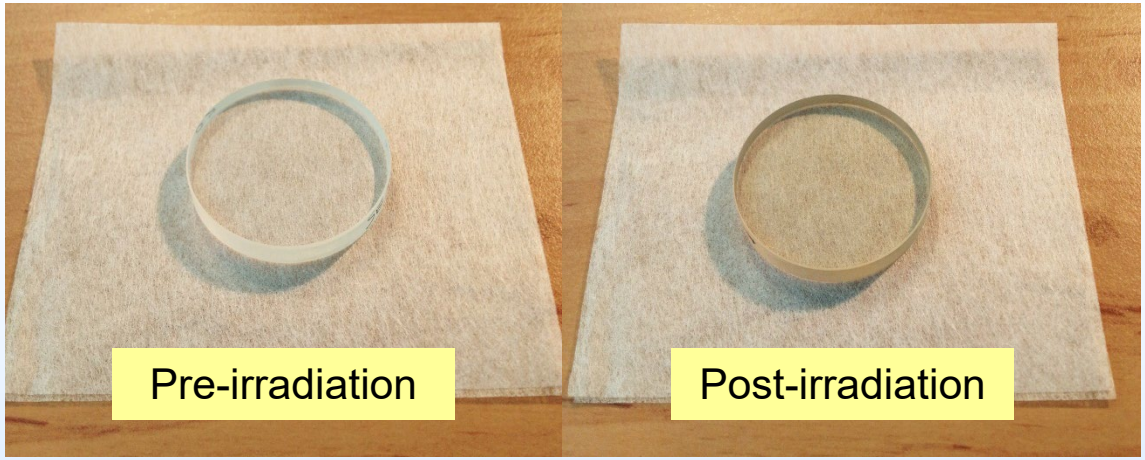
M. Campola (GSFC 561), Adapted from Avionics Radiation Hardness Assurance (RHA) Guidelines NASA TM−20210018053. Table 7.4-1. SEE Type Susceptibility of Various Technologies and Part Types. And Table 9.2-1. Driving Factors for Radiation Testing and Analysis Methodologies.

Dose Correlation

- Mid and high energy protons can be used to impart dose upon a collimated target when the electrical circuitry requires the dose to be isolated to a small area of the test vehicle. This cannot be achieved in a total ionizing dose (TID) irradiator. A test trial to reach these fluences is approximately 5 minutes. (The changes between the rows are noted)
  - 1×10^{11} protons/cm^2 at 200 MeV would deposit ~600 rad(Si) of dose
  - 1×10^{10} protons/cm^2 at 200 MeV would deposit ~450 rad(Si) of dose
  - 1×10^{10} protons/cm^2 at 63 MeV would deposit ~2000 rad(Si) of dose
- TID irradiation is based on dose rate which is controlled by physical proximity to the source and thickness of Pb/Al shielding.
  - TID testing can take a range of time -- dose rates of 50-300rad(Si)/s for CMOS and Bipolar, and <.01rad(Si)/s for bipolar are standard

Adapted from Edward Wyrwas' ISSI IS46DR16640B-25DBA25 DDR2 SDRAM Total Ionizing Dose Characterization Test Report. STI DAA number 20190001289

Material Degradation

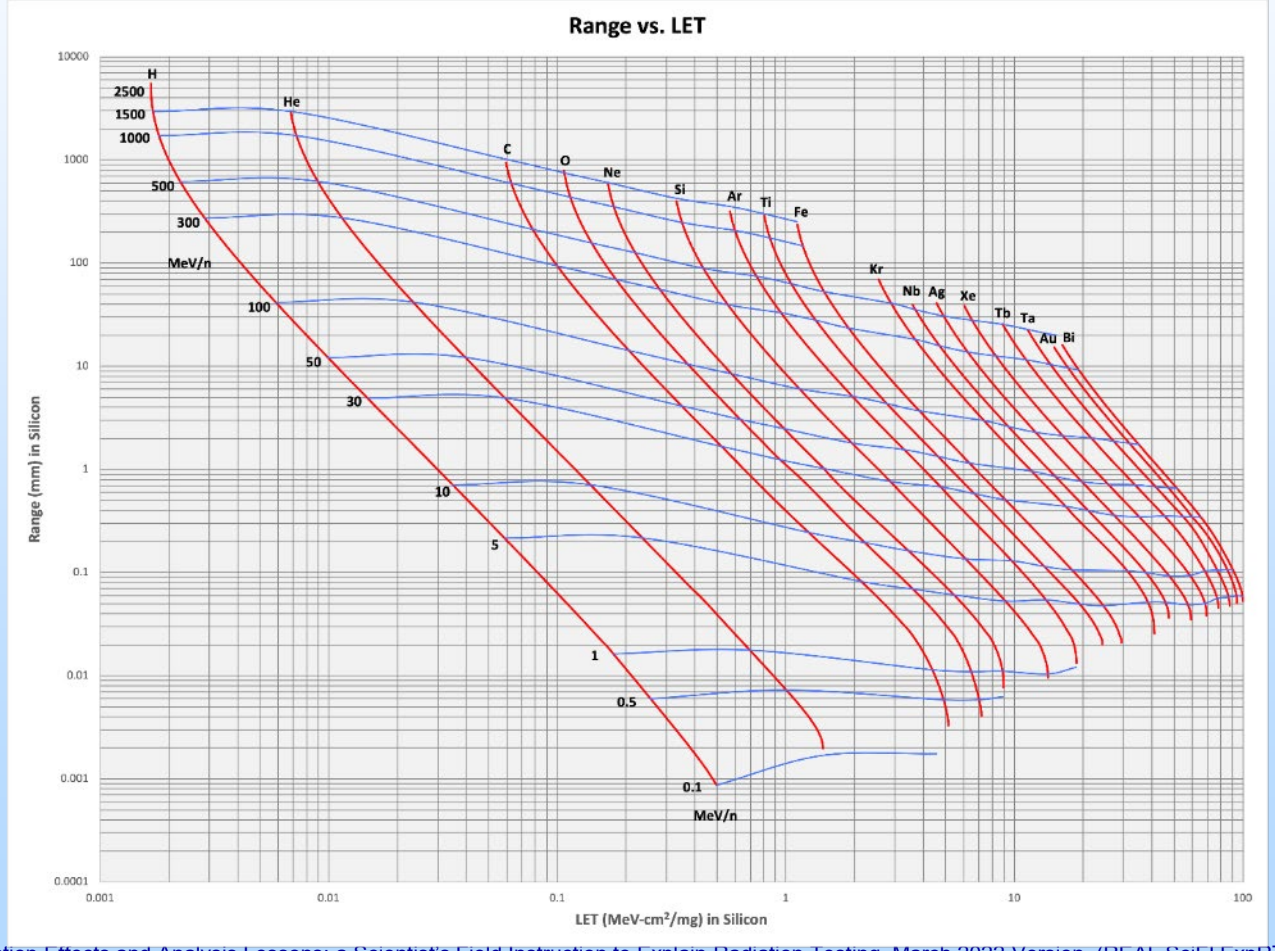


- Transparent materials darken; Materials become brittle; Materials absorb charge
  - Example shown are glass discs from the ESA RADGLASS study
- Displacement damage is due to cumulative long-term non-ionizing damage from the ionizing radiations. The collision between an incoming particle and a lattice atom subsequently displaces the atom from its original lattice position.
- In complimentary metal-oxide semiconductor (CMOS) devices, oxide interface traps generated by ionizing radiation, cause the threshold voltage of the transistor to shift left, effectively turning on N-type and turning off P-type transistors.

High resolution images and reuse permission received from Ilias Manolis of ESA (Netherlands) and the ESA RADGLASS study.

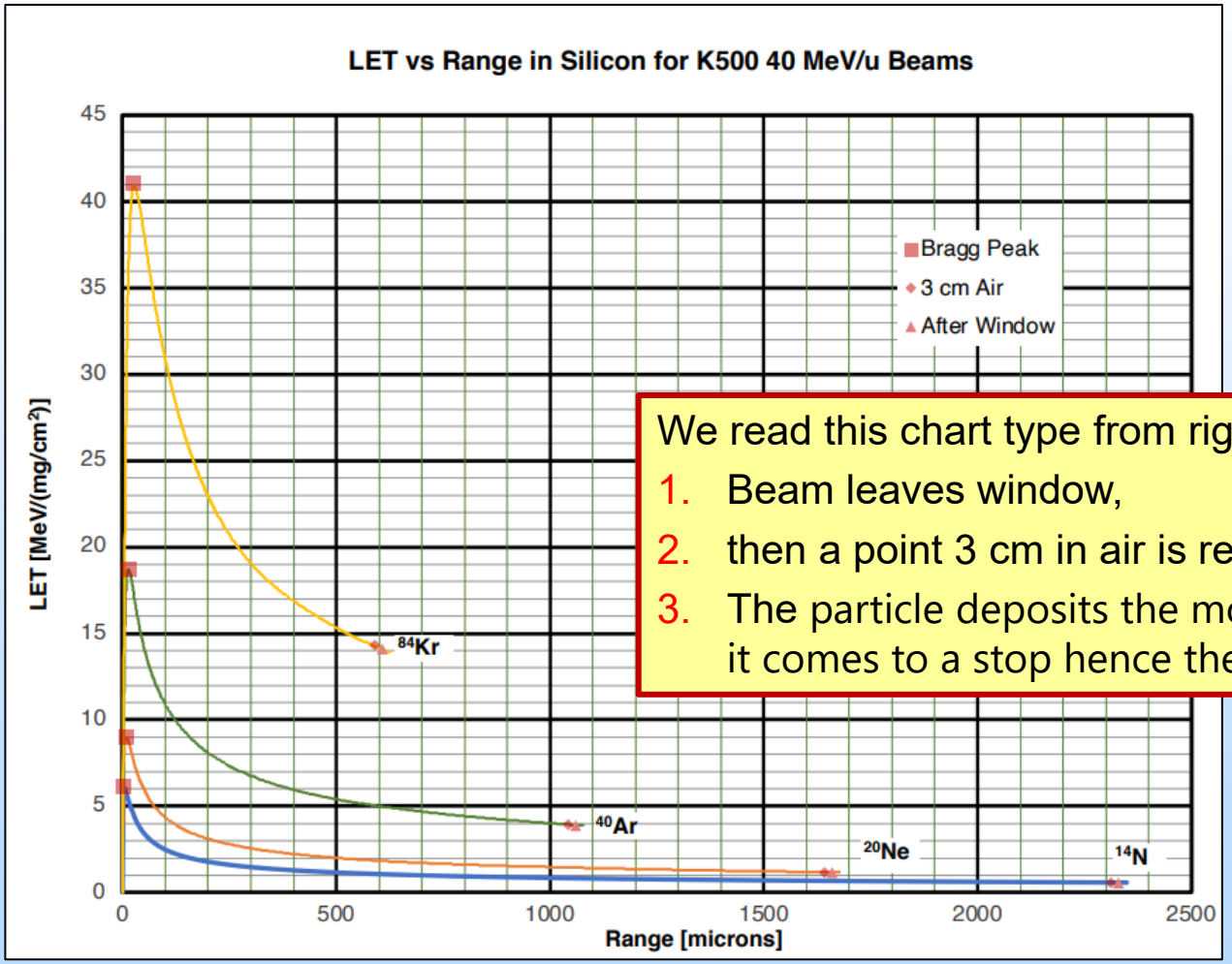
Line of Sight and Range

- When die are thinned, we reduce the amount of material to which the particles travel through before they reach the sensitive volume
- Energy deposition and material stack-up calculations are performed using simulation software to determine the ranges of heavy ion particle types to see if they will reach the intended volume.
  - NASA Space Radiation Laboratory's (NSRL) Stopping and Range of Ions in Matter (SRIM) calculator



Limited Range Constraints

- Texas A&M University's Cyclotron – "Air testing".



We read this chart type from right to left:

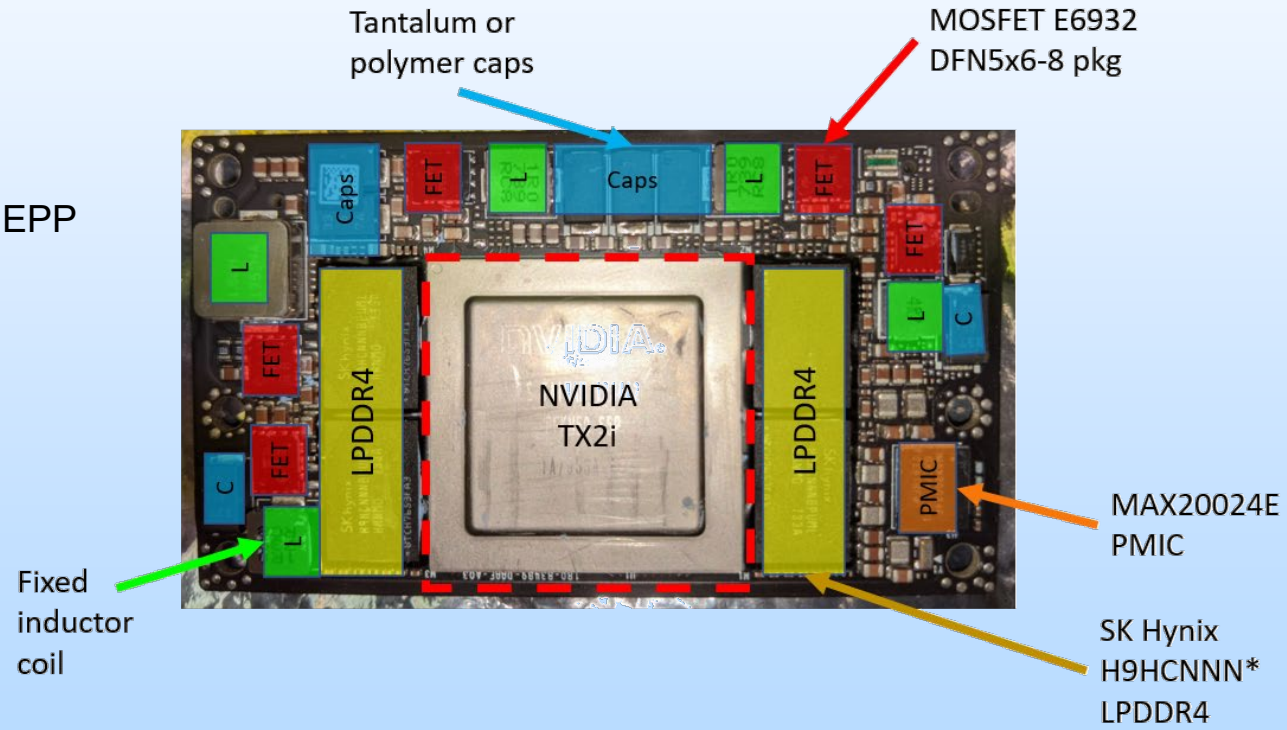
1. Beam leaves window,
2. then a point 3 cm in air is reached.
3. The particle deposits the most energy as it comes to a stop hence the Bragg peak.

Image reuse permission received from Dr. Henry L. Clark, Ph.D. Cyclotron Institute. Texas A&M University College Station, TX 77843.

Spallation Concerns

- There is scattering that happens along the perimeter of the beam outline due to the collimator and from the collisions of the particles on the metallization. This is the biggest issue for proton testing.
- Instances of spallation increase as you go up in energy. It can be caused by species dependent features close to sensitive volume such as tungsten plugs.

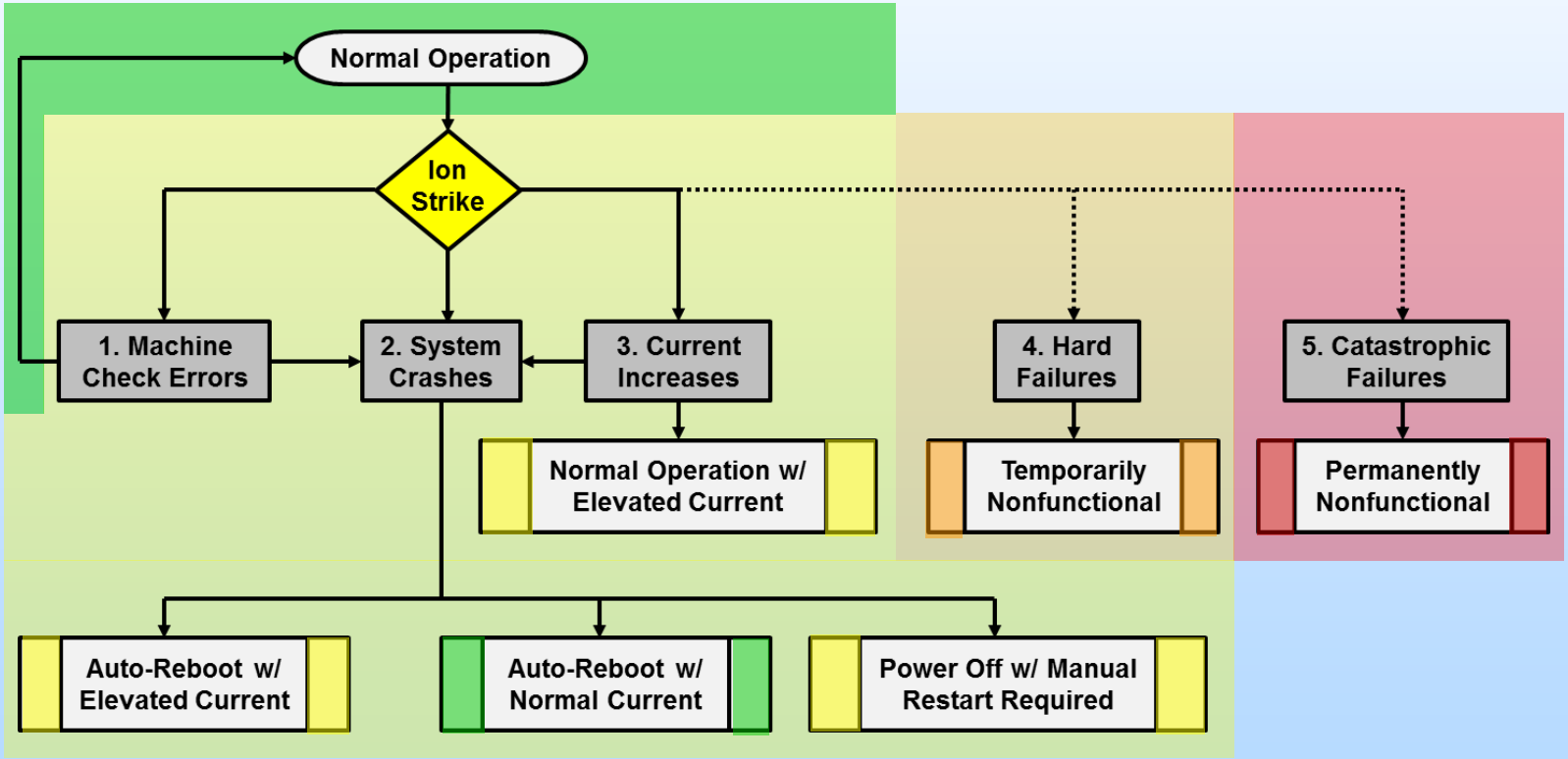
Image courtesy of NEPP



The small tan, gray and black rectangles which dominant the board real estate are ceramic capacitors, film resistors and ferrite beads (mostly radiation immune)

Test Flow & Fault Tree

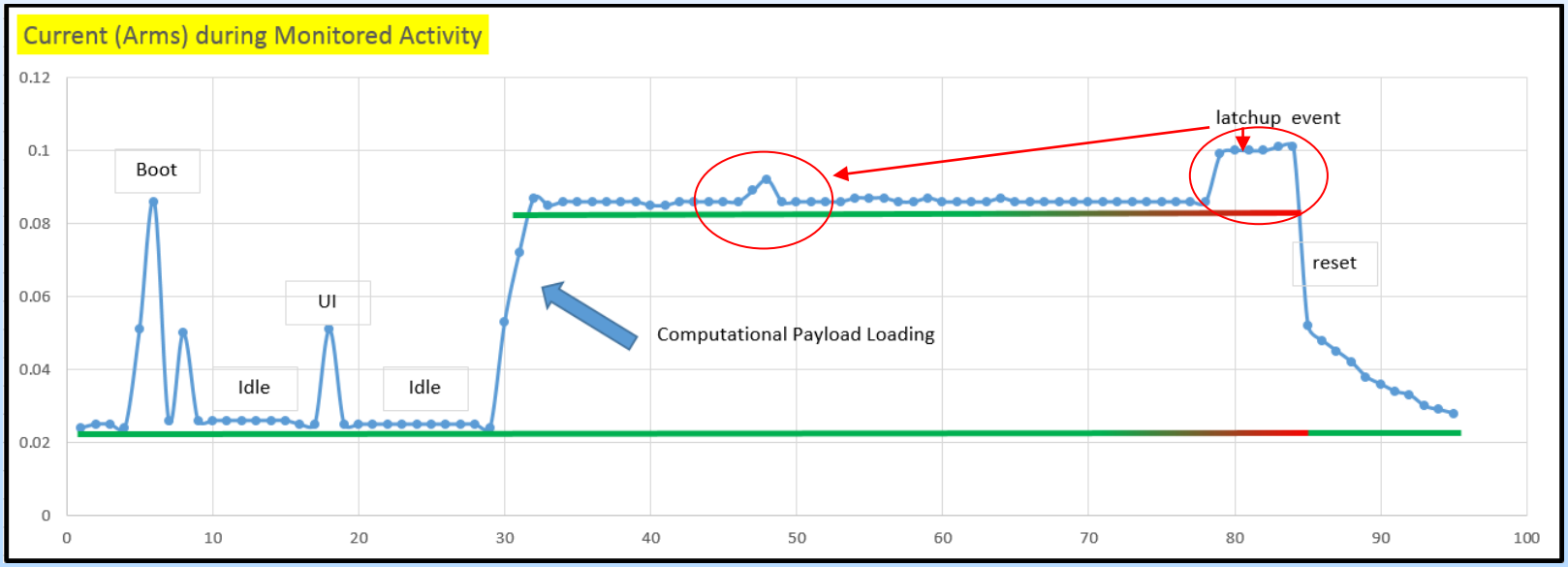
- These qualitative bins are how we attempt to classify error signatures recorded during testing.
- A disturbance is not the same as an upset. There are recoverable errors, much like there are unrecoverable ones.



Adapted from Edward Wyrwas' presentation from the 12th Space Computing Conference in Pasadena, CA. July 30 – August 1, 2019. STI DAA number 20190028690

Identifying Patterns to Create Mitigation Solutions

- If we can identify an electrical behavior which indicates particle collisions are happening, then we can abort a computational routine to save the science payload or isolate the component in question.
  - For the NVIDIA TX2, we can simply monitor current consumption against a threshold. When that threshold is exceeded, we disregard the current computation, reset the system to prevent bad data, and avoid a system crash.

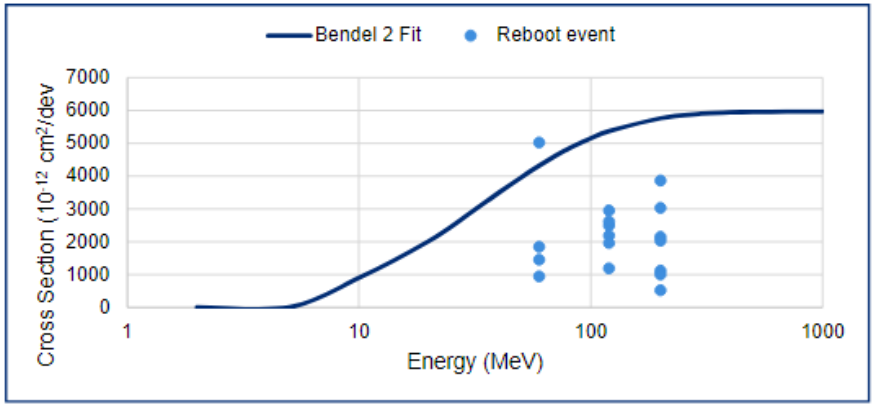


Adapted from Edward Wyrwas' presentation from the 12th Space Computing Conference in Pasadena, CA. July 30 – August 1, 2019. STI DAA number 20190028690

Data Analysis

- We record:
  - the elapsed time (seconds)
  - at a given flux (known particles per second per unit area)
  - to determine the fluence (total quantity of particles delivered during the irradiation time per unit area)
- We simply count the errors and do some algebra – we plot cross section of each test trial. If we tested at different energies, a polynomial would emerge.
- We try to delineate between failure types – some failures may not be attributed to the component we are actually testing and are otherwise due to peripheral circuitry and bus controllers.
- If we are able to evaluate using different energy levels, then we can statistically plot the data to a Weibull or Bendel function and extract the statistical parameters.
- We than use Monte Carlo simulation software to do the mathematical correlation between test conditions and orbit conditions.

TX2i ID	Proton energies (MeV)	Total Fluence	Flux
200	60	1.95E9	4.3E6 - 4.7E6
201	60 and 120	2.25E9	2.1E6 – 9.9E6
202	120 and 200	2.23E9	4.0E6 – 7.2E6
203	200	4.37E9	3.5E6 – 9.0E6



Bendel 2 Parameters	
B = 2.81	A = 1.51

NVIDIA TX2i 200MeV Proton Data

Correlation from Test to Environment

- We use tools, such as CREME-96 hosted by Vanderbilt, to predict environmental conditions based on modelled data, and estimate single-event effect rate by incorporating experimental results from ground-based testing.
- These tools contain historical orbital data for radiation exposure at various inclinations and altitudes to predict single event effects rates
- In many cases, we consider four (4) scenarios which bound the worst cases of solar proton events (SPE) and galactic cosmic rays (GCR) [tabulated on the right] and use a shielding thickness of 100mil of Al for unmanned satellites

1	Trapped Proton Min	
	Quiet Weather (Wost GCR)	
	Solar Min - Trapped Proton Min	
	Solar Max - Trapped Proton Min	
	Worst Week - Trapped Proton Min	7.5 days
	Worst Day - Trapped Proton Min	18 hours
	Worst 5 minutes - Trapped Proton Min	5 minutes
2	Trapped Proton Min	
	Stormy Weather (Worst SPE)	
	Solar Min - Trapped Proton Min	
	Solar Max - Trapped Proton Min	
	Worst Week - Trapped Proton Min	7.5 days
	Worst Day - Trapped Proton Min	18 hours
	Worst 5 minutes - Trapped Proton Min	5 minutes
3	Trapped Proton Max	
	Quiet Weather (Wost GCR)	
	Solar Min - Trapped Proton Max	
	Solar Max - Trapped Proton Max	
	Worst Week - Trapped Proton Max	7.5 days
	Worst Day - Trapped Proton Max	18 hours
	Worst 5 minutes - Trapped Proton Max	5 minutes
4	Trapped Proton Max	
	Stormy Weather (Worst SPE)	
	Solar Min - Trapped Proton Max	
	Solar Max - Trapped Proton Max	
	Worst Week - Trapped Proton Max	7.5 days
	Worst Day - Trapped Proton Max	18 hours
	Worst 5 minutes - Trapped Proton Max	5 minutes

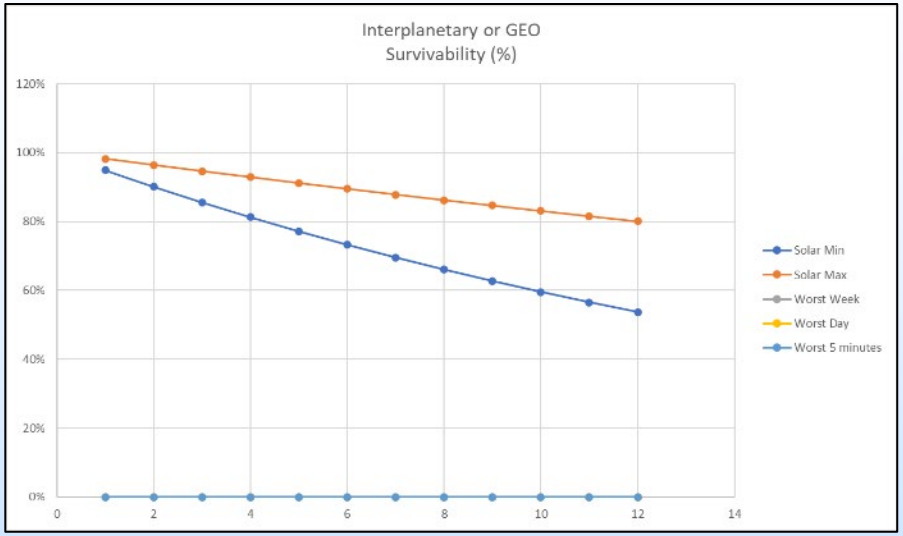
https://creme.isde.vanderbilt.edu/

The Difficulty with Models

- Models may not be fully applicable for a given device architecture.
  In fact, they usually aren't applicable, but can be used to approximate.
- Hard to isolate architecture versus process related problems
- Models only cover what we know about, they never cover the phenomenon we don't know about or have not measured yet
- Every NASA vehicle has new technology. We build prototypes and test the heck out of flight designs. When technologies have been used previously, we can draw some early conclusions based on similarity.
- Error bars and confidence levels
  - Our radiation cross section results are only a slice of statistics – the system must consider the mountain of uncertainty
  - Each piece of the circuit hierarchy and system topology come with their own error bars and confidence levels
  - Risk is a statistical value
  - Rate (i.e., survivability rate) is with error bars
  - There is never one singular value that represents the reliability of a device. Time and many other conditions are always counted.

Vanderbilt CRÈME-96

- The following is a rather crude approximation of this statistical methodology:
  - When devices have quantifiable components, where we fully understand the physical relationship between transistor layout and the bytes they affect, we can determine an on-orbit single event effects rate per bit.
  - When we are testing a black-box component we must consider the entire sensitive volume as 1 bit.
  - For Bendel parameters 1.51 and 2.81, we achieve the following results from CRÈME-96.



						Survivability at Quantity of days (Quarter Breakdown shown)											
	SEE/bit/ day	# of bits / device	SEE/dev/ day	SEE/bit/ Total	SEE/dev/ Total	1	2	3	4	5	6	7	8	9	10	11	12
Solar Min	2.27E-03	1	2.27E-03			95%	90%	86%	81%	77%	73%	70%	66%	63%	60%	57%	54%
Solar Max	8.12E-04	1	8.12E-04			98%	96%	95%	93%	91%	89%	88%	86%	85%	83%	82%	80%
Worst Week	2.42483	1	2.42483	1.82E+01	1.82E+01	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Worst Day	1.01E+01	1	1.01E+01	7.55E+00	7.55E+00	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Worst 5 minutes	3.70E+01	1	3.70E+01			0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%

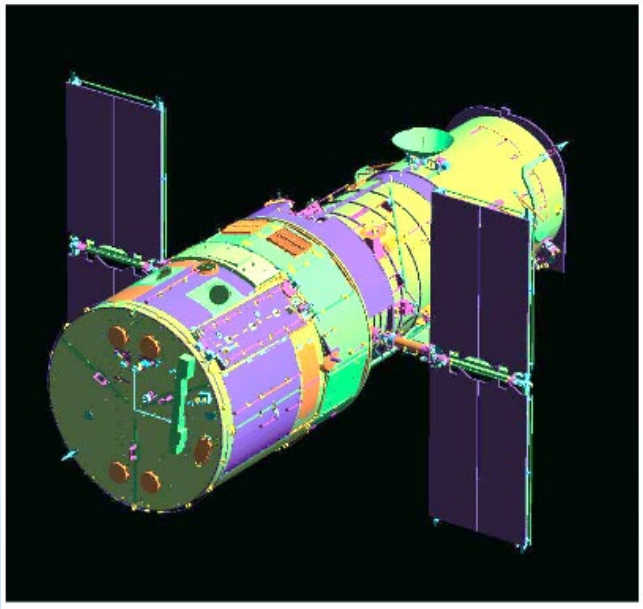
$$Survivability = e^{(-\text{rate per day} * time\ in\ days)}$$

NOVICE Transport Models

Experimental & Mathematical Physics Consultant's (EPMC) NOVICE is the leading software suite for space systems radiation effects. It is, and has been for decades, a mission-critical part of satellite and deep space probe programs.

1. NOVICE is a radiation transport code that allows complex shielding geometry to be accounted for through the use of CAD file input
2. It allows total ionizing dose (TID) and Total Non-Ionizing Dose (TNID) to be calculated for specific points within instruments and spacecraft
3. It provides improved TID and TNID **requirements** compared to dose-depth curves.

https://empc.com/novice-software/



Hubble Space Telescope NOVICE CAD model

Adapted from M. Xapsos. How Long can the Hubble Space Telescope Operate Reliably? – A Total Dose Perspective. STI Document number 20160005759 and How Long Can the Hubble Space Telescope Operate Reliably?. STI Document number 20140017805.

But Aren't There Rules of Thumb?

- There are many variations in manufacturing
  - Equipment calibration, room conditions, mask set age, foundry staff
  - Substrate changes – Bulk Si, Silicon on Insulator (SOI)
  - Conductor changes – Al, Cu, Ag, Au, W, Alloys
  - Dielectric changes – SiO_2, low-k (e.g., polyamide, air), high-k (i.e., hafnium based)
  - Gate Geometry changes – planar, fin, gate all around
  - Lithography sizes scaling smaller
- When we test parts, we try to procure enough components to achieve a small statistical bin to capture the smallest amount of variance – preferably to an individual Lot Date Code (LDC).
- For every example of a 'rule', someone in the radiation effects community can offer a counter example. There are far too many to list.
- Because of all these factors, there are No Rules of Thumb.
  - However, we have seen some trends between generations of specific (AKA "the same") architectures when manufactures make singular process changes (e.g., shrink pattern by 30%, lower the voltage by 10%, same design but two different substrates)

Trends and Opinions, Not Rules

- Bipolar and Analog devices have known circuit breakdown behavior and tend to be more susceptible to radiation effects than modern scaled CMOS devices; though CMOS *does* have Latchup and total dose concerns
- CMOS devices smaller than 150nm feature size are an increased risk of SEE due to transistor threshold voltages and cell sizes being smaller
  - Was true until transistor geometry changed (planar vs fin vs column)
- There is not a voltage sweet spot for current consumption, supply voltages, or bias voltages – nor can we compare two different manufacturers in a single device category
- When electrical derating isn't possible because of the complexity of the device type (i.e., microprocessor), testing must evaluate the device as close to flight-like as possible from a standpoint of computational operation and memory access patterns
  - To assure the 'state machine' has been thoroughly explored
  - To assure we can see what pieces of the software workflow or program routine can successfully complete, can identify or capture errors, and handle interrupts
  - So that we can put together a plan to mitigate some, or all the negative effects imparted by the radiation

Similar Experiences

- Ceramic capacitors found on many High-Performance Computing (HPC) devices
- Ceramic capacitor packages used on flight hardware are rarely smaller than *0805* (SI) / *2012* (metric) sizes (2.0mm x 1.2mm) due to their dense plates and high capacitances
- Radiation Induced Charge Loss
  - During radiation, the capacitor leakage resistance decreases. Therefore, the time constant of the circuit will also decrease. If the capacitor is in a critical timing circuit, the timing circuit may produce errors that affect system performance.
- Radiation Induced Conductance
  - The amount of radiation-induced conductivity (RIC) can vary widely with dielectric material type.
  - For a dielectric (insulator) the band gap is large relative to room temperature thermal energies, the valence band is full, and the conduction band is empty. This leaves no electrons available to participate in the conduction process. However, **in the presence of ionizing radiation** where the energy from the radiation that can be imparted to an electron exceeds that of the band gap, an electron may transition to the conduction band and electrical conduction will take place. This **can cause a catastrophic short circuit depending on the electrode spacing within the component**.

Adapted from Edward Wyrwas' Body of Knowledge for Graphics Processing Units (GPUs). STI Document number 20180006915.

Old Trends, Far From Rules

- Silicon substrate changes: An evaluation of 45nm SOI multi-core processors has been conducted by university researchers from France. They compare their work to 45nm bulk silicon multi-core processors. In these tests, a 3-5X improvement to SEE immunity is seen when switching from bulk silicon to silicon on insulator for the same technology node.
  - Pabo Ramos, Vanessa Vargas, M. Baylac, F. Villa, S. Rey, et al.. Evaluating the SEE sensitivity of a 45nm SOI Multi-core Processor due to 14 MeV Neutrons. IEEE Transactions on Nuclear Science, Institute of Electrical and Electronics Engineers, 2016, 63 (4), pp.2193 - 2200. <10.1109/TNS.2016.2537643>. <hal-01280648>
  - S.S. Stolt and E. Normand, “A Multicore Server SEE Cross Section Model,” IEEE Trans. Nucl. Sci., vol. 59, pp. 2803–2810, Dec. 2012.

- Voltage scaling accompanied with feature size scaling reduces the critical charge required to flip a bit. This allows even lower-energy particles to cause soft errors. Due to these reasons, soft-error rate at 16nm is expected to be more than 100X than that at 180nm
  - S. Mittal et al., “A Survey of Techniques for Modeling and Improving Reliability of Computing Systems,” IEEE TPDS, 2015.

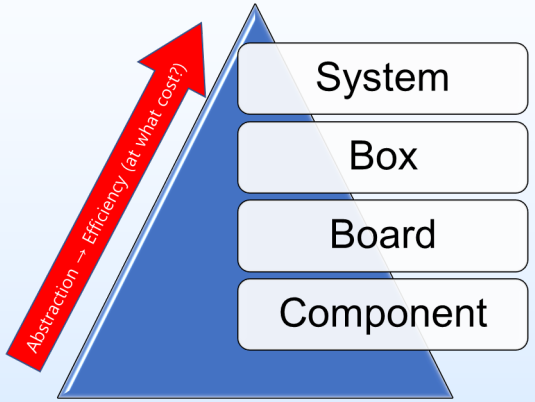
- Zhang et al. characterized soft error vulnerabilities across the stacked layers under 3D integration technology. They show that the outer dies can shield more than 90% particle strikes for the inner dies, which leads to a heterogeneous error rate across layers in a 3D chip.
  - W. Zhang et al., “Microarchitecture soft error vulnerability characterization and mitigation under 3D integration technology,” in International Symposium on Microarchitecture, 2008, pp. 435–446.

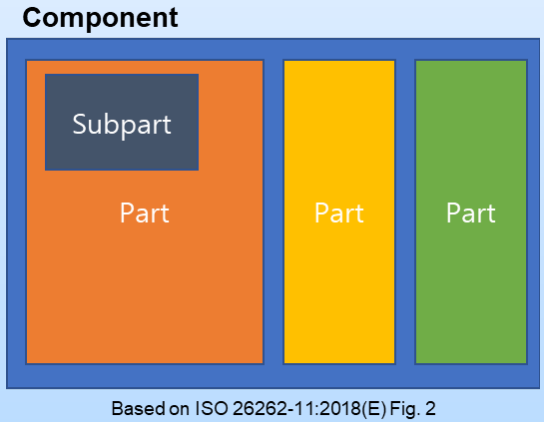
Understanding Risk

- A satellite has independent systems. The requirement of Avionics systems is to function and survive during the mission. It isn't checking in with the science payload and won't reset these systems 'along the way'.
  - Paraphrased from NEPP Processor Enclave teleconference 1/21/2022
- Historical data may not be related and therefore should not be considered as providing radiation assurance. This includes previous testing with neutrons, model correlations from different orbits, components with slightly different architectures, component generations with different lithography nodes.
- Extensive testing should always be performed to reduce risk.
- Questions should arise from testing:
  - Will the component meet its primary mission objective, aka will it still be functioning when it reaches its first rendezvous to do its activity? Are we able to fly powered off to extend survivability?
  - Will redundancy improve the survivability of the system?
  - What did we determine from the test results? Did we learn anything new? Are we able to quantify the unknowns?
  - Are we able to correlate the device's intended usage in a flight system to how we performed our test? (i.e., software applications and memory utilization)

What Did We Learn?

- No rules of thumb in radiation effects
  - There are too many variables and manufacturing variations to have one standard model at any granularity in our abstraction diagrams
  - Through a campaign of lot-based testing, we can characterize the radiation tolerance of high-performance computing (HPC) and artificial intelligence (AI) devices with a high degree of confidence.
  - We use best practices and the knowledge of our entire radiation effects community to reduce risk associated with flying SOTA computational devices which subsequently improves mission assurance.





Based on ISO 26262-11:2018(E) Fig. 2

Fin

- This work was sponsored by:
  - NASA Electronic Parts and Packaging (NEPP) Program
  - GSFC Radiation Effects and Analysis Group (REAG), Code 561

- Acknowledgements:
  - Peter Majewicz (GSFC, NEPP)
  - Jonny Pellish (GSFC, NEPP)
  - Michael Campola (GSFC, 561)
  - Ray Ladbury (GSFC, 561)
  - Ted Wilcox (GSFC, 561)
  - Megan Casey (GSFC, 561)
  - Jean-Marie Lauenstein (GSFC, 561)
  - Jason Osheroff (GSFC, 561)
  - Landen Ryder (GSFC, 561)
  - Alyson Topper (GSFC 561, SSAI)
  - Ken LaBel (GSFC 561, SSAI)
  - Martha Obryan (GSFC 561, SSAI)
  - Mike Xapsos (GSFC 561)
  - Steve Guertin (JPL, NEPP)
  - Doug Sheldon (JPL, NEPP)
  - Glen Steele (JSC)
  - Richard Alena (ARC)
  - Mike Lowry (ARC)
  - Eli Kawam (Microchip Technology)
  - Ian Troxel (Troxel Aerospace)
  - Mitra Yoonessi (Raytheon Technologies)
  - Eric Miller (The Boeing Company)