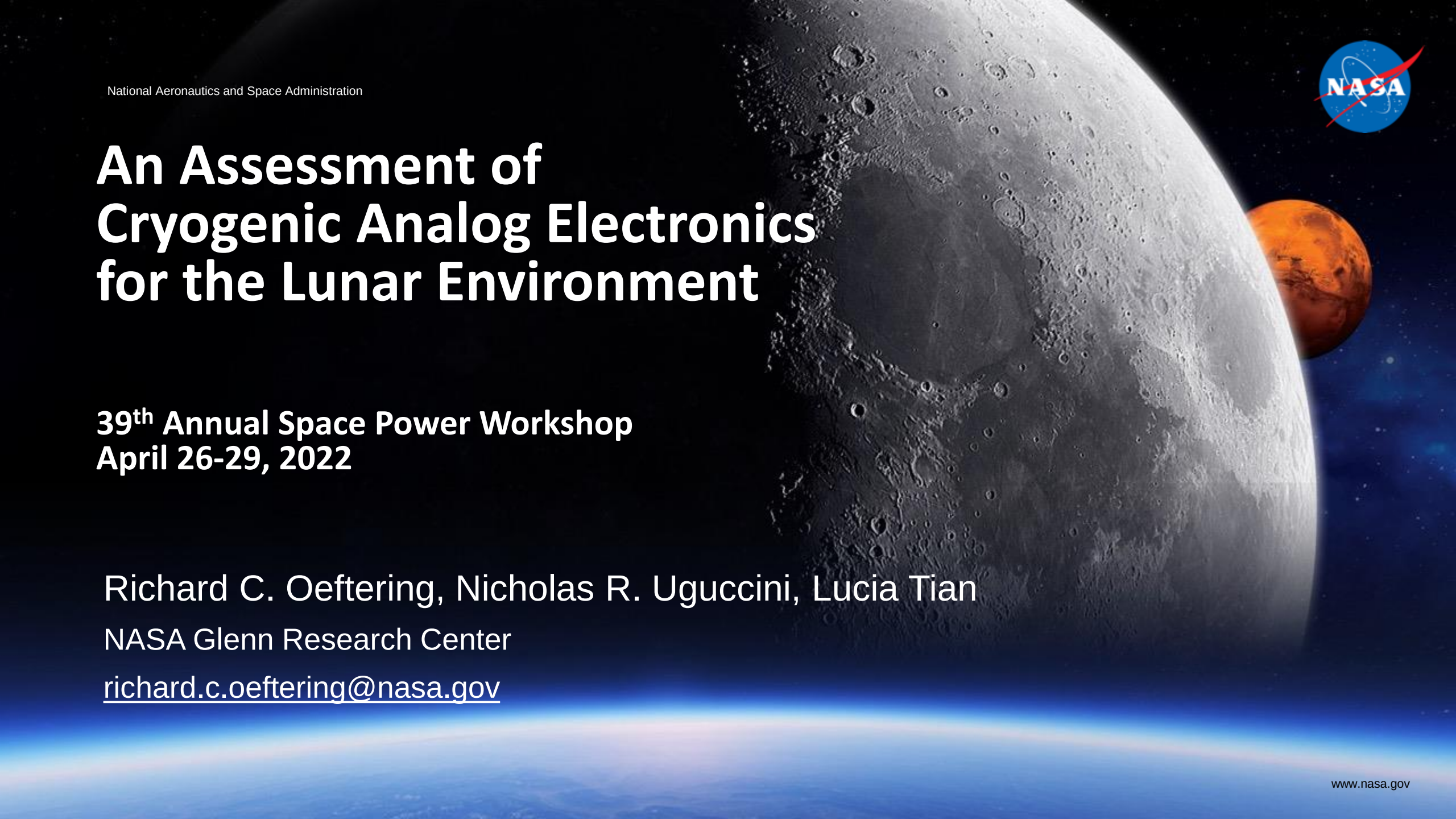
National Aeronautics and Space Administration



An Assessment of Cryogenic Analog Electronics for the Lunar Environment

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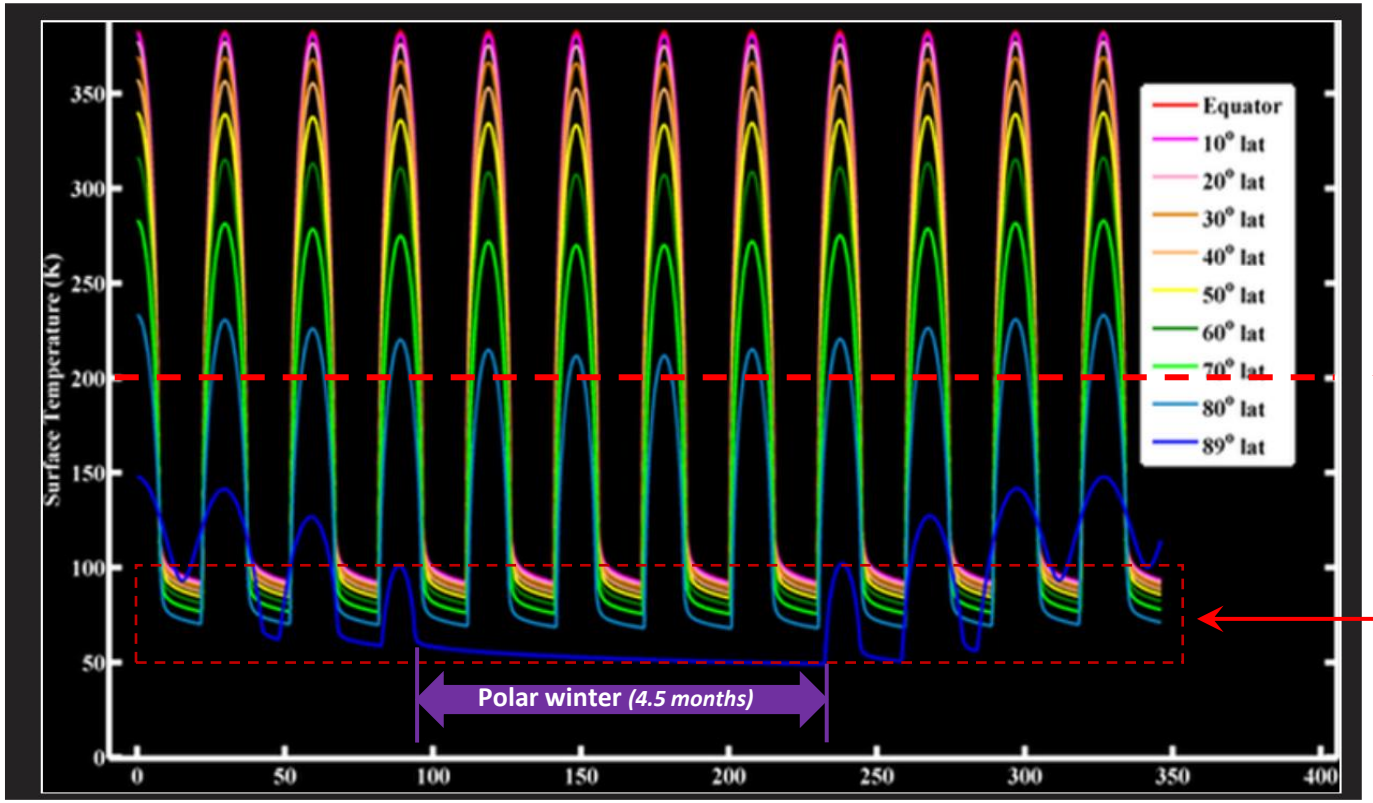
Background
The Extreme Lunar Environment

LRO DIVINER: Lunar Day/Night Temperature Range by Latitude



- Day: 100-400 K highs based on latitude
- Night: 50-100 K lows for *all* latitudes
  - Duration (non-polar): ~354 hrs (~15 Earth days)
  - Duration (polar): winter sun below horizon for ~4.5 months

Li-ion battery approx. freeze temperature

Lunar night is extremely cold *everywhere*

Thermal model calculations of monthly & annual lunar surface temperature variations at various latitudes

Image permissions per Dr. N Petro/NASA GSFC, Dr. D Paige/UCLA

Background
Proposed Survival Strategy

- **Lunar Power Hibernation**
  - Extends capabilities & duration of lunar missions
  - Reduces dependency on radioisotopes, pre-established infrastructure
  - Success depends on
    - Cryo-tolerant Li-ion batteries: 18650 cells survive lunar night conditions
    - Cryo-tolerant electronics (majority of electronics passively survive)
    - Cryo-operable electronics to perform cold start and safely restore power
- **Hibernation Applications**
  - Commercial Lunar Payload Services (CLPS)
    - Landers currently provide only a single lunar day of operation
  - Robotic elements of the Artemis Program
  - Lunar *in situ* resource utilization (ISRU) systems
  - Survival & recovery options in contingency situations

Background
Hibernation Electronics Definitions

- **Cryo-Tolerant**
  - Required for all spacecraft electronics (power, avionics, comm)
  - Must passively withstand thermal environment down to 50 K without damage
  - Can depend on manufacturing processes & materials/packaging

- **Cryo-Operable**
  - Required for hibernation electronics that restore power at lunar dawn
  - Must start up and operate in 50-100 K lunar dawn
  - Depends on device properties & stability of interactions

Background
Example Dawn Start-Up Sequence

Key

Cryo-tolerant

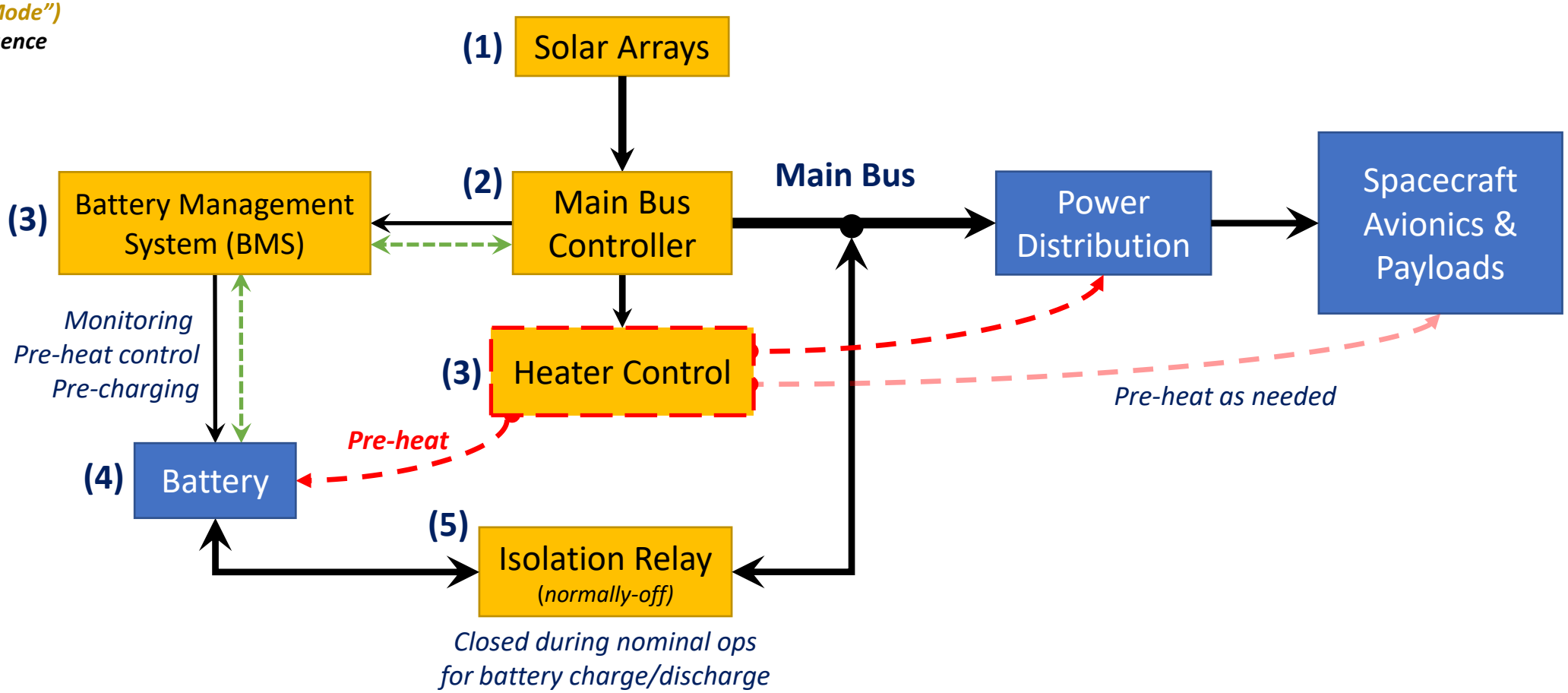
Cryo-operable ("Dawn Mode")

(#) – Dawn start-up sequence

→ *Power*

→ *Thermal*

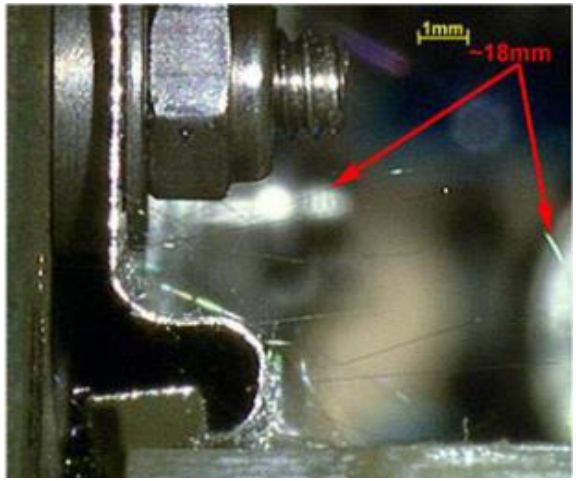
→ *C&DH*



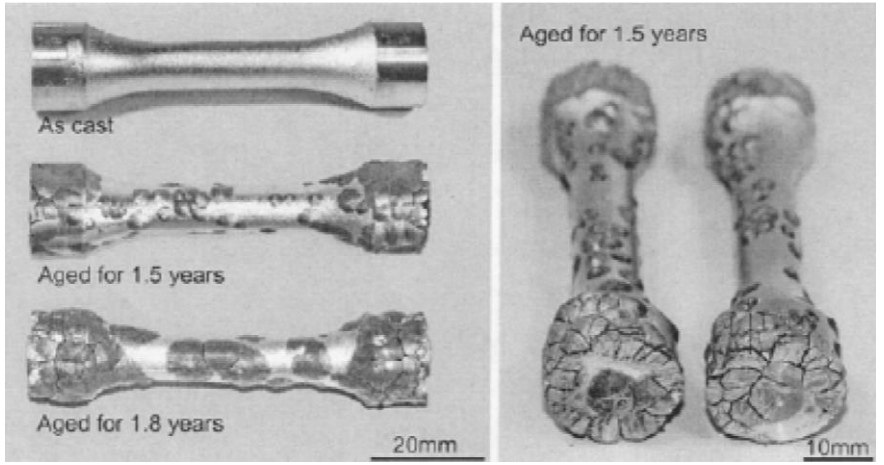
Cryo-Tolerant Electronics
Circuit Packaging: Printed Circuit Board (PCB)

- Copper-clad laminate & fiberglass-reinforced plastic (FRP) are well-matched (CTE)
- Target small boards & devices, matched CTE, mechanical compliance
- Avoid pure tin: tin whiskers and tin pest

Feature	Recommendation	Mitigates
Board	Match material CTEs Minimize PCB size	PCB warping, Cu delamination, joint separation
Joints	Use smaller boards & smaller devices (size matters)	Strain & stress due to greater tolerance of CTE mismatch
	Limit thermal cycles below “fatigue life”	Progressive joint cracking & failure
Plating	Replace tin plating with nickel-gold	Tin whiskers
Soldering & Bonding	Avoid pure tin if possible; recommend Pb-Sn alloy (≥ 3% Pb) Indium is possible tin substitute	Tin whiskers Tin pest
Coatings	Avoid thick coatings with high CTE	Thermal stress
Encapsulation	Utilize encapsulants with matching CTE	Thermal fatigue on device wire bonds



Tin whiskers: *Single-crystal tin filament growths can create short circuits.*

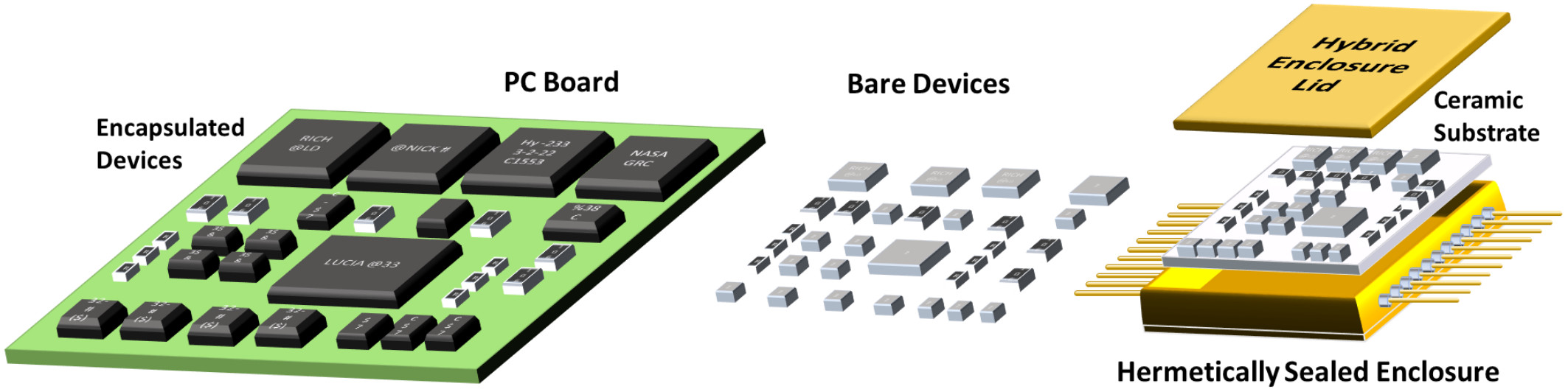


Tin pest: *Tin can transform to a brittle non-metallic form between 0°C and -30°C, expanding 27% and disintegrating joints.*

Image Credit: NASA Electronic Parts and Packaging (NEPP) Program

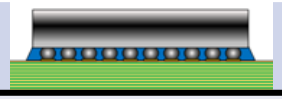
Cryo-Tolerant Electronics
Circuit Packaging: Hybrid Microcircuit

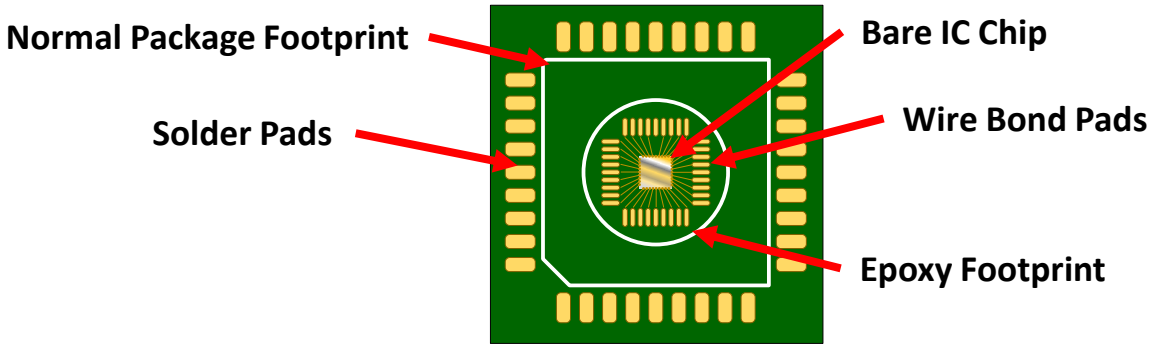
- Commonly used in analog circuits (semiconductors & passive components)
- Encapsulated in a hermetically sealed metal enclosure
  - Bare devices assembled on a low-CTE ceramic substrate
  - Eliminates thermal stress of plastic encapsulants on electrical joints
  - Connected directly to thick film traces via wire-bond or flip-chip technique
  - Reduces overall size and thermal stress
  - Improves thermal conductivity

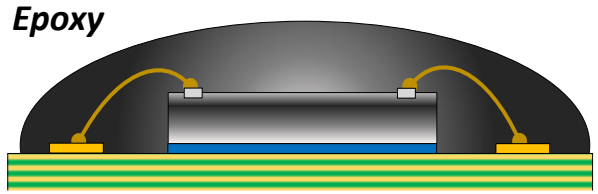


Conversion of PCB to Hybrid Circuit

Cryo-Tolerant Electronics
Circuit Packaging: Hybrid Microcircuit & COB

Circuit	Component	Description	Pros	Cons
Hybrid Circuit	Board	Miniaturized (single high-density module); Typically ceramic	• Smaller device footprint • No internal stresses from mismatched encapsulant CTE	• Cost • Limited number of layers
	Enclosure	Metal or ceramic	• Improved internal heat conduction • Shortened thermal paths	
	Substrate	Ceramic preferred	• CTE values tailorable	• Co-fired process for traces can be more costly & difficult
	Device mounting *(bare die)*	Wire bonding *(without encapsulant)*	• Compliant connection minimizes thermal expansion stress	• Larger footprint than flip-chip 
		Flip-chip – using solder bumps 	• Smallest footprint	• More susceptible to thermal stress
Chip-on-Board	Device mounting *(bare die to PCB)*	Wire-bond or flip-chip	• *See above*	• *See above*
	Encapsulation	Post-installation	• Low-cost alternative to hybrid encapsulation • Dramatic size reduction	• Unproven for cryo applications • Mismatched encapsulant CTE reduces life





Chip-on-Board Encapsulated

Cryo-Operable Electronics
Semiconductor Devices

Device			Pros	Cons
Diodes	**P-N Junction Diode**		• Can be operational at lunar temperatures with proper design	• Forward voltage increases at cryo temperatures • On-resistance increases below 100 K
	Schottky Diode		• On-resistance decreases with temperature (GaN only)	• Forward voltage increases at cryo temperatures • On-resistance increases faster than P-N below 100 K (Si & SiC)
Transistors	**Bipolar Transistor**	Bipolar Junction Transistor (BJT)	• Increased gain at cryogenic temperatures (SiC)	• DC gain decreases dramatically with temperature (Si) • Likely unsuitable for use due to freeze-out (Si)
		SiGe Heterojunction Bipolar Transistor (HBT)	• Extreme mK performance (SiGe) • Transitions from thermal to electron tunneling conductance	• Significant property changes over 50-400 K
	Field Effect Transistor (FET)	Junction-Gate FET (JFET)	• Normally-on JFET performance at lunar night temperatures similar to that at room temperature (SiC)	• Carrier freeze-out increases on-resistance as temperatures decrease past ~200 K (VJFET more susceptible)
		Metal Oxide Semiconductor FET (MOSFET)	• On-resistance decreases with low temperature until ~77 K (Si) • Switching time improves with low temperature (Si)	• Threshold voltage increases; breakdown voltage decreases (Si) • Enhancement-mode SiC unsuitable – extreme carrier freeze-out
		High-Electron-Mobility Transistor (HEMT)	• On-resistance/switching time improves with low temperature; breakdown/threshold voltage doesn't change (GaN)	
		Complementary Metal-Oxide-Semiconductor (CMOS)	• Generally shares properties with Si MOSFETs	• Hot carrier injection reduces reliability
	Insulated-Gate Bipolar Transistor (IGBT)		• Improved switching speed, forward voltage, & transconductance	• Breakdown voltage decreases • Threshold voltage slightly increases

Cryo-Operable Electronics
Passive Components

Component		Description	Pros	Cons
Resistors	Metal Film	• Resistive layer sputtered on substrate • Typically nichrome	• Low TCR, tight tolerances	
	Wire-Wound	• High-resistance, high-temp wire • Has inherent inductance	• Low TCR, tight tolerances	
	Thick Film	• Resistive paste deposited on ceramic substrate SMT		• Sensitive to temperature
	Bulk Metal Foil	• Metal foil laminated to ceramic substrate & etched	• Self-compensated TCR	• Testing needed to confirm cryo performance
Capacitors	Multilayer Ceramic (MLCC)	• Capacitor with a ceramic dielectric • Variety of compositions/properties	• Class I (paraelectrics): Good capacitance stability over temperature	• Class II (ferroelectrics): Higher variability over temperature ranges
	Electrolytic	• Polarized capacitor with electrolyte cathode • Produces high capacitance values	• Solid tantalum electrolytics will operate marginally	• Aluminum electrolytic (liquid): Electrolyte freezes at cryo temperatures • Tantalum electrolytic (solid): Higher dissipation factor & ESR, lowered capacitance at higher frequencies
Inductors	Air Core	• No core material • Generally lower inductance, higher saturation point	• Insensitive to temperature • Wire can go superconductive	
	Solid Core	• Solid cylindrical or toroidal core • Generally higher inductance, lower saturation point		• Requires special core material tailored for low losses at cryo temperatures

Cryo-Electronics Testing
Device & Circuit Testing Recommendations

- **Device Characterization Tests**
  - Driven by modeling needs
  - Assess cold-start capability
  - Be aware of superconductivity effects – electron tunneling
- **Cryo-Tolerance Testing**
  - Screen legacy circuits for cryo-tolerance (tin, large devices, mismatched CTE)
  - Perform thermal cycling to evaluate structural integrity
  - Perform pre- & post-qual functional tests
  - Use non-destructive evaluation: ultrasound & x-ray to detect hidden flaws
- **Cryo-Operable Testing**
  - Screen legacy circuits for devices that will not operate at cryo temps
  - Perform thermal cycling to simulate lunar conditions (dT/dt rate)
  - Demonstrate cold starts

Summary

- **Lunar Power Hibernation Architecture**
  - Cryo-operable & cryo-tolerant electronics enable robust, low-cost robotic missions to operate over multiple lunar cycles
- **Component Findings**
  - Most semiconductors can operate at cryogenic temperatures (50-100 K)
    - Carrier freeze-out & electron tunneling may be a concern
  - Solutions exist for most implementations of passive devices
  - Circuits may require modification/compensation to span 50-400 K
- **Board Design Recommendations**
  - Minimize footprints, match CTE, avoid tin
  - Conventional PCB assemblies: expect limited life
  - New designs: use hybrid microcircuits
    - Improved protection, low CTE, long-term reliability

Future Work

- Publish cryo-electronics design guidelines
- Continue review of academic works, including unreported components (film caps, crystal oscillators, etc.)
- Build parts model library for simulation
- Test cryogenic operation of discrete parts
- Develop prototype cryo-circuit based on guidelines
- Conduct circuit-level testing with batteries & solar cells

- **Seeking collaboration opportunities!**

Thanks for Listening

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