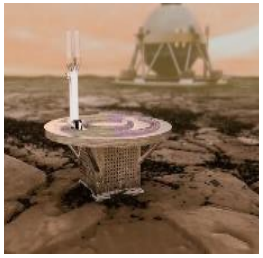
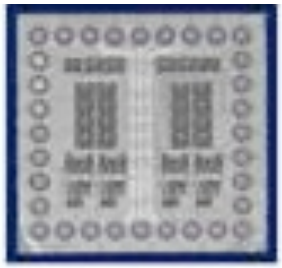
Non-Volatile, Low Power, and High Density SiC Memory For Future Venus Missions

HOTTech – High Operating Temperature Technology

Long lived memory would transform Venus landers & missions



Venus durable memory demonstrated in earlier HOTTech with impractically high power and low bit capacity



This project seeks to develop and demonstrate the world's first Venus-durable low power memory device (Non-Volatile Random Access Memory (NVRAM) to enhance extended Venus surface missions.

Team Member(s)/Institution(s)

- P. Neudeck/NASA Glenn Research Center
  PI Responsible for Overall Project Implementation.
- D. Spry/NASA Glenn Research Center
  Process Development/Materials Characterization Lead.
- N. Prokop/NASA Glenn Research Center
  Lead of electrical testing including GEER.

Technology Overview/Description

- Low power and high data storage capacity Venus-durable memory would dramatically enhance Venus surface missions.
- SiC JFET-R Random Access Memory (RAM) integrated circuits (ICs) have been demonstrated to be long-term Venus surface durable. However, to reach mission-impactful data storage capacities these SiC memory chips consume too much battery power for practical use in long-duration Venus landers.
- Leveraging SiC JFET-R IC technology, low power Venus durable Non-Volatile Random Access Memory (NVRAM) cells and ICs will be developed and demonstrated. SiC JFET-R NVRAM will be able to retain stored data without electrical power.
- Will complement and be directly compatible with high temperature electronics development for long lived lander platforms.
- Will demonstrate the world's first high temperature zero-power data retention memory cells and ICs operable in Venus surface conditions and 500 °C in Earth atmosphere.

Technology Goals

460 °C Durable Memory Metric	**2022 Start** IC Gen. 12	**2025 End** NVRAM IC	Project Gain
Chip Power Needed to Retain Stored Data	1.2 W	0 W	> 1000X
Average Chip Power*	**1.2 W**	**0.016 W**	~ 75X
Average Power/Bit*	5 mW/bit	0.016 mW/bit	~ 312X
1 kbit Average Energy Cost/Hour*	18000 J/hour	57 J/hour	~ 316X

*LLISSE-like duty cycle 2 minutes awake / 8 hours sleep = 0.4%

- Venus surface conditions test of memory chip in GEER.
- Initiate a months of 500 °C Earth air oven memory chip test.

Starting TRL: 2-3 **Ending TRL: 4-5**