National Aeronautics and Space Administration

The Path Towards Realistic ASIC Deployment Into Previously Impractical Extreme Application Environments

Philip G. Neudeck[1], David J. Spry[1], Michael J. Krasowski[1], and Liangyu Chen[2]

[1]NASA Glenn Research Center
[2]Ohio Aerospace Institute

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https://go.nasa.gov/sic

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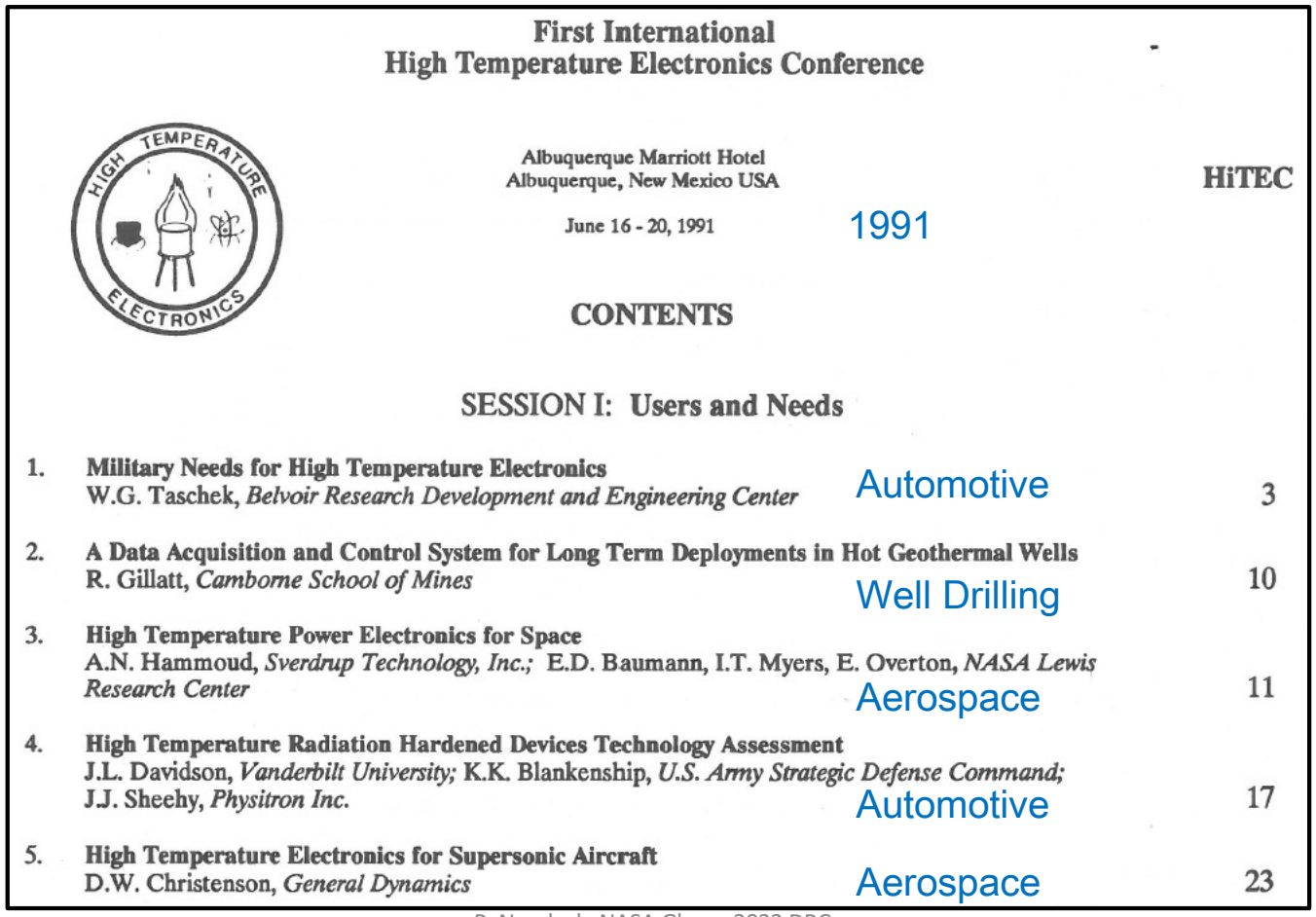
Amir Avishai

Potential Benefits of High Temperature Electronics Has Been Recognized for Decades



First International
High Temperature Electronics Conference

Albuquerque Marriott Hotel
Albuquerque, New Mexico USA

June 16 - 20, 1991

1991

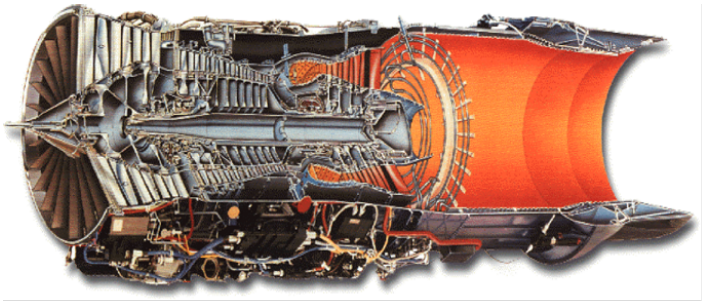
HiTEC

CONTENTS

SESSION I: Users and Needs

High-T Electronics Benefits to NASA Missions

Intelligent Propulsion Systems

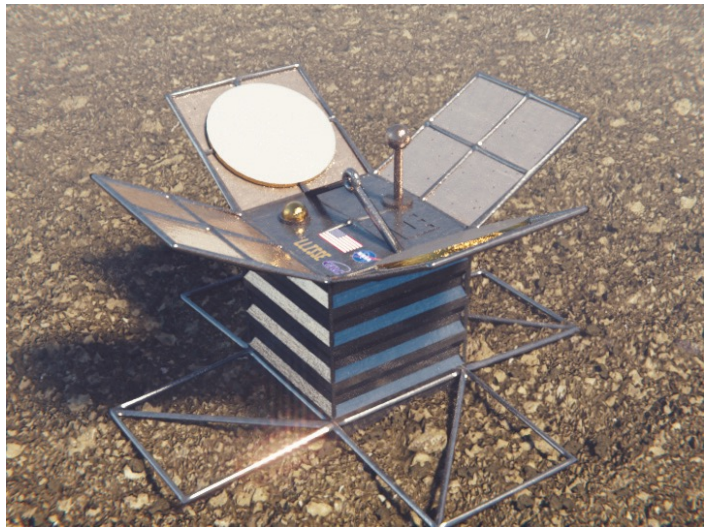


T > 450 °C sensors with electronics in key engine areas for realizing advanced concepts in distributed control and compressor/combustion instability detection and avoidance for improving engine performance

- Thrust to weight ratio
- Fuel efficiency & emissions

Power devices for aerospace electric propulsion and actuation

Venus Exploration Landers



Venus surface: **460 °C**
AND 92X Earth pressure
AND chemically reactive gasses

Long duration landers require electronics that endure the Venus surface environment

High Temperature Semiconductor Device Development

Prototype T > 450 °C operation has been reported for decades.

- Multiple research groups (industrial, academic, and governmental)
- Multiple semiconductor materials (SiC, III-N, silicon-on-insulator)
- Multiple transistor approaches (JFET, MESFET, MOSFET/CMOS, and Bipolar)

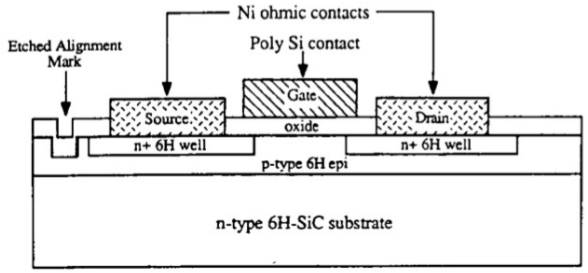
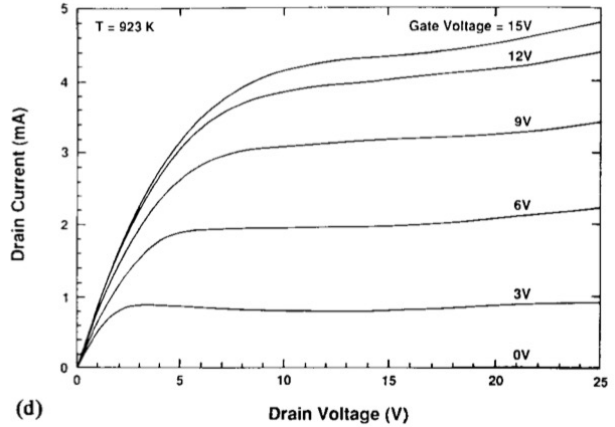


Fig. 19. Material structure of a 6H-SiC MOSFET fabricated at Cree Research, Inc.



Davis et al., Proc. IEEE, vol. 79, no. 5 pp. 677-701 (1991).

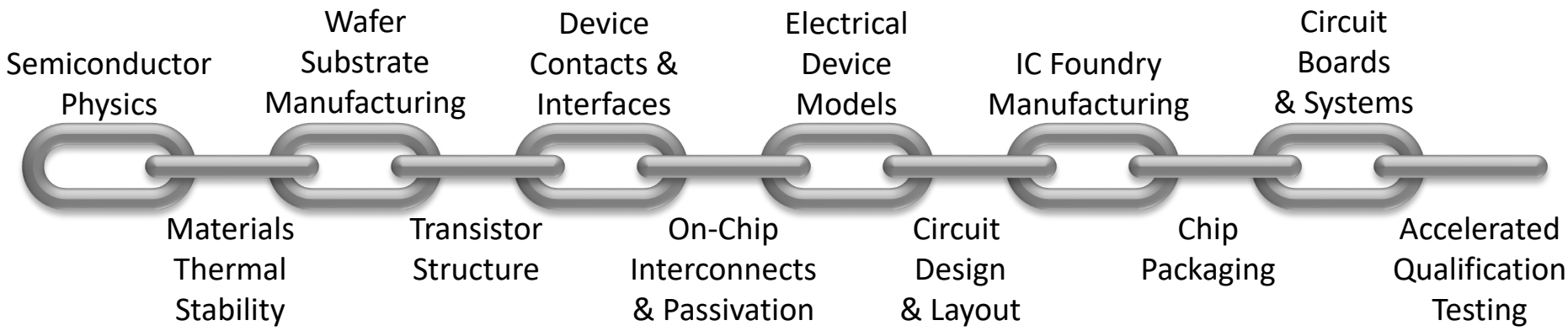
Missing from majority of reports: Long term operational stability at T > 450 °C

- In most cases, only brief (~ 1 hour) heated probe-station testing is reported.

Demonstrations insufficient for serious consideration by systems designers

IC Electronics Technology Chain

Chain that is taken for granted at conventional temperatures,
but is far from trivial to expand to temperature extremes.



Any single weak link will prevent practical infusion and deployment of electronics.

IN THE DESIRED APPLICATION ENVIRONMENT, ALL LINKS MUST

1. FUNCTION INTEGRATED TOGETHER
2. BE PROVEN LONG-TERM DURABLE/STABLE - WITH MARGIN!

NASA Glenn SiC IC Technology Development Goals

Greatly expand the application-viable IC operating temperature envelope

Bring initial IC electronics capability reliably to previously unthinkable places
- Enable new approaches to systems dealing with harsh environments

- At least 500 °C operation for long duration
  - More than 200 °C above silicon-on-insulator practical limit

- At least 2000 hours of stable electrical operation at 500 °C
  - Jet engine ground test, Venus surface missions

- At least 2 levels of 500 °C durable on-chip interconnect
  - Enable more complex, higher density ICs

- Chip packaging and multi-chip circuit boards for 500 °C operation
  - Integration with sensors, wireless communications, subsystems

- Infusion of beneficial 500 °C ICs into missions and systems

NASA Glenn SiC IC Development Philosophy

"Over-design" every aspect to make high temperature durable ICs

- De-prioritize other device metrics (such as power & frequency)
- Seek compatibility IC manufacturing materials, tools, and techniques

Device Foundation

- SiC epilayer PN homojunction transistor (not MS or MOS gate)
- Stable ohmic contacts

On-chip Integration

- Stable interconnect
- High circuit density (2-level interconnect, small devices & isolation)
- Temperature and process tolerant circuit design

Ceramic packaging and circuit boards

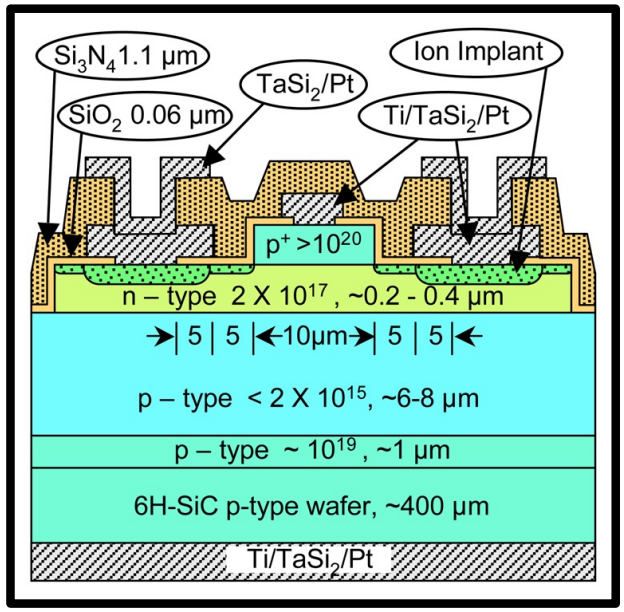
Demonstrate initial 500 °C durable IC capability, infuse and improve in parallel

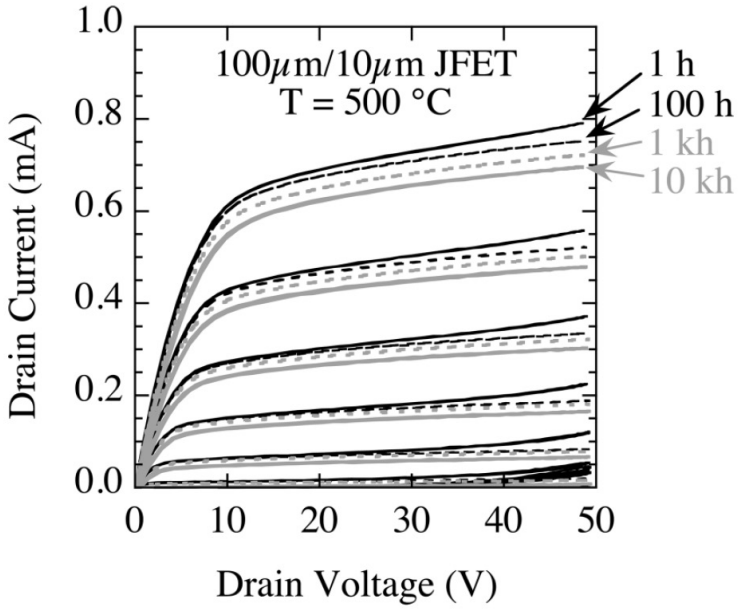
"LEARN BY DOING" OVER SUCCESSIVE GENERATIONS (CYCLES) OF PROTOTYPE IC FABRICATION AND CHARACTERIZATION.

NASA Glenn Low-Power 6H-SiC JFET ICs

(Results from ICSCRM 2007 & ECSCRM 2008)

Discrete packaged JFETs operate with excellent stability for 10,000 hours at 500 °C





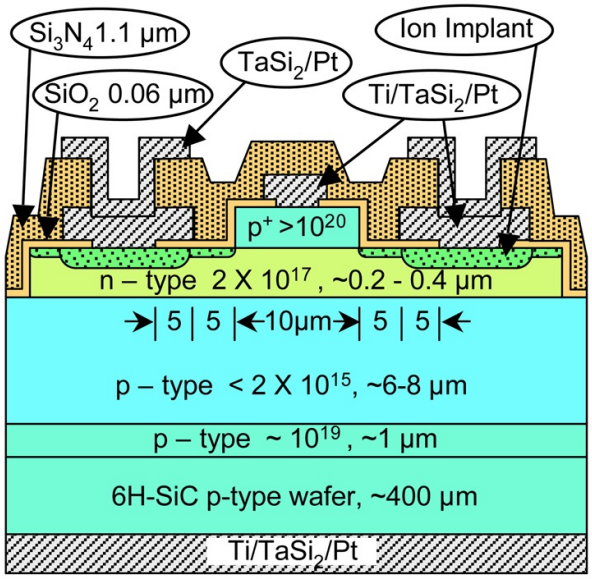
< 10% changes during 10,000 hours of electrical operation in air at 500 °C!

D. Spry et al, Mat. Sci. Forum vol. 600-603, p. 1079 (2008)
Ohmic Contacts from R. Okojie et al, J. Appl. Phys, vol. 91, p. 6553, (2002)

Transistor Device Approach

Epitaxial SiC n-JFETs developed as the most straightforward foundational transistor for achieving long-term device stability at T ≥ 500 °C

2007 NASA 6H-SiC JFET [1]



SiC is the most stable/inert semiconductor crystal
- Low impurity diffusion, low reactivity

Inherent JFET High-T Stability Advantages
- Majority carrier device
- Low-leakage epilayer PN homojunctions
- Minimal sensitivity to p-type (gate) contact
- N-type ohmic contacts/implants

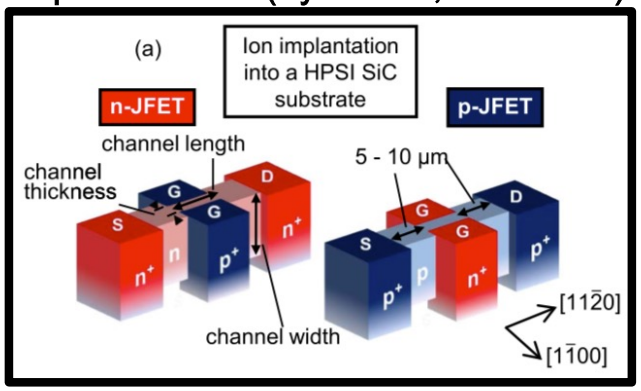
Other transistor types more challenging to render stable/durable at T > 450 °C.
- Bipolar transistors: n-type AND p-type contact AND minority carrier sensitivity
- MOSFETs/CMOS: MOS junction sensitivity
- MESFETs: Rectifying metal-semiconductor junction leakage & sensitivity
- III-N HFETs: Heterojunction sensitivity, more diffusion, more reactive than SiC

[1] Neudeck et al., IEEE Electron Device Lett. vol. 25, no. 5, pp 456-459 (2008).

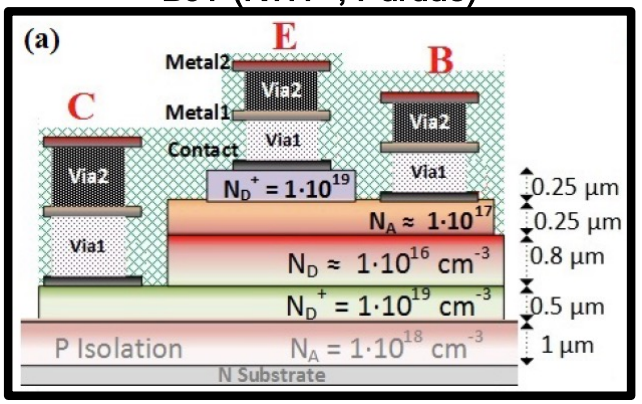
Alternative Device Approaches

- **Worthwhile benefits IF/WHEN prolonged and stable 500 °C operation achieved**
- Challenging integration with durable interconnect & packaging?

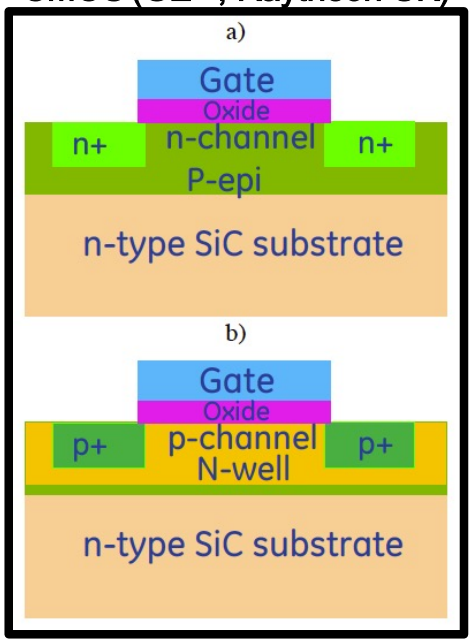
Implanted JFET (Kyoto U.[1], United SiC)



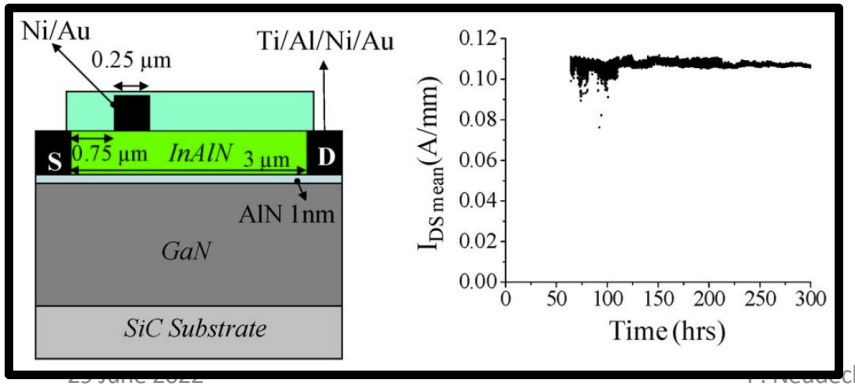
BJT (KTH[3], Purdue)



CMOS (GE[2], Raytheon UK)



III-N FETs[4]

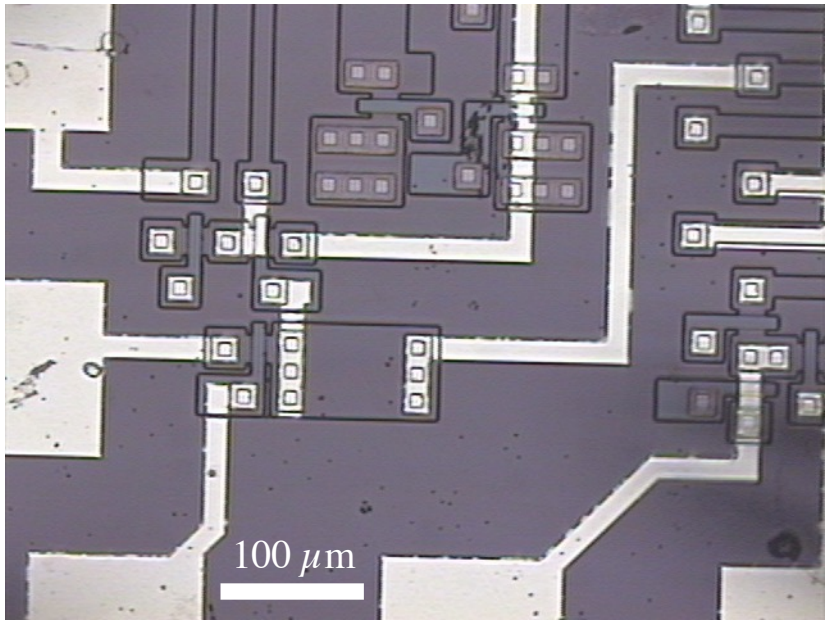


[1] Nakajima et al, IEEE Electron Dev. Lett., **40**, 866 (2019).
[2] Chen et al., 2014 IMAPS Int. Conf. High Temp. Electronics, p. 72.
[3] Shakir et al., Electronics. 8, 496 (2019).
[4] Maier et al., IEEE Trans. Device and Mat. Rel., **4**, 427 (2010).

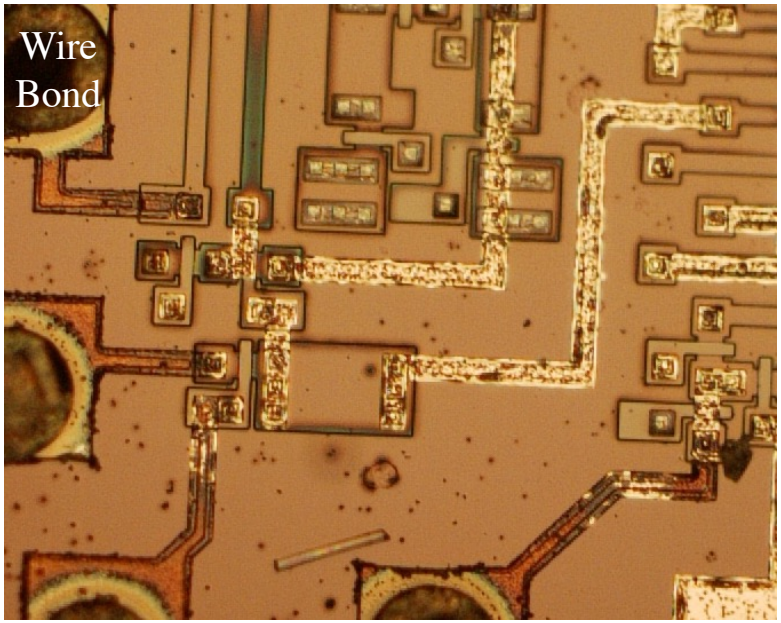
Early-Generation NASA Glenn Single-Level Interconnect

(Slide Presented at 2011 Electrochemical Society Meeting)

As-fabricated chip

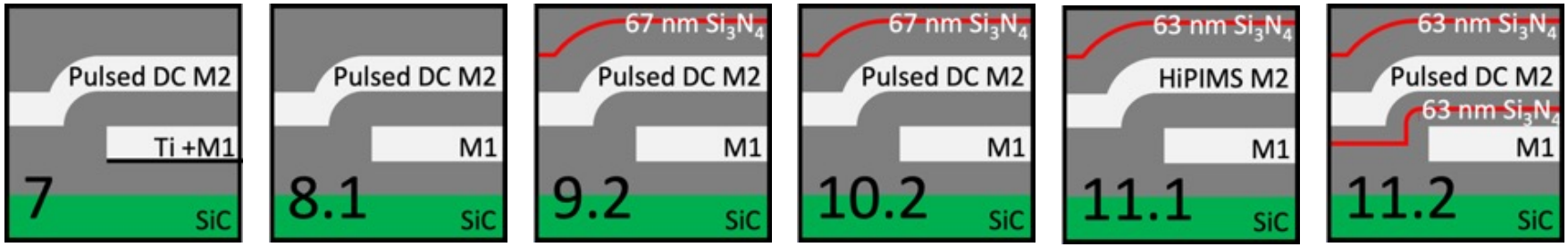


After prolonged 500 °C test



SiC JFET IC Interconnect Development[1]

(Simplified Cross-Sections of Multiple Generations of Prototype 2-Level Interconnect)



- 7 - Only 720 °C LPCVD TEOS, M1 has Ti adhesion layer

Proximity sputtering of $TaSi_2$ (21 mm target-substrate)

7 devices were not functional because of bond pad

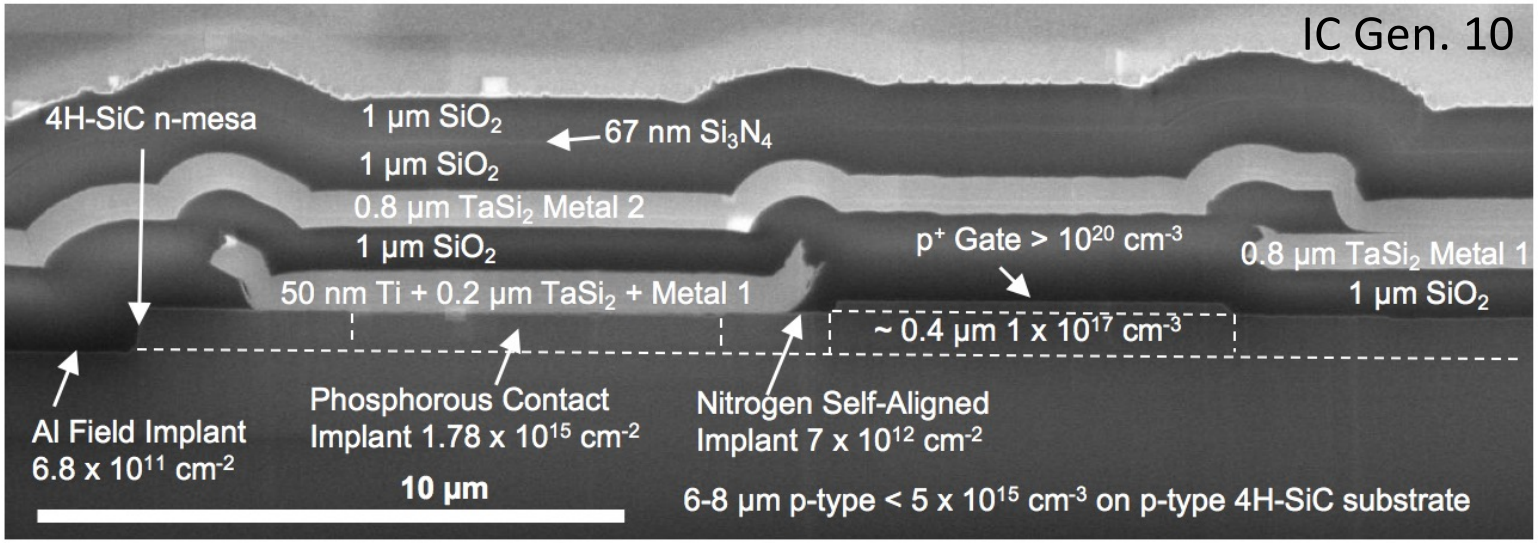
- 8.1 Bond pads were only made by etching Via3 back to SiC and depositing Metal 3 during a single pump down of TaSi2/Pt/Ir/Pt
- 9.2 Added 63 nm of LPCVD stoichiometric Si_3N_4 above Metal 2
- 10.2 - Pulsed-DC $TaSi_2$ and 1 Si_3N_4 layer above Metal 2
- 11.1 - HiPIMS $TaSi_2$ and 1 Si_3N_4 layer above Metal 2
- 11.2 - Pulsed-DC $TaSi_2$ & 2 Si_3N_4 layers

-above Metal 2 &

between M1 & M2

[1] D. Spry & P, Neudeck, 2021 Int. Conf. Compound Semiconductor Manufacturing Technology (CS-MANTECH)

500 °C Stable Two Levels Interconnect[1]

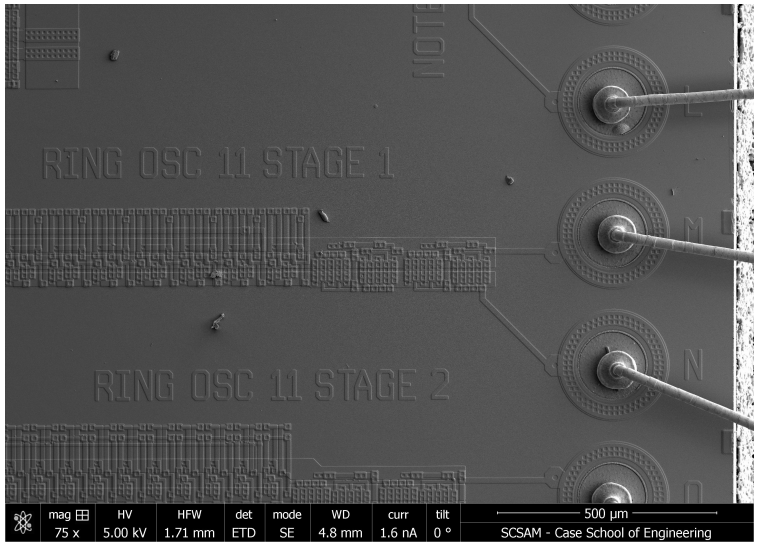


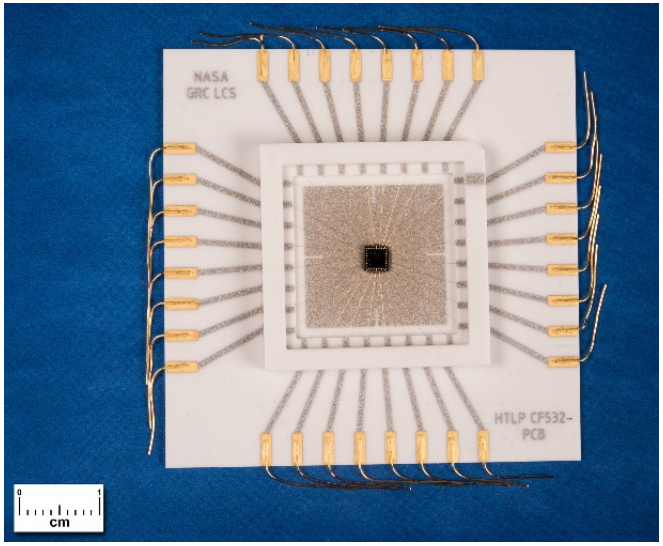
IC processing and materials compatible with SiC power device tools & manufacturing

- Close-proximity sputtering of $TaSi_2$ (21mm target to substrate spacing)
- LPCVD tetraethyl orthosilicate (TEOS) and Si_3N_4 layers deposited at 720 °C
- **All interconnect completely buried/passivated beneath dielectric.**

[1]P. G. Neudeck, et al., 2018 IMAPS High Temperature Electronics Conf. pp. 71-78

500 °C Stable Bond Pads and Packaging[1,2]



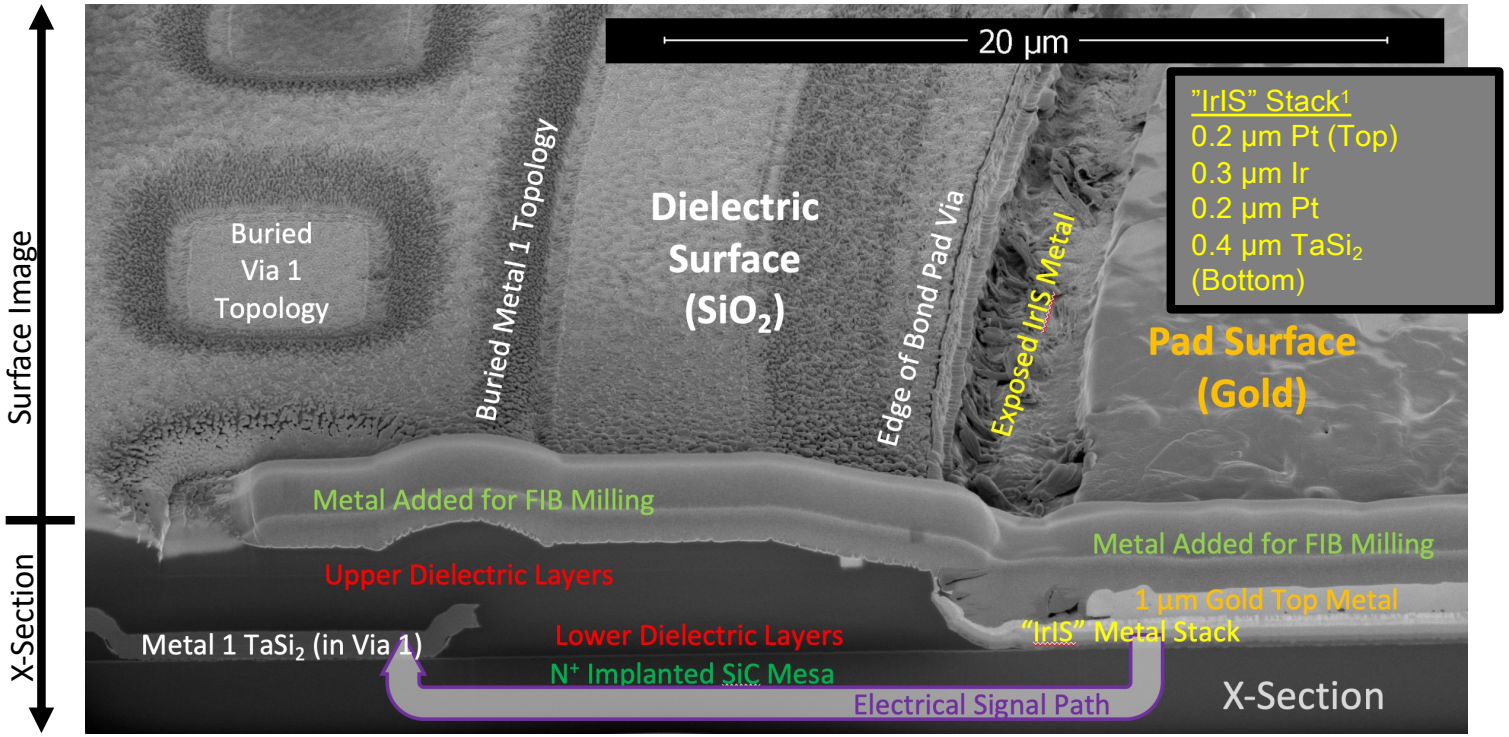


- "IrIS" bond pad metal stack anchored directly to SiC[1]
- Pt thick-film traces, Au/Pt pads, Au die attach (600 °C), and Au ball bonding[2].

[1]D. Spry & D. Lukco, J. Electronic Materials 41 p. 915 (2012)
[2]L. Chen, et al., Proc. 2016 IMAPS High Temperature Electronics Conf. pp. 66-72

500 °C Durable "IrIS" Bond Pad[1]

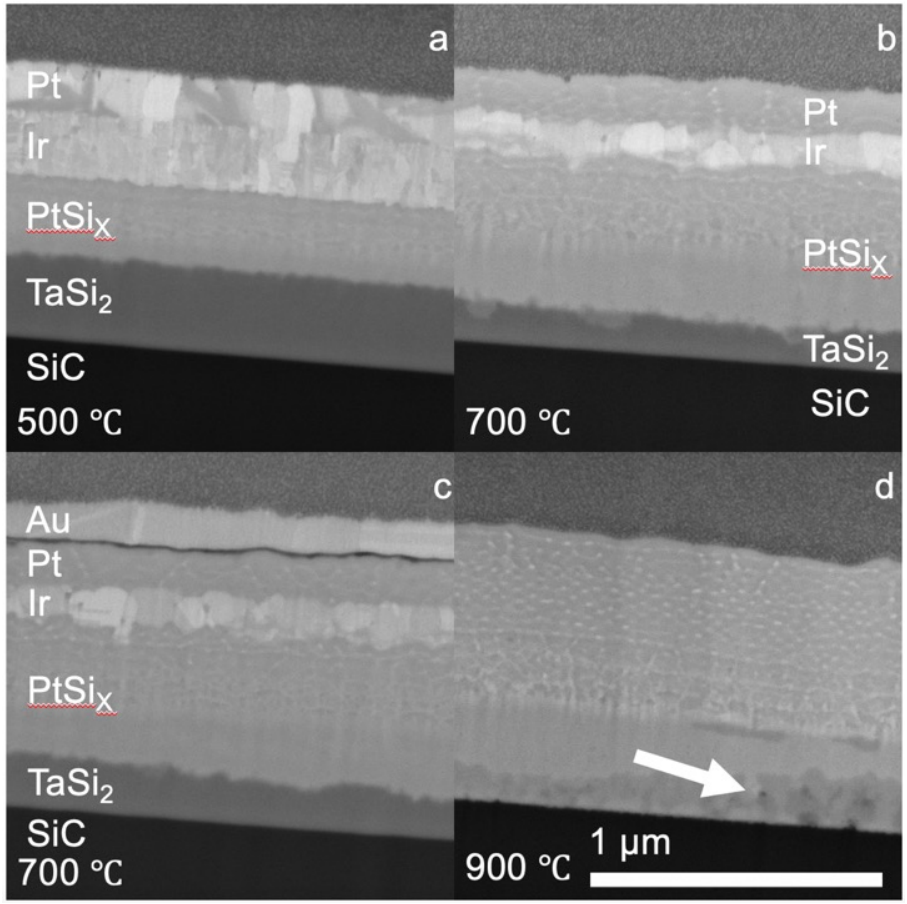
(FESEM FIB Cross-Section)



Large-area "IrIS" metal bond pad stack is anchored directly to hard SiC crystal foundation.
Interconnect Metals 1 & 2 are 100% buried in dielectric and DO NOT TOUCH "IrIS" metal.
- N+ Implanted SiC connects "IrIS" with Metal 1 (~ 100 Ω series resistance).

[1]Spry et al., J. Electronic Materials 41(5) p. 915 (2012).

Annealing Study of Thermal Limits of "IrIS" Bondpads[1]



The first clear structural temperature limit is just above 700 °C.

Image **a** after 500 °C anneal the IrIS stack has segregated into its planed layers of $TaSi_2$ that contacts the underlying SiC, $PtSi_X$, Ir, Pt.

Image **b** post 700 °C image of bond pad without Au cap reveals a thickened $PtSi_X$ zone that comes closer to SiC interface, the contact remains a smooth and abrupt interface between $TaSi_2$ and SiC.

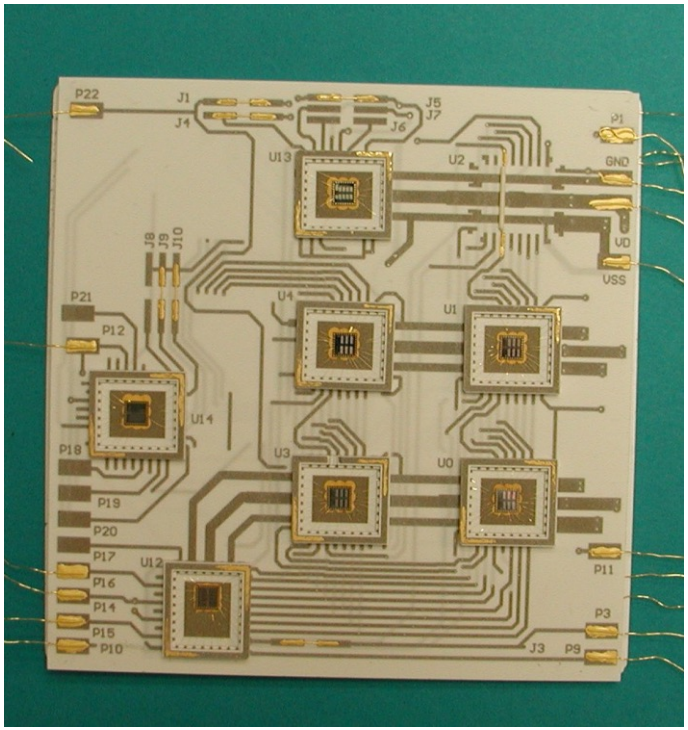
However, image **c** of 700 °C anneal IrIS stack with Au cap shows evidence of oxygen accumulation at the Au/Pt interface which could become a bonding failure point if the Au ball bond attached during chip packaging is not thick enough to prevent oxygen penetration.

Image **d** at 900 °C, the Fig. 2d image shows Pt has reached the SiC interface along with evidence of voiding (white arrow).

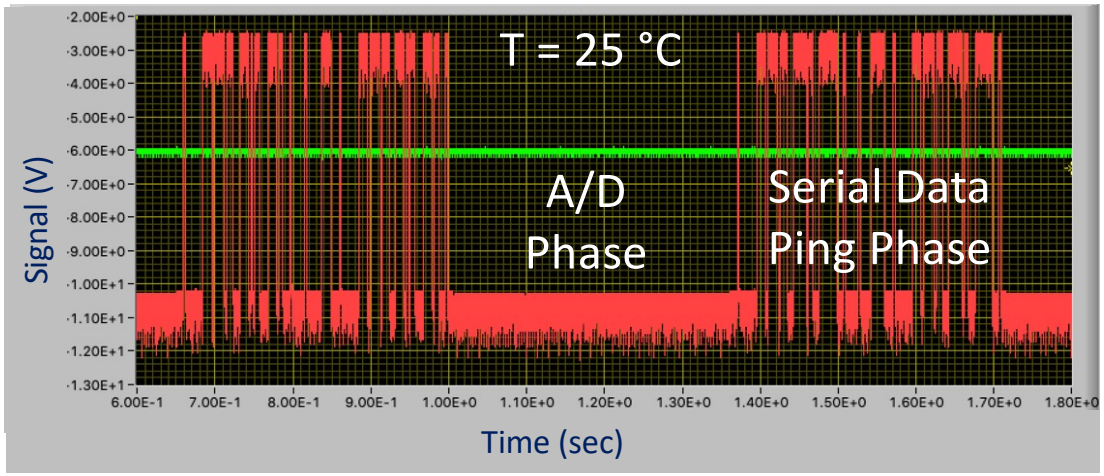
[1] D. Spry & P, Neudeck, 2021 Int. Conf. Compound Semiconductor Manufacturing Technology (CS-MANTECH)

Prototype Venus Lander Circuit Board

Simple “state machine” to digitize and serial data ping signals from analog sensors

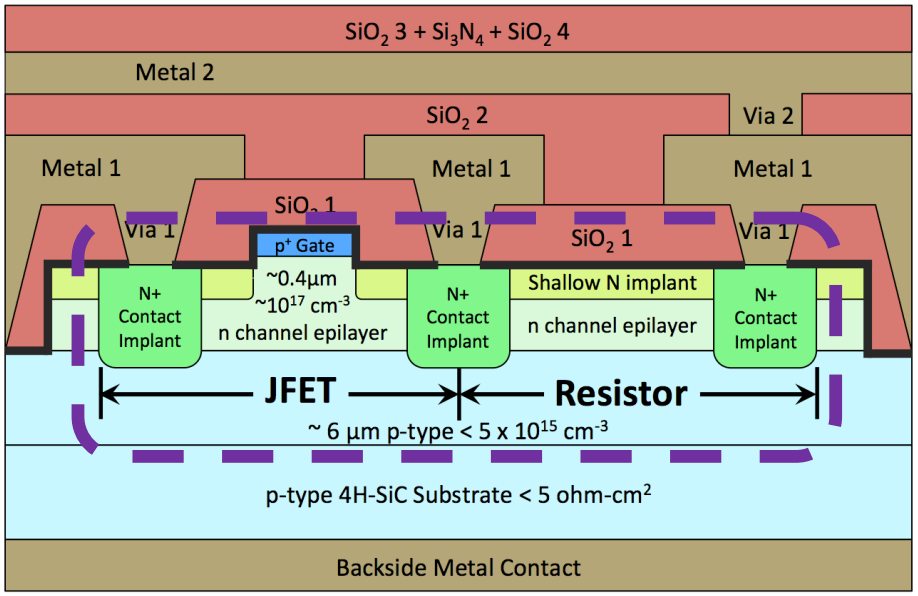


8-bit A/D with serial data ping for 6 sensor channels
4-layer HTCC circuit board 4.5 inches x 4.5 inches
9 packages of Gen. 11.1 chips (7 topside, 2 underside)
Awaiting GEER Venus chamber test (COVID-delayed)

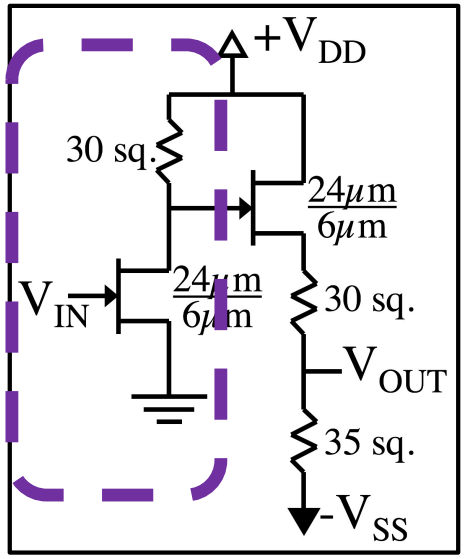


Ceramic packages and circuit boards commercially purchased. Designed and integrated by NASA.

Circuit Approach[1,2]



NOT Logic Gate Schematic



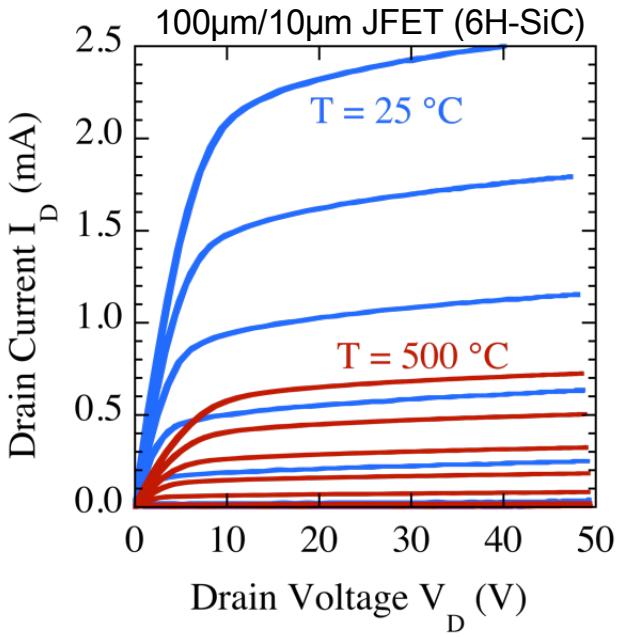
- Resistors made with same epi as JFET → well-matched T dependence
- Layout ratio-based circuit design (not absolute component values)
- Negative threshold voltage V_T → negative signal voltages (roughly -1V to -10V logic)
- Typical V_{DD} = +25 V, V_{SS} = -25V Chip backside is biased at V_{SS}

[1]M. J. Krasowski, US Patent 7,688,117 (2010).
[2]P. G. Neudeck, et al., Proc. IMAPS High Temperature Electronics Conf., 2016, pp. 263-271.

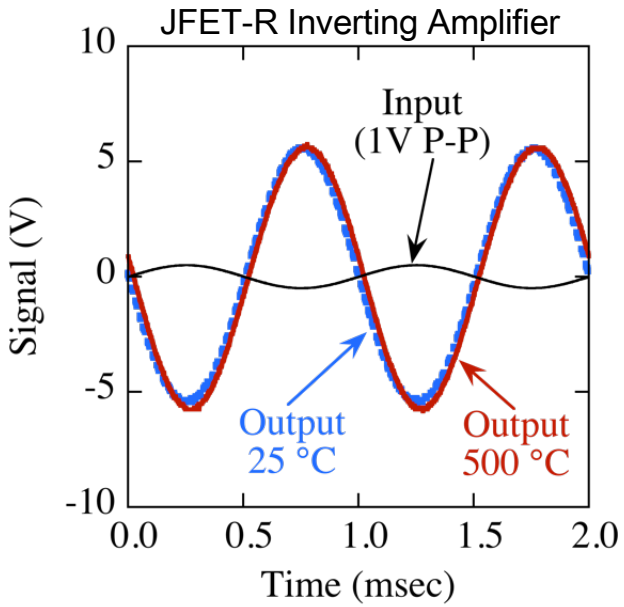
Temperature Performance

(Slide Presented at 2011 Electrochemical Society Meeting)

Transistor Characteristics



Circuit Characteristics

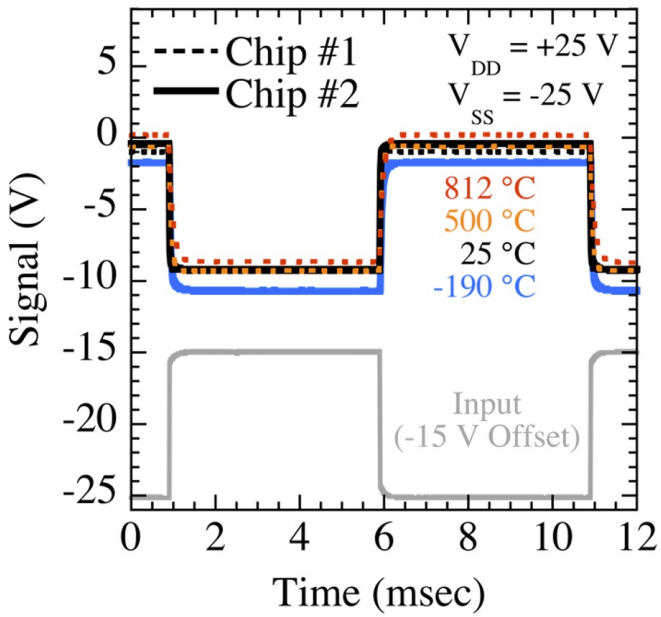


Despite large (> 3X) change in JFET characteristics…

…nearly temperature-independent circuit operation can be achieved!

-190 °C to +812 °C "Go Anywhere" Functionality[1]

(Generation 10.1 NOT Gate Testing)

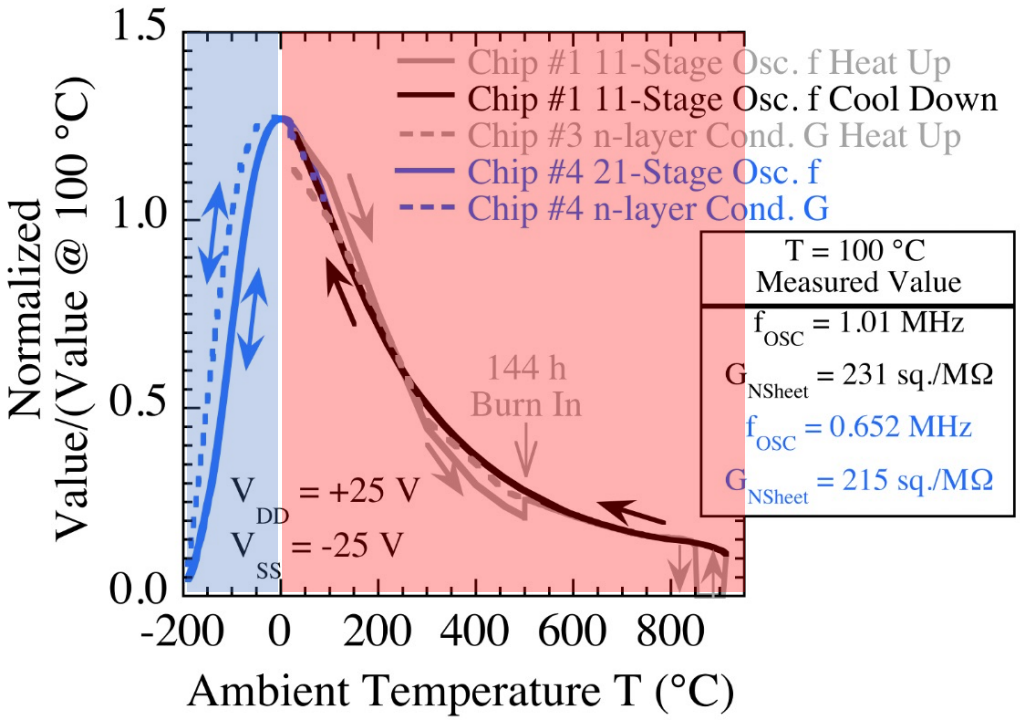


- 1000 °C temperature span WITHOUT changing signal/supply input voltages!
- *SiC JFET ICs function in cold environments WITHOUT "cold start" issues.*
- Temperature-accelerated 800 °C lifetime testing for long-duration 500 °C missions.
- Straightforward functional yield screening at 25 °C (on-wafer probe test).

[1]Neudeck, Spry, Krasowski, Prokop, Chen, Materials Science Forum, vol. 963, pp. 813-817 (2019).

Sheet Conductance & Ring Oscillator Frequency vs. Temperature[1]

Circuit frequency & power track 4H-SiC n-layer conductivity change



Low Temperature (T < 0 °C):
Incomplete ionization "freezeout effect" dominates 4H- SiC n-layer conductivity

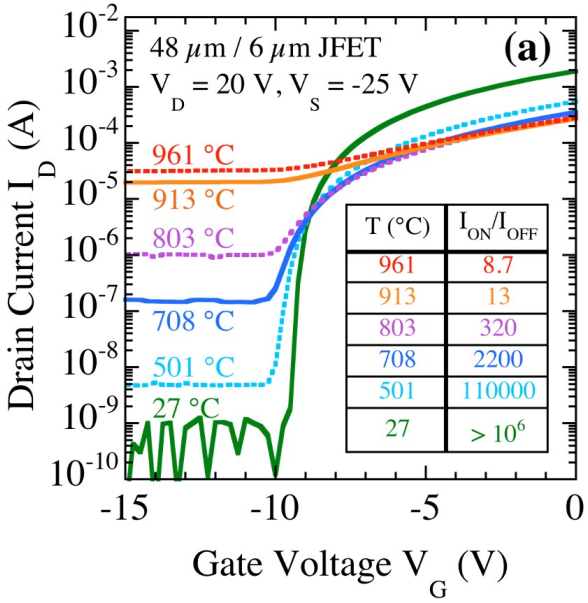
High Temperature (T > 0 °C):
Carrier mobility reduction due from thermal phonon scattering dominates 4H-SiC n-layer conductivity.

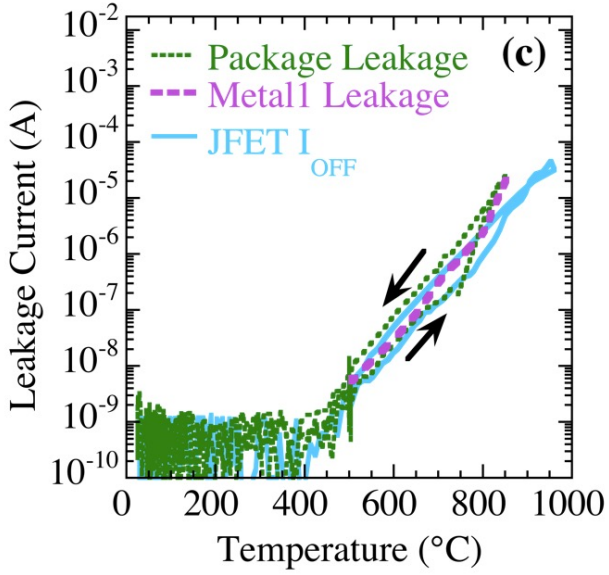
Circuit frequency and power are highest near 0 °C, decrease by roughly factor of 4-5 as temperature increased to 500 °C.

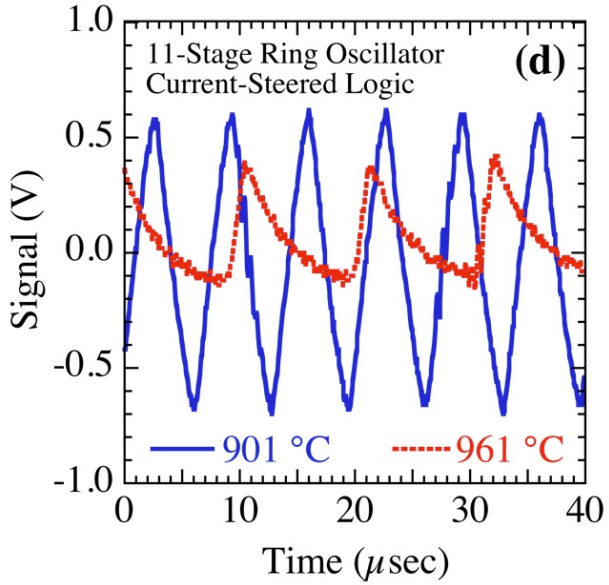
[1]Neudeck, Spry, Krasowski, Prokop, Chen, Materials Science Forum, vol. 963, pp. 813-817 (2019).

Short-Term Operation Demonstrated Above 900 °C[1]

Enables temperature-accelerated lifetime qualification testing for 500 °C applications.







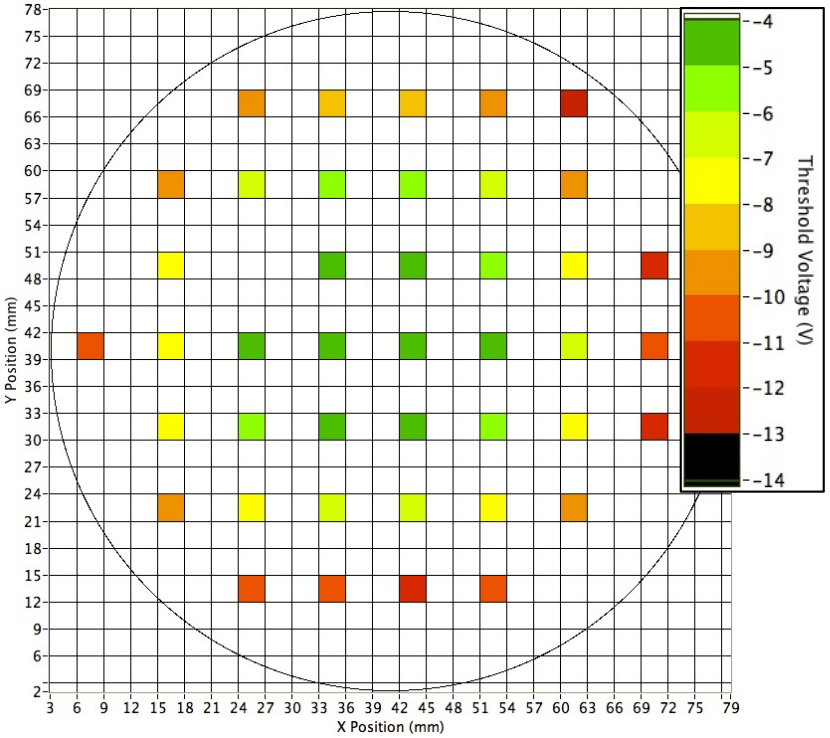
(Note: Waveforms are probe-loaded)

- Packaging leakage was limiting experimental factor, package was designed for 500 °C.
- **"Intrinsic" JFET-R IC high-temperature limit remains to be ascertained.**

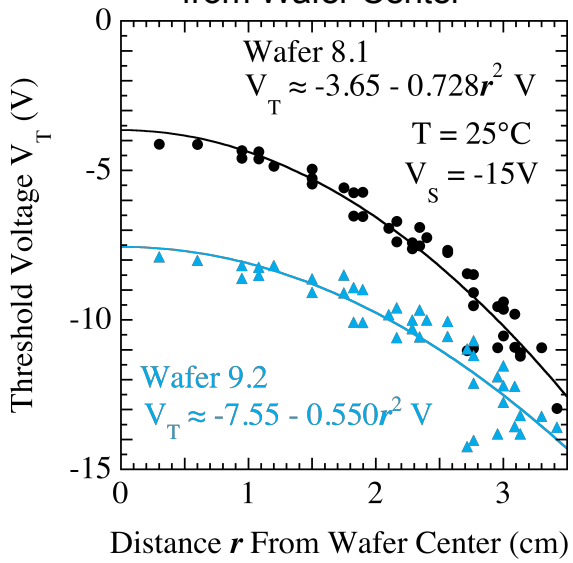
[1]P. Neudeck, et al., IEEE Electron Device Lett. 38 (2016) 1082-1085.

Experimental JFET Threshold (V_T) Non-Uniformity[1]

Wafer Probe Map of Wafer 8.1 JFET V_T
T = 25 °C, V_D = 20V, V_S = -15V
(76 mm diameter wafer)



Plot of Measured JFET V_T
vs. Radial Distance (r)
from Wafer Center



Positional variation of JFET V_T is radial and due to thickness non-uniformity in as–grown epilayers.

[1]P. Neudeck et al., Materials Science Forum **858** p. 903 (2016).

Circuit Design Tradeoffs: Power, Frequency, & Area

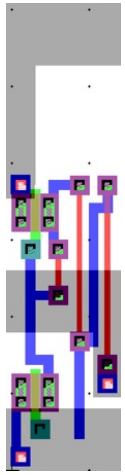
To-Scale Comparison of Gen. 11 NOT Logic Gates

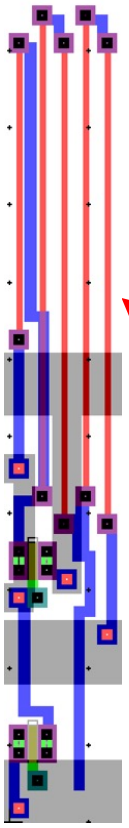
Standard
"Base Power" (BP)
NOT Gate

Average Power:
2 mW @ 460 °C
(near Gen. 10)

Layout Size:
74 µm x 304 µm
= 22496 µm^2

Active Region:
74 µm x 192 µm
= 14208 µm^2





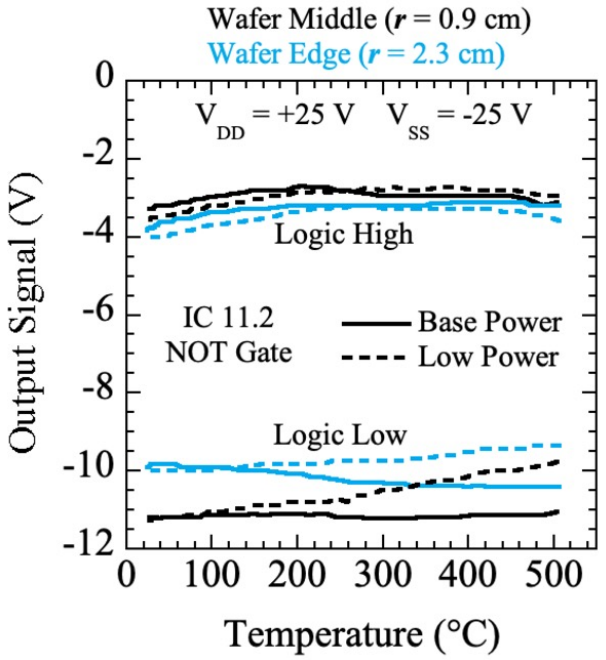
LLISSE
"Low Power" (LP)
NOT Gate

Average Power:
0.4 mW @ 460 °C
(20% of BP Gate)

Layout Size:
71 µm x 532 µm
= 37772 µm^2
(167% of BP Gate)

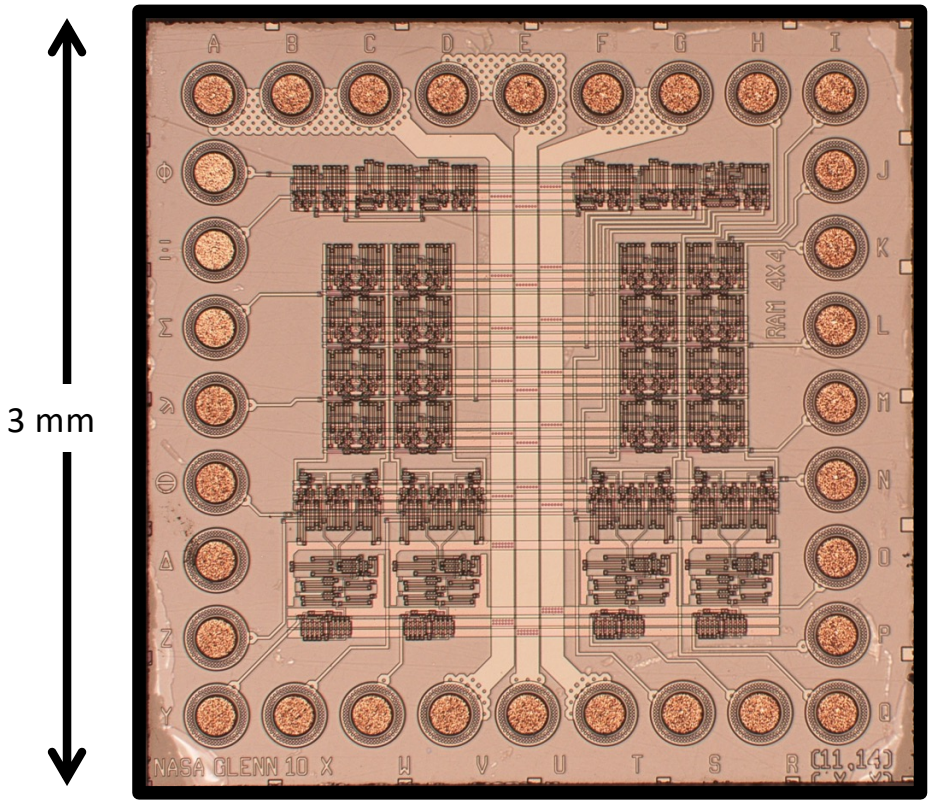
Active Region:
71 µm x 532 µm
= 37772 µm2
(265% of BP Gate)

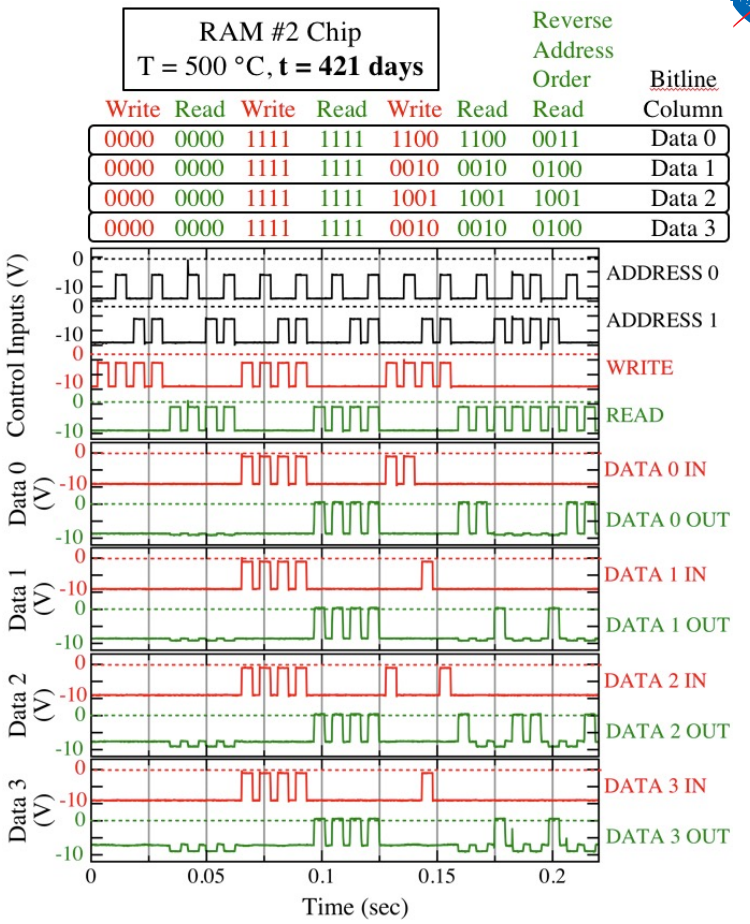
Measured Output Voltages vs. Temperature



Larger resistors achieve 5-fold reduced power goal.
- At much less than 5-fold layout area penalty.
- Logic swing (above) and other metrics acceptable.

500 °C Durable NASA Glenn Gen. 10 SiC JFET-R RAM Chip[1]



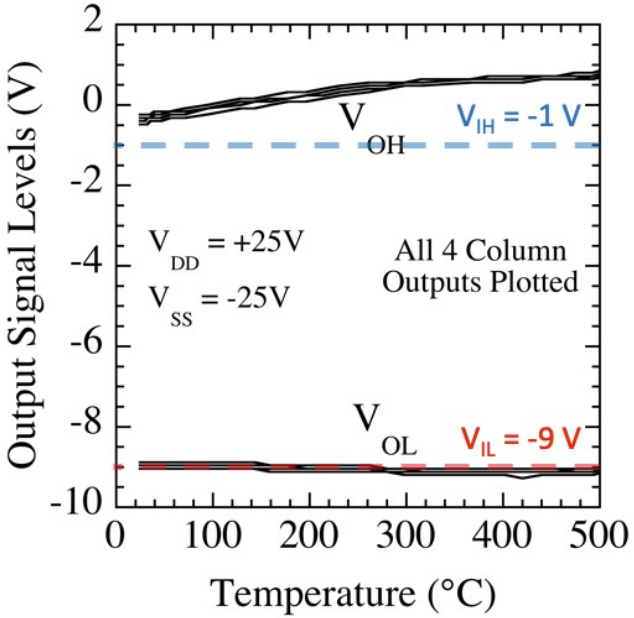


[1]P. G. Neudeck, et al., 2018 IMAPS High Temperature Electronics Conf. pp. 71-78

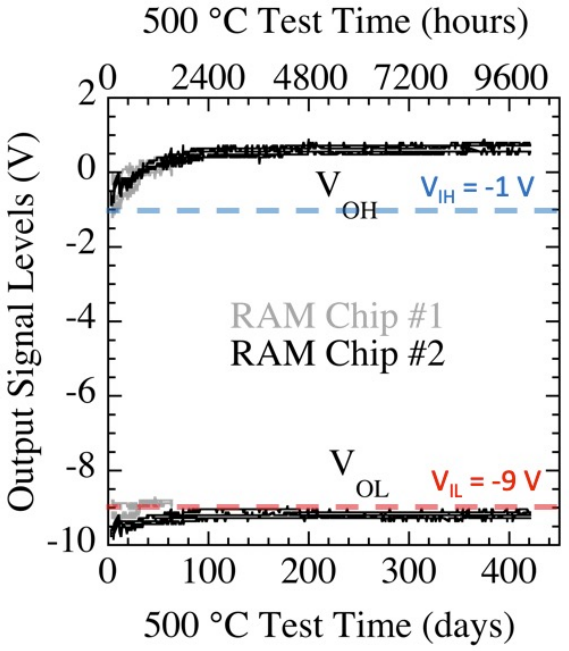
NASA Glenn Gen. 10 RAM Chip Output Levels

(2018 IMAPS High Temperature Electronics Conference)

vs. Temperature

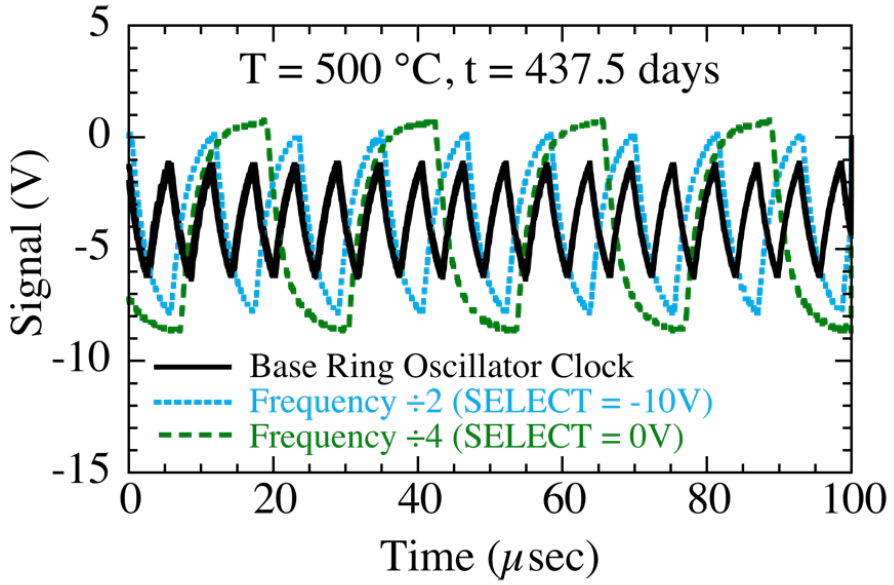


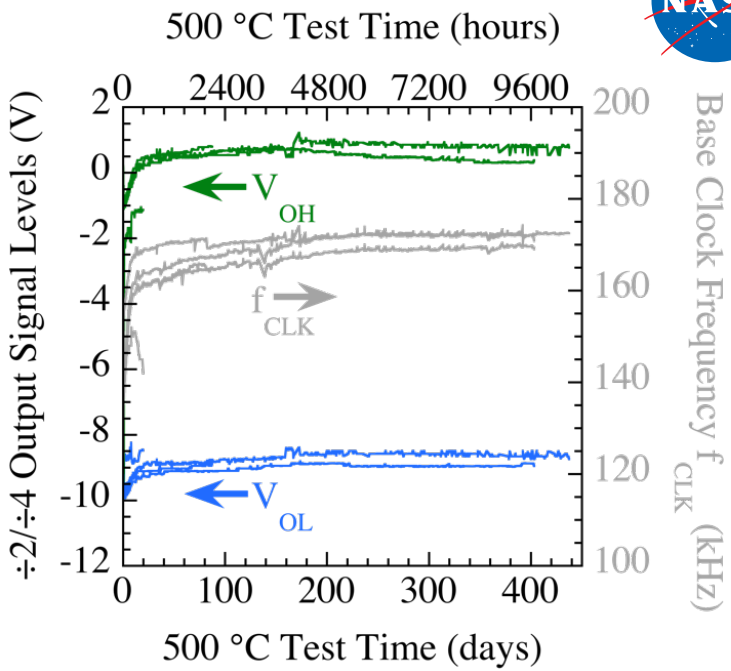
vs. Time @ 500 °C



- ✓ Operation over broad application temperature range
- ✓ Prolonged (year+) operation at T > 450 °C for applications

500 °C Oven-Test Results[1]





- Some IC Gen. 10 chips last more than 1 year, but a few "infant fail" much sooner
- After initial burn-in, output characteristics change < 10%

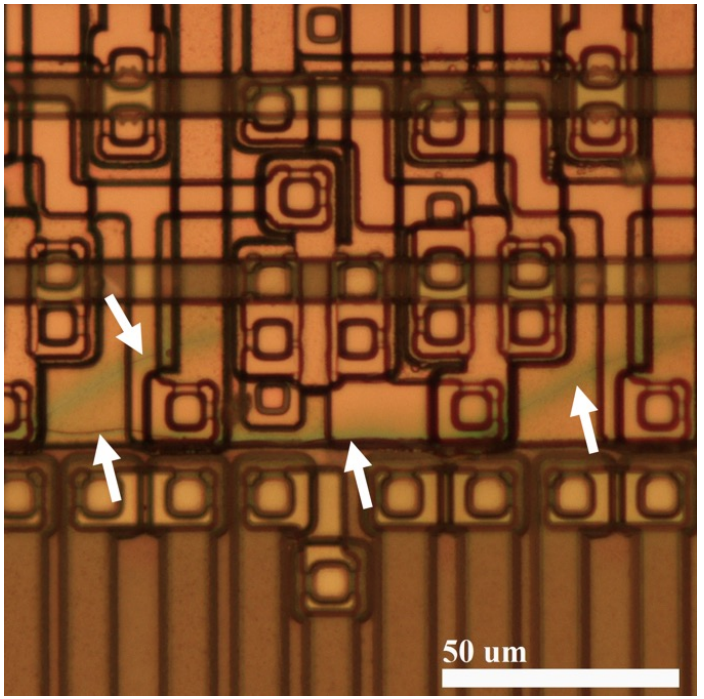
[1]P. G. Neudeck, et al., 2018 IMAPS High Temperature Electronics Conf. pp. 71-78

Primary Failure Mode: Cracks in Dielectric[1]

$TaSi_2$ interconnects oxidize beneath cracks leading to open-circuit failure

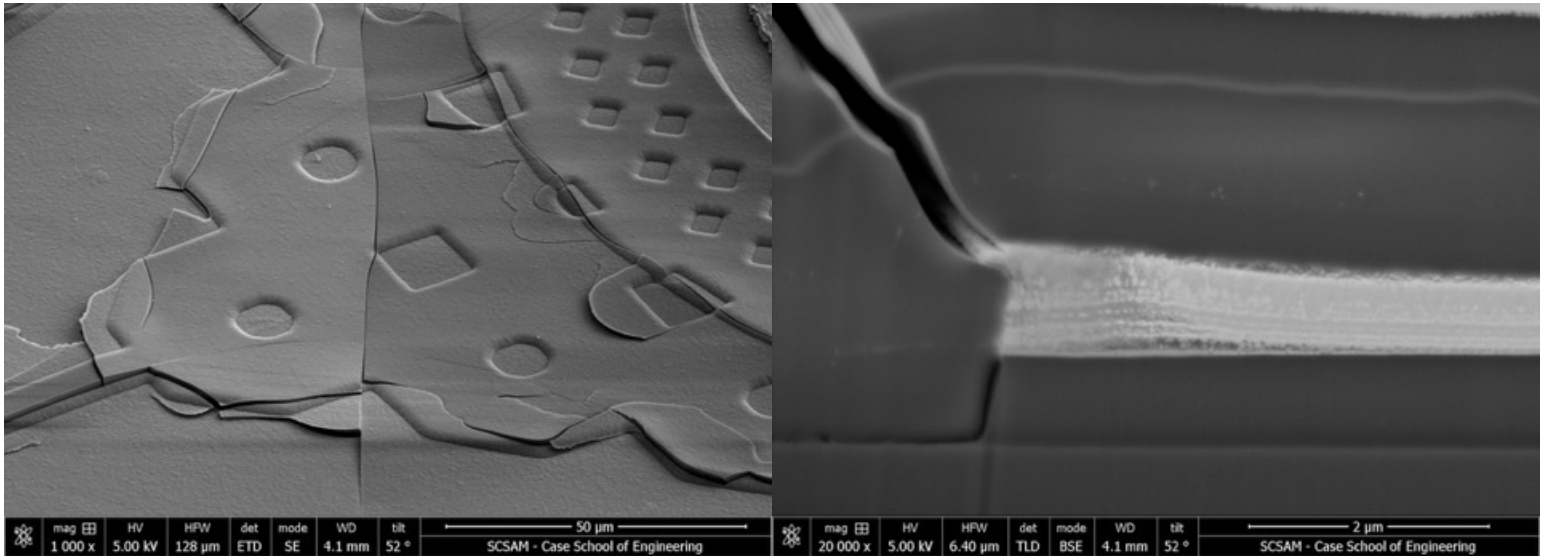
Table I. 500 °C JFET IC Test Summary

Packaged IC Sample	*r* (mm)	500 °C Time	Test Status
RAM #1	13.4	63 days	Suspended
RAM #2	6.7	420 days	Running
Clock #1	24.2	19 days	Failed
Clock #2	15.3	437 days	Running
Clock #3A	12.4	403 days	Running
Clock #3B	12.4	403 days	Running
Clock #3C	13.4	87 days	Failed



[1]P. G. Neudeck, et al., Proc. 2018 IMAPS High Temperature Electronics Conf., pp. 71-78

Cracks Observed After 727 °C Anneal in Earth Air[1]



- This IC Generation 9.2 sample was annealed at 727 °C.
- Same kind of behavior (to far lesser degree) is observed on some 500 °C annealed samples.
- At least some cracks linked to dicing, handling, design rules, and bonding.

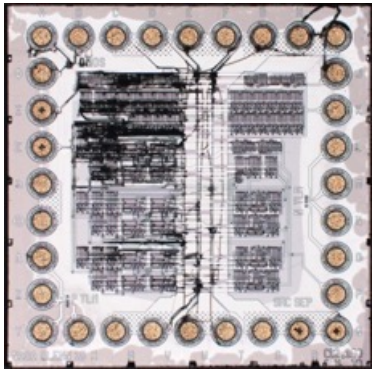
[1]D. Spry et al., Proc. SPIE vol. 9836 (2016)

10-cycle "Accelerated Aging" 720 °C Anneal Test Results[1]

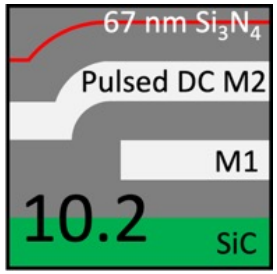
[1]D. Spry et al., Materials Science Forum, vol. 1004, pp. 1148-1155 (2020)

Cracks & Oxidation

500 °C Durable IC

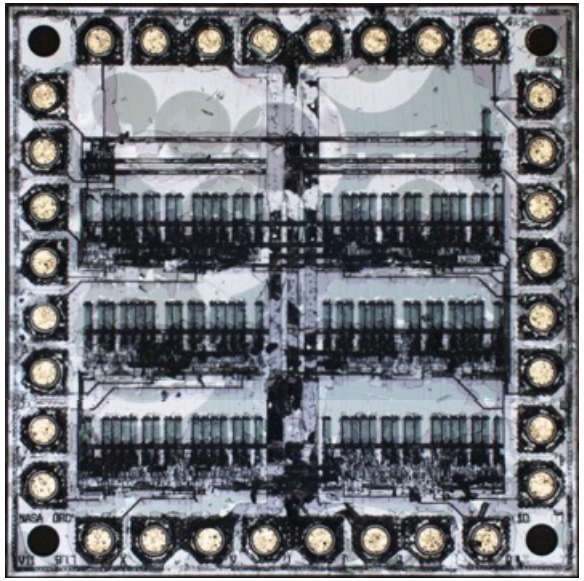


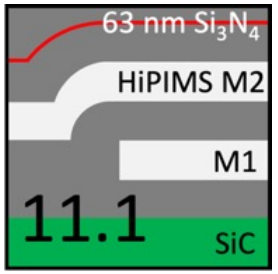
1 mm



Cracks & Oxidation

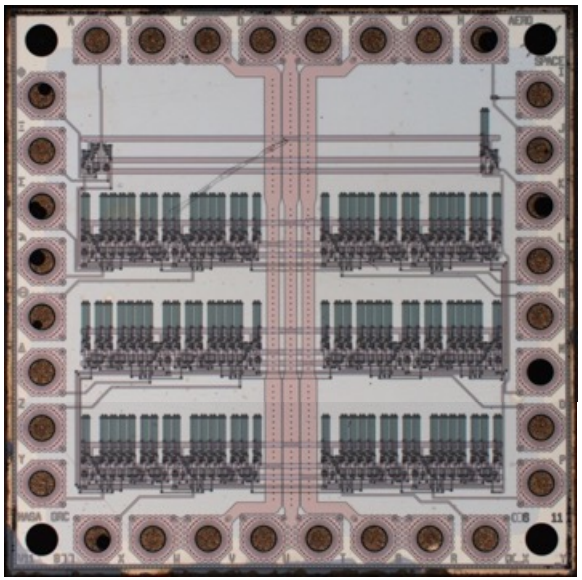
NOT 500 °C durable

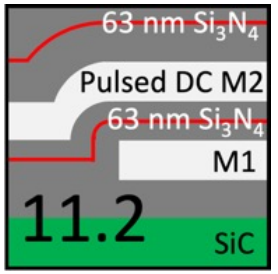




No Cracks, No Oxidation

NOT 25 °C Functional

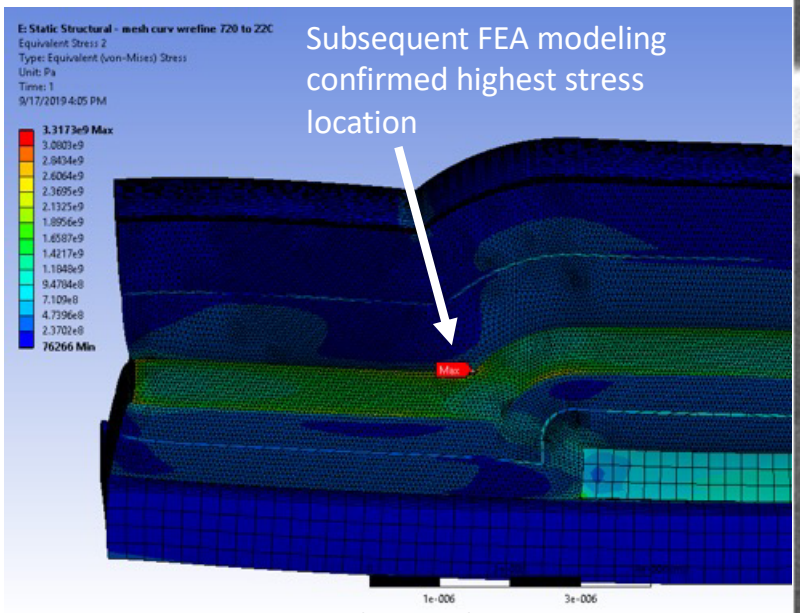




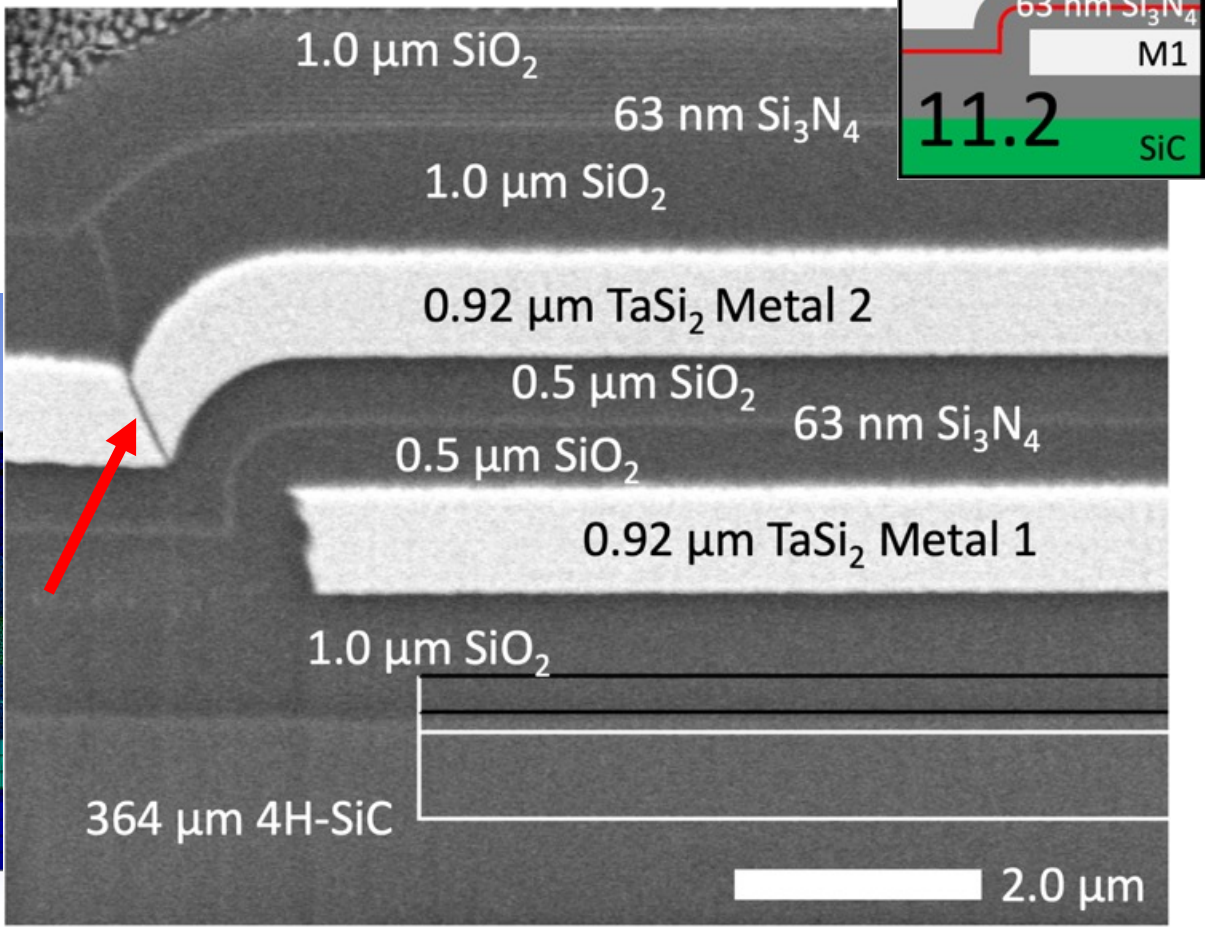
IC Prototype Wafer 11.2 – IC-Killing Metal 2 Crack

(Present in all as-fabricated 11.2 chips)

As seen in the microscopic cross-sections, metal cracks opened in all Metal2 traces running over topology during final Si_3N_4 720 °C deposition, resulting in electrical failure of all the large integrated circuits.

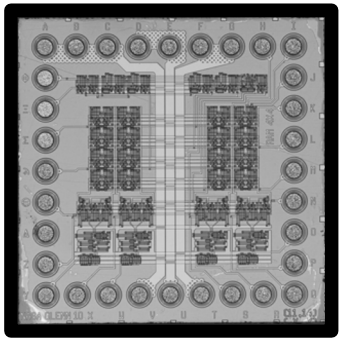


Ansys FEA by C. Chang

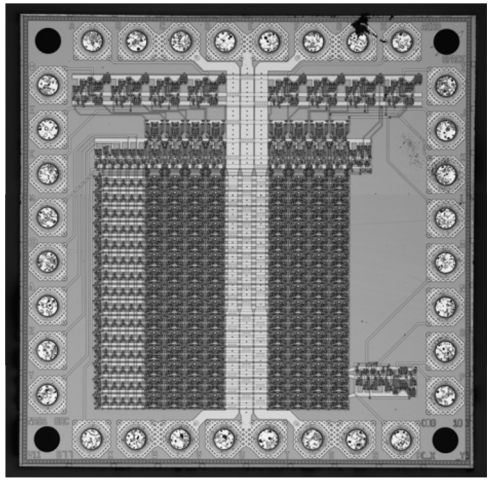


Upscaling from MSI to LSI

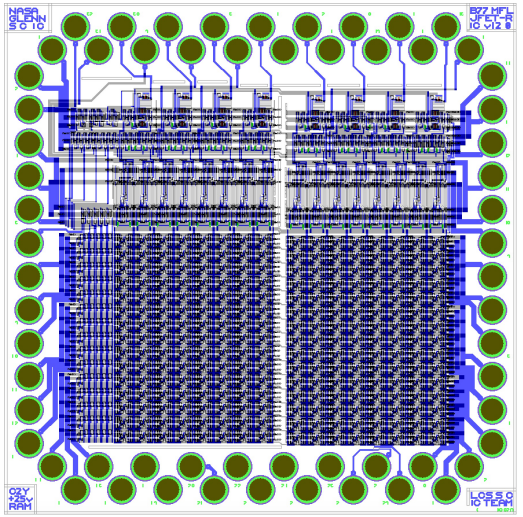
"IC Gen. 10" (2017)
16-bit RAM



"IC Gen. 11" (2018-19)
120-bit RAM, ~ 1000 JFETs



"IC Gen. 12" (2022*)
248-bit RAM, ~ 2000 JFETs



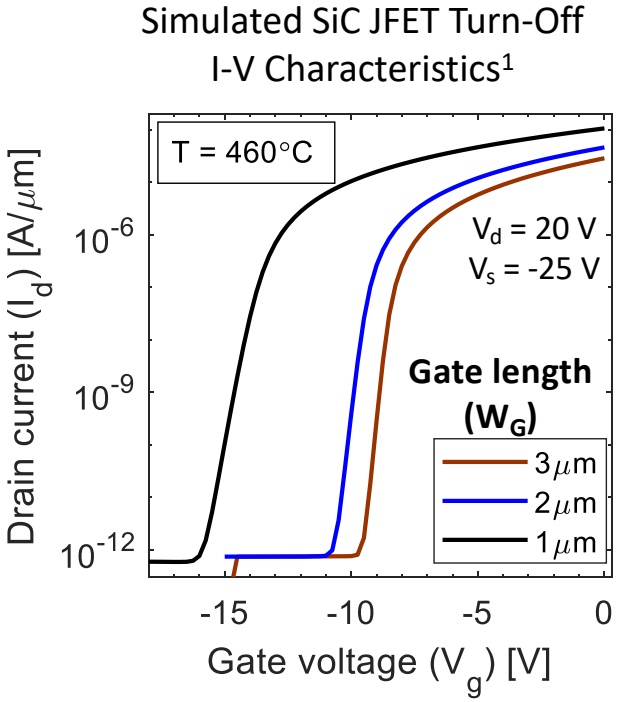
	Gen. 10	Gen. 11	Gen. 12	Gen. 13
Gate Length	6 µm	6 µm	3 µm	3 µm
Res. Width	6 µm	3 µm	2 µm	1 µm
Contact Via	6 µm	6 µm	3 µm	2 µm
JFETs/Chip	~ 200	~ 1000	~ 3000	~ 10000
Die Width	3 mm	4.65 mm	5 mm	5 mm
Year	2017	2019	2022*	2023

* Fabrication delayed by prolonged COVID-19 NASA Glenn SiC lab closure.

Shift from contact-aligner lithography to stepper lithography planned for IC Gen 13.

SiC JFET-R Scaling Limitations

10,000 JFETs/chip practical limit??



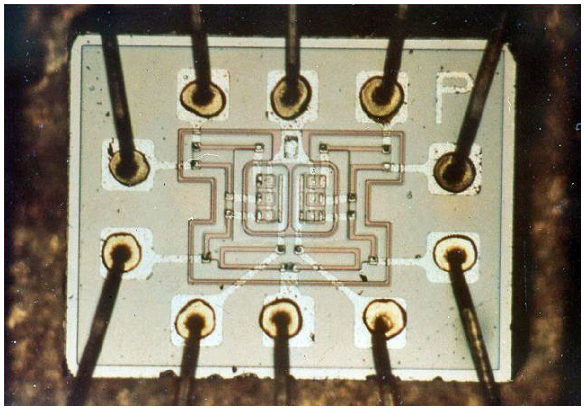
Present-day process & tolerances NOT sufficient for submicron gate length JFETs

Power density limitations (self-heating) also likely to limit JFET-R IC upscaling

Paths to further upscaling (submicron gate lengths):
- Tighter process control (including epilayers)
- Lower threshold voltage → lower supply voltage
- Alternative device topologies
    - Implanted-channel SiC JFET, III-N HFETs?

[1]Mehta, Neudeck, Lawson, Mat. Sci. Forum vol. 1062 p. 519 (2022)

“Simple” ICs Explored The Solar System



David Thornley, Computer History Museum
https://commons.wikimedia.org/wiki/File:ApolloGuidanceComputerwithDSKY.dwt.jpg

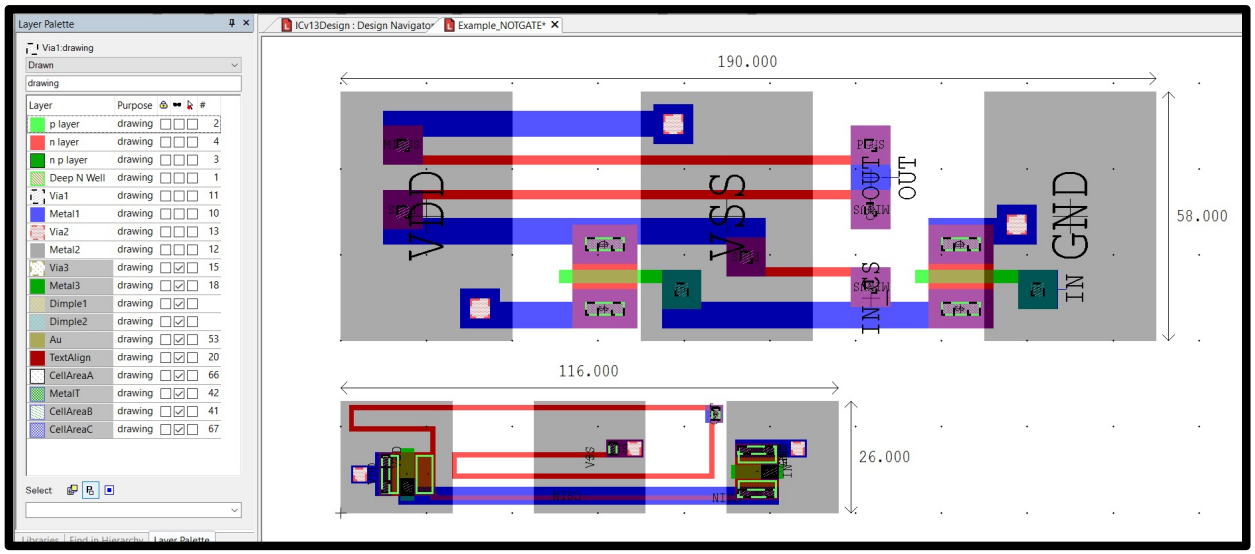
Apollo flew using 6 transistors per chip ICs.

Voyager spanned the solar system using few thousand transistors/chip ICs.

500 °C durable SiC ICs are already at mission-enabling level of complexity.

Online SiC JFET IC Design Guide

https://go.nasa.gov/jfetic



Gen. 12
NOT Gate Area
11021 µm^2

Gen. 13
NOT Gate Area
3016 µm^2

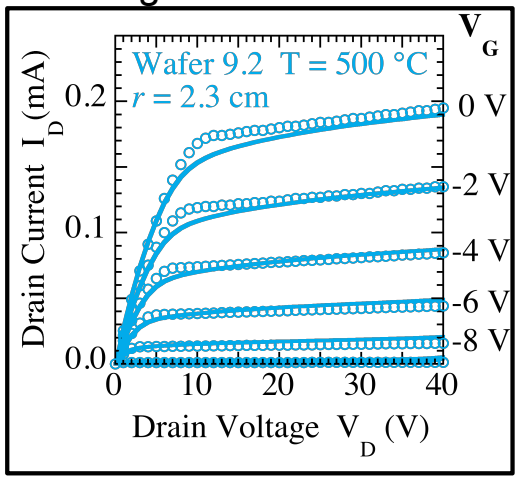
- SPICE models for circuit design and mask layout rules (Gen. 12 and Gen. 13)
- External partner IC designs are in Gen. 12 fabrication run (Space Act Agreements)
- Commercial SiC JFET-R IC design services available (https://www.ozarkic.com)

SPICE Modeling[1,2]

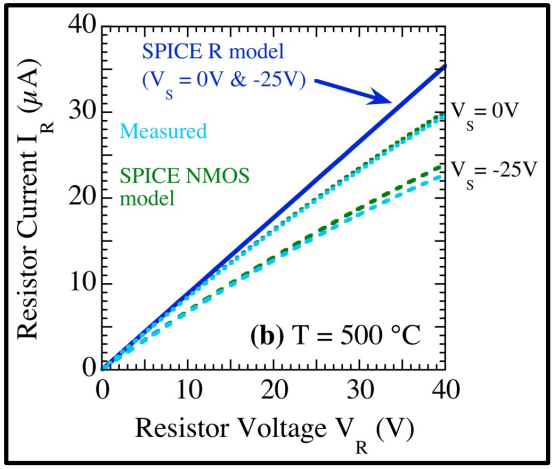
NASA Glenn models JFETs and Resistors using SPICE NMOS Level 1 device model.

- Matrix of models for key cases of temperature and wafer position.
  - Refined for each JFET-R IC generation using measurements and physics calculations.
  - First order accuracy only. Adequate given experimentally measured data scatter.
- **Substrate body bias effect very important! (Especially since substrate biased at V_{SS} ~ -25V)**

Integrated SiC JFET[1]



Integrated SiC Resistor[2]

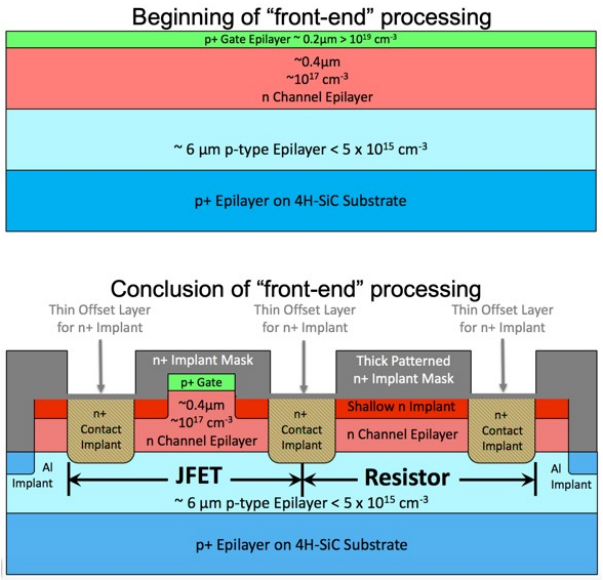


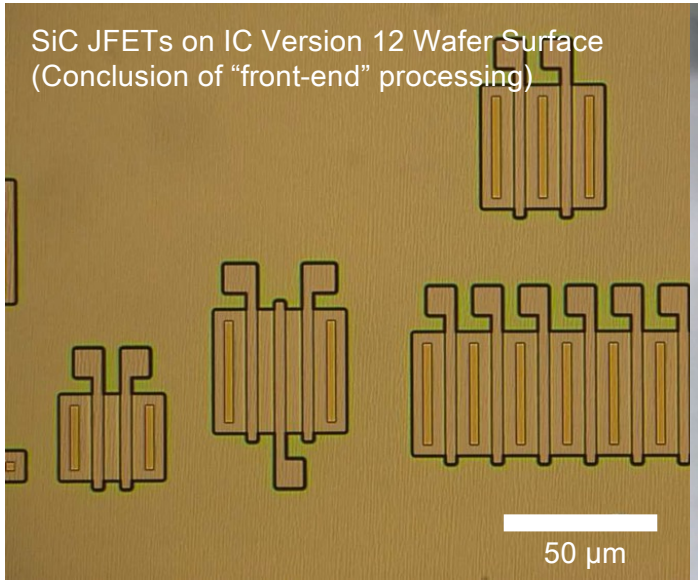
Estimated SPICE models for present NASA Glenn Generation 12 IC run and upcoming Generation 13 run posted at https://go.nasa.gov/jfetic

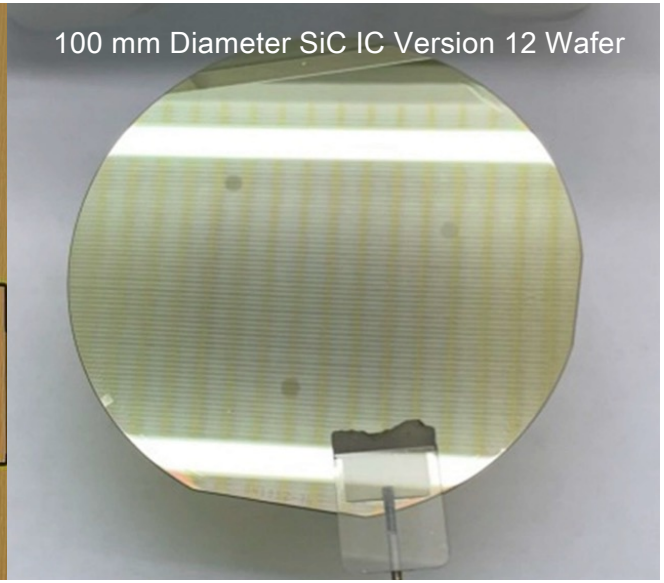
[1]P. Neudeck et al., 2016 IMAPS International High Temperature Electronics Conf. p. 263.
[2]P. Neudeck, Materials Science Forum 924 p. 962 (2018).

IC Gen. 12 Wafer Fabrication Status

- Starting SiC epi-wafers procured from Cree/Wolfspeed.
- "Front end" processing steps (that form JFETs and resistors in SiC) competitively outsourced to GE Research.
  - Conventional SiC processing steps that can be readily accomplished by commercial SiC foundries.
- Completion of 500 °C durable "back end" interconnects and bond pads delayed by COVID-19.
  - 11-month closure of NASA Glenn B77 Microfabrication Laboratory.







Revised interconnect process to be verified on SiC dummy wafers prior to implementing on IC Gen. 12 SiC epi-wafers.

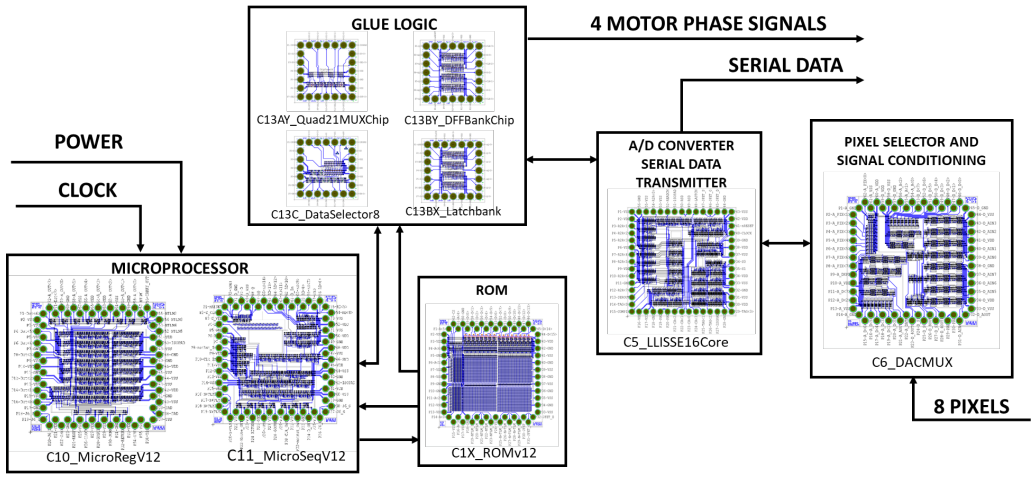
2022-23 Planned Prototype Chips and Systems

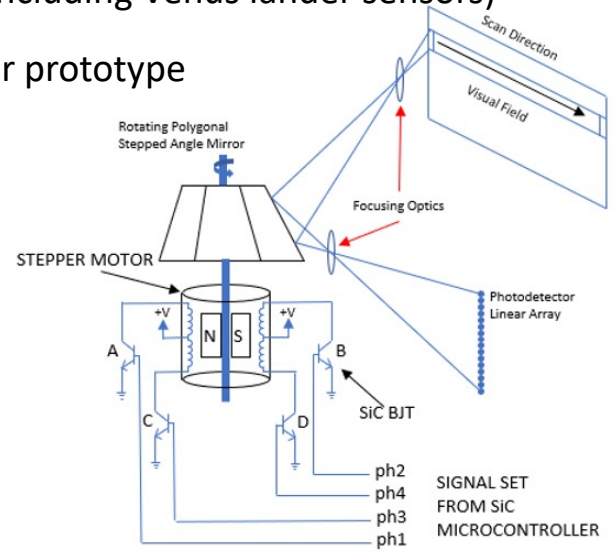
50 Application Specific Integrate Circuit (ASIC) designs are being fabricated in IC Gen. 12

Highlight SiC JFET-R IC designs enabling to unprecedented "go anywhere" durable capability include:

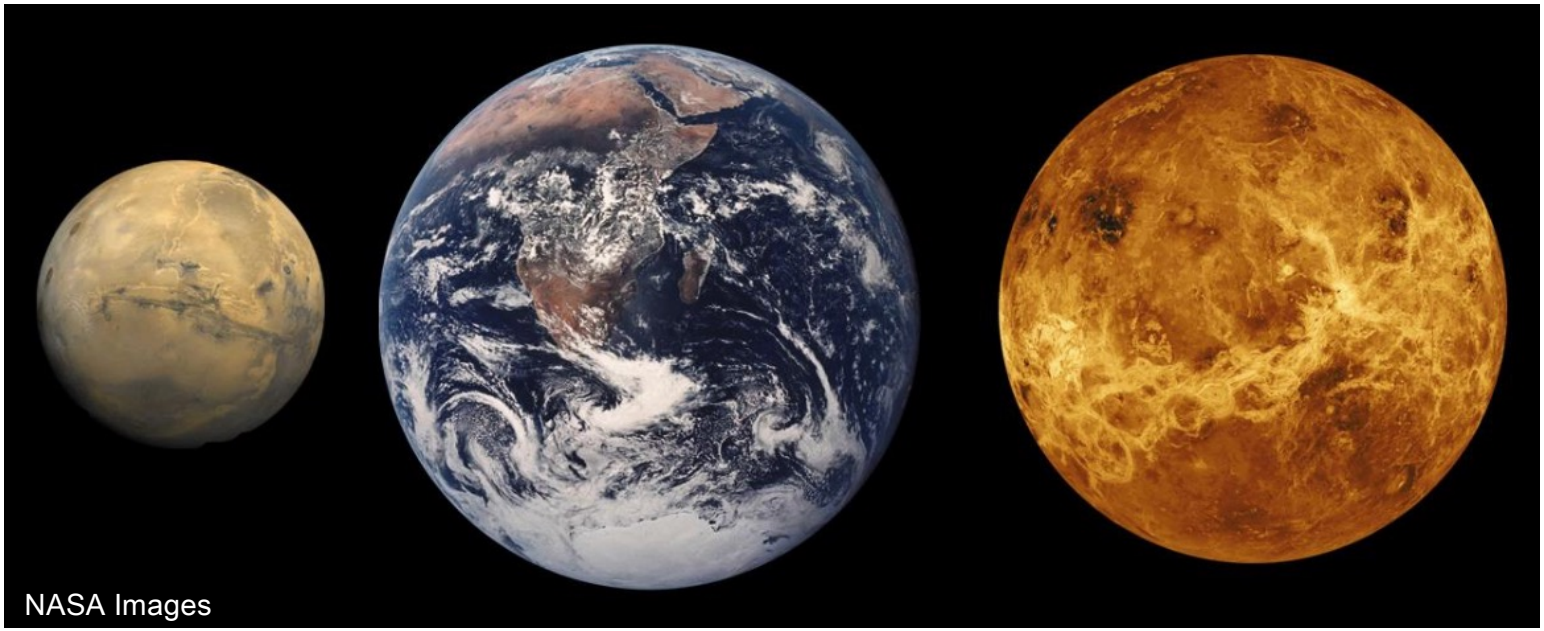
- **8-bit microprocessor dual-chip (assembly language, transport-triggered architecture)**
- 8-bit analog to digital (serial output), digital to analog
- 2-kbit ROM, 248-bit RAM, microseconds to hours clock/timer
- Variety of analog sensor-customized ASICs and amplifiers (including Venus lander sensors)

Example: Microprocessor controlled motor-driven Venus imager prototype





Which Planet is Earth's Closest Planetary Neighbor?

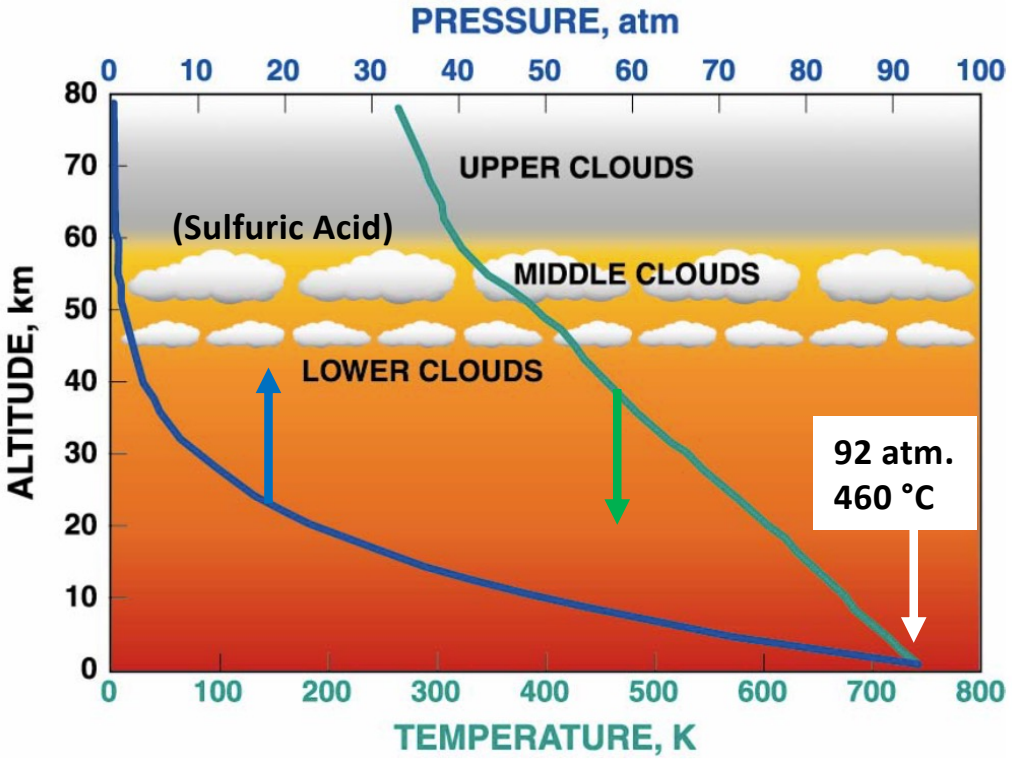


Mars
Mass: 10% Earth
Orbit: 150% Earth
T (surface): -143 °C to +35 °C
Lander Missions: **Years** of data

Venus (Radar Image)
Mass: 82% Earth
Orbit: 72% Earth
T (surface): +460 °C
Lander Missions: **Hours** of data

Surface of Venus: Toughest Place In Solar System

Combination of Temperature, Pressure, and Reactive Gas Extremes.

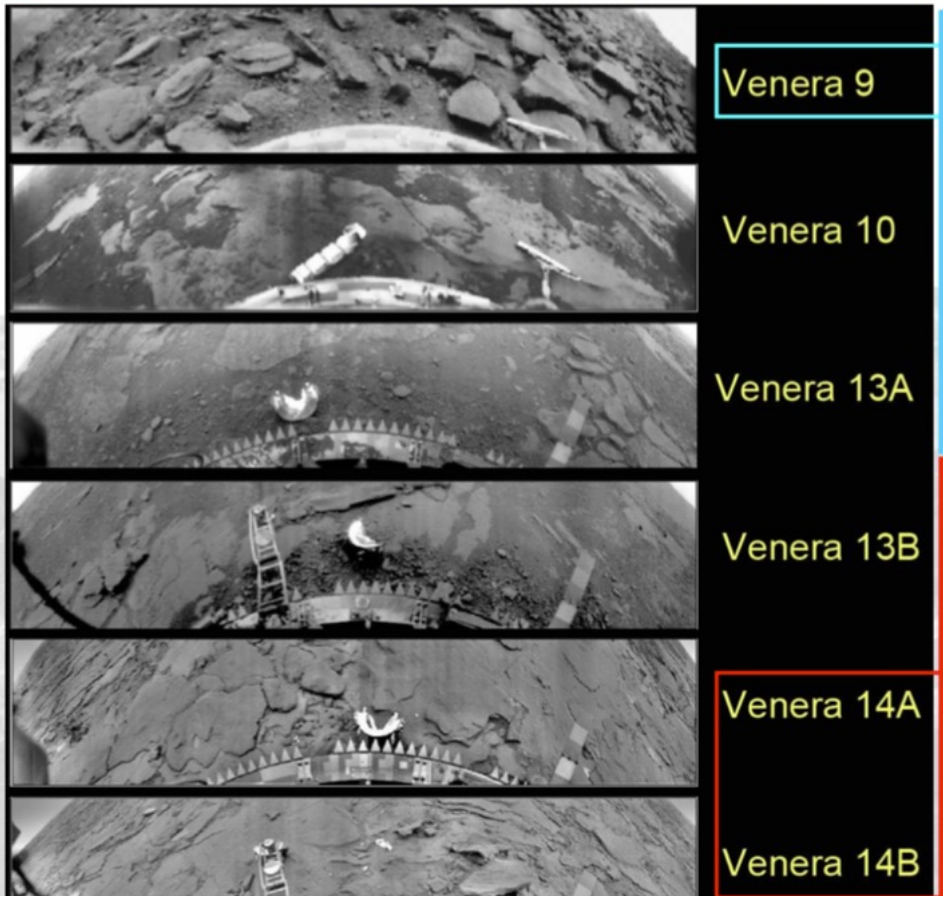


Gas Composition at Surface of Venus

Gas	Ratio
CO_2	0.965
N_2	0.035
SO_2	18.0×10^{-5}
OCS	5.10×10^{-5}
H_2O	3.00×10^{-5}
CO	1.20×10^{-5}
H_2S	0.20×10^{-5}
HCl	5.00×10^{-7}
HF	2.50×10^{-9}

Figure modified from E. Kowala et al., Extreme Environment Technologies for Future Space Science Missions, NASA Jet Propulsion Laboratory, Pasadena, CA, USA, 2007, Report JPL D-32832. p. 49.

Past Missions:
Close-up Surface Features on Venus (USSR)



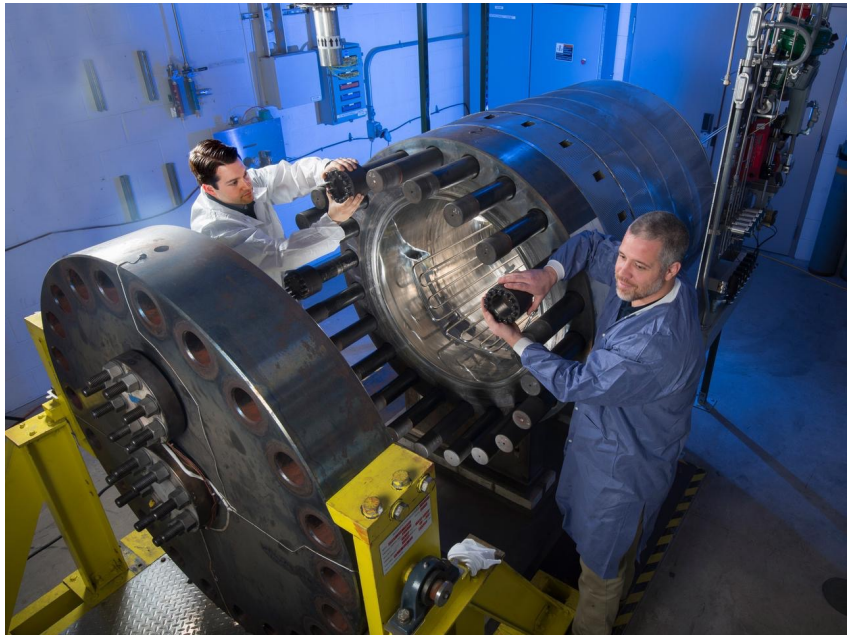
Source: https://www.lpi.usra.edu/vexag/chapman_conf/presentations/ocampo_for_saunders.pdf

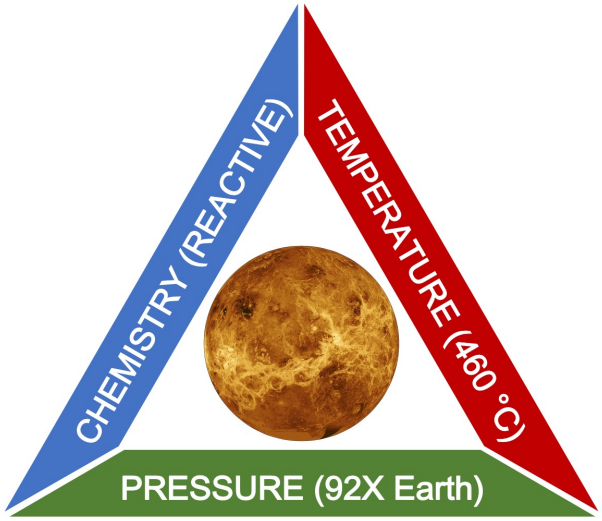
4

NASA Glenn Extreme Environment Rig (GEER)

https://www1.grc.nasa.gov/space/geer/

800-liter test chamber for high-fidelity simulation of Venus surface environment





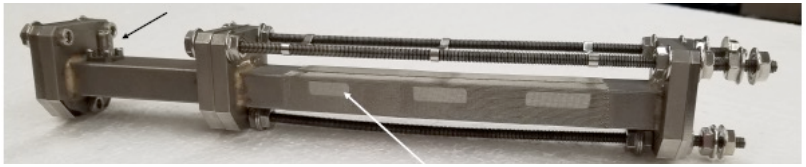
- **First 10 chemical constituents of Venus atmosphere.**
- 460 °C (860 °F), 1350 psia (~ 92 Earth atmospheres).
- Long duration (months) test runs.

NASA Glenn GEER Testing Experience

Full surface conditions (including gas composition to small concentrations) is relevant!

Many commonly-used elements react badly. **Sufidization instead of oxidation.**

Encapsulation/passivation of parts against Venus surface atmosphere is problematic.



Before Test

After Test

Venus Atmosphere

Gas	Ratio
CO_2	0.965
N_2	0.035
SO_2	**18.0×10^{-5}**
OCS	**5.10×10^{-5}**
H_2O	3.00×10^{-5}
CO	1.20×10^{-5}
H_2S	**0.20×10^{-5}**
HCl	5.00×10^{-7}
HF	2.50×10^{-9}

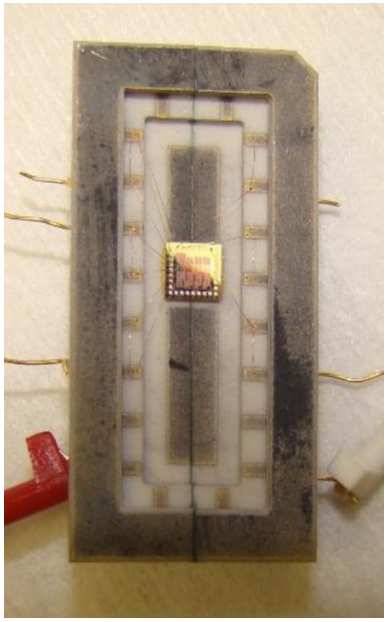
Large sulfide crystals formed on metal-alloy waveguide exposed to Venus surface conditions for 60 days in GEER.

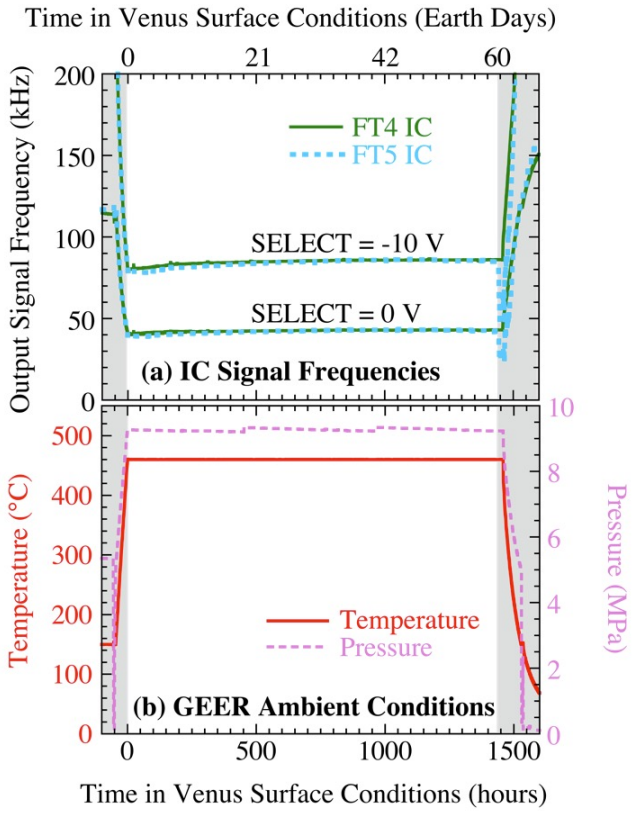
60-Day Venus Environment IC Test (in GEER)[1,2]

Two Generation 10 ÷2/÷4 Clock ICs (175 JFETs/chip) successfully operated in GEER Venus surface conditions for 60 days duration (lidless package).

Before GEER

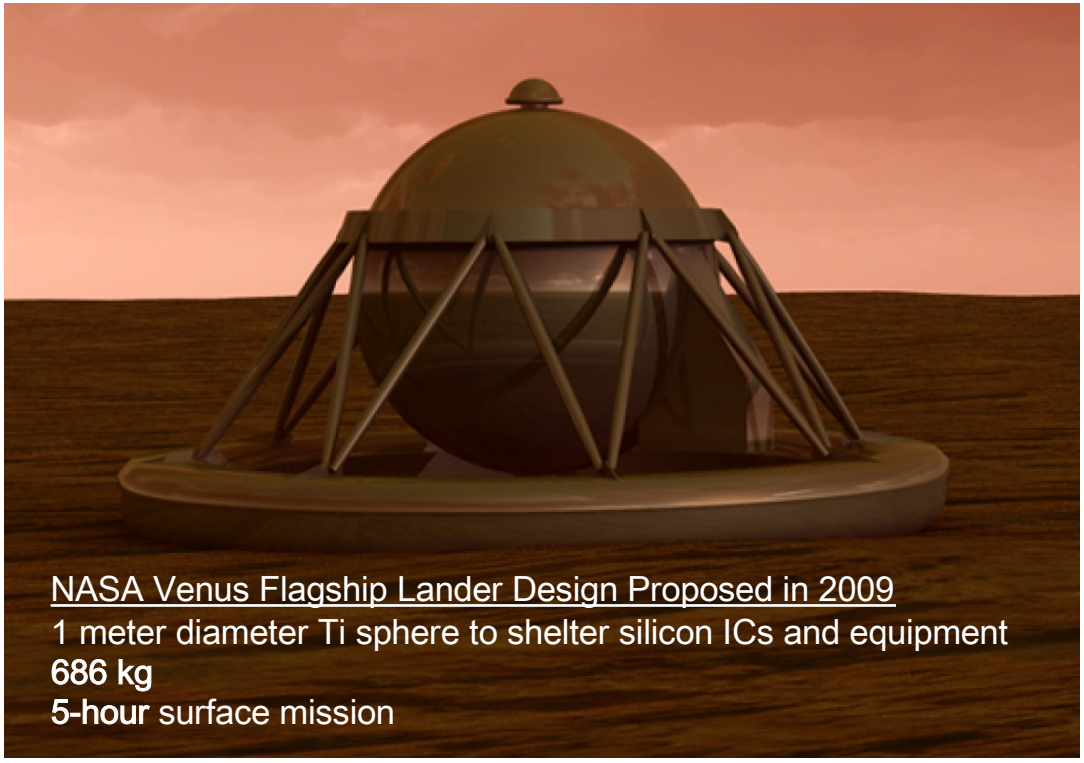
After 60 days GEER





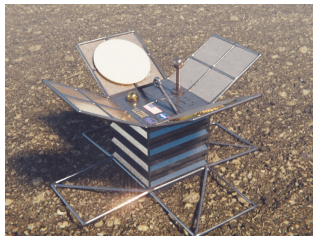
[1]Neudeck et al., IEEE J. Electron Devices Soc., vol. 7, p. 100 (2018).
[2]Chen et al., Proc. 2018 Int. High Temperature Electronics Conf.

Impact of Extreme Environment SiC Electronics



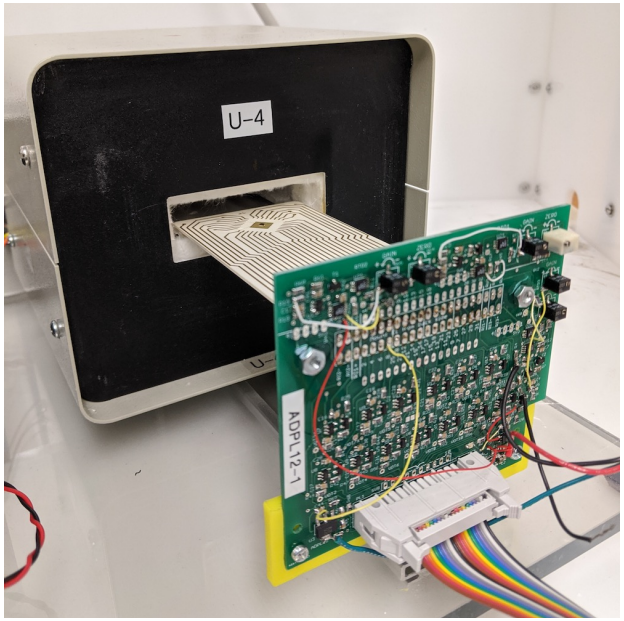
NASA Venus Flagship Lander Design Proposed in 2009
1 meter diameter Ti sphere to shelter silicon ICs and equipment
686 kg
5-hour surface mission

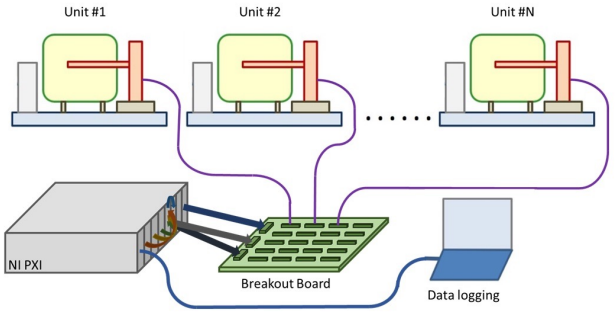
New Venus Lander Concept
Unsheltered SiC ICs
< 20 kg (mostly battery)
60-day surface mission



Completely new engineering approach enabled by Venus-durable SiC ICs.

Electronics Qualification for Long-Term 500 °C Operation





Aerospace & automotive electronics qualification processes practiced for decades need to be extended/adapted to cover much higher temperature

- Testing statistics (parallel testing)
- Chips, packages, and multi-chip circuit boards
- Temperature acceleration, voltage/current acceleration
- Repeated thermal cycling and shock testing
- Vibration testing at high temperature
- **Failure mechanism documentation & understanding**

NASA Glenn expansion of parallel testing capacity using "small pizza oven" concept[1]
- Chip (+ package) on ceramic board inserted into oven slit.
- Goal is 50 parallel IC tests with rapid thermal cycling.

[1]Izadnegahdar et al., 2021 IMAPS Int. High Temperature Electronics Conf., pp. 76-82

500 °C Durable Electronics Technology Gaps

(Priorities to be addressed)

SiC JFET-R is confined to relatively low operating frequency (few MHz at most)
- Other technologies (e.g., SiC BJT) needed for ≥ 100 MHz (e.g., RF transmitter)

SiC JFET-R is “normally on” device poorly suited for power switching & management
- Other technologies (e.g., SiC BJT) needed for “normally off” high power switching
- High-voltage (kV) high-current (10-100A) 500 °C durable chip packaging not demonstrated

SiC JFET-R logic requires more than 10-fold higher power than complementary (CMOS) logic

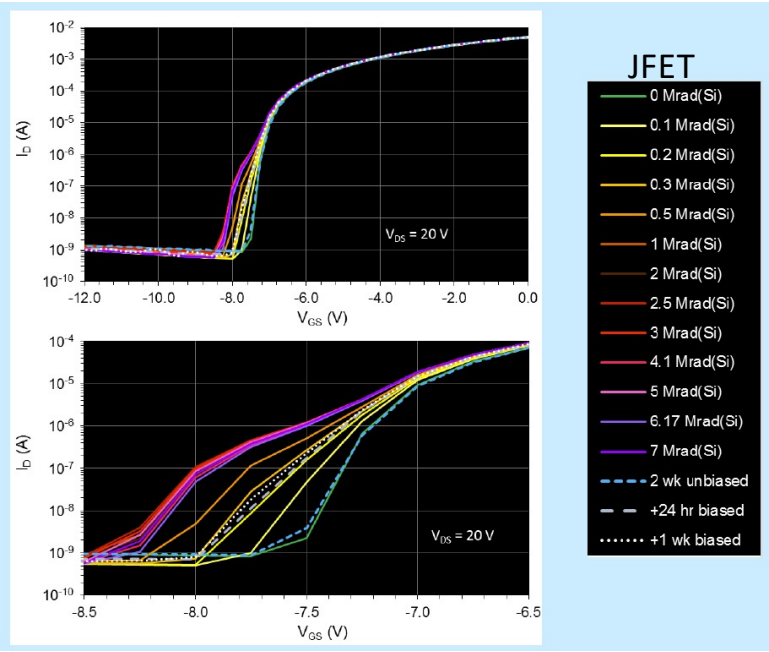
500 °C durable memory is primitive compared to modern room-temperature memories
- Less than 1 kbit/chip, mW/bit RAM storage power, mask-programmed ROM
- Electronically burnable 500 °C durable non-volatile memory/FPGA yet to be demonstrated

500 °C durable “quartz crystal” like timing reference clock has yet to be demonstrated
- SiC JFET-R ring oscillators are non-precise, though stable to within 10%

Radiation Testing of NASA Glenn JFET ICs[1]

Generation 10 JFETs, Oscillators, Flip-Flops, Op-Amps tested by NASA Goddard

Total Ionizing Dose (Gamma)



Single Event Effects (Heavy Ion Strike)

Ring Oscillator

- No destructive effects at LET(Si) = 86 MeV-cm²/mg
- Only small glitches recorded

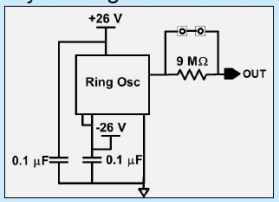


Fig.16. Ring oscillator test circuit.

Summary

Prototype 4H-SiC JFET ICs developed & fabricated at NASA GRC for harsh Venus conditions demonstrate potential for Jovian-type environments as well:

- **> 7 Mrad(Si) TID tolerance**
- **No destructive SEE at LET(Si) = 86 MeV-cm²/mg**
- **SEUs occurred in the clock circuit**
  - **3.5 MeV-cm²/mg ≤ onset LET(Si) ≤ 9.6 MeV-cm²/mg**

[1]Lauenstein et. al., 2019 IEEE Radiation Effects Data Workshop (REDW)

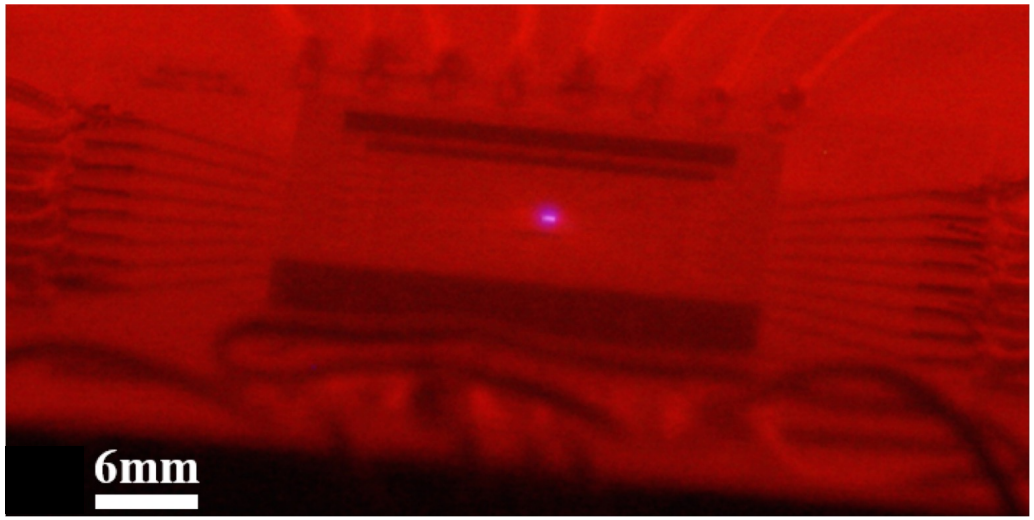
Juno Mission Electronics Vault

https://www.nasa.gov/mission_pages/juno/news/juno20100712.html
https://en.wikipedia.org/wiki/Juno_Radiation_Vault

- Anticipated mission total ionizing dose near 20 Mrad(Si).
- The vault weighs about 200 kg, comprised 1 cm thick titanium walls.

Summary

SiC JFET-R ICs now demonstrating application-viable prolonged functionality in previously inaccessible extreme temperature environments.

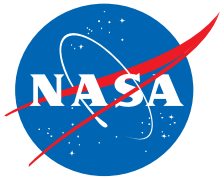


Potentially "Go Anywhere" ICs

- High temperature +500 °C
- Low temperature -190 °C
- High radiation 7 MRad(Si)
- Venus surface +460 °C
- Analog and digital
- Ceramic packaging

Important new extreme environment operational capability becoming available.

https://go.nasa.gov/sic
https://go.nasa.gov/jfetic


NASA