Pt/HTCC Alumina based Electronic Packaging System and Integration Processes for High Temperature Harsh Environment Applications

Liang-Yu Chen[1,a], Philip G. Neudeck[2,b], David J. Spry[2,c], and Gary W. Hunter[2,d]
[1] Ohio Aerospace Institute/NASA Glenn Research Center, 21000 Brookpark Road, Cleveland, Ohio 44135
[2] NASA Glenn Research Center, 21000 Brookpark Road, Cleveland, Ohio 44135
[a]Email: liangyu.chen-1@nasa.gov, [b]Email: neudeck@nasa.gov, [c]Email: david.j.spry@nasa.gov,
[d]Email: gary.w.hunter@nasa.gov

Abstract

Electronic devices capable of operation at 500°C are required for long term Venus surface missions, as well as for *in situ* monitoring and control of next generation aeronautical engines. High temperature sensors and electronics can also find many applications in military, and energy and automobile industries. Various silicon carbide (SiC) sensors and electronic devices have been developed for operation at 500 °C, and a compatible packaging system is needed for long term test and deployment of these high temperature devices. High temperature co-fired ceramics (HTCC) alumina with platinum (Pt) conductor was proposed for high temperature electronic packaging. A prototype Pt/HTCC alumina packaging system including chip-level package and circuit board has been briefly reported previously for long-term electrical testing of SiC integrated circuits at 500 °C, and brief testing at much higher temperatures. HTCC alumina is an excellent dielectric material with acceptable dielectric constant and low dielectric loss over wide temperature and frequency ranges. Pt is chemically noble and can be co-fired with HTCC alumina in air ambient producing a viable electronic packaging material system for high temperature applications. This paper presents a more detailed description of this packaging system including prototype low power packages and circuit boards based on HTCC alumina and Pt metallization for 500°C and other harsh environment applications. The key technical considerations for chip-level packaging and circuit board assembly, including materials and processes for 500 ˚C durable wire-bonding and SiC die attach, and integration of multi-chip circuit boards, are presented. Experimental test results of this packaging approach applied to SiC integrated circuits at 500 ˚C and 700°C are discussed as well.

Keywords: High temperature, electronic packaging, HTCC, Venus, SiC, harsh environment.

1. Introduction

Different kinds of ceramic substrates and Au thick-film metallization based electronic packages and circuit boards were previously developed for testing silicon carbide (SiC) high temperature electronics for NASA space and aeronautical applications [1, 2a, 2b, 3a, 3b]. These ceramic materials have different mechanical and electrical advantages for different packaging needs, including 90% alumina with relatively lower hardness and fabrication cost, and aluminum nitride with closer thermal expansion coefficient to SiC, and 96% alumina with better dielectric performance at high temperatures. A prototype 96% alumina packaging system successfully facilitated 500°C electrical test of SiC electronics at 500 °C for over 10,000 hours in air ambient. However, the fabrication process for these pre-fired ceramic substrates based ceramic packages is not compatible with current co-fired technology based packaging industry process [4]. In order to solve this issue, the dielectric performance of a selected HTCC alumina was tested and compared with pre-fired 96% alumina as well as other selected cofired alumina [5]. HTCC alumina was selected due to its dielectric performance for further 500 °C packaging testing. A prototype Pt/HTCC alumina chip -level package with 32-I/O was fabricated and dielectrically characterized at low frequencies up to 1 MHz in a temperature range up to 550 °C indicating its applicability for many envisioned SiC ICs [6]. Various SiC JFET based analog and digital ICs have successfully been packaged and long term tested at 500 °C with this package, and short term tested above 800 °C, all in oxidizing air ambient [7a, 7b, 7c]. An experimental Pt/HTCC alumina package also facilitated 60 earth days test of a SiC JFET IC in high-fidelity simulated Venus surface environment [8].

The Pt/HTCC alumina packaging system that facilitated these SiC IC tests includes a chip-level package on a circuit board, as well as a compatible integration process steps including die-attach, wire-

bonding, component attachment, and I/O wire attachments to the circuit board [6]. This paper provides detailed information on chip-level packaging and circuit board assembly steps not disclosed in our previous publications.

2. Chip-level Package

A commercially fabricated 32-pin Pt/HTCC alumina package with an attached and wire-bonded prototype SiC chip is shown in the center of Figure 1. Figure 1 also shows the package attached to a ceramic circuit board with gold wire attachments (that is detailed in Section 3). Pt is used for both surface (and interlayer) metallization, and the hermetically sealed conductive via of the package [9]. The package is fabricated using a commercial HTCC process, except firing in air instead of noble environment necessary for co-firing reflective metal-based conductors [9]. This package is designed for low power and low frequency SiC JFET based high temperature durable ICs intended for prolonged operation around 500 °C. It is a surface-mount package with 32 Input/Outputs (I/Os) and it measures about 27.3 mm x 27.3 mm x 2.5 mm (1.07 in. x 1.07 in. x 0.1 in.).

The Pt surface metallization of the package floor is composed of a central square and four surrounding L-shaped patterns (not apparent in Fig. 1). This allows a multi-chip mixture with individual substrate bias of up to five separate IC dies in a single package. Pt pads for wire-bonding (visible in Fig. 1) are electrically connected to the Pt pads on the bottom side of the package through hermetic Pt via. The pads on the bottom of the package for surface mount measure 1.27 mm x 2 mm, and the spacing between two neighboring pads along the same edge is 1.27 mm. This spacing between two neighboring pads are relatively large compared to conventional packages towards accommodating the increasing dielectric loss of the ceramic matrix with temperature [5].The package can be capped/sealed with a compatible lid (not shown in Fig. 1) that is 1.02 mm (40 mil) thick. The first pad clockwise from the notch, shown in Figure 1, is connected to the pad or ring (two different designs) for connection to possible lid metallization for electrically surrounding/shielding the IC chip with conductor if desired.

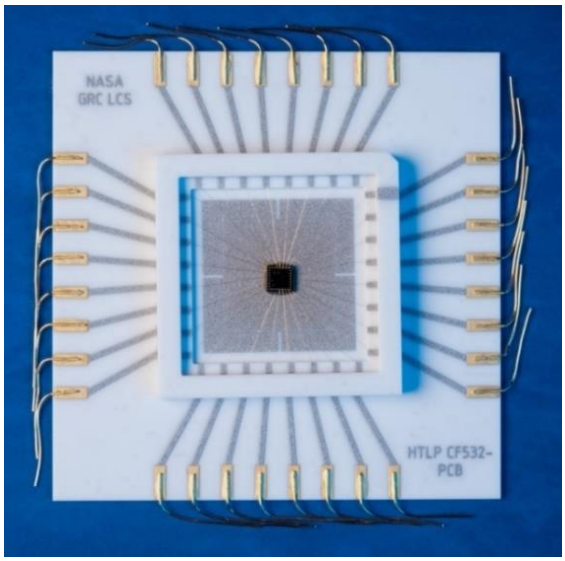

Figure 1: The picture of top view of 32-pin co-fired Pt/92% alumina package measured 27.3 mm x 27.3 mm x 2.54 mm (1.07 in x 1.07 in x 0.1) with a SiC IC, the circuit board measured 5.1 cm x 5.1 cm x 0.64 mm (2 in. x 2 in. x 25 mil). 32 I/O wires attached to the circuit board.

The electrically measured parasitic parameters between two sets of neighboring I/Os are shown in Tables 1 and 2 [6]. The parasitic capacitance (upper number) in unit of pF and parallel AC conductance (lower number) in unit of μS between I/O1 and neighboring I/O2 with I/O1 connected to all of five metallization pads on the package floor using wire-bonding.

Table 1: Parasitic capacitance (upper) in unit of pF and AC conductance (lower) in unit of μS between I/O1 and I/O2 without a lid on. I/O1 is connected to ground pads. Contributions of gold wires have been subtracted [6].

T (°C) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
120	1.0	0.7	0.6	0.4	0.3	0.5	0.4	0.6	0.7	1.4	1.4
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.001	<0.001
1K	0.4	0.2	0.5	0.5	0.3	0.4	0.5	0.5	0.5	0.5	0.4
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
10K	0.5	0.4	0.5	0.5	0.4	0.4	0.4	0.5	0.5	0.4	0.4
	<0.001	0.0013	<0.001	<0.001	<0.001	<0.001	<0.001	0.003	<0.003	<0.003	<0.003
100K	0.5	0.3	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.4
	0.01	0.016	0.014	0.016	0.016	0.011	0.014	0.029	0.035	0.026	0.045
1M	0.5	0.4	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.5
	<0.010	<0.010	0.013	0.012	0.011	0.006	0.009	0.018	0.021	0.022	0.026

Table 2: Parasitic capacitance (upper) in unit of pF and AC conductance (lower) in unit of µS between I/O2 and I/O3 without a lid on. Contributions of gold wires have been subtracted [6].

T (°C) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
120	0.7	0.6	0.5	0.4	0.3	0.4	0.4	0.6	0.5	0.6	0.6
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
1K	0.3	0.3	0.4	0.4	0.2	0.4	0.3	0.5	0.3	0.5	0.5
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.0013	0.001	<0.001
10K	0.4	0.3	0.4	0.4	0.3	0.3	0.4	0.4	0.4	0.4	0.3
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
100K	0.3	0.3	0.4	0.4	0.2	0.3	0.3	0.4	0.4	0.4	0.3
	0.005	0.005	<0.005	<0.005	<0.005	0.005	0.013	<0.010	0.014	0.012	<0.010
1M	0.3	0.4	0.4	0.4	0.2	0.3	0.3	0.4	0.4	0.4	0.3
	<0.010	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020

The measured parasitic capacitance is between 0.3pF and 1.4pF, generally trending higher at lower frequencies and higher temperatures with the peak capacitance measured at 120 Hz and 500 °C and 550 °C. The measured parasitic conductance is 0.035 µS (at 100kHz 450 °C) or less, between room temperature and 500 °C, generally trending higher at higher frequencies and higher temperatures with the peak capacitance at 100 kHz and 450°C. The parasitic parameters between other neighboring I/Os (e.g., I/O2 to I/O3 parameters shown in Table 2) are generally lower than those for I/O1-I/O2 since I/O1 is connected to a much larger metallization area. These data indicate that this package provides satisfactory electrical functionality and performance for deployment of low-power and low-frequency SiC ICs for 500 °C applications.

Figure 2 shows the I-V curves measured between I/O27 and I/O28 (counting clockwise from the package notch shown in Figure 1) initially at 500 °C (blue) and then at 69.4 hours (red) after the initial measurement. The slopes of linear fits of these I-V curves measure the DC resistances of the pair neighboring I/Os. The insulation resistance initially at 500 °C is approximately 7.6 GΩ, increasing to 9.7 GΩ after 69.4 hours at 500 °C. Since I/O27 was connected to a SiC chip and the package and I/O28 was connected to the circuit board only, and the package was mounted on a ceramic circuit board, these DC resistance measurements can be expected to slightly overestimate the package DC resistance between two neighboring I/Os due to the leakages through other package pads, circuit board, and wiring.

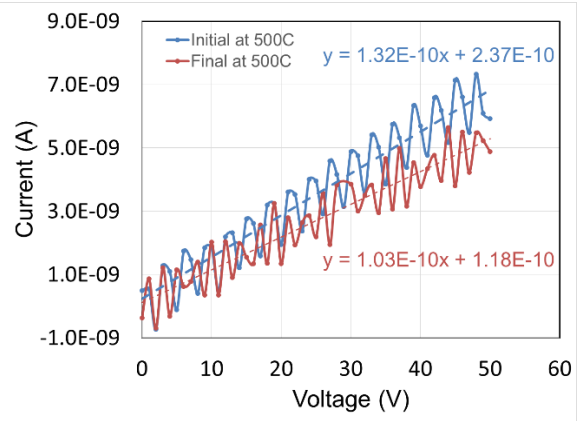

Figure 2: I-V curves measure between I/O27 –I/O28 of the co-fired package at initially at 500°C (blue) and 69.4 hours after (red). The noise was attributed to interference from the running oven. The dash lines are the linear fits [6].

3. Circuit Board Assembly / Packaging

The single side metallized Pt/HTCC alumina circuit board, shown in Figure 1, interconnects the chip package with a SiC IC to the testing instruments outside the oven. The board measures 5.1 cm x 5.1 cm x 0.64 mm (2 in. x 2 in. x 25 mil). The board has 32 Pt pads matching those of the package for electrical connections. The pads on the board may be Au coated, but that is not generally assumed below. For reasons discussed in Section 5, the overall packaging / assembly process is non-conventional in the sense that it starts with I/O wire attachments to the circuit board (Section 3.1), followed by package attachment (Section 3.2), then die attachment (Section 3.3), and finally wire bonding (Section 3.4). This is described below.

3.1 I/O Wire Attachment

A glass-binder(s) free thick-film Au paste, DuPont 5063D [10], is used for brazing. DuPont 5063D doesn't contain glass-based binder(s), so additional Au paste material won't generate excessive binder which can detrimentally become mobile at high temperature and electric bias [11].

The approach is to braze Au wires on Au coated Pt metallization pads along four edges of the ceramic circuit board. Pt pads of co-fired ceramic board are first manually coated with DuPont 5063D layer, then dried in an oven at 150 °C for 10-15 minutes (min.) in air. Both the metallization pad and Au wire are then coated with DuPont 5063D paste. For this special step, the viscosity of commercial DuPont 5063D needs to be increased by reducing the amount of organic carrier component in the paste. This can be accomplished by draining 10% to 15% of the carrier (fluid), after the solid particles in the paste precipitated (settled to the bottom of the container) after storage, or by using a centrifuge. While the Au paste on both the pad and wire are still wet, the Au wire is placed flat onto the pad with Au paste covering both Au wire and vicinity pad surfaces. The assembly is heated at 150 °C for about 15 min. to dry the Au paste, then immediately heated up to 850 °C for a 20 min. bake to solidify the Au paste. The baking can be done in a belt oven or a box oven in air ambient. If a belt oven is used, the temperature profile suggested by the thick-film manufacturer datasheet [10] should be used. Figure 1 shows 32 Au wires with diameter of 10 mil attached to the pads at four edges of the Pt/HTCC alumina board using this procedure.

3.2 Package Attachment

Package attachment process is very similar as that used for attaching Au wires. This involves the Pt pads on the package, and those on the circuit board that provide for package mechanical attachment and electrical connections. The Pt pads of both the package and the circuit board are separately coated with DuPont 5063D first. Both parts are heated to 150 °C for 10-15 min. to dry the paste followed by heat treatment at 850 °C for 15 min. in air. In order to improve mechanical strength of the attachment, sometimes additional matching mounting pads (not part of the electrical circuits) on both package and circuit board are used to increase attachment area.

The package pads then mate with the circuit board pads for attachment and interconnection. The Au thick-film coated pads on circuit board are coated with DuPont 5063D again. While this 2nd paste is still wet, the package is placed onto the board with horizontal alignment to match pads. The assembly is then dried at 150 °C first for 10-15 min. followed by 20 min. final heat treatment at 850 °C in air ambient. The oven is naturally cooled.

3.3 SiC Chip Die-attachment

It is important to note that the SiC chip backside in our work is a wafer-manufacturer polished carbon-face surface blanket coated with "IrIS" bond pad metal stack [7d] and 1 um thick electron-beam evaporated gold layer. The wafer is annealed at 720 °C in nitrogen tube furnace as the last step in the SiC IC wafer fabrication process prior to diamond-saw dicing of the wafer [7b].

The Pt die-attach pad of co-fired Pt/HTCC package is coated with a layer of Au thick-film paste of DuPont 5063D using either stamping or micro-dispensing using a die bonder (die bonding machine). The coating area is about or slightly bigger than the SiC IC die footprint as shown in Fig. 3. An Au coat layer thickness, after firing, of ~10 microns is appropriate [10]. After the printing, the assembly is settled in air for 15 min., then dried at 150 °C followed by firing at 850 °C in air with temperature profiles dependent on the heating method. If a belt oven is used for drying and firing, the standard temperature profile recommended on the manufacturer data sheet for the paste material should be used [10]. If a box oven is used to heat the die-attach assembly, the oven temperature is raised to 150°C at a rate of 40 °C/minute and dwelled at 150 °C for 20 minutes to dry the paste layer, then the temperature immediately is raised to 850 °C with a ramp rate of 40°C/min and dwell at 850 °C for 20 min, in air. The box oven cooling process can thereafter be natural. Electrolysis Au coating on Pt surface can also be used to replace the first step of Au thick-film process above; our newly made packages are electroplated with Au.

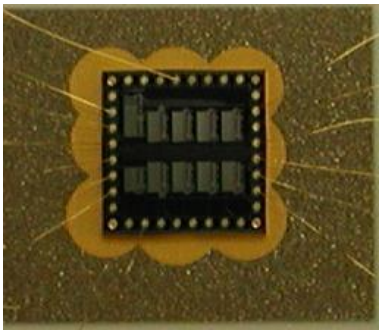

Figure 3: A 4.65 mm x 4.65 mm SiC JFET IC die attached to Pt/HTTC alumina package with Au thick-film paste- DuPont 5063D.

After the first gold coating and firing of the die attach region is finished, a second layer of DuPont 5063D is applied using stamping or micro-dispensing (through a die-bonder again). For this second application, DuPont 5063D needs to have above normal viscosity as described in Section 3.1. The coating area is again about or slightly larger than the SiC IC die foot- print. While the Au paste is wet, the SiC IC die is picked up and placed onto the wet Au paste pad. The distance between the backside IC die

from the solid surface of Au/Pt/HTCC alumina surface (after the first Au layer coating) determines both the thickness of wet 5063D within the area covered by the IC die, and the final thickness of (second) 5063D layer between the IC die and the Au coated substrate (Au/Pt/alumina). The thickness of 5063 layer between IC die and Au thick-film (5062D) coated package substrate ~ 30 microns after firing is appropriate. The assembly is dried in a box oven in air at 150 °C for 20 min with ramping temperature rate from room temperature of 3°C/min. After this drying, the temperature is immediately raised to 600 °C with rate of 3°C/min and dwell at the temperature for 3 hours at 600 °C in air. After the curing process the oven with the die-attach assembly is cooled naturally taking several hours.

This IC die-attach technology is designated for small size high temperature harsh environment ICs packaging, especially for SiC ICs with Au thin-film backside metallization. The assemblies, including SiC ICs attached to a co-fired Pt/HTCC alumina electronic packages, have been long term tested for operation at 500°C in oxidizing environment [7c], and short term tested at temperature above 800°C [12].

3.4 Wire-bonding

Bond pad surfaces on SiC IC die are usually thin-film Pt [7b,7d] with a cap layer of thin film Au, and the bond pads on the alumina package are Pt with or without thin- or thick-film Au [6, 8]. Thermo-sonic gold wire bonding is used for interconnecting the IC die to the package. One of the challenges of high temperature packaging is electromigration of conductors under electrical bias at high temperature. In order to reduce and control electromigration in thin Au wire, 1 mil diameter 98% (2% impurity) Au wire [13a], is used with commercial ball-wedge thermal sonic wire-bonder [12a]. The ball-bond is applied on Pt pad surface on SiC IC die as the first bond, and wedge bond is applied on the package bond-pad. Typical wire-bonder settings for 1 mil Au wire were used [13b]. When the packaged ICs were tested in high temperature (500 °C) air, the impurities in the wire material migrated to the surface and quickly formed a low-reflective oxides surface layer passivating the wire surface, beneficially slowing down the electromigration process along wire surfaces (This topic will be explored more in the future to optimize Au wire formula for high temperature applications). This surface oxide is stable in 500°C air.

4. Test Results of Packaged SiC ICs

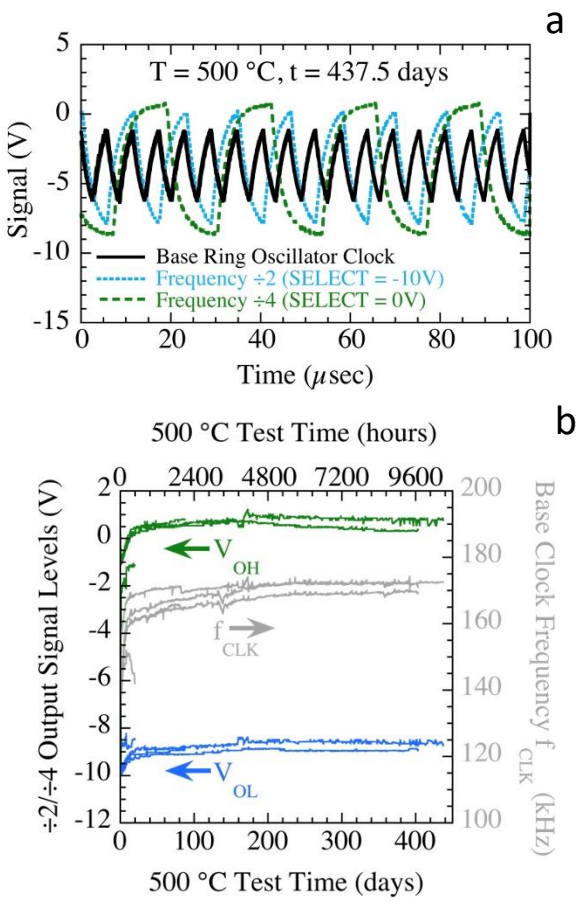

Figure 4: SiC JFET ÷2/÷4 Clock IC waveforms recorded at 437.5 days of 500 °C testing. [14a].

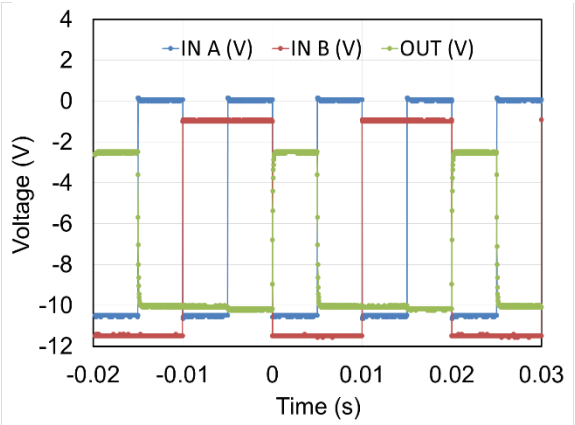

Figure 5: The inputs and output waveforms of a packaged two-inputs NOR logic gate based on SiC JFETs developed at NASA GRC. The data was recorded at 700 °C after 143.5 hours test [14b]. The waveform of Input B is shifted -1 V to avoid overlapping with Input A.

This Pt/HTCC alumina packaging system has been used to facilitate long term tests of multiple analog and digital SiC JFET integrated circuits at 500 °C and above. Figure 4 plots test data of ÷2/÷4 Clock

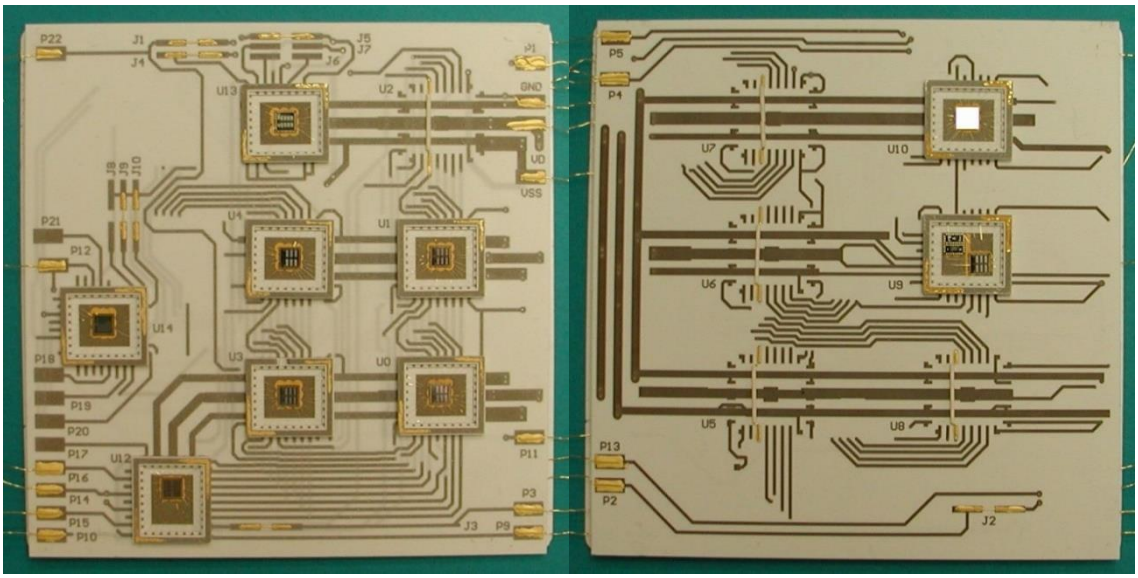

Figure 6: A double sided four-layer Pt/HTCC alumina circuit board with ten SiC JFET IC chips in nine Pt/HTCC packages. The picture also shows 17 attached Au I/O wires, and 12 jumpers. The circuit board has been examined at room temperature, is currently in queue for NASA relevant environment test in near future.

#2 chip, (4a) shows output waveforms of base clock output, frequency ÷2, and frequency ÷4 recorded at 437.5 days of 500 °C testing [14a]. It is important to note that the waveforms are non-square to varying degree due to capacitive and resistive loading effects arising from the combination of the setup cabling, oven wiring and oscilloscope probes. As expected, the lower-frequency ÷4 measured waveform more closely approximates square-wave output shape. Figure 4b plots the measured base clock frequency (f_{CLK}) and output low (V_{OL}) and high (V_{OH}) signal voltage levels of the ÷4 output signal as a function of 500 °C testing time for multiple ÷2/÷4 clock chips that were oven-tested [14a].

In order to assess short term survivability of both SiC ICs and the packaging system at higher temperatures, packaged SiC ICs were electrically tested at temperatures up to 700 °C [14b]. Figure 5 shows the input and output waveforms of a packaged 2-input NOR gate (4-input NOR gate with inputs tied together in order to test using fewer pulse generators) based on SiC JFETs recorded after 143.5 hours of continuous test at 700 °C. The logic "0" is -10.5V, and logic "1" is 0V for inputs. This SiC logic gate lasted 143.5 hours at 700 °C [13b]. No catastrophic packaging failure was visually observed or electrically detected during and after the test.

Figure 6 shows a picture [15] of both sides of a double sided HTCC circuit board with nine packages, ten packaged SiC JFET ICs (one package accommodates two IC chips), 17 I/O wires, and 12 jumpers. The circuit board has been examined at room temperature, and currently in queue for test in NASA relevant environment in near future.

5. Discussion and Conclusions

Based on the dielectric properties of a commercial HTCC alumina material at high temperatures, a prototype high temperature co-fired Pt/92% HTCC alumina packaging system including chip-level packages and multilayer capable circuit boards, for low power high temperature ICs was developed, fabricated, and electrically tested. Both AC and DC parasitic parameters of a 32-I/O package have been characterized at the frequencies up to 1 MHz between room temperature to 550 °C indicating its feasibility for packaging SiC ICs. This packaging system was developed with high temperature durable conductive die-attach, wire-bonding, I/O wire attachment to circuit board, and component (package) attachment to circuit board as a system. This packaging system has been long term tested with SiC integrated circuits at 500 °C, and briefly at much higher temperatures. This package/PCB system is fabricated using standard packaging materials and processes currently available in industry, so it can be implemented for mass production when needed in the future.

Since currently Au thick-film paste is used to attach chip-level packages to a circuit board, firing at 850 °C is needed. To avoid damaging chips intended for 500 °C operation, the chip-level packaging steps such die-attach and wire-bonding were accomplished after attachment of the packages. In order to adapt a more conventional packaging sequence, in which

chip-level packaging is accomplished first followed by board level integration of packages containing chips, the material and process to attach packages to circuit board needs to be improved. Basically, the process temperature needs to be lowered to avoid unnecessary exposure of ICs for 500 °C operation to extremely high temperature (even though the SiC JFET ICs have been demonstrated operation at temperatures above 800°C). More long term and thermal cycling tests of this packaging system with SiC ICs is needed to further evaluate the performance and reliability of this packaging system for pronged and repeated operations at application temperatures of 500 °C and higher.

Acknowledgements

The authors wish to gratefully acknowledge the contributions of Diana I. Centeno-Gomez, Carol M. Tolbert, and Rainee N. Simons for approval reading. This work is supported by the NASA Transformative Tools and Technologies (TTT) project, and especially the NASA Long-Lived In-Situ Solar System Explorer (LLISSE) project and Planetary Instrument Concepts for the Advancement of Solar System Observations (PICASSO) programs.

Reference

1. G. W. Hunter and A. Behbahani, "A Brief Review of the Need for Robust Smart Wireless Sensor Systems for Future Propulsion Systems, Distributed Engine Controls, and Propulsion Health Management", 58th International Instrumentation Symposium, San Diego, CA, June 4-78, (2012).

2a. F.P. McCluskey, R. Grzybowski, and T. Podlesak, (1997) "High Temperature Electronics," CRC Press, Boca Raton, LA.

2b. J. D. Cressler and H. A. Mantooth, Extreme Environment Electronics (Part I Introduction), CRC Press, Boca Raton, FL, 2013.

3a. P. Neudeck, et al., *Proc. 2018 IMAPS Int. Conf. High Temperature Electronics*, pp. 71-78. https://ntrs.nasa.gov/citations/20180003391

3b. P. G. Neudeck, S. L. Garverick, D. J. Spry, L.-Y. Chen, G. M. Beheim, M. J. Krasowski, and M. Mehregany, "Extreme Temperature 6H-SiC JFET Integrated Circuit Technology," Phys. Status Solidi A, 1-17 (2009).

4. L. Chen, P.G. Neudeck, D.J. Spry, and G.W Hunter, "A 96% Alumina based Packaging System for 500°C Test of SiC Integrated Circuits," in Proceedings of iMAPS International High Temperature Electronics Conference (HiTEC), global virtual event, April 26 – 29, 2021.

5. L.-Y. Chen, "Electrical Performance of Co-Fired Alumina Substrates at High Temperatures," in Proceedings of iMAPS International High Temperature Electronics Conference (HiTEC), Albuquerque, NM, May 8-10, 2012.

6. L. Chen, P.G. Neudeck, D.J. Spry, G.M. Beheim, and G.W Hunter, "Electrical Performance of a 32-I/O HTCC Alumina Package for High-Temperature Micro-electronics," Journal of Microelectronics and Electronic Packaging (2017) 14, 11-16.

7a. P. Neudeck, et al., "Progress Towards Prolonged IC Deployment Into Previously Inaccessible Hostile Environments Via Development of SiC JFET-R ICs," Proc. 2018 IMAPS Int. Conf. High Temperature Electronics, pp. 71-78.

7b. D. J. Spry, P. G. Neudeck, L.-Y. Chen, D. Lukco, C. W. Chang, G. M. Beheim, M. J. Krasowski, N. F. Prokop, "Processing and Characterization of Thousand-Hour 500 °C Durable 4H-SiC JFET Integrated Circuits," in Proceedings of 2016 iMAPS HiTEC, Albuquerque, NM, May 9-12, 2016.

7c. P. G. Neudeck et al., "Stable Electrical Operation of 6H–SiC JFETs and ICs for Thousands of Hours at 500 °C," *IEEE Electron Device Letters*, vol. 29, no. 5, pp. 456-459, May 2008, doi: 10.1109/LED.2008.919787.

7d. D. J. Spry and D. Lukco, J. Electronic Materials 41(5) p. 915 (2012).

8. L. Chen, P. G. Neudeck, R. D. Meredith, D. Lukco, D. J. Spry, L. M. Nakley, K. G. Phillips, G. M. Beheim, and G. W. Hunter, "Sixty Earth-Day Test of a Prototype Pt/HTCC Alumina Package in a Simulated Venus Environment," Journal of Microelectronics and Electronic Packaging 16, pp. 78-83, April 2019. DOI:10.4071/imaps.873073

9. http://www.adtechceramics.com/materials

10.https://www.dupont.com/content/dam/dupont/amer/us/en/transportation-industrial/public/documents/en/5062D_5063D.pdf

11. R. Zhang, R. W. Johnson, A. Vert, and T. Zhang, Failure Mechanism in Thick Film Materials for 300°C degrees C Operation, IEEE Transactions on Components, Packaging and Manufacturing Technology 2(11): 1750-1758.
DOI: 10.1109/TCPMT.2012.2204995

12. Philip G. Neudeck**,** David J. Spry, Michael J. Krasowski, Norman F. Prokop, and Liangyu Chen, "Demonstration of 4H-SiC JFET Digital ICs Across 1000 °C Temperature Range Without Change to Input Voltages," in Materials Science Forum 963:813-817, July 2019. 10.4028/www.scientific.net/MSF.963.813

13a. https://www.kns.com/

13b. Operations and Maintenance Manual for K&S 4500 Series Digital Series Manual Wire Bonders, March 2002.

14a. P. Neudeck, D. Spry, M. Krasowski, N. F. Prokop, G. M. Beheim, L. Chen, and C. W. Chang, "Year-long 500°C Operational Demonstration of Up-scaled 4H-SiC JFET Integrated Circuits", iMAPS Journal of Microelctronics and Electronic Packaging, October 2018 15(4): 163-170.

14b. D. J. Spry, P. G. Neudeck, L.-Y. Chen, D. Lukco, C. W. Chang, G. M. Beheim, M. J. Krasowski, N. F. Prokop, "Processing and Characterization of Thousand-Hour 500 °C Durable 4H-SiC JFET Integrated Circuits," in Proceedings of 2016 iMAPS HiTEC, Albuquerque, NM, May 9-12, 2016.

15. P. Neudeck, D. Spry, M. Krasowski, and L. Chen, Progress Towards Prolonged IC Deployment Into Previously Inaccessible Hostile Environments Via Development of SiC JFET-R ICs,