National Aeronautics and Space Administration

Power Hibernation to Survive the Lunar Night

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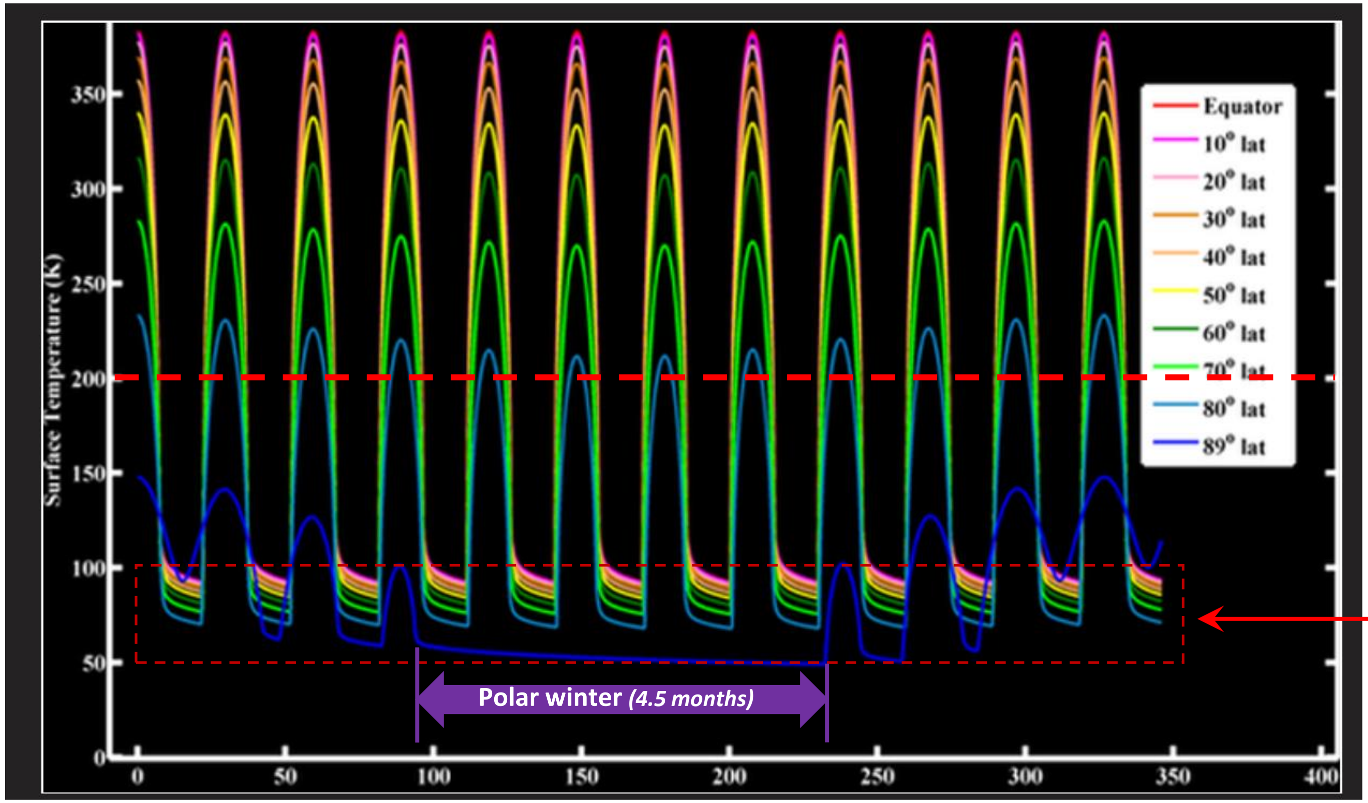
Background
The Extreme Lunar Environment

LRO DIVINER: Lunar Day/Night Temperature Range by Latitude



Thermal model calculations of monthly and annual lunar surface temperature variations at various latitudes

- Day: 100-400 K highs based on latitude
- Night: 50-100 K lows for *all* latitudes
  - Duration (non-polar): ~354 hrs (~15 Earth days)
  - Duration (polar): winter sun below horizon for ~4.5 months

Li-ion battery approx. freeze temperature

Lunar night is extremely cold *everywhere*

Image permissions per Dr. N Petro/NASA GSFC, Dr. D Paige/UCLA

Background
Lunar Power Systems

- **Power System Survivability**
  - Radioisotope systems provide nighttime heat and power, but are regulated and costly
  - Traditional solar panel and small battery systems *cannot* survive reliably
  - Large batteries providing sufficient heat are mass-prohibitive due to night duration

- **Lightweight Battery Solution**
  - Surveyor (1966-1968) used silver-zinc batteries
    - Not designed to survive night conditions, but a few experienced unexpected battery activity after returning to daylight
  - Recent research shows that lithium-ion (Li-ion) batteries can be safely frozen and thawed without apparent performance degradation
    - Relies on cryogenically tolerant and operable electronics to properly manage revival

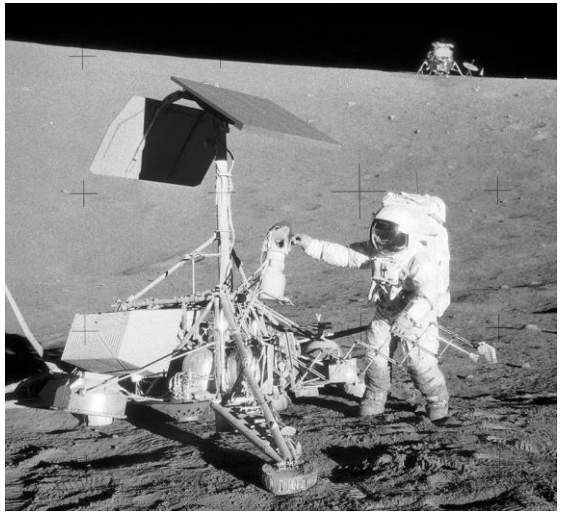


Image Credit: NASA

Overview

Proposed Survival Strategy

- **Lunar Power Hibernation**
  - Extends capabilities and duration of lunar missions
  - Reduces dependency on radioisotopes, pre-established infrastructure
  - Success depends on:
    - Cryo-tolerant Li-ion batteries
    - Cryo-tolerant electronics to operate reliably in nominal conditions (after dawn)
    - Cryo-operable electronics to perform cold start and safely restore power

- **Hibernation Applications**
  - Commercial Lunar Payload Services (CLPS)
    - Landers currently provide only a single lunar day of operation
  - Robotic elements of the Artemis Program
  - Lunar in-situ resource utilization (ISRU) systems
  - Survival and recovery options in contingency situations

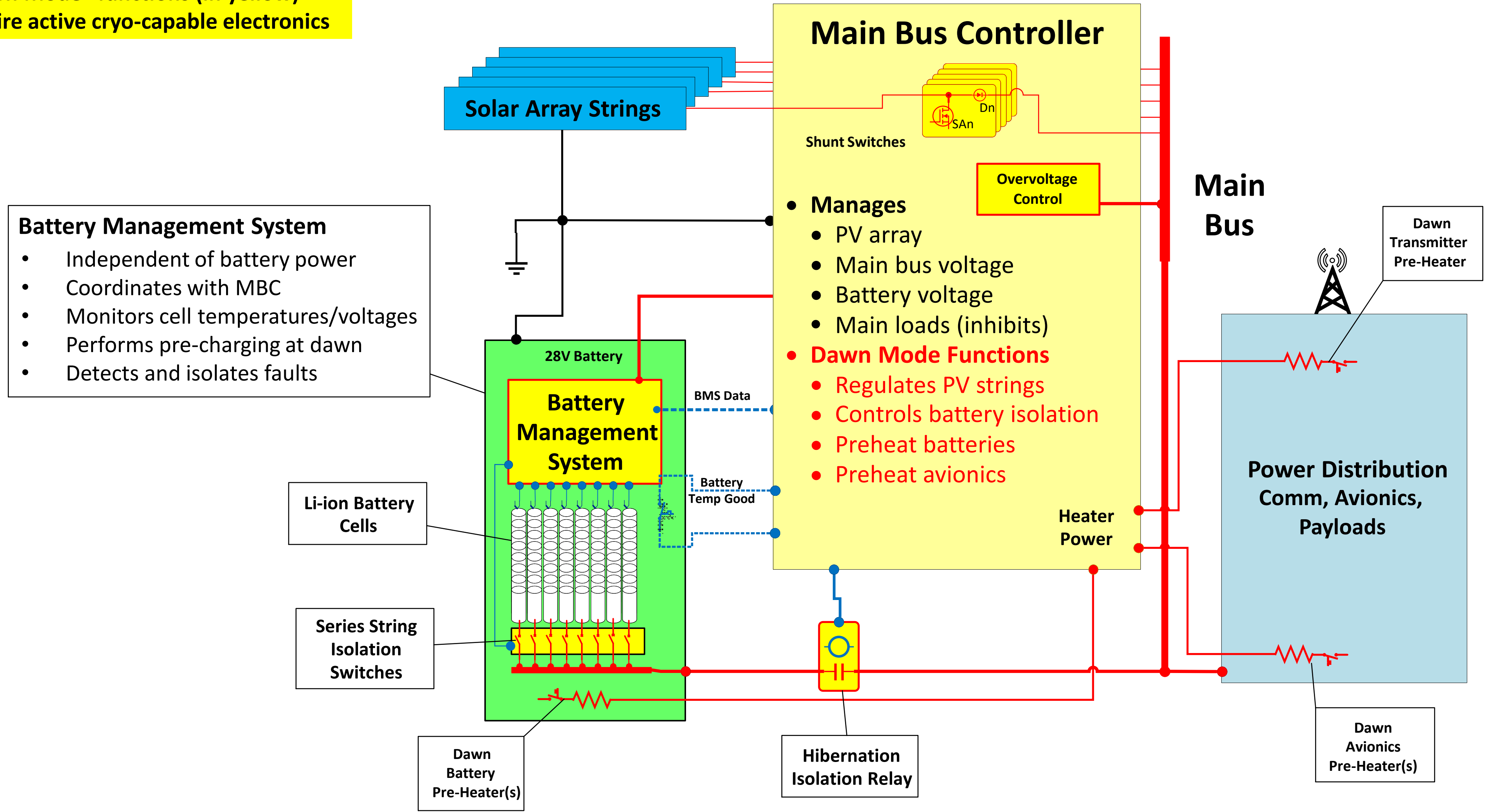
Overview
Hibernation Electronics Definitions

- **Cryo-Tolerant**
  - Required for all spacecraft electronics (power, avionics, comm)
  - Must passively withstand thermal environment down to 50 K without damage
  - Can depend on manufacturing processes and materials/packaging

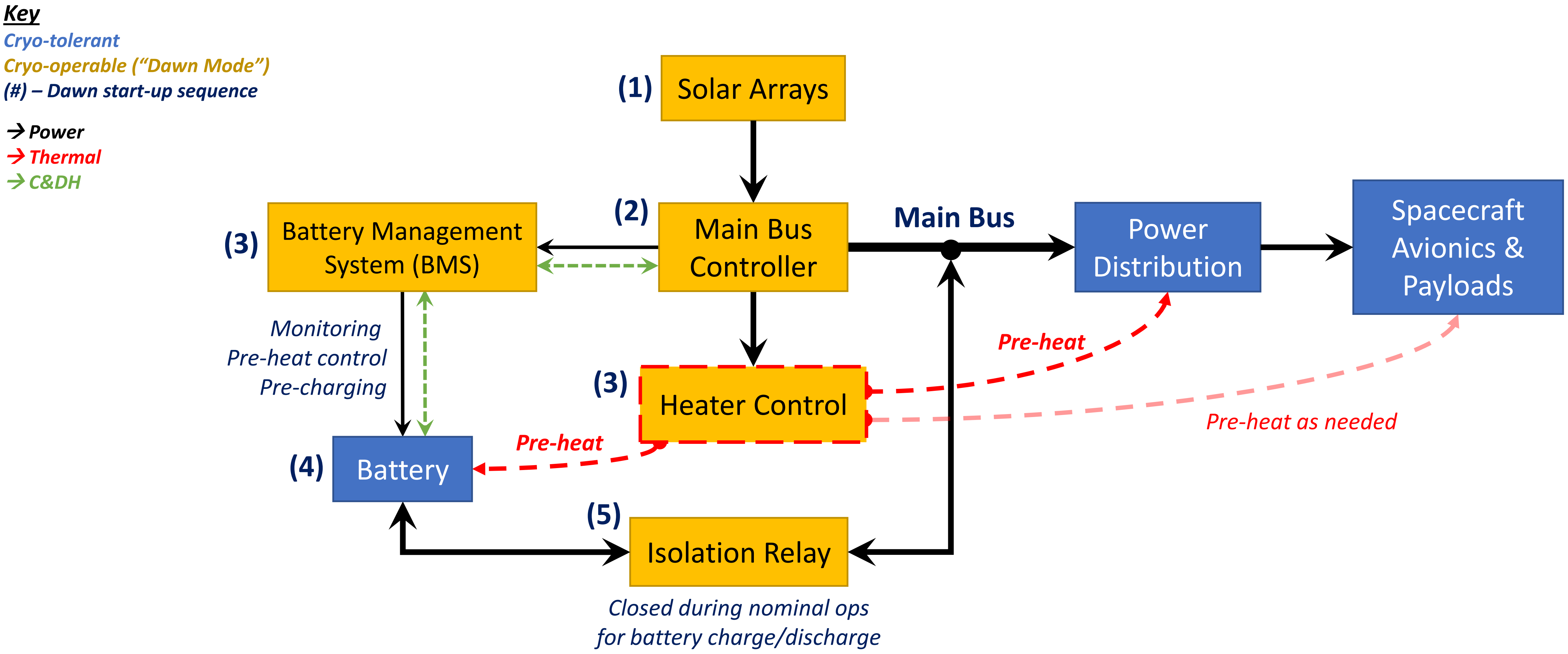
- **Cryo-Operable**
  - Required for hibernation electronics that restore power at lunar dawn
  - Must start up and operate in 50-100 K lunar dawn
  - Contingent on device properties and stability of interactions

Overview
Hibernation Power Architecture

"Dawn Mode" functions (in yellow) require active cryo-capable electronics



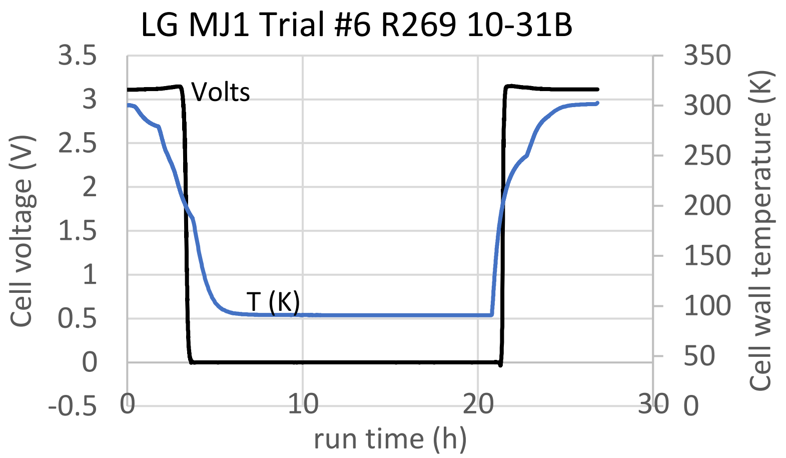
Overview
Sample Revival Sequence

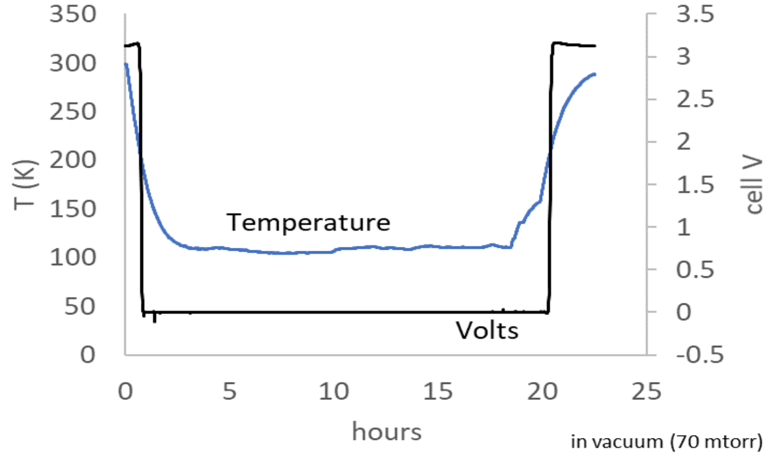


Batteries

Lithium-Ion Cell Investigation at NASA GRC

- **Initial Tests**
  - Performed at 1 atmosphere
  - LN2 vapor chilled to 80 K (-193 °C)
- **Refined Tests**
  - Performed in vacuum (70 mTorr)
  - Cryocooler chilled to 100 K (-173 °C)
- **18650 Cell Results**
  - Near 200 K (-70 °C), voltage drops to 0 V
  - Above 200 K, voltage and capacity recover
  - No apparent degradation

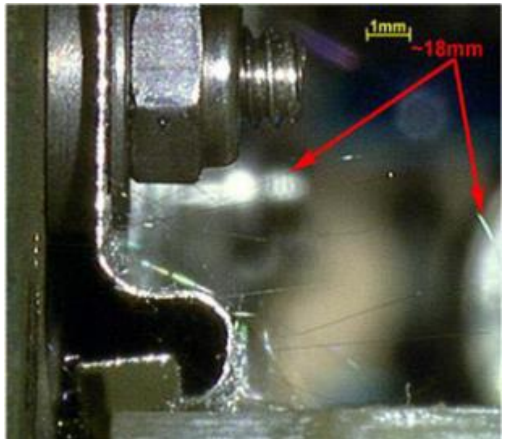




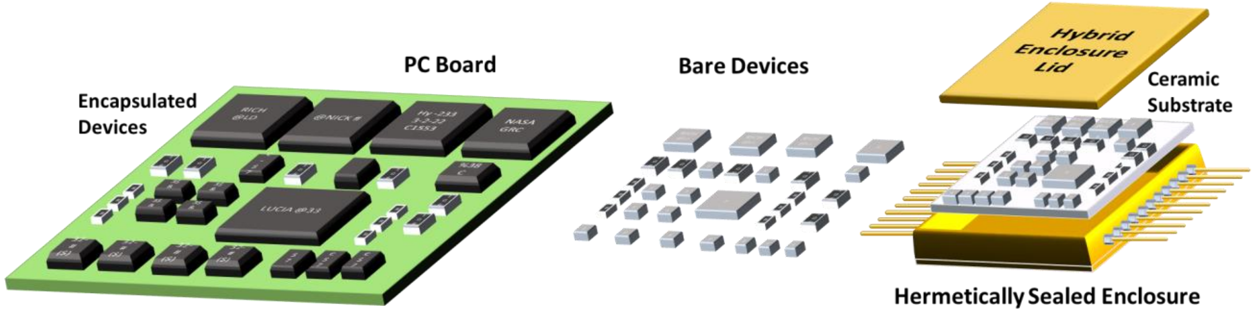
Figures courtesy of W. Bennett / NASA GRC

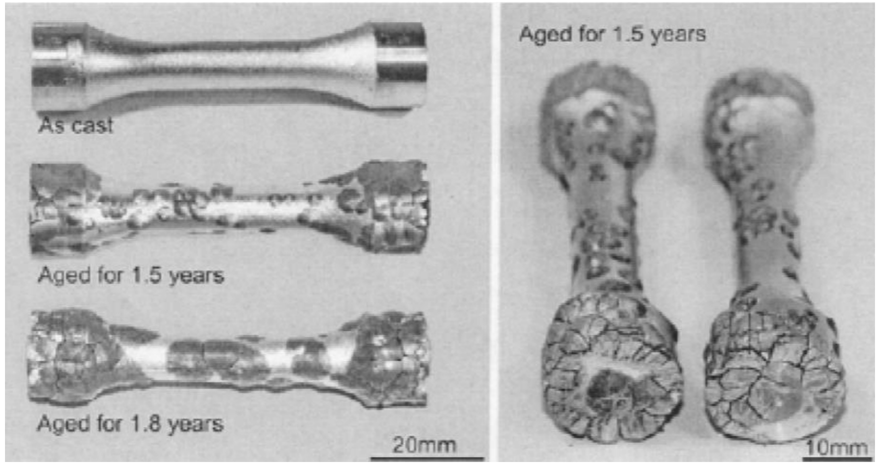
Electronics
Circuit Packaging for Cryo-Tolerance

- **Printed Circuit Boards**
  - Copper-clad laminate and fiberglass-reinforced plastic (FRP) have well-matched coefficients of thermal expansion (CTEs)
  - Target small boards and devices, matched CTE, mechanical compliance
  - Avoid pure tin: tin whiskers and tin pest
- **Hybrid Microcircuits**
  - Bare devices assembled on a low-CTE ceramic substrate
  - Encapsulated in a hermetically sealed metal enclosure
  - Eliminates thermal stress from plastic encapsulants
  - Improves thermal conductivity



***Tin whiskers:** Single-crystal tin filament growths can create short circuits.*





***Tin pest:** Tin can transform to a brittle non-metallic form between 0°C and -30°C, expanding 27% and disintegrating joints.*

Image Credits: R. Oeftering / NASA GRC (left), NASA Electronic Parts and Packaging (NEPP) Program (right)

Electronics
Choosing Components for Cryo-Operability

	Device	Advantages	Challenges
Semiconductors	Diodes (PN, Schottky)	• Can be operational at lunar temperatures with proper design and part selection	• Forward voltage generally increases at cryo temperatures • On-resistance increases below 100 K (except for GaN Schottky)
	Bipolar Junction Transistor (BJT)	• Increased gain at cryogenic temperatures (SiC)	• DC gain decreases dramatically with temperature (Si) • Likely unsuitable for use due to carrier freeze-out (Si)
	Junction-Gate FET (JFET)	• Normally-on JFET performance at lunar night temperatures similar to that at room temperature (SiC)	• Carrier freeze-out increases on-resistance as temperatures decrease past ~200 K
	Metal Oxide Semiconductor FET (MOSFET)	• On-resistance decreases w/ low temperature until ~77 K (Si) • Switching time improves w/ low temperature (Si)	• Threshold voltage increases; breakdown voltage decreases (Si) • Enhancement-mode SiC unsuitable – extreme carrier freeze-out
	High-Electron Mobility Transistor (HEMT)	• On-resistance/switching time improves w/ low temperature; breakdown/threshold voltage doesn't change (GaN)	
	Insulated-Gate Bipolar Transistor (IGBT)	• Improved switching speed, forward voltage, and transconductance	• Breakdown voltage decreases • Threshold voltage slightly increases
Passives	Resistors	• Wire-wound and metal film have low TCRs (temp coefficients of resistance)	• Thick-film and carbon are greatly affected by temperature
	Ceramic Capacitors	• Class I (paraelectrics): Good capacitance stability over temperature	• Class II (ferroelectrics): Higher variability over temperature ranges
	Electrolytic Capacitors	• Solid tantalum electrolytics will operate marginally	• Aluminum electrolytic (liquid): Electrolyte freezes at cryo temperatures • Tantalum electrolytic (solid): Higher dissipation factor and ESR, lowered capacitance at higher frequencies
	Inductors	• Air core inductors likely have little change in properties due to no core material	• Solid core inductors require special core material tailored for low losses at cryo temperatures

Summary

- **Lunar Power Hibernation Architecture**
  - Reduces dependency on other prohibitive forms of power delivery
  - Enables longer-term missions across multiple lunar cycles
  - Can be implemented on existing designs at low cost and mass
- **Lithium-ion Battery Management**
  - Proven to be capable of freezing and thawing w/ little-to-no loss of performance
  - BMS should be implemented to control warming
- **Electronics Design Considerations**
  - Minimize size of boards and part footprints, match CTE, avoid tin
  - Most semiconductors can operate at cryogenic temperatures (50-100 K)
    - Carrier freeze-out and electron tunneling may be a concern
  - Solutions exist for most implementations of passive devices

Future Work

- Characterize safe Li-ion hibernation management
- Continue review of academic works
- If possible, build parts model library for simulation
- Test cryogenic operation of discrete parts
- Develop prototype cryo-circuit based on guidelines
- Conduct circuit-level testing with batteries and solar cells

- **Seeking collaboration opportunities!**

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Acronyms and Abbreviations

- BJT Bipolar Junction Transistor
- BMS Battery Management System
- C&DH Command and Data Handling
- CLPS Commercial Lunar Payload Services
- Comm Communications
- Cryo Cryogenic
- CTE Coefficient of Thermal Expansion
- ESR Equivalent Series Resistance
- FET Field-Effect Transistor
- FRP Fiberglass-Reinforced Plastic
- GRC Glenn Research Center
- HEMT High-Electron Mobility Transistor
- IGBT Insulated-Gate Bipolar Transistor
- ISRU In Situ Resource Utilization
- JFET Junction-Gate FET
- Li-ion Lithium-ion
- LRO Lunar Reconnaissance Orbiter
- MBC Main Bus Controller
- MOSFET Metal Oxide Semiconductor FET
- NEPP NASA Electronic Parts and Packaging
- PCB Printed Circuit Board
- TCR Temperature Coefficient of Resistance
- Temp Temperature

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