Gateway Power Quality Lessons Learned

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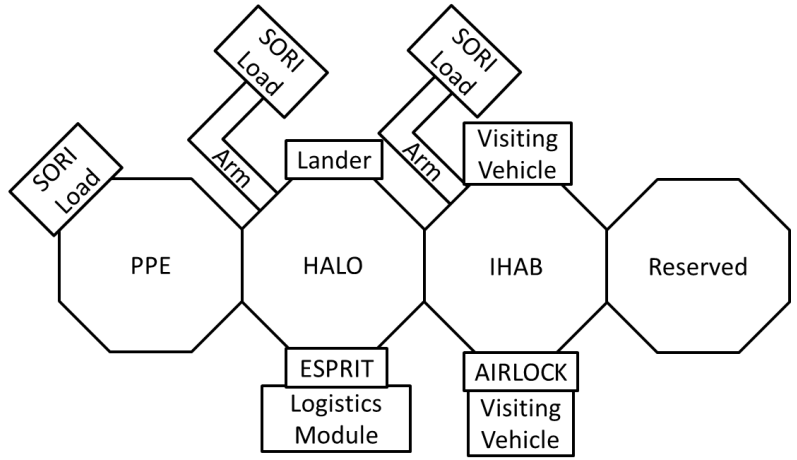
Background

- **Power Quality Lessons learned from Space Station are that requirements need to be defined early in a program**
  - This allows for hardware vendor designs to be compatible with each other from day one
- **What is Power Quality?**
  - A physical description of the electrical characteristics that allow the system to function properly without significant loss of performance or life.
  - The physical description includes:
    - steady state voltage limits, transient voltage limits in normal/abnormal conditions, ripple voltage, stability, fault conditions, and more.
- **Why is it so important?**
  - Years of experience from previous programs have taught that having a Power Quality Specification plays an important role in a successful power system design.
    - Improves reliability
      - Reduces component failures by defining operational boundaries
      - Ensures stable operation
      - Defines/drives proper fault recovery
    - Ensures ‘plug and play’ approach to design & integration

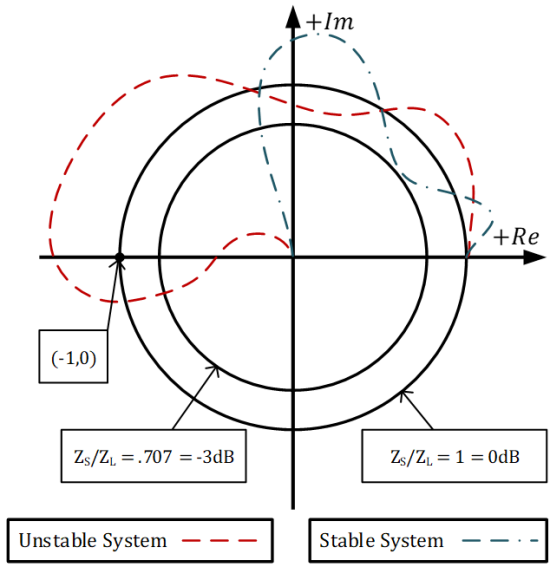
Power Quality Specification Purpose and Scope

- **Lessons learned from previous programs has identified the following areas and practices need to be addressed for both source and load developers.**
  - Scope of Specification must apply to every element
    - Major interfaces
    - Load user interfaces
  - A Specification must cover General Requirements such as Grounding, Isolation, Stability, etc.
  - Source/Load Interoperability and Compatibility must be defined early
    - Defined Element to Element and Vehicle to Vehicle
    - Defined between any Electric Power System (EPS) and Electric Power Consuming Equipment (EPCE)
  - Specification must ensure Reliability and Safety
  - Specification should be all encompassing
    - EPS and EPCE requirements defined in a single document
      - Historically has been two separate documents
      - Combining source and load Improves discussion
    - Verification self-contained
    - Appendix for recommended test methods
  - Open and ongoing discussion on requirements and verifications with suppliers is important

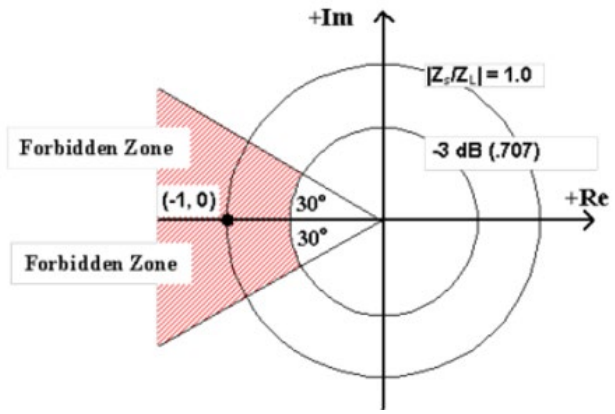


Power System Stability and Impedance

- **A typical cause of system instability is negative load impedance combined with non-ideal source impedance.**
- **Source and load impedances can be measured and characterized for stability independently.**
- **The impedance criterion has a significant advantage over other stability-analysis tools for large-scale systems.**
  - It analyzes the whole system based on the input-output impedance characteristics of each subsystem
    - Instead of on the detailed internal properties of subsystems.



Nyquist Plot of Unstable and Stable System Loop Gains



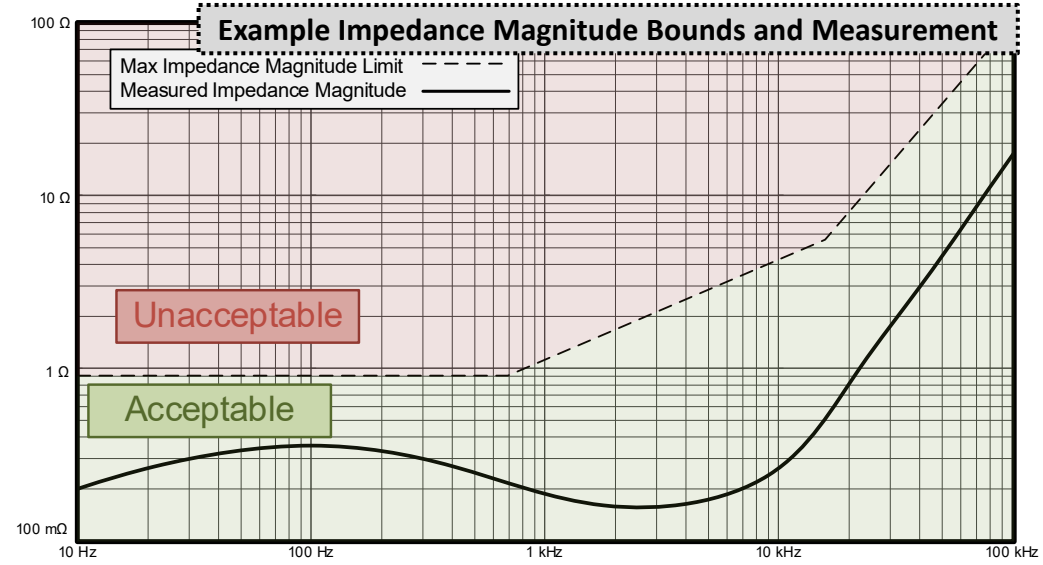
Forbidden Zone providing gain and phase margin

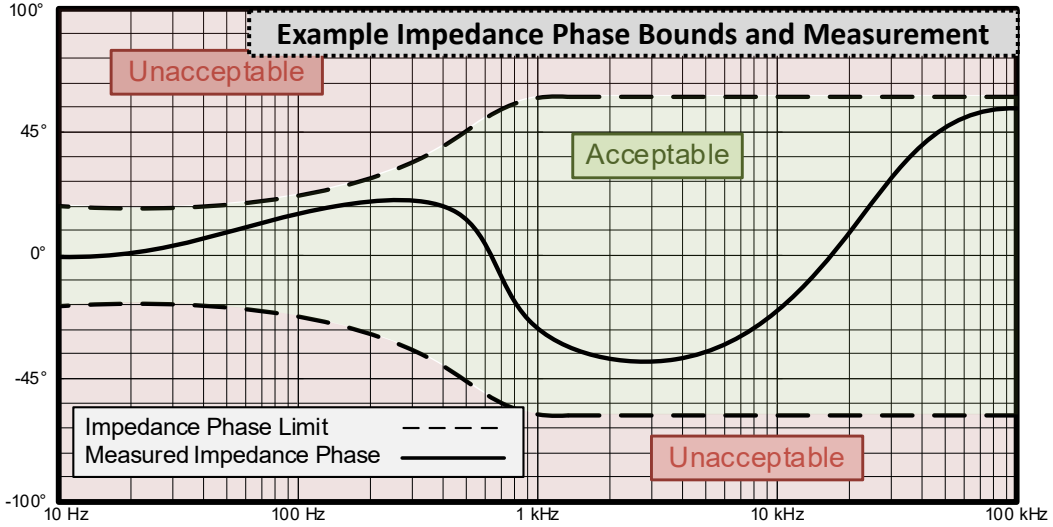
Source Impedance

- **Requirements are needed on source impedance and load impedance**
  - To ensure system stability
  - Allow relocation of loads
- **If the bounds are met, verifying system stability requirements is simplified**
  - Loads can design to derived load limits and system will be guaranteed stable

Source Impedance

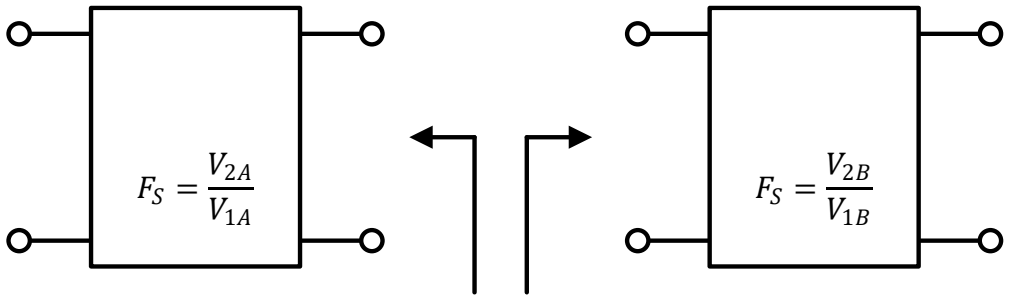
The source impedance shall be within the limits defined by the curves shown.

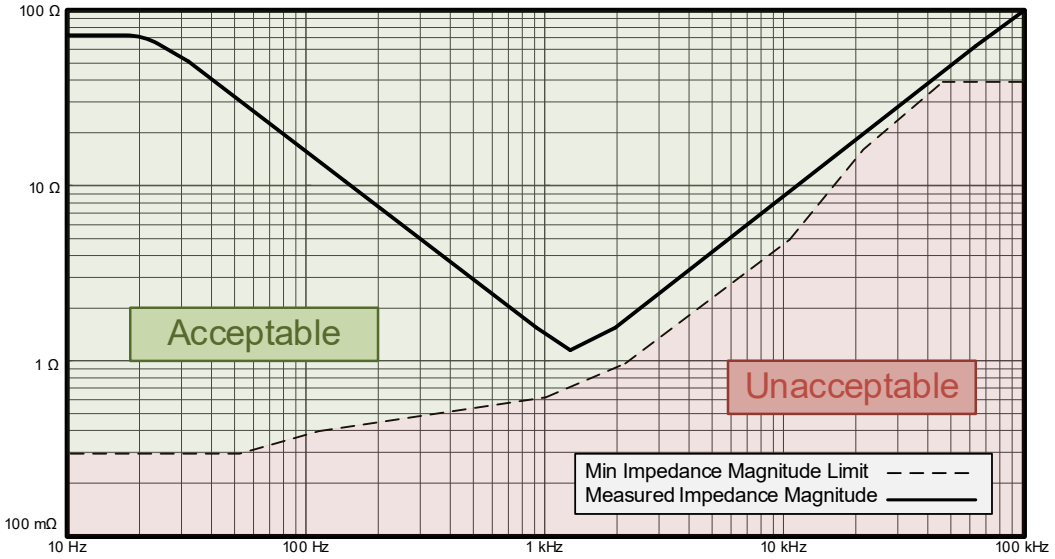


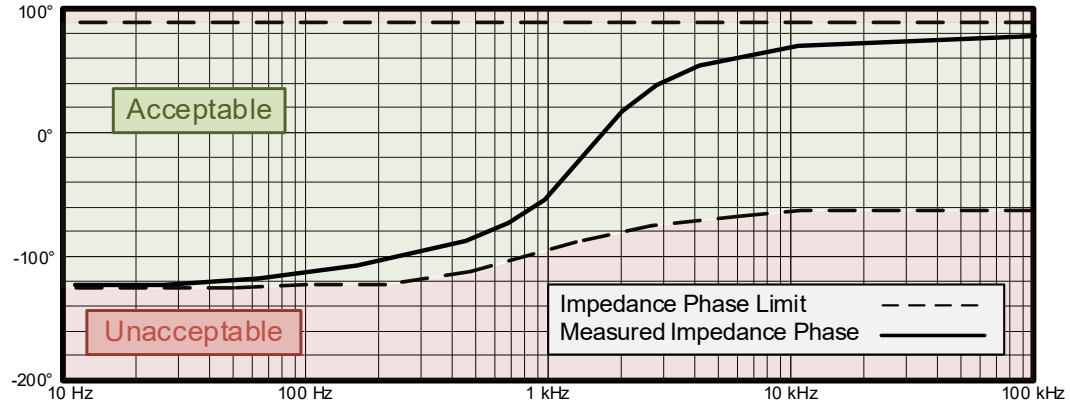


Load Impedance

- **Bounds are also stipulated for the input impedance of the EPCE system**
  - EPCE must meet magnitude **or** phase
- **If the bounds are met, verifying system stability requirements is simpler**







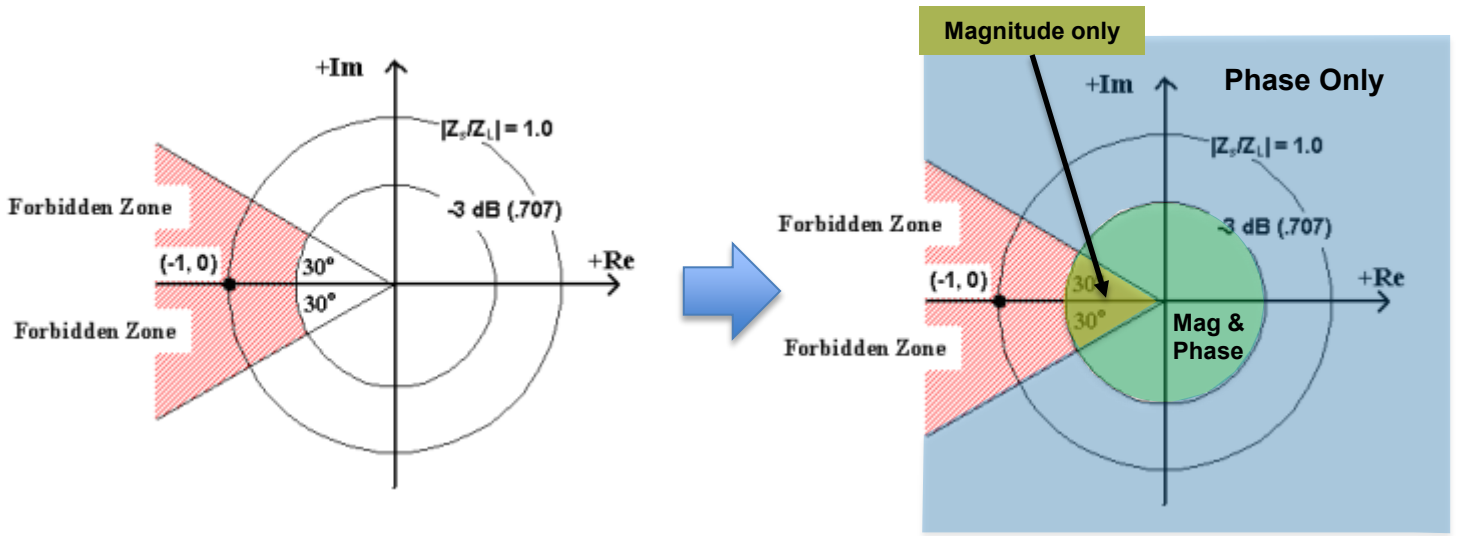
Load Impedance

The input impedance shall be within the limits defined by the curves shown.

Load Impedance constraints must be defined from Source Impedance limits

Small-Signal Stability

- **If source and load impedance requirements are not met, a more robust (Nyquist) analysis is required**
  - The ratio of ZS/ZL is plotted
  - If the curve does not enter the hatched red region, it is considered compliant
    - 30 degrees Phase margin if magnitude greater than 3dB
- **Not necessary to do this test if both EPS and EPCE comply to their impedance curves**



Small Signal Stability

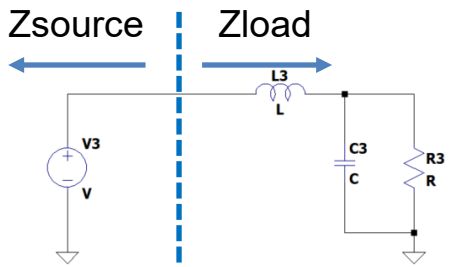
A complex impedance margin shall be maintained for the source impedance divided by the load impedance ratio that remains outside the hatched area (Forbidden Zone) shown.

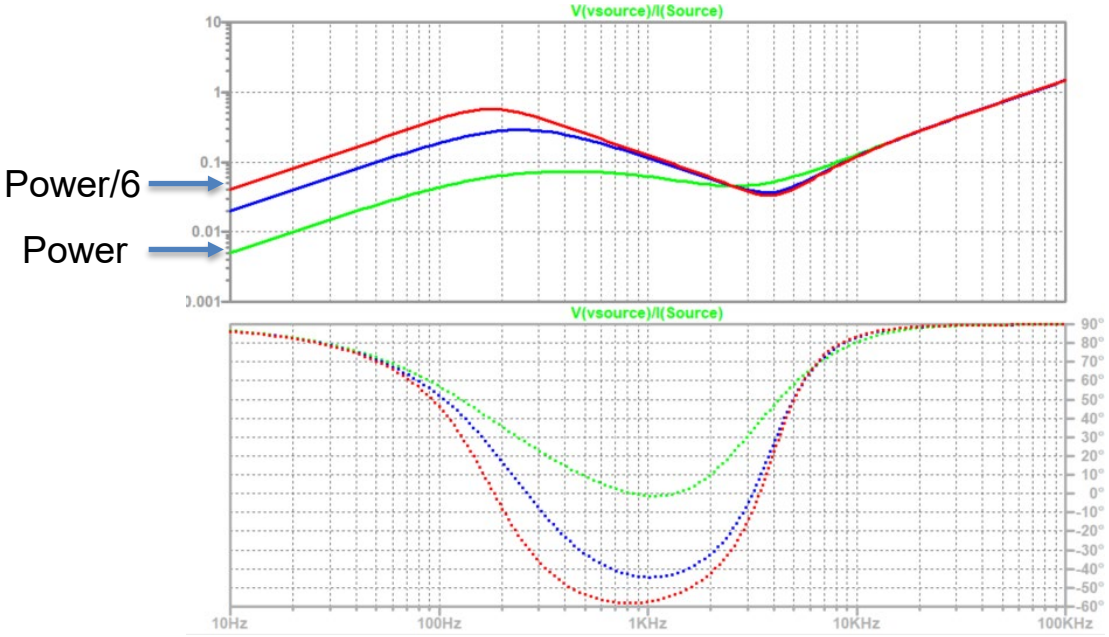
EPCE Meets Magnitude	EPCE Meets Phase	EPS Meets Magnitude	EPS Meets Phase	Result
X	X	No	No	Might be unstable Nyquist is required
X	X	No	Yes	
X	X	Yes	No	
No	No	Yes	Yes	
No	Yes	Yes	Yes	Stable
Yes	No	Yes	Yes	Stable
Yes	Yes	Yes	Yes	Stable

Stability can be verified via several different means.

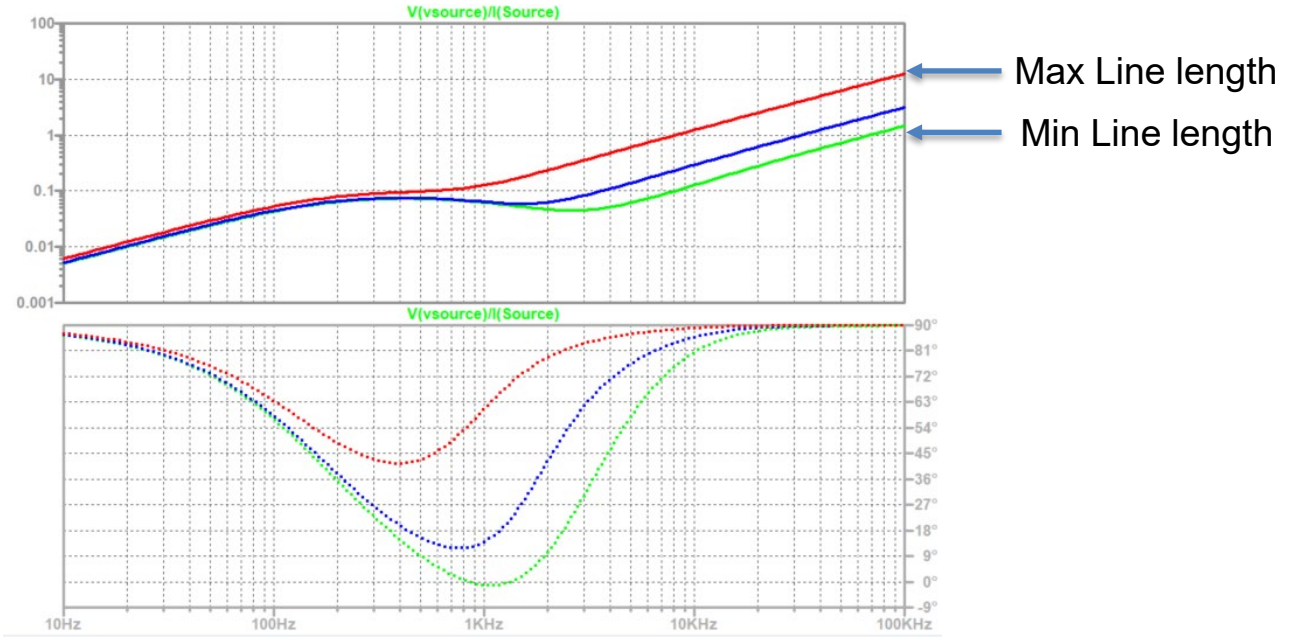
Additional Thoughts on Defining Impedance Limits - Sources

- **It is often thought that Source and Load impedance limits can be simplified using a Per-unit approach based on expected loading**
  - Multiplying or dividing by a common base to create a "family" of Impedance limit curves
    - Ideally cover multiple power levels or distribution lengths with a single requirement.
  - **However, one can per-unitize by power or line length, but not both**





Impedance Varying Output Power Only

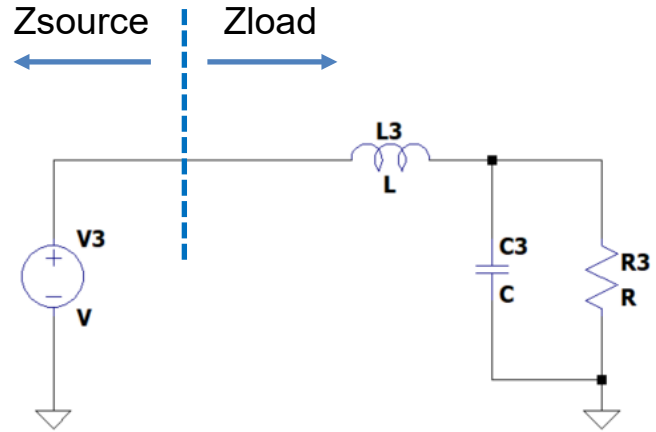


Impedance Varying Line Length Only

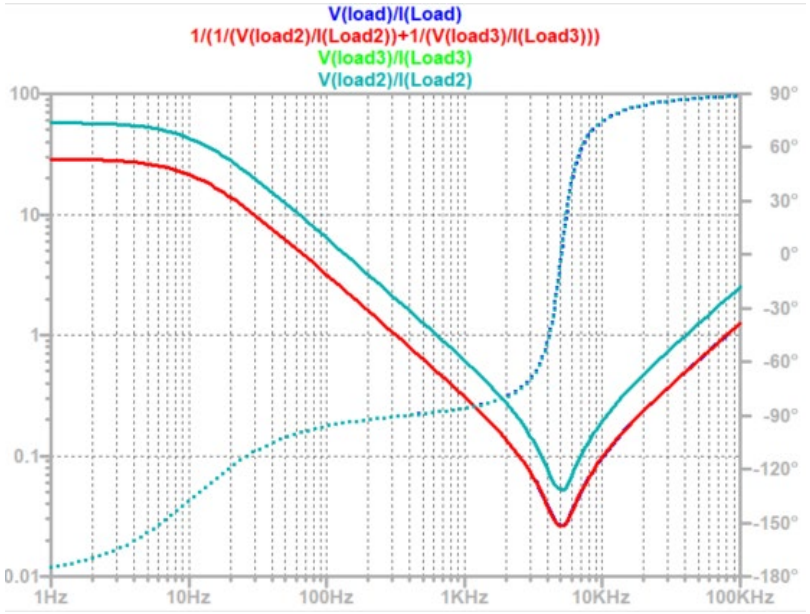
Specifying Source Impedance Limits in Per Unit is not Good Practice

Additional Thoughts on Defining Impedance Limits - Loads

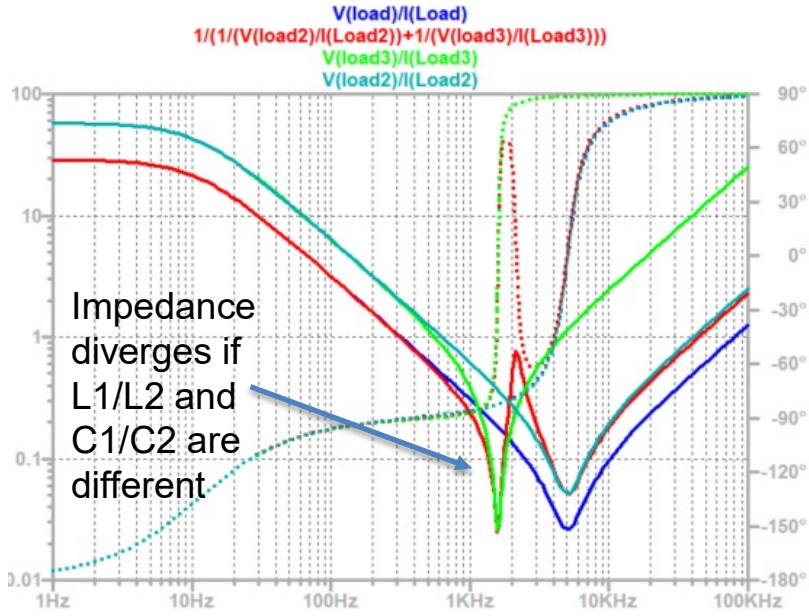
- **Similar to the Source Impedance**
  - Load impedance does not scale linearly with frequency
  - In practice varying filters and system configurations prevent a single simplified limit scaled based on power to ensure stability

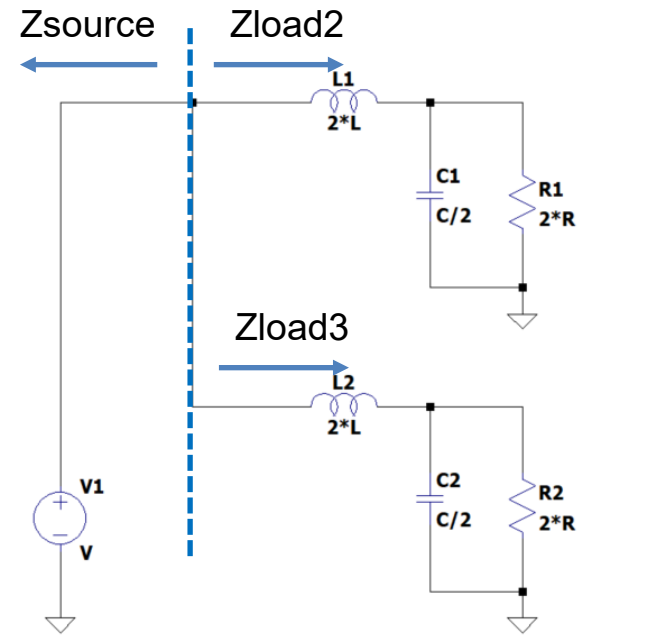


Identical Parallel loads vs Worst case load
Zload = Zload2 + Zload3



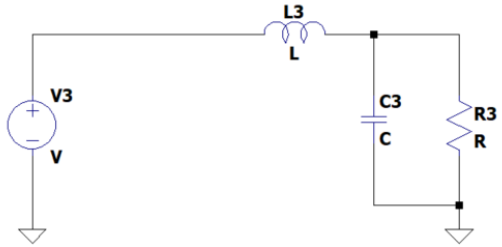
Non-identical Parallel loads vs Worst Case Load
Zload ≠ Zload2 + Zload3





Impedance Limits – Loads (continued)

- **Impedance Limits derived for the maximum load a DC-DC converter can support cannot use Per-unit to encompass all possible load and filter configurations across the power quality frequencies of interest.**
  - This is only true until non-linear filter characteristics dominate the response

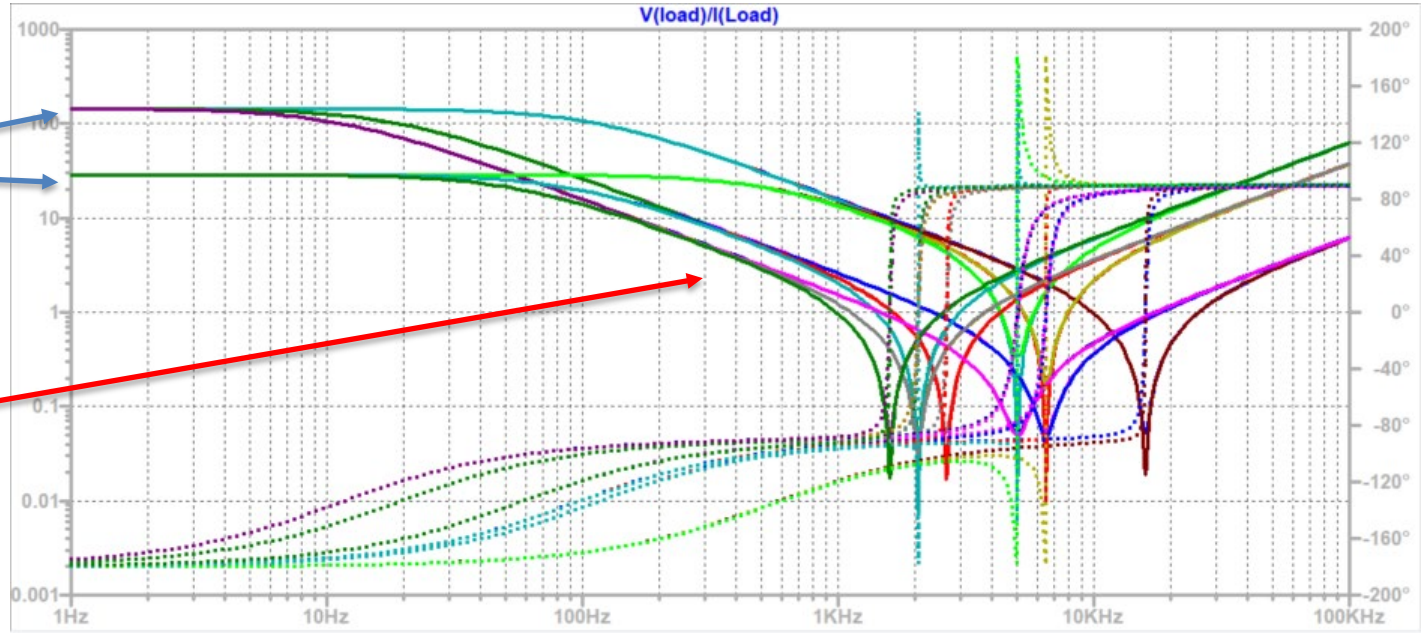


Per unit could be used to scale DC Impedance if the power of load **R** was increased by a factor of 5

150Ω

30Ω

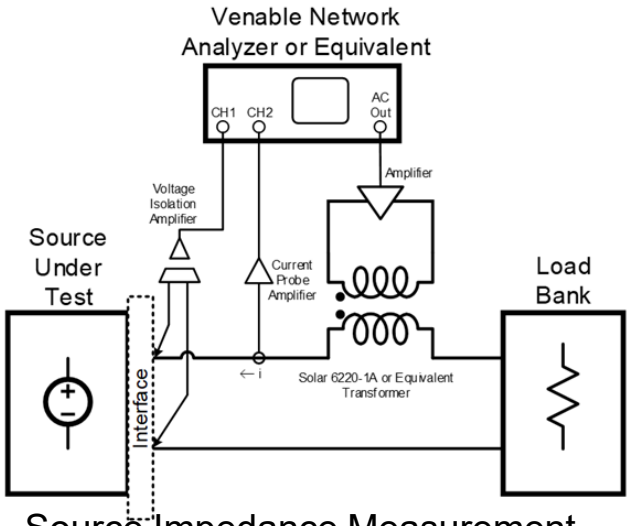
However, per unit scaling does not capture varying high frequency impedance dynamics if **L** and **C** vary by similar factors



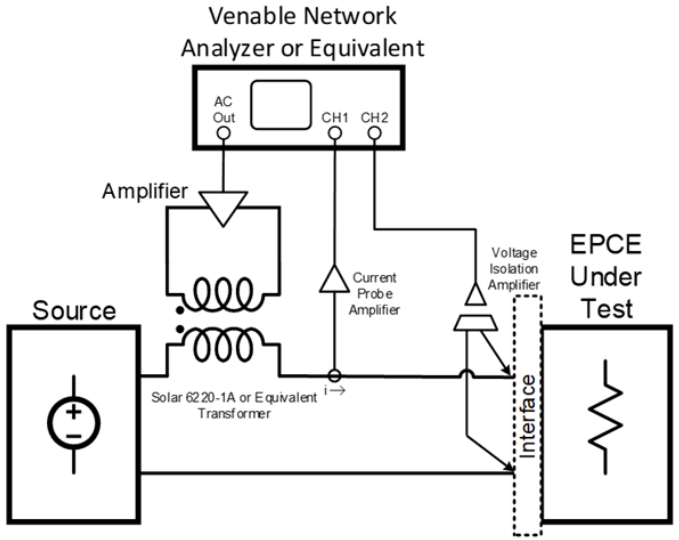
Interface Performance must be defined analytically for worst case

Impedance Testing

- **Goal is to obtain Source and Load impedance characteristics**
  - Source and load can be tested independent of each other
- **Recommended Steps**
  - Configure the network analyzer to calculate $Z_{EPS} = V_{ac}/I_{ac}$, where V_{ac} and I_{ac} are the AC components of the measured voltage and current.
  - Configure source or load to desired operating point
  - Sweep frequency to obtain Bode plots for magnitude and phase over desired frequency range
    - The most accurate test results will come from a series voltage perturbation that is just large enough in amplitude to produce a current response above the noise floor, and no greater.



Source Impedance Measurement

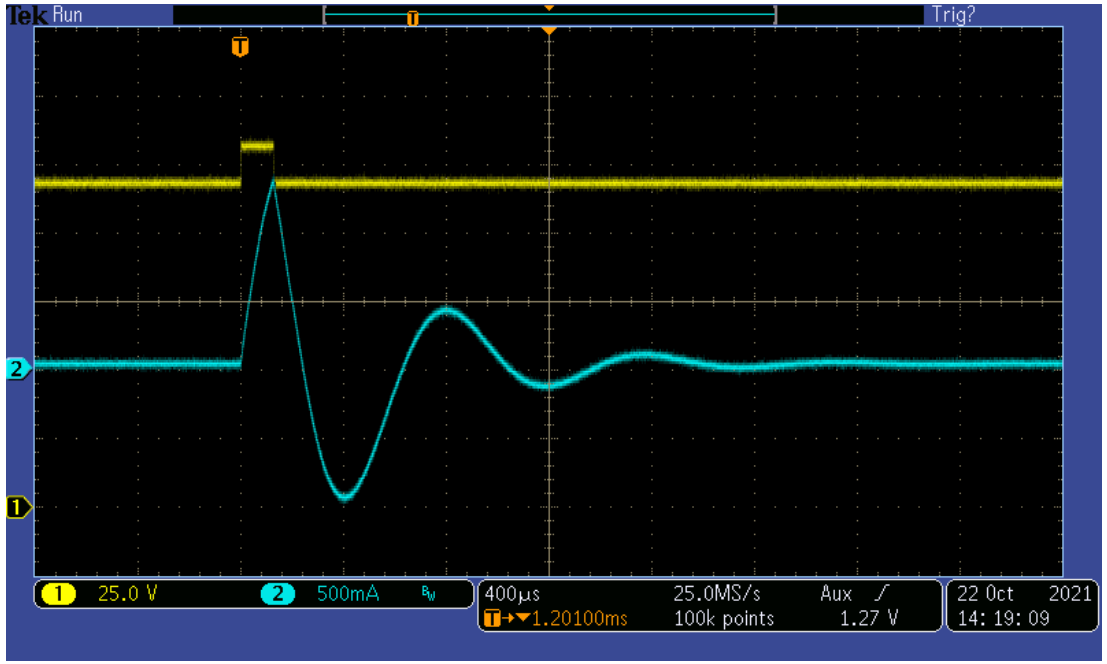


Load Impedance Measurement

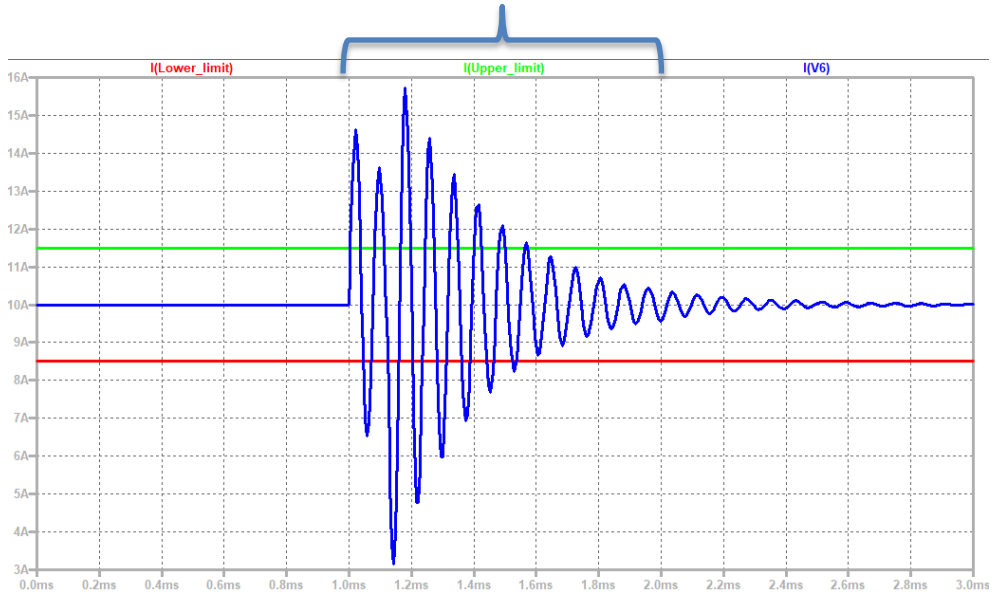
Large-Signal Stability

- **Impulses are applied to a load**
  - Magnitude of pulse adjusted to produce approximately 150% of steady-state current
  - Response must decay to 10% of peak magnitude within 1ms to comply
    - Ensures adequate damping of loads with no unintended resonances
- **Using a stiff source and measuring current removes source interaction from test**

Compliant Load Test, Large-Signal Response



Simulation model
Load settles within 1ms



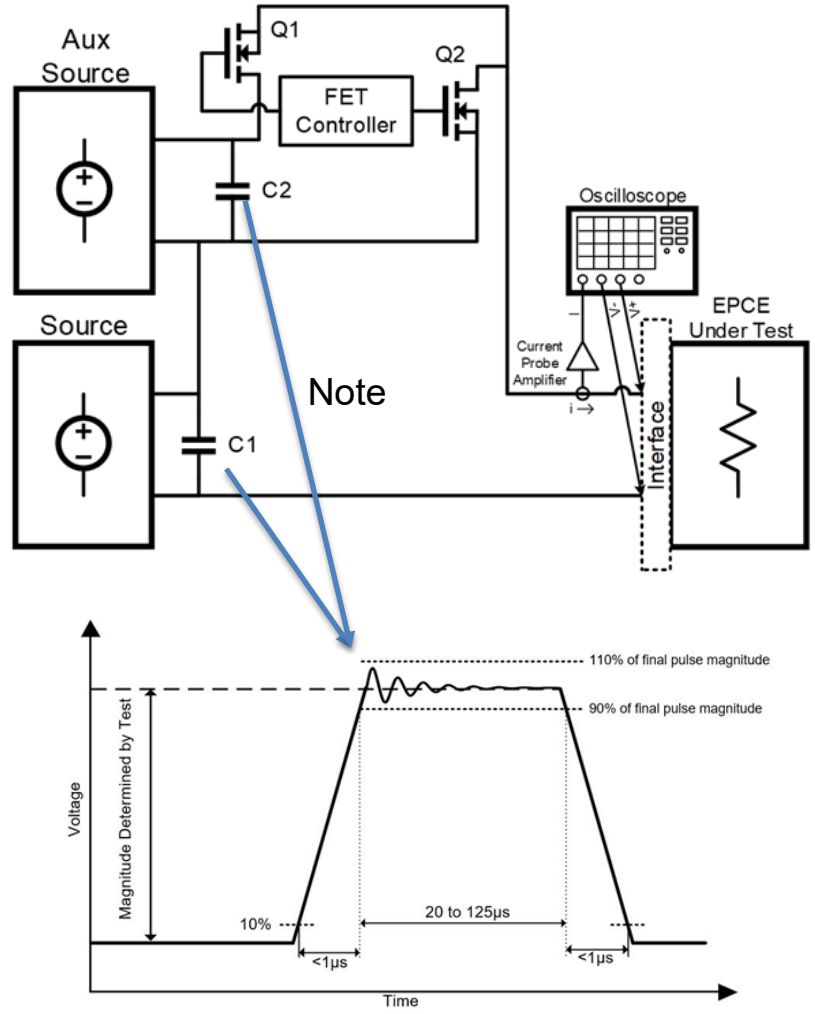
Testing for adequate damping of loads is important to overall stability

Large Signal Stability Test

- **Stiff source required to isolate EPCE performance**
- **Pulse must be adequately quick to produce proper response.**

Using a signal generator and an amplifier to drive the transistors Q1 and Q2 in complements, apply the pulses dictated in the verification requirement. Capture the voltage and current inputs to the EPCE.

Note: Stiff sources are required for this test. Capacitors C1 and C2 are optional and may be necessary if the source cannot meet the required injection voltage. Noncompliant input voltage pulses impact the results of the test. C1 and C2 must be low-ESR ceramic capacitors or equivalent. C1 should be selected to maintain the stiffness of the main source. C2 should be selected to remove any high frequency distortion when the auxiliary source is switched in. An example of the target injection waveform is shown in the figure. Analysis should be done with an ideal voltage source for worst-case performance.



Large Signal Stability Pulse

Source contributions must be removed for checking Load stability

Defining Ripple Voltages

- **What are ripple voltages?**
  - The total system ripple voltage is comprised of the collective contributions from sources and loads.
  - Voltages are superimposed on the power system.
  - Ripple voltages negatively impact sensitive loads, such as instrumentation.
  - Ripple is defined by three characteristics; peak ripple voltage, ripple voltage amplitude, and ripple voltage spectrum.

1) **Peak** Ripple Voltage

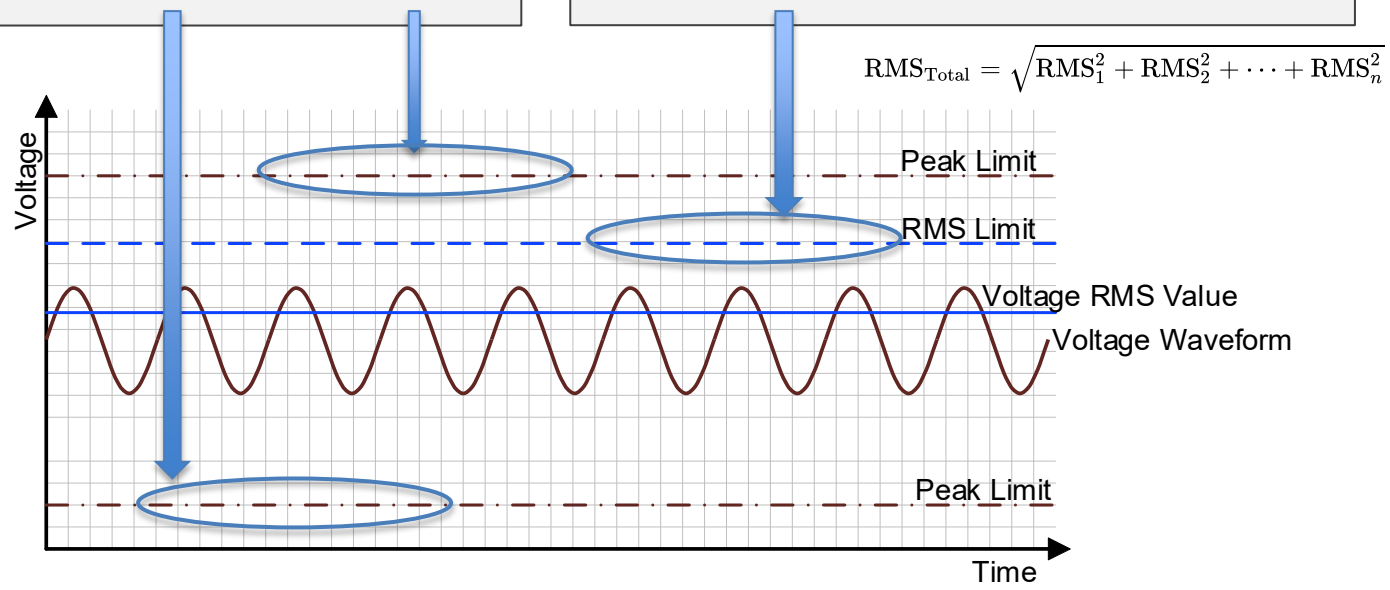
The peak ripple voltage at the Interface shall be less than X Vp (peak) in a bandwidth of 30Hz to 1 MHz.

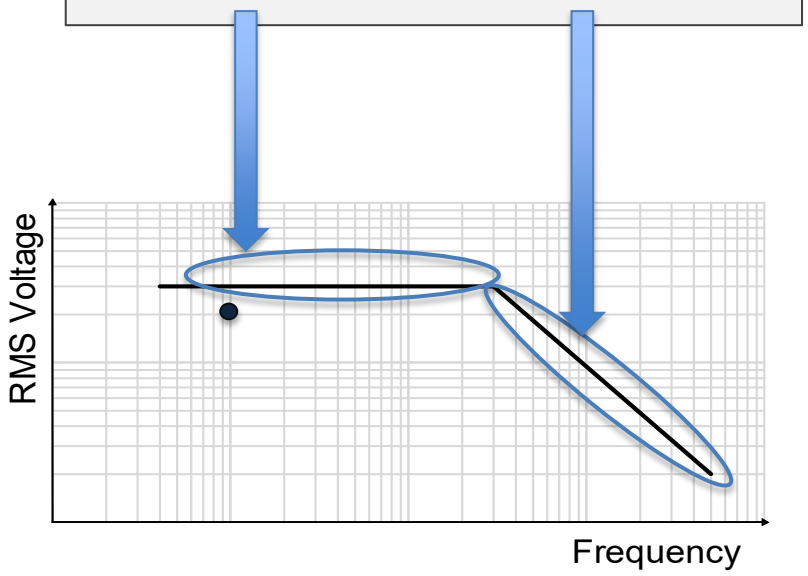
2) Ripple Voltage **Amplitude**

Interface ripple voltage amplitude shall be less than Y Vrms in a bandwidth of 30 Hz to 1 MHz.

3) Ripple Voltage **Spectrum**

The frequency distribution of the ripple voltage shall remain within the limits shown from the figure.

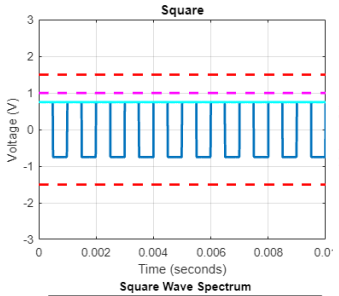
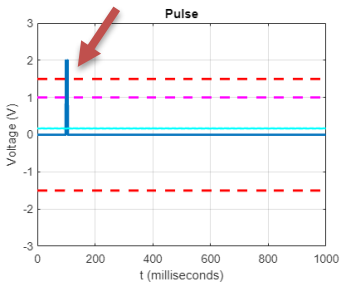
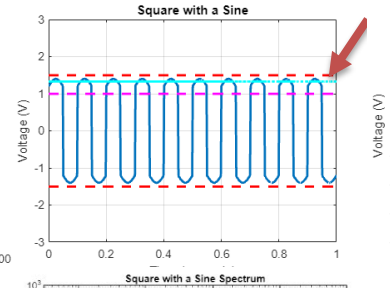
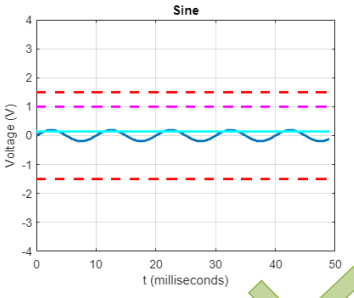
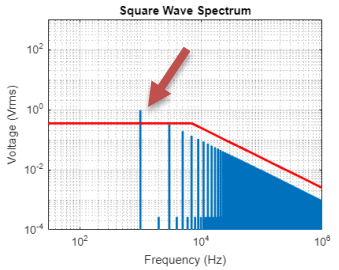
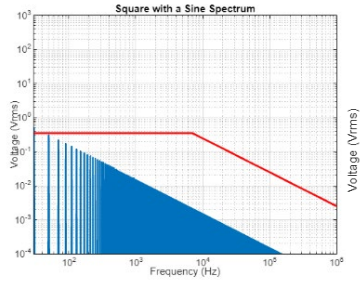
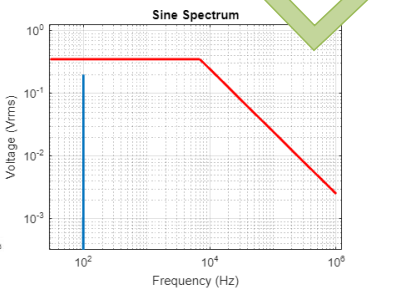




Why Three Ripple Voltage Requirements

- **Why three ripple voltage requirements?**
  - Different waveforms violate different requirements; see examples

Examples

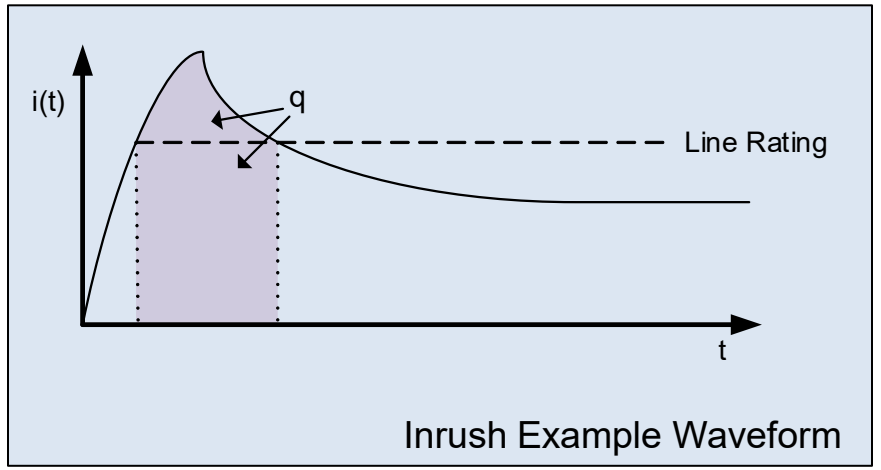
Violates only **spectrum** requirements	Violates only **peak** requirements	Violates only **amplitude** requirements	All requirements met
			
	N/A		

Three distinct ripple requirements are necessary to cover all waveforms

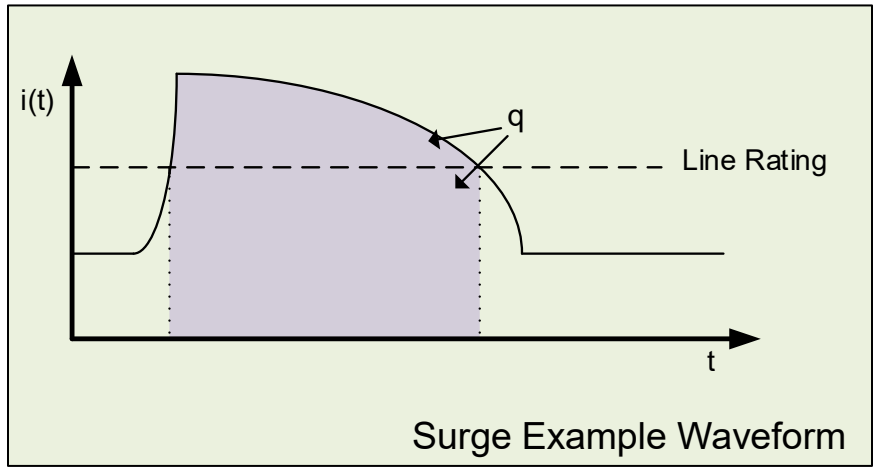
Inrush/Surge Requirements

- **Inrush requirements**
  - Stipulate how much overcurrent the EPS must allow when a new load is energized or connected
- **Surge requirements**
  - Stipulate how much overcurrent the EPS must allow during changes in operating modes or loading conditions
- **Requirements bind the amount of current in terms of area under current curve within bounds of worst-case load rating**
  - Measured in charge (Amps*Seconds)
  - Function is a requirement of line rating

Interface shall support load inrush/surge currents of:
0.012 A*Sec / A for loads with currents 0A < i < 10A
0.00253 A*Sec / A + 0.0947 for loads with currents 10A < i < 200A



Inrush Example Waveform

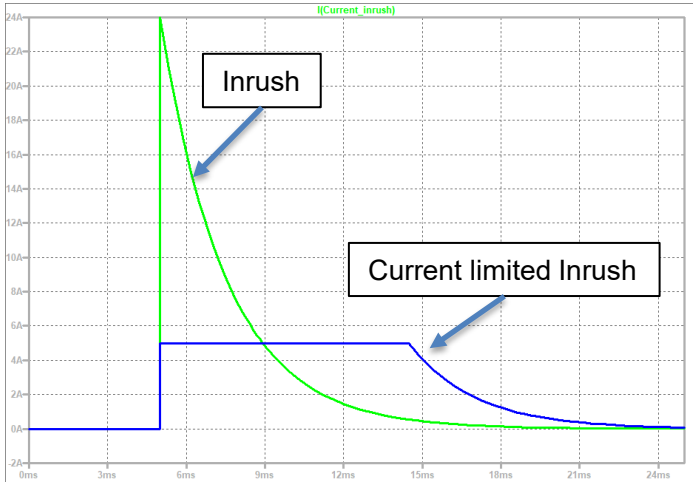


Surge Example Waveform

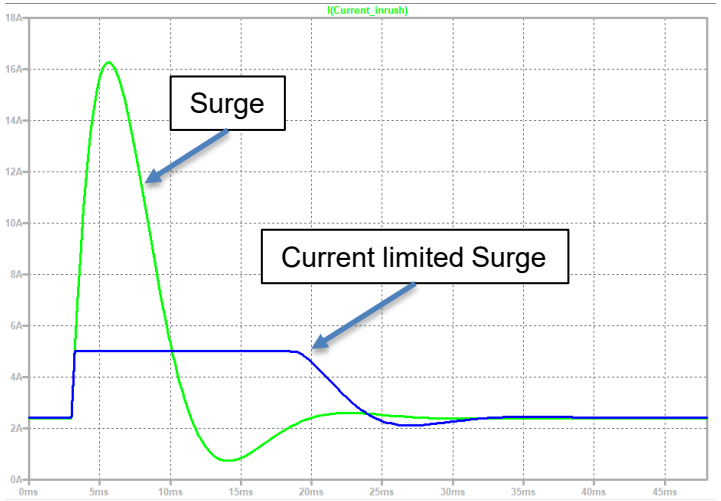
Inrush/Surge Current Transients

- **Inrush and surge currents behave differently if a line is current-limiting**
- **EPCE are allowed to have a certain amount of inrush during startup or surge during operation**
  - Allows for input filter capacitance and/or mode changes in load
    - Value based off historical space loads
- **Load compliance to requirements ensures proper operation with current limiting switchgear**
- **Requirement based on charge allows for optimal current limiting switch designs that still meet intent**
  - Charging of input filters on loads and protection against faults

5A line EPCE Inrush with No Load Example



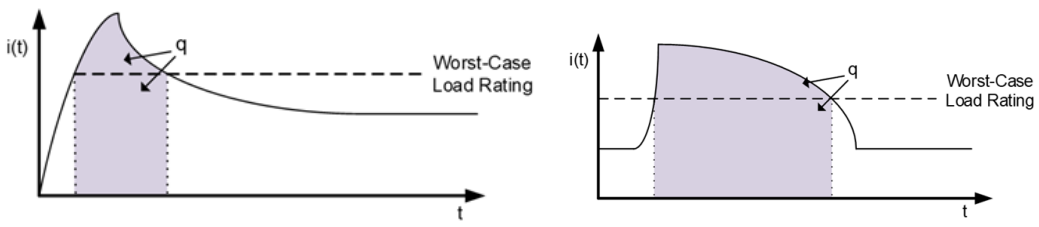
5A line EPCE with 2.5A load Surge Example



Loads must be designed to operate using current limiting switchgear

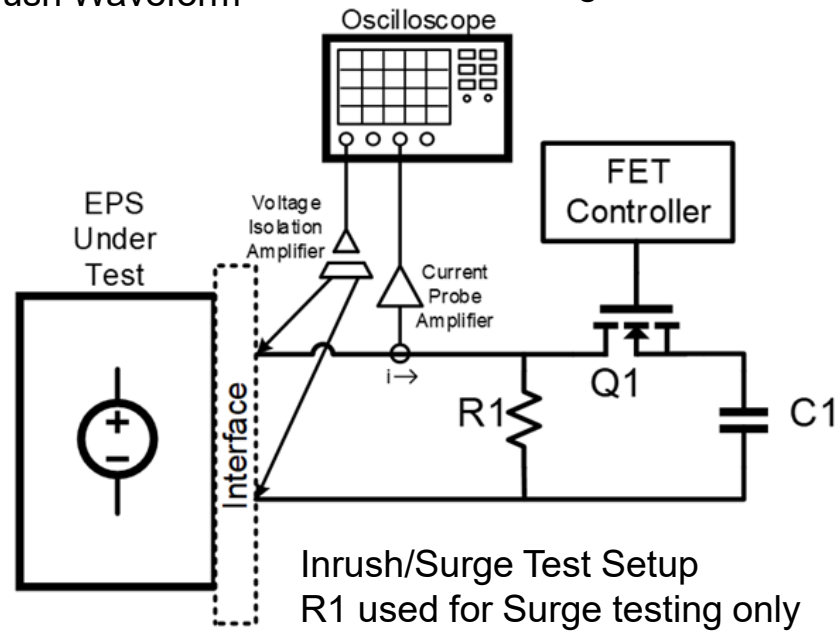
Surge and Inrush Testing

- **The inrush verification is successful by charging the equivalent capacitor without causing a trip of current limiting switchgear or other current limiting devices.**
- **Similarly, surge verification is successful by charging a smaller capacitor without causing a trip of current limiting switchgear or other current limiting devices with a parallel load present.**
  - The capacitor size for surges can be calculated by taking the charge divided by the voltage
    - The current split between R1 and C1 must be taken into account during this calculation
  - This test is necessary due to different startup and run characteristics of switches



Inrush Waveform

Surge Waveform

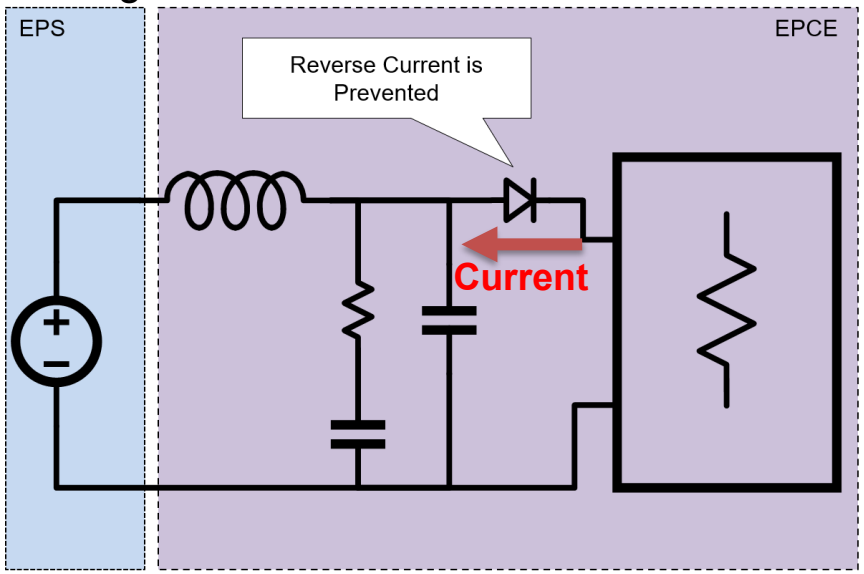


Inrush/Surge Test Setup
R1 used for Surge testing only

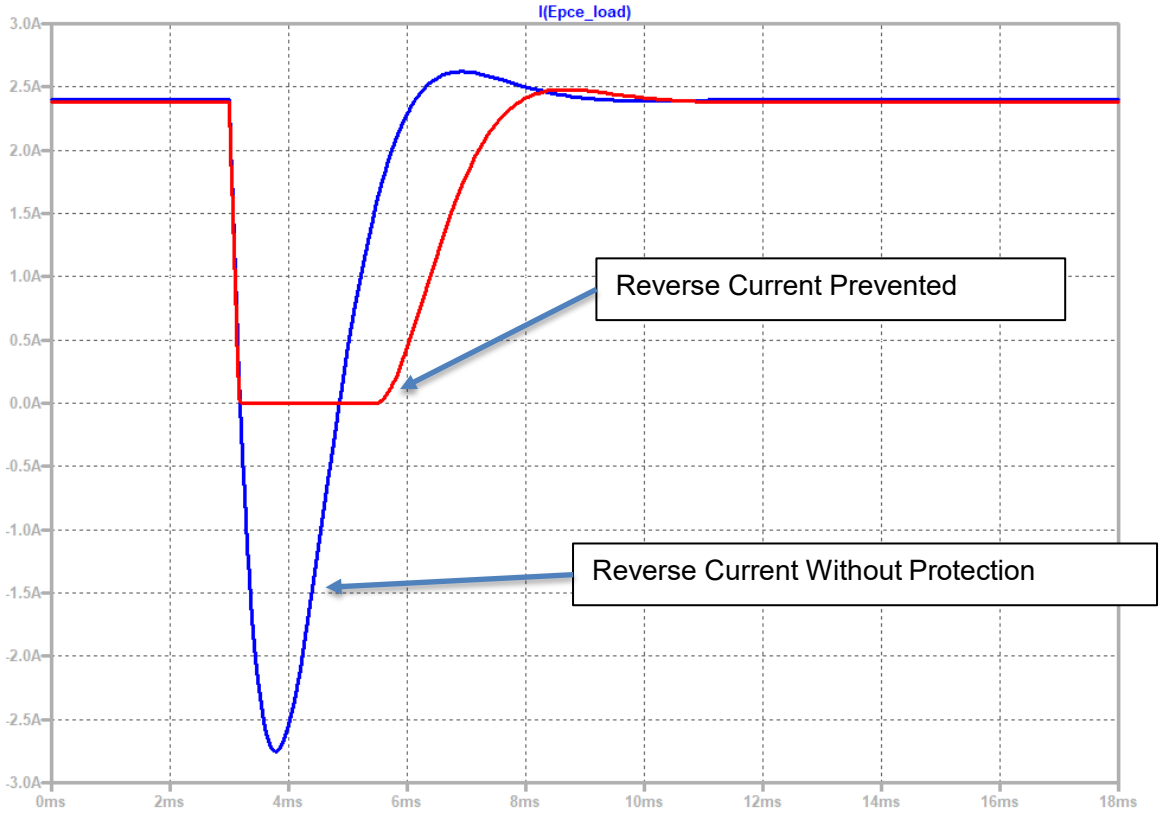
Testing with a switched capacitance demonstrates worst case expected performance

EPCE Reverse Current Example

- **EPCE must be designed to prevent reverse currents back into the EPS**
  - Uncontrolled regenerative energy can destabilize a power system
  - Exception input filter allowed capacitance
- **Current must remain positive under normal operation**
  - Necessary to ensure EPS remains in control of bus voltage



EPCE Reverse Current Example



Loads must be designed to prevent reverse currents back onto the power system

Conclusion

- **Historical knowledge and lessons learned play a major role in the development of a Power Quality Specification and have taught that:**
  - Requirements for overall performance of a power system are necessary for integration of independently designed sources and loads
    - Small and Large signal stability requirements are needed ensure stability once integrated
    - Current limiting switchgear requirements allow for circuit protection while still allowing for necessary design features
    - Reverse current requirements on the EPCE ensure bus regulation
    - Fault coordination is required to ensure large complex buses are protected from failure
    - Multiple ripple requirements are needed to cover all possible AC bus voltages
  - Source and Load requirements in a single document helps drive integration
  - Current limiting switchgear requirements defined by charge allows for optimal design of protective switchgear against faults while preventing overdesign of switchgear
    - Charging of a load input filter less severe than a hard fault
  - Including and properly defining Verifications and example test setups in document increase repeatability of tests and help to guide intent of the requirements themselves
- **Open and ongoing discussion on requirements and verifications with suppliers is important**
- **Lessons learned from past programs should always be considered and incorporated into future specifications**

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