Workshop H : BUILDING RELIABLE CIRCUIT BOARD ASSEMBLIES - THE LESSONS LEARNED

Bhanu Sood

NASA Goddard Space Flight Center

Phone: +1 (301) 286-5584

bhanu.sood@nasa.gov

August 23rd and 24th, 2022

SAFETY and MISSION ASSURANCE DIRECTORATE Code 300

Safely Achieve Amazing Science Through Mission Success

Disclaimer

The material herein is presented “for guidance only”. We do not warrant the accuracy of the information set out on this presentation. It may contain technical inaccuracies or errors and/or non-updated data.

Information may be changed or updated without notice.

Course Outline

- **Section 1: Introduction**
- **Section 2: PCB Technology**
- **Section 3: Failure Mechanisms**
- **Section 4: Moisture Effects**
- **Section 5: Tests and Inspection**
- **Section 6: Recent Data on PCB Assurance**
- **Section 5: Closure**

What is Reliability?

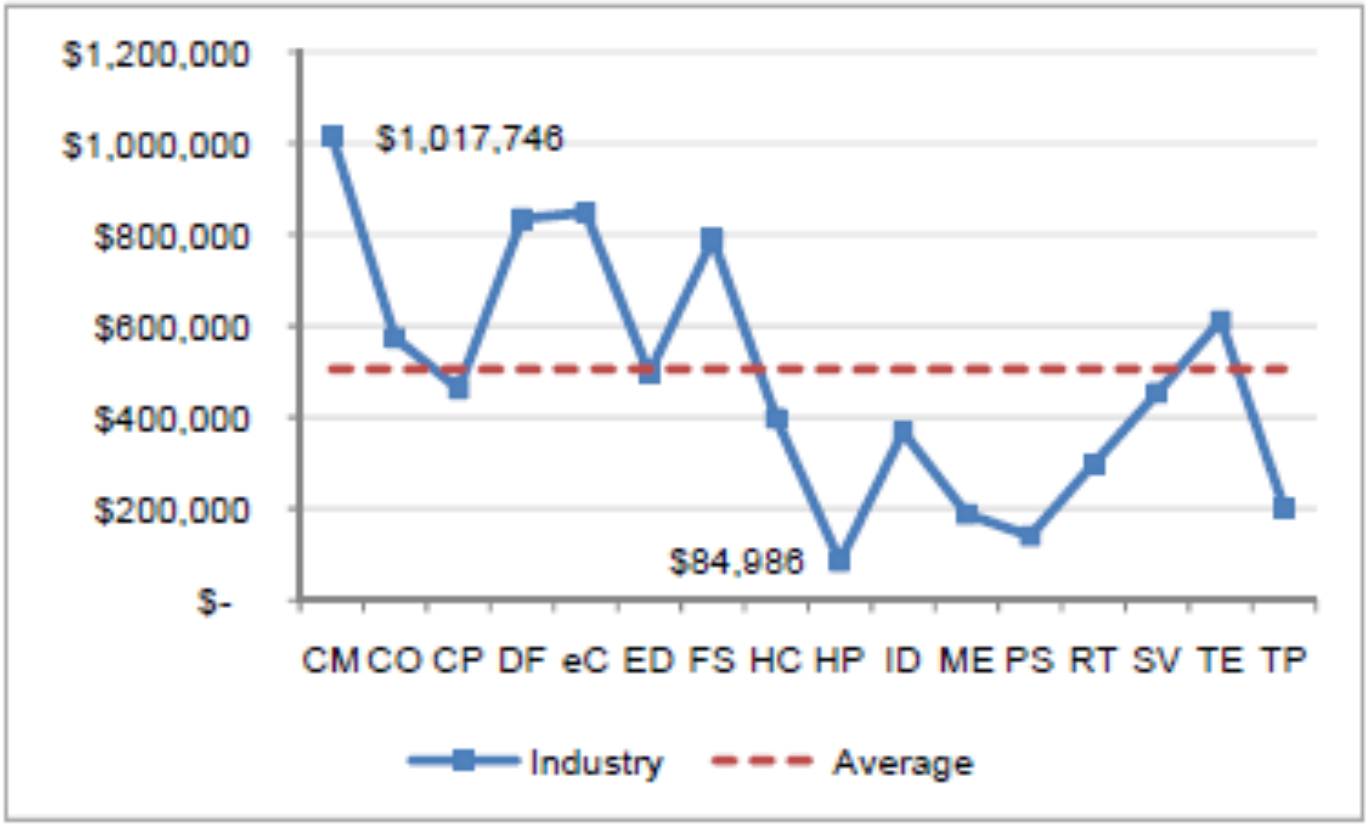
Reliability is the ability of a product to properly function, within specified performance limits, for a specified period of time, under the life cycle application conditions

- Within specified performance limits: A product must function within certain tolerances in order to be reliable.
- For a specified period of time: A product has a useful life during which it is expected to function within specifications.
- Under the life cycle application conditions: Reliability is dependent on the product's life cycle operational and environmental conditions.

When a Product Fails, There Are Costs . . .

- To the Manufacturer
  - Time-to-market can increase
  - Warranty costs can increase
  - Market share can decrease. Failures can stain the reputation of a company, and deter new customers.
  - Claims for damages caused by product failure can increase
- To the Customer
  - Personal injury
  - Loss of mission, service or capacity
  - Cost of repair or replacement
  - Indirect costs, such as increase in insurance, damage to reputation, loss of market share

Cost of a Single Unplanned Data Center Outage Across 16 Industries



Industry	Code
Communication	CM
Co-location	CO
Consumer	CP
Defense	DF
eCommerce	eC
Education	ED
Financial	FS
Healthcare	HC
Hospitality	HP
Industrial	ID
Media	ME
Public sector	PS
Retail	RT
Services	SV
Technology	TE
Transportation	TP

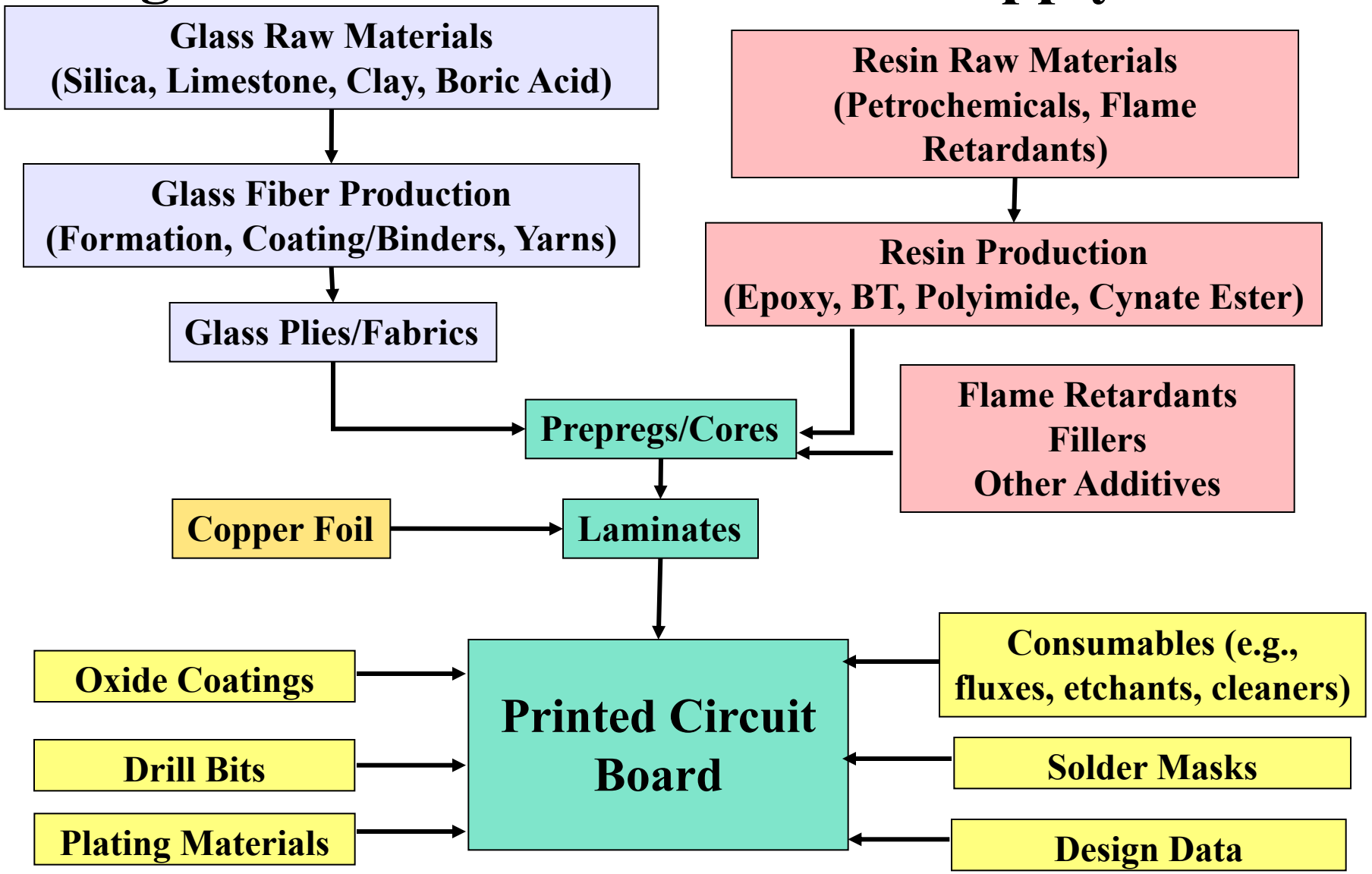
The average cost of data center downtime across industries was approximately **$5,600 per minute.**

Ref: Ponemon Inst., "Calculating the Cost of Data Center Outages," Feb. 1, 2011.

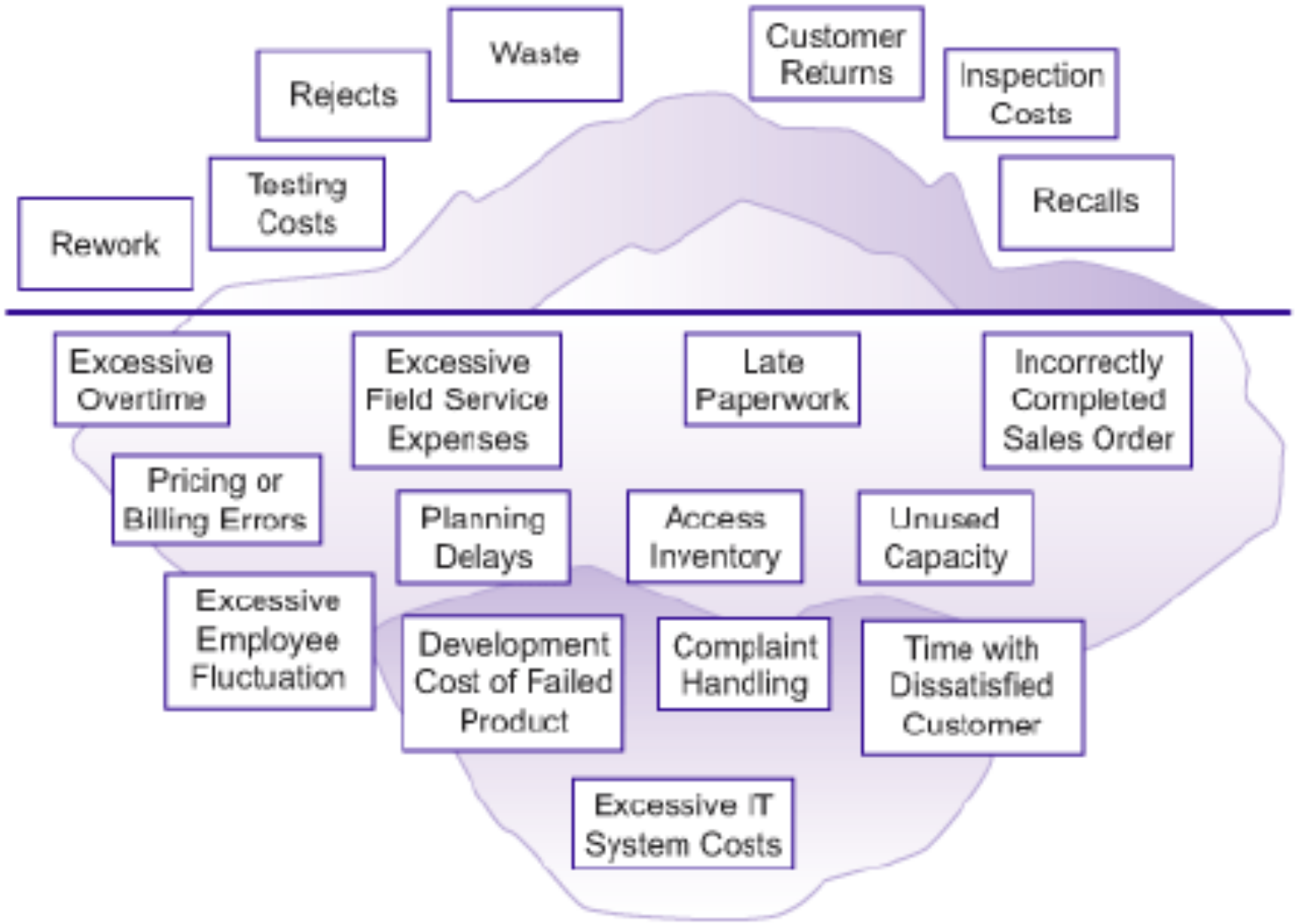
Reliability Requires that we Manage the Supply Chain

- Many companies do not adequately consider quality and reliability in the creation and management of efficient and cost effective supply chains
- Thus, many companies do not know what they are getting and what is changing

Organic Printed Circuit Board Supply Chain



Iceberg Model of Cost of Poor Quality



Ref: A. Buthmann, "Cost of Quality: Not Only Failure Costs," iSixSigma.

Some Failure Related Definitions*

Failure……	product no longer performs the intended function
Failure Mode……	change in performance by which a failure is observed (can vary in a system or sub-system context)
Failure Mechanism…..	physical, chemical, thermodynamic or other process that results in failure
Failure Site……	location of the failure
Fault/Defect……	weakness (e.g., crack or void) that can locally accelerate damage accumulation and failure
Load……	application/environmental condition (electrical, thermal, mechanical, chemical...) that can precipitate a failure mechanism
Stress……...	intensity of the applied load at a failure site

**** - definitions are piece part, PCB or assembly level***

PCB Failures – Moisture

- Printed circuit board (PCB) quality, reliability and functionality are highly influenced by moisture (both ambient and internal).
- PCBs witness moisture at various stages:
  - Lamination
  - Assembly
  - Rework
  - Transportation
  - Maintenance
  - Wet process
  - Screening
  - Storage
  - Operation
- Moisture can be initially present in the epoxy glass prepreg, absorbed during the fabrication of PCB or diffuse into PCB during storage
  - Presence effects the mechanical properties (Tg, CTE) and electrical performance.
- PCB handling and storage guidelines are required to prevent inadvertent damage and maintain reliability.

PCB Failures – Process

- The transition to lead-free soldering of printed circuit boards (PCBs) using solder alloys such as Sn/Ag/Cu has resulted in an increase in peak temperature exposures (by 30-40°C) and longer time above liquidus (by 15-30 seconds) during assembly compared with eutectic Sn/Pb solders.
- Rework and repair of assembled circuit boards also contributes to additional high temperature exposures.
- The high temperature exposures associated with lead-free soldering can alter the circuit board laminate material properties and can affect the performance and reliability of the PCB and entire electronic assembly.
- Knowledge of laminate material properties and their dependence on the material constituents, combined with their possible variations due to lead-free soldering exposures is an essential input in the selection of laminates for appropriate applications.

Board Level Failures

Plated Through Hole (PTH)/Via

1. Fatigue cracks in PTH/Via wall
2. Overstress cracks in PTH/Via wall
3. Land corner cracks
4. Openings in PTH/Via wall
5. PTH/Via wall-pad separation

Electrical

6. Electrical overstress (EOS)
7. Signal interruption (EMI)

Board

8. CFF (hollow fiber)
9. CFF (fiber/resin interface)
10. Electrochemical migration
11. Buckling (warp and twist)

Copper Metallization

12. Cracks in internal trace
13. Cracks in surface trace
14. Corrosion of surface trace

Assembly Level Failures

Solder Interconnect

- Poor Solderability/Wettability
  - Tombstoning; Can accelerate other solder failure mechanisms
- Overstress Interconnect Failures
  - Solder Fracture (accelerated by intermetallic formation)
- Wearout Interconnect Failures
  - Solder Fatigue, Solder Creep
- Solder Bridging
- Component Failure due to Handling

Common Failures in Today's PCB

- Initiated at plated through holes (PTHs)
- Initiated by handling (bow and twist)
- Pad cratering (stress)
- Conductive filament formation (CFF)
- Electrochemical migration (PCB cleanliness)

Section - 2

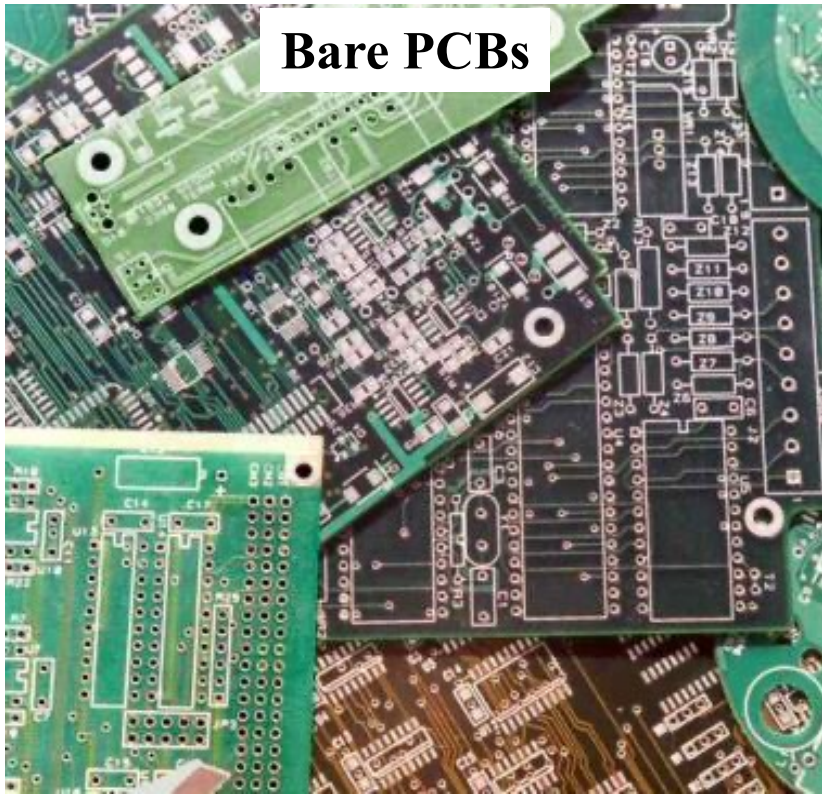
Introduction to PCB Technology

Printed Circuit Board

Printed circuit boards are the baseline in electronic packaging – they are the interconnection medium upon which electronic components are formed into electronic systems.

FR-4 PCB materials are glass reinforced PCBs.

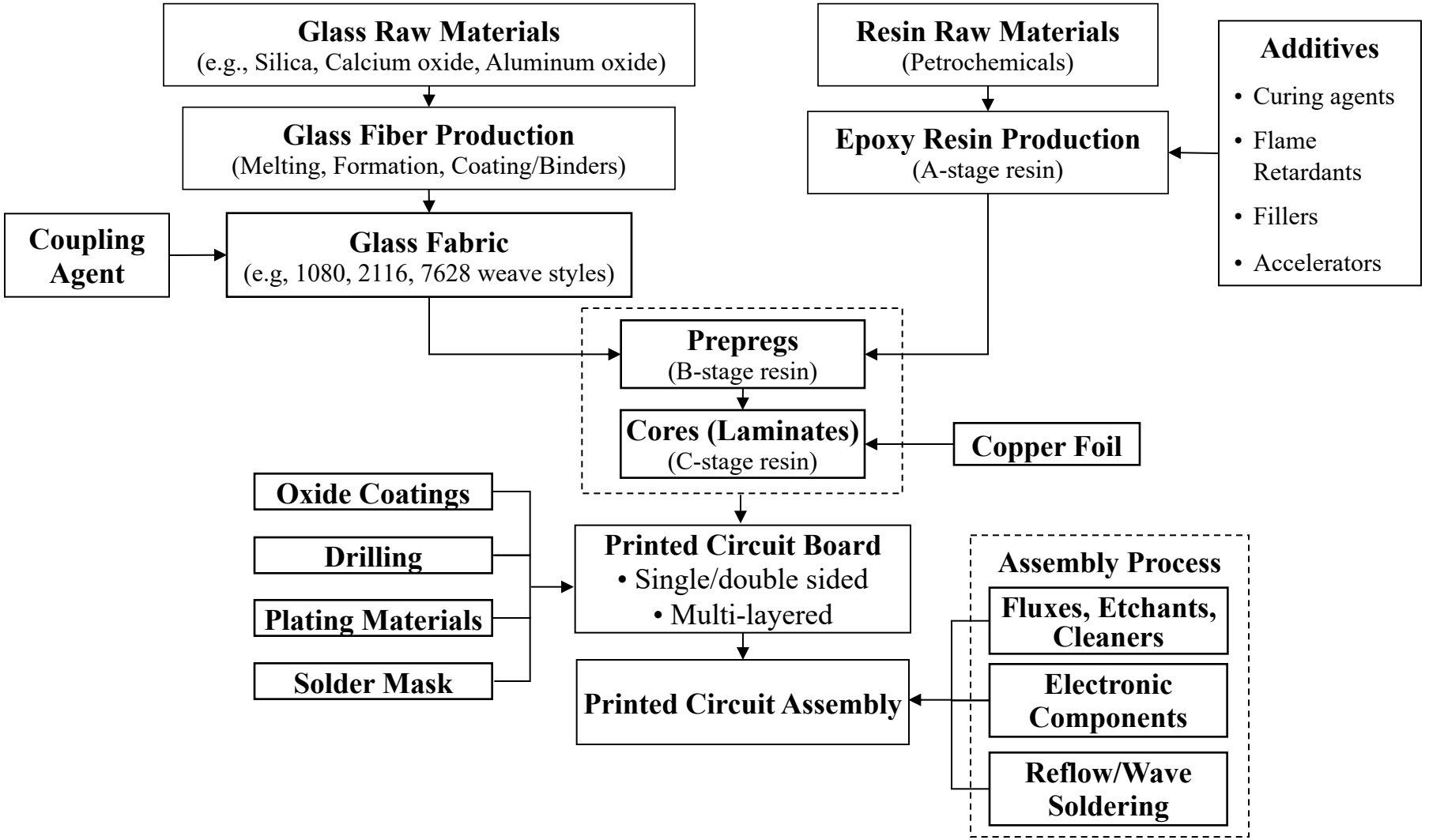
- Epoxy resin reinforced with woven glass.
- "FR" stands for flame retardant.



PCB Classification

- PCBs are generally classified based on the following criteria:
  - Dielectric materials used – Epoxy, Bismaleimide Triazine, Cyanate Ester, Polyimide, Polytetraflouroethylene (PTFE), Phenolics, Polyester
  - Reinforcement materials – Glass fabric, Kevlar fabric, PTFE fabric, Paper, Polyethylene terephthalate (polyester), Silicon carbide
  - Circuit type – Digital, Analog, Mixed, RF, Microwave
  - Electronic components – Through-hole, Surface-mount, Mixed-technology
  - Board construction – Single-sided, Double-sided, Multilayer, Flex, Rigid-flex
  - Design complexity – Circuit density, and Low, moderate or high manufacturability
- There are differences in materials, processing steps or both depending on the PCB

Printed Circuit Board Assembly Fabrication



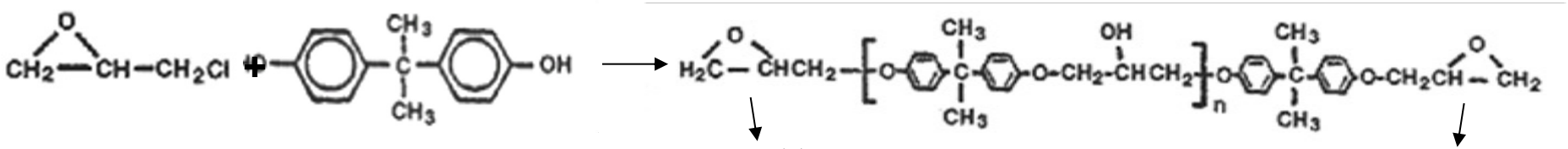
Constituents of FR-4 Laminates

Constituent	Major function (s)	Example material (s)
Reinforcement	Provides mechanical strength and electrical properties	Woven glass (E-grade) fiber
Coupling agent	Bonds inorganic glass with organic resin and transfers stresses across the structure	Organosilanes
Resin	Acts as a binder and load transferring agent	Epoxy (DGEBA)
Curing agent	Enhances linear/cross polymerization in the resin	Dicyandiamide (DICY), Phenol novolac (phenolic)
Flame retardant	Reduces flammability of the laminate	Halogenated (TBBPA), Halogen-free (Phosphorous compounds)
Fillers	Reduces thermal expansion and cost of the laminate	Silica, Aluminum hydroxide
Accelerators	Increases reaction rate, reduces curing temperature, controls cross-link density	Imidazole, Organophosphine

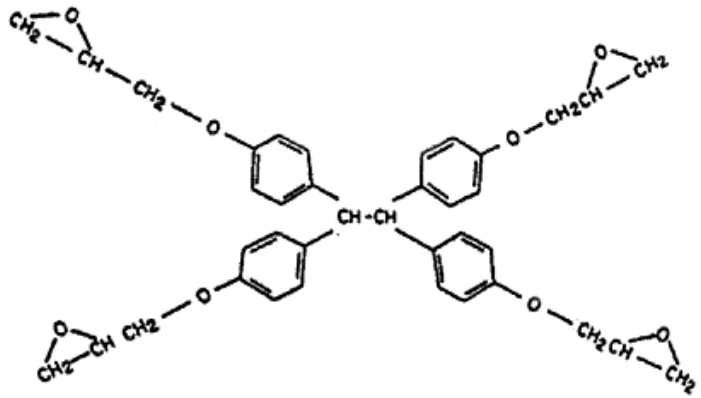
Constituents of FR-4 Laminates

-Resin-

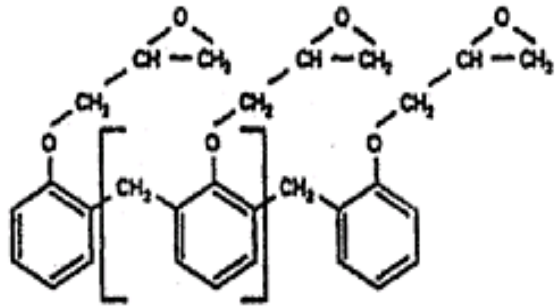
- Diglycidyl Ether of Bisphenol-A (DGEBA) is the epoxy resin used in FR-4 laminates
- DGEBA is derived from the reaction of Epichlorohydrin with Bisphenol-A



Epichlorohydrin Bisphenol-A Epoxide DGEBA (Bi-functional epoxy resin) Epoxide



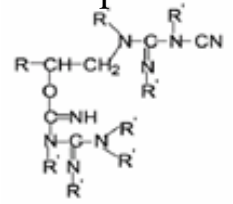
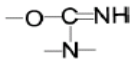
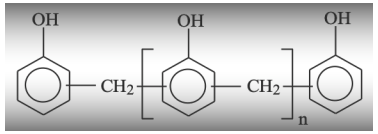
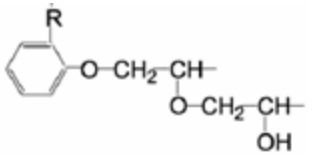
Tetra-functional epoxy resin



Multi-functional epoxy resin

- The epoxy groups react in subsequent resin polymerization and result in curing of the resin system

Curing Agents Comparison*

Dicy cured resin system	Phenolic cured resin system
• **Curing agent:** – dicyandiamide  – low molecular weight organic compound  • **Cured resin system:** – linear aliphatic molecule – These aliphatic bonds can be broken at elevated temperatures and hence dicy cured systems have lower thermal decomposition temperature – The presence of highly polar carbamidine-carbamide bond results in hygroscopic nature (less CAF resistant compared to phenolic systems)  – Strong polar nitrogen atom can destabilize brominated epoxy resin at higher temperatures resulting in the increase in bromine content	• **Curing agent:** – phenolic (resin)  – high molecular weight organic compound with greater resonating structures (relatively more stable than dicy) • **Cured resin system:** – Aromatic molecule  – More stable aromatic bonds and hence higher thermal resistance when compared to dicy systems

*** Peng, Y., Qi X., and C. Chrisafides, "The Influence of Curing Systems On Epoxide-based PCB Laminate Performance", Circuit world, Vol. 31, No. 4, pp. 14-20, 2005**

Coupling Agents

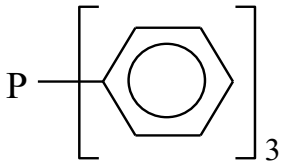
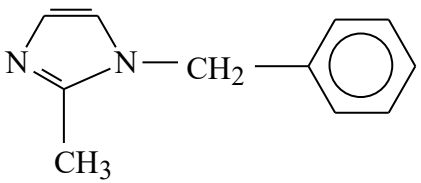
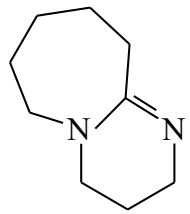
- Coupling agents bond inorganic glass fibers to organic epoxy resin
- They take care of high magnitude of shear forces that are established in bonding interface due to a significant difference in the CTE (10X) of glass fibers and epoxy resin, when subjected to high temperatures
- Ex: Organo silanes $Y\text{-}(CH_2)_n\text{-}Si\ (OX)_3$

  (Y-organo functional group; OX- silicon functional group)

Fillers

Common filler materials	Typical functions
Silica	Reduce cost
Hydrated alumina	Decrease coefficient of thermal expansion
Aluminum Silicate	Improve flammability
Ceramic Zircon	Reduce moisture absorption
Calcium Carbonate	Increase thermal conductivity
Aluminum Powder	Increase compressive yield strength
Mica	Improve arc resistance
Magnesium Silicate	Increase surface hardness
Zirconium Sulphate	Improve thermal shock resistance
	Reduce tensile strength
	Decrease flexural strength and modulus
	Reduce volume resistivity

Accelerators

Type	Characteristics	Chemical Structure
Organophosphine	• Storage stability • Low water absorption • Good acceleration • Good electrical property* • Good heat and humidity resistance	
Imidazole	• High heat resistance • High reactivity • Poor electrical property* • High water absorption • Good acceleration	
Lewis Base Salt	• Good electrical property* • Storage stability • Low water absorption	

* Electrical properties include dielectric constant, dissipation factor, volume resistivity, dielectric strength

Flame Retardants

- FR-4 PCBs, being plastics, are inherently flammable. Flame retardants are added into the resin system to enhance their self-extinguishing property.

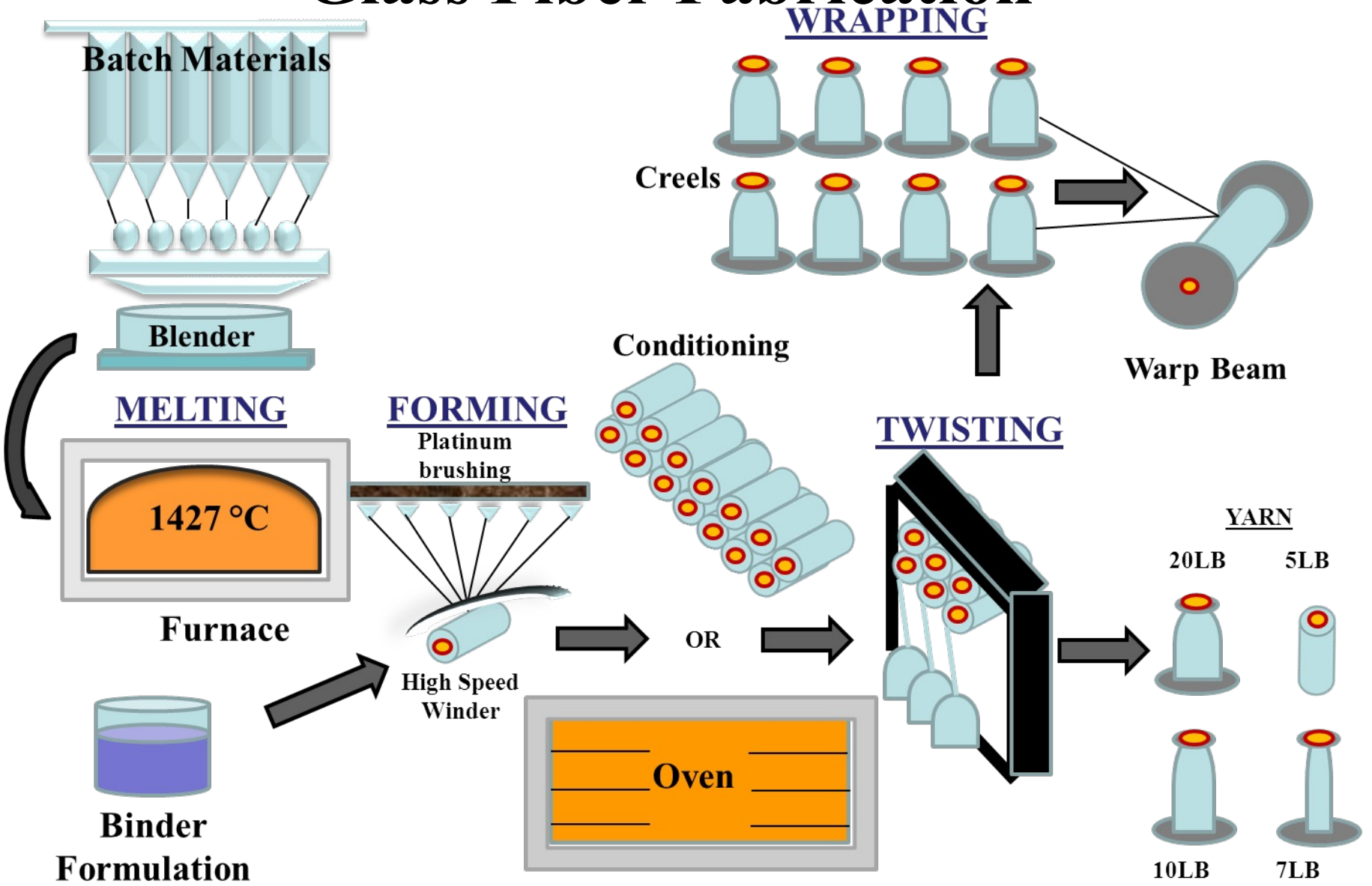
- Typical flame retardants used in PCBs
  - Halogenated flame retardants (Brominated and chlorinated)
  - Inorganic flame retardants [Aluminum trioxide, Magnesium hydroxide, Ammonium polyphosphate, Red phosphorus (elemental phosphorous-polymeric P_n)]
  - Organophosphorus flame retardants (Phosphate esters)
  - Nitrogen-based organic flame retardants

Reinforcement: E-Glass

Typical composition of E-glass:

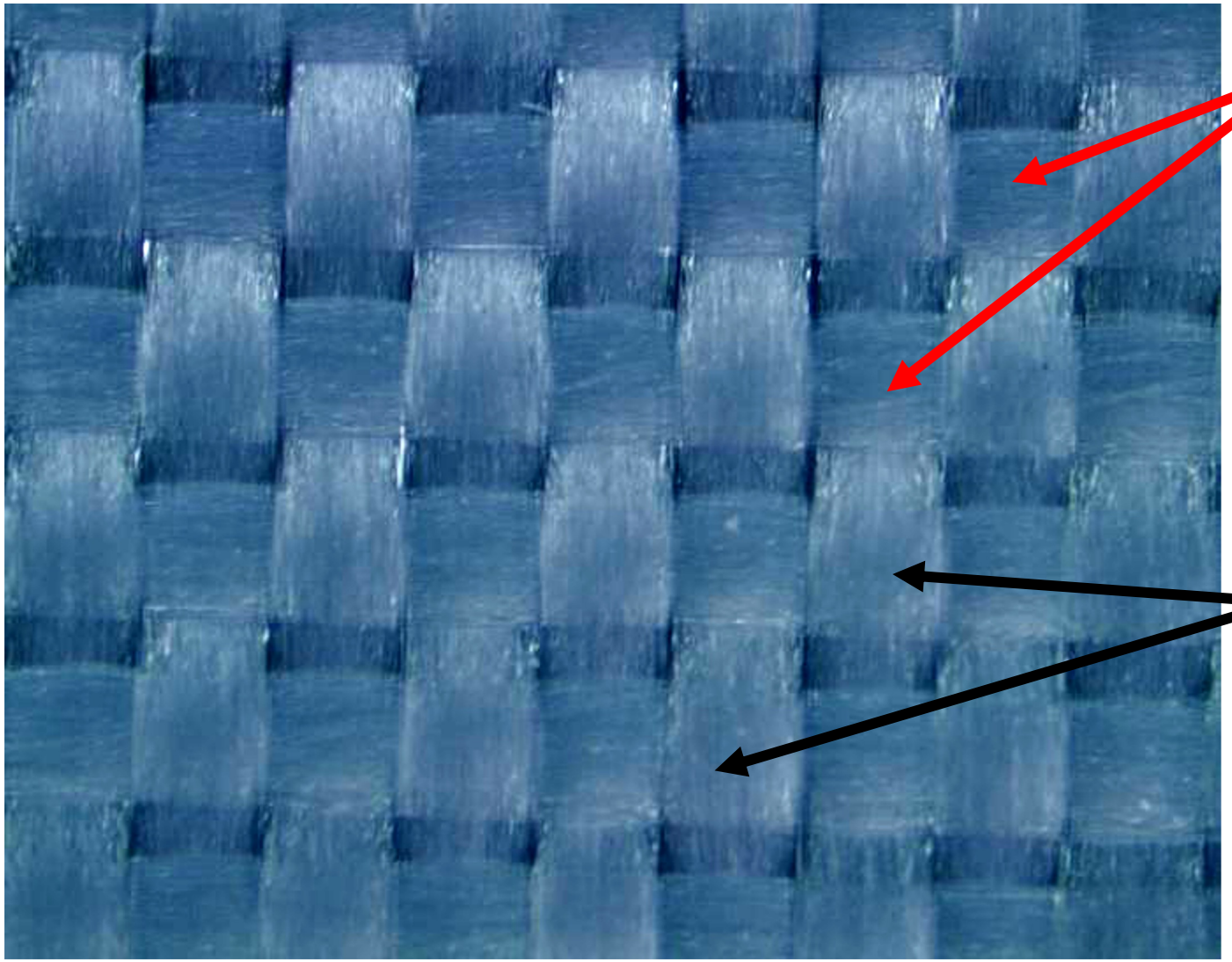
Component	% Composition
• Silicon dioxide (SiO_2)	52-56
• Calcium oxide (CaO_2)	16-25
• Aluminum oxide (Al_2O_3)	12-16
• Boron oxide (B_2O_3)	5-10
• Sodium oxide (Na_2O)+Potassium oxide (K_2O)	0-2
• Magnesium oxide (MgO)	0-5
• Iron oxide (Fe_2O_3)	0.05-0.4
• Titanium oxide (TiO_2)	0-0.8
• Fluorides	0-1

Glass Fiber Fabrication



Lu, Daniel, and C. P. Wong, eds. Materials for advanced packaging. New York: Springer, 2009.

Woven Fiberglass Fabric



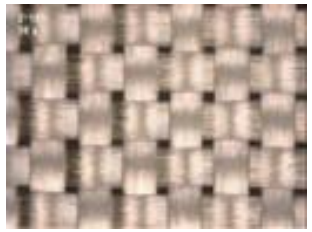
The initial set of parallel fiber bundles is known as the warp, and lie in the machine direction

A second set of parallel fiber bundles known as the fill, is woven through the first set

Glass Fabric Styles*



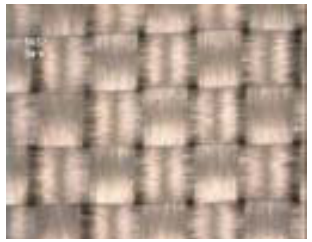
106 Style
Count: 56x56 (ends/in)
Thickness: 0.0015 (in)



2116 Style
Count: 60x58 (ends/in)
Thickness: 0.0038 (in)



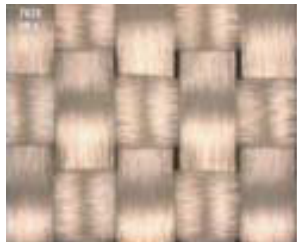
1080 Style
Count: 60x47 (ends/in)
Thickness: 0.0025 (in)



1652 Style
Count: 60x58 (ends/in)
Thickness: 0.0038 (in)



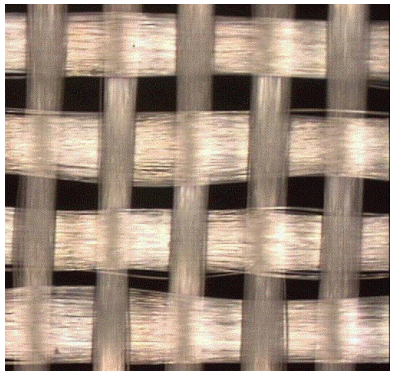
2113 Style
Count: 60x47 (ends/in)
Thickness: 0.0025 (in)



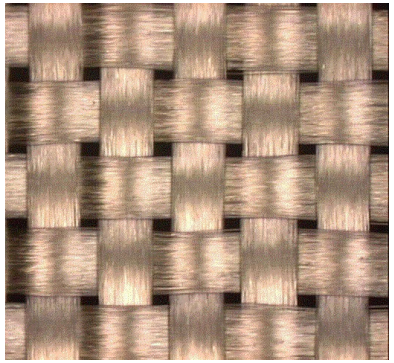
7628 Style
Count: 60x58 (ends/in)
Thickness: 0.0038 (in)

*** - Brist and Long, 2009**

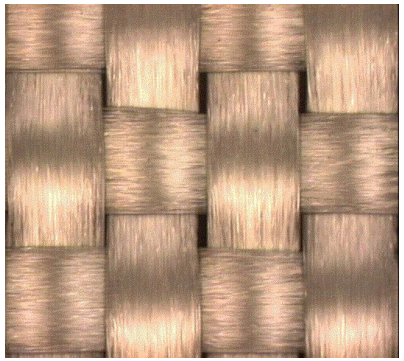
Glass Fabric Styles



1080 Style
Thickness: 63µm
Nominal glass dia.: 5µm

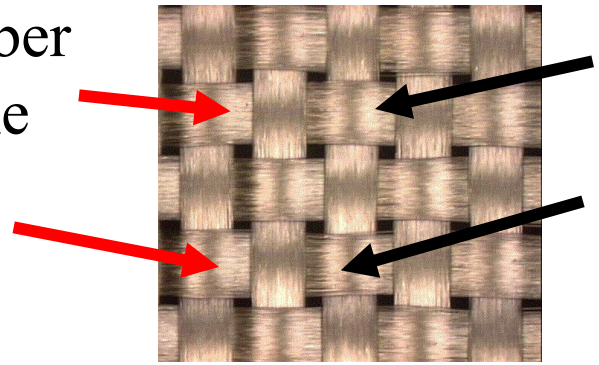


2116 Style
Thickness: 96µm
Nominal glass dia.: 7µm



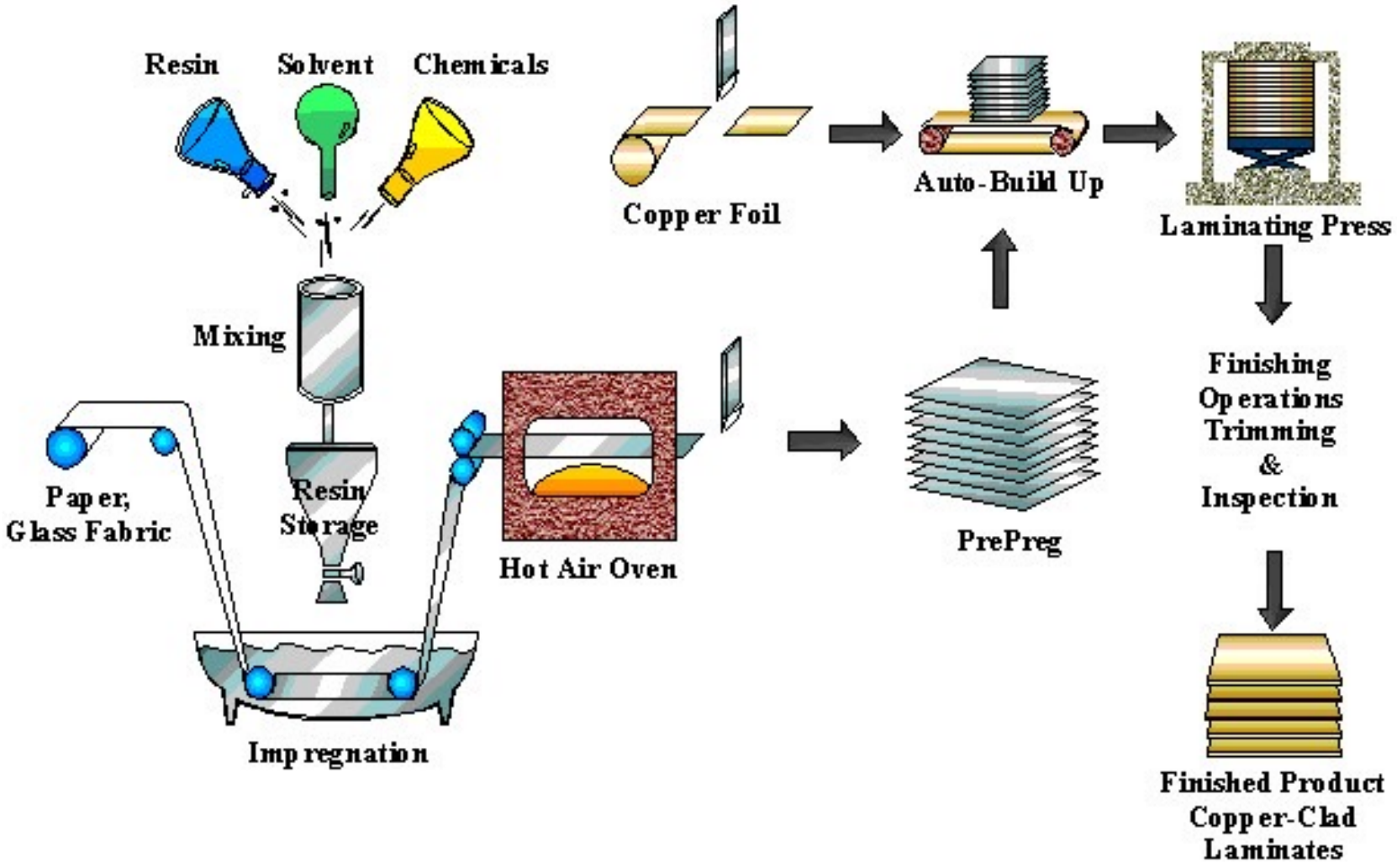
7628 Style
Thickness: 172µm
Nominal glass dia.: 9µm

Initial set of parallel fiber bundles is known as the warp, these lie in the machine direction.



A second set of parallel fiber bundles known as the fill, is woven through the warp bundles.

Laminate Fabrication



Types of PWBs

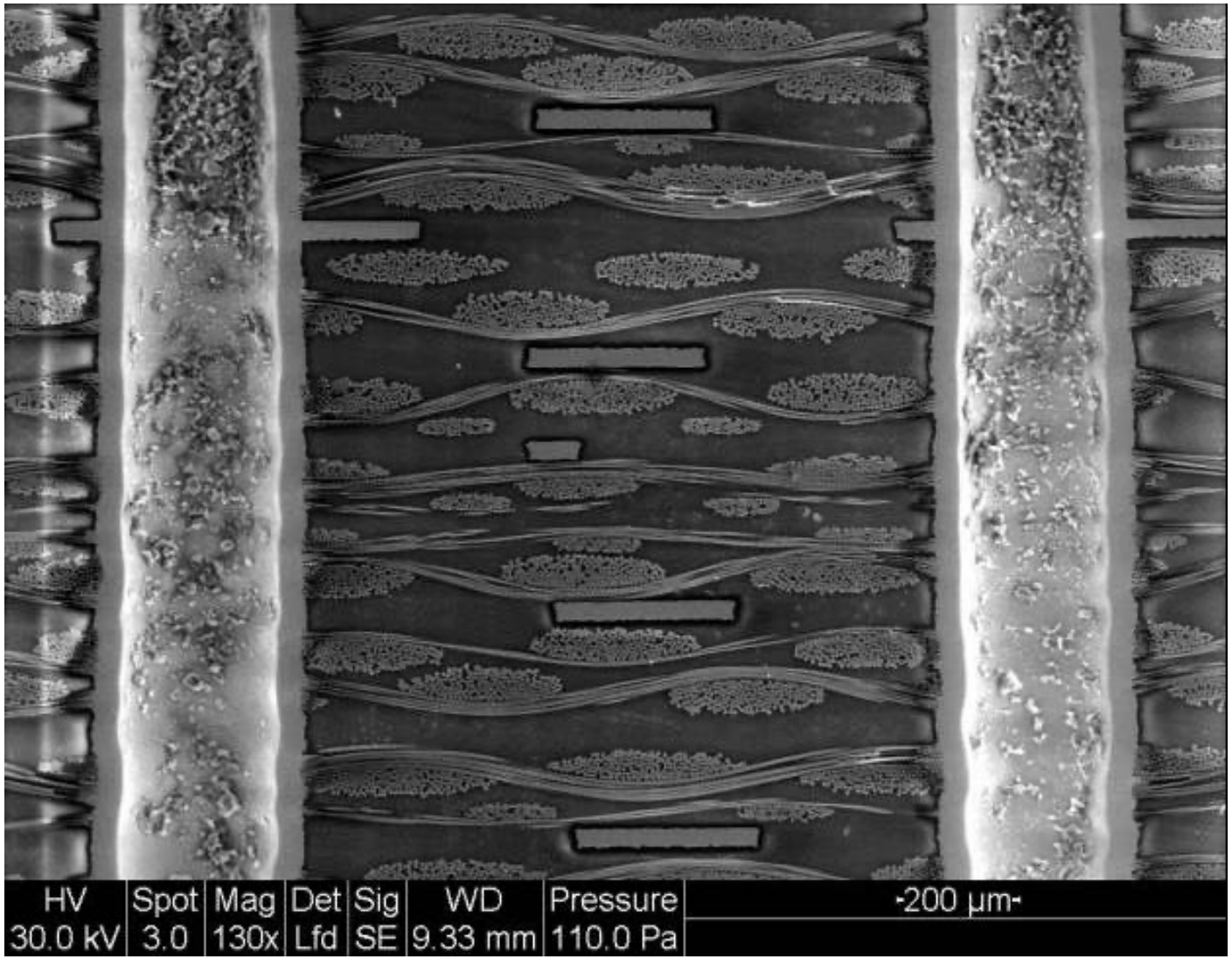
Complexity

- Single sided
- Double sided
- Layer count: Multilayer

Materials

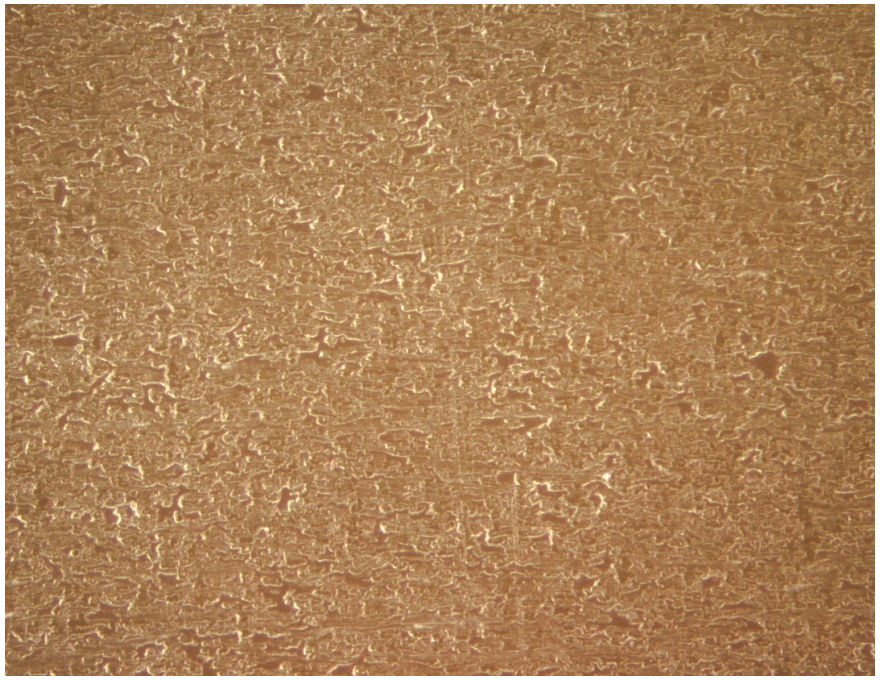
- Organic
  - FR-1, FR-2, CEM, FR-4, FR-5, BT, Polyimide, CE
- Ceramic
  - Alumina, Glass-Ceramic, Aluminum Nitride
- Silicon

E-SEM View of PCB Cross-section - Woven Fabric



Paper Based Materials

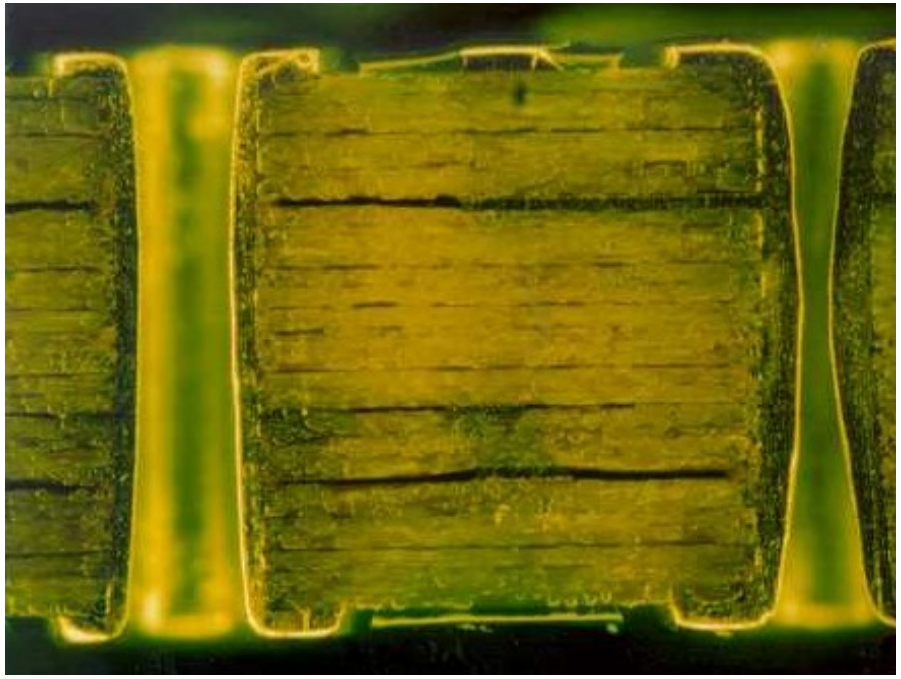




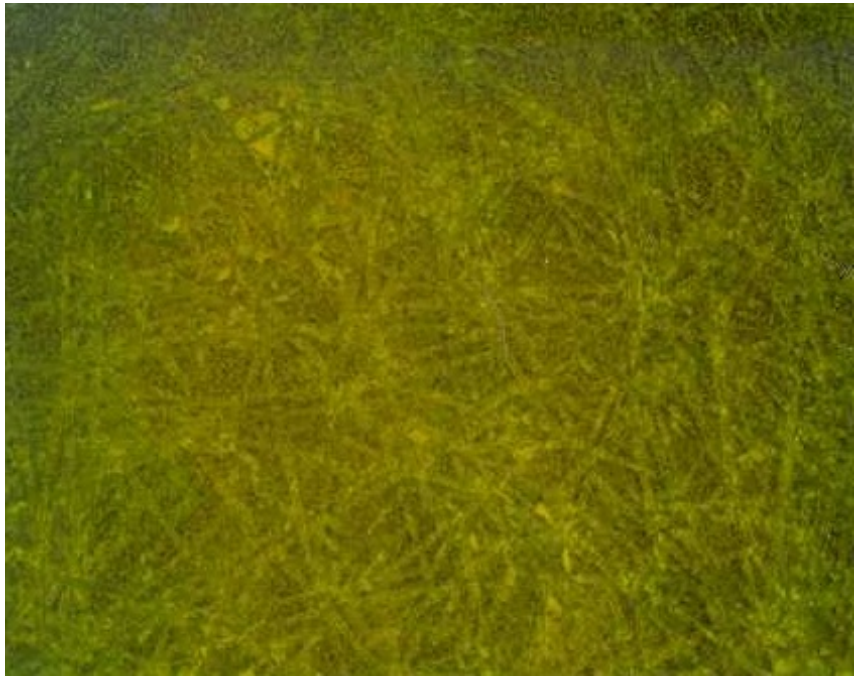
FR1, FR2, FR3, and CEM-1 are examples of paper-based laminates.

- FR1 and FR2 use phenolic resin binder. These two differ in their glass transition temperatures (130°C for FR1 and 105°C for FR2).
- FR3 uses an epoxy resin binder. The basic layer is paper. It is not suitable for plated through holes.
- CEM-1 is a paper based laminate with one layer of woven glass fabric. It is not suitable for plated through holes.

Non-woven Aramid Reinforcement



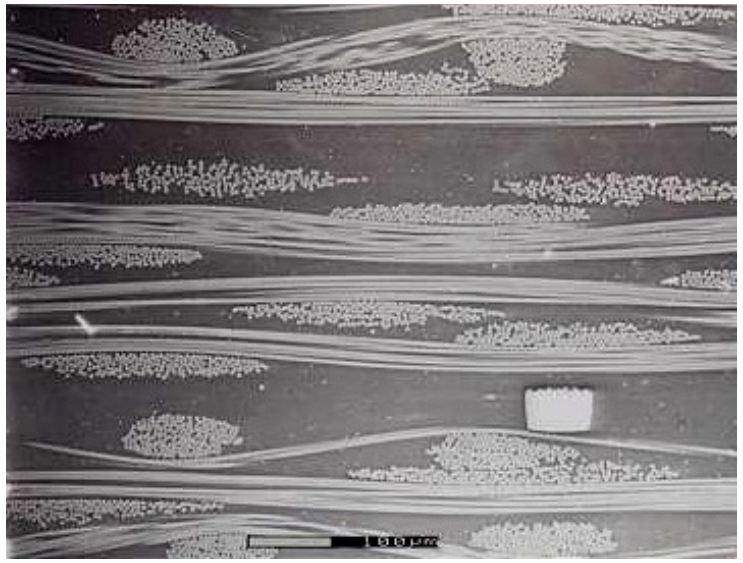
Side View



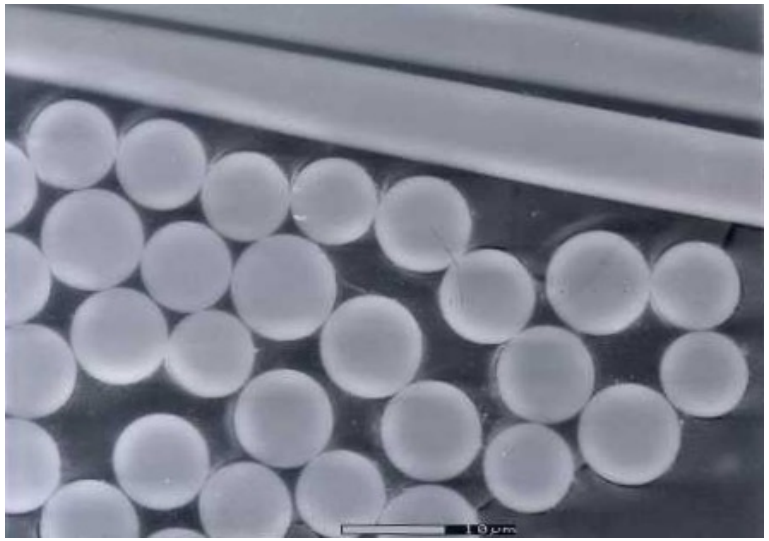
Top View

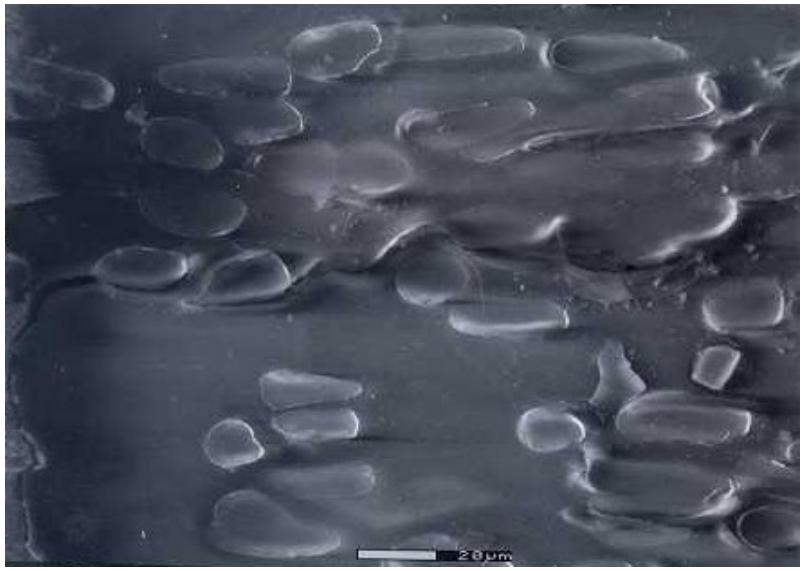
Generally, non-woven laminates have compositions that are more homogeneous, can be made smoother, and have more isotropic properties than woven laminates. These properties are all important for fine pitch surface mount applications, where thermal mismatch and coplanarity are key to the ease of manufacture and component attachment (e.g., solder joints, direct attach or flip-chip) reliability.

Comparison of Woven & Non-woven Fabric









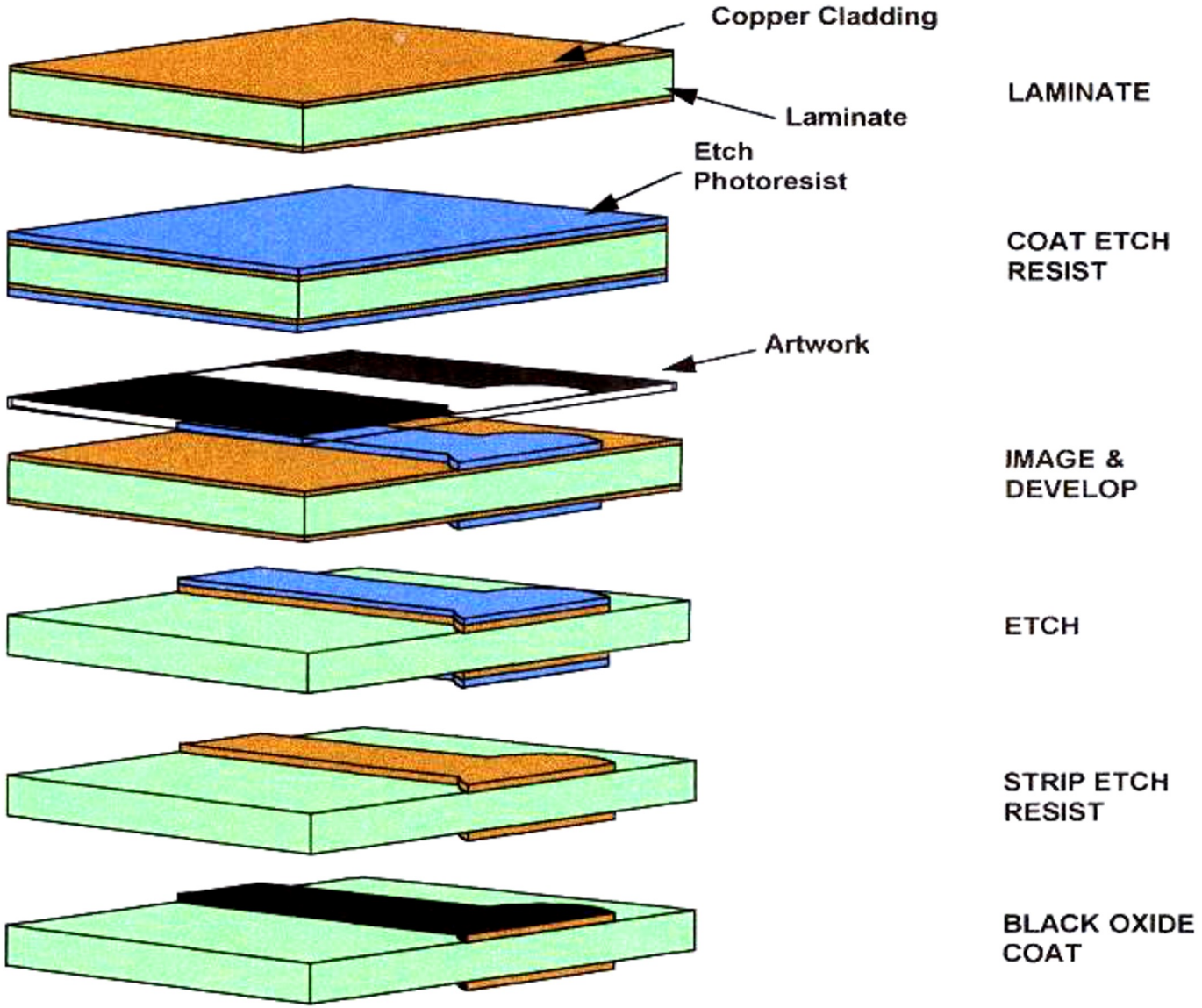
Copper Foil

- Thickness measured in oz./ft^2
  - 1 oz/ ft^2 => 1.35 mil, 2 oz/ ft^2 => 2.70 mil
- Electrodeposited copper
  - formed from plating polished steel drum; smooth and rough side; rough side makes for a good adhesive bond with laminate; grains elongated in direction perpendicular to sheet; not as ductile as rolled foil
- Rolled copper foil
  - progressive rolling and annealing; surface needs to be treated to form a good adhesive bond with laminate

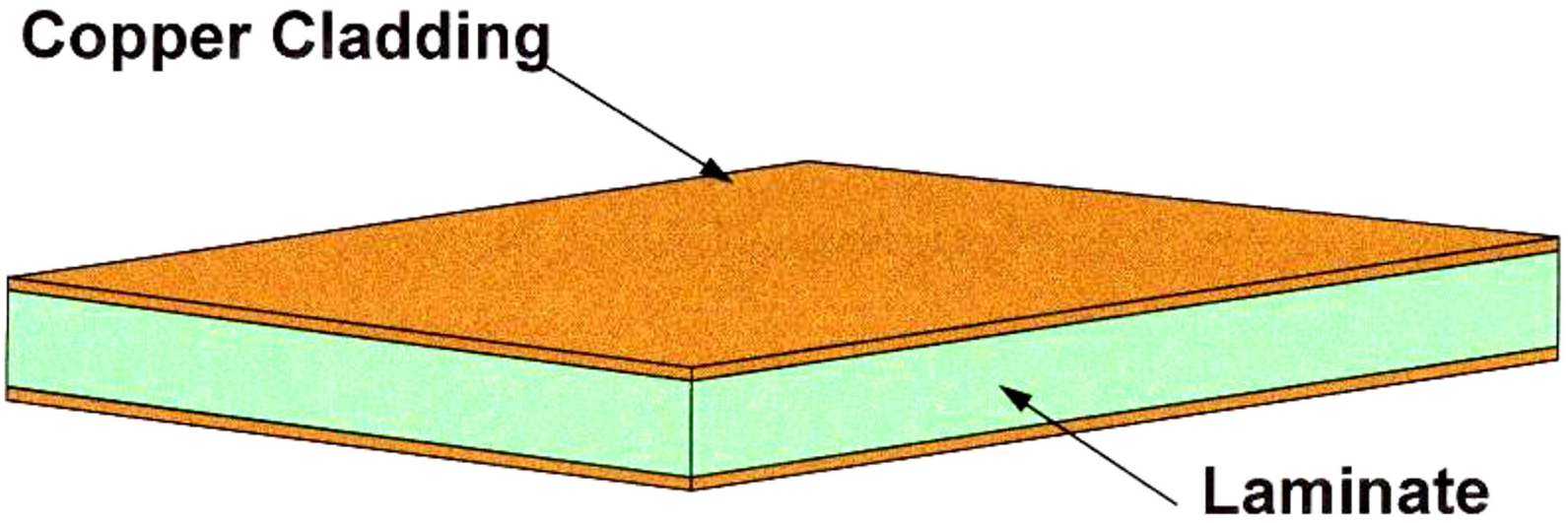
Factors in Selecting Circuit Board Materials

- Cost
- Electrical characteristics
  - Surface and volume resistivity and dielectric constant
- Mechanical properties
  - Flexural strength, modulus of elasticity, coefficient of thermal expansion (in plane and out of plane), glass transition temperature

Inner Layer Process Steps

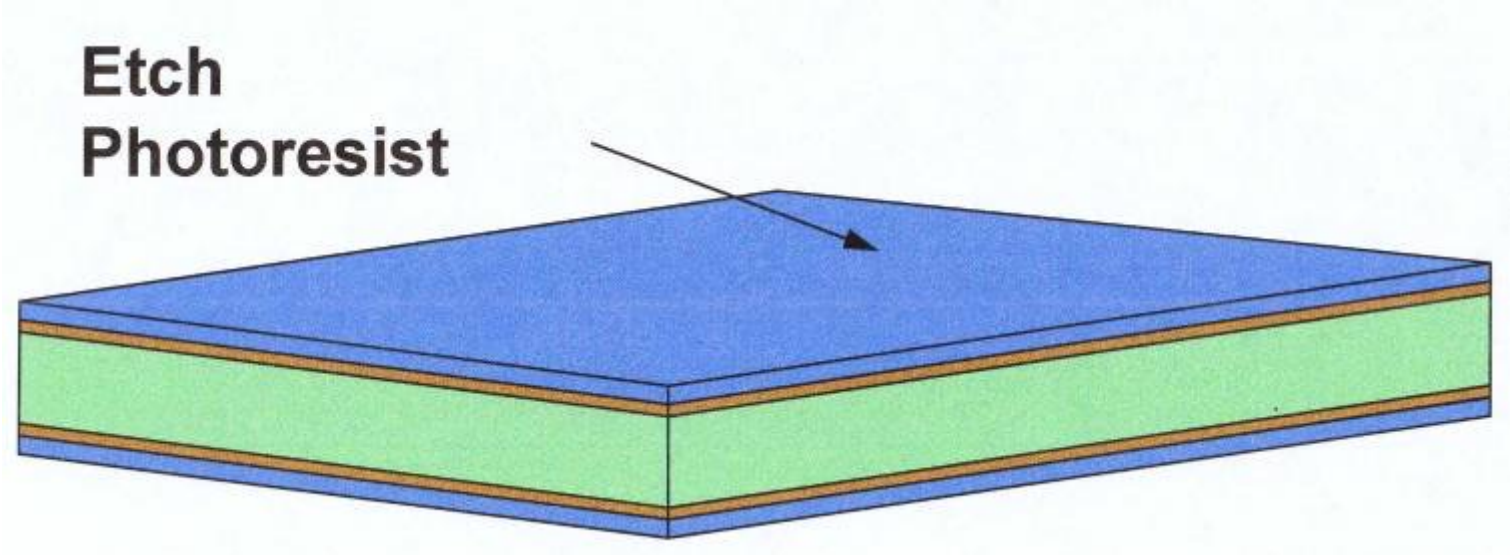


Laminate



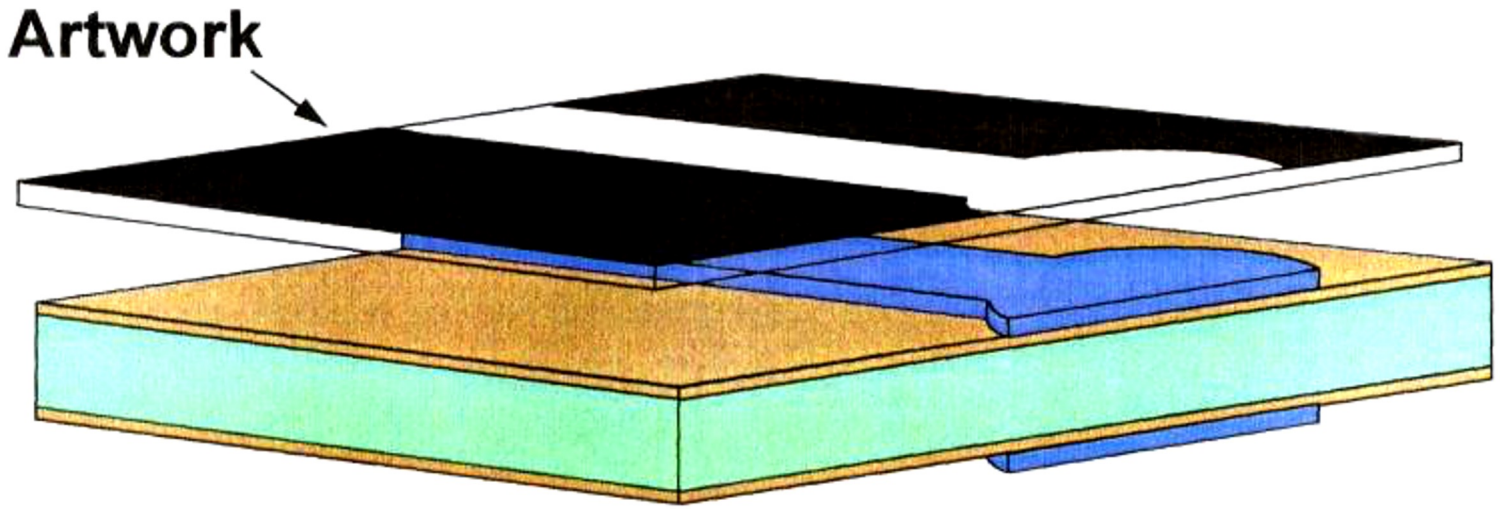
First, the proper laminate (core) is chosen. A core is made up of fully-cured epoxy resin ("C"-stage) sandwiched between two layers of copper cladding. The core must be the proper thickness, along with the required amount of copper cladding. The copper cladding will eventually become two inner layers, and the laminate will act as the dielectric spacing between these layers. The most common copper thickness for inner layers is one ounce of copper per square foot (typically 1.3 mils thick). Core thicknesses can run anywhere from 0.0015" to 0.070". The cores are either cut to size from larger sheets of material, or purchased to the specified panel size.

Coat Etch Resist



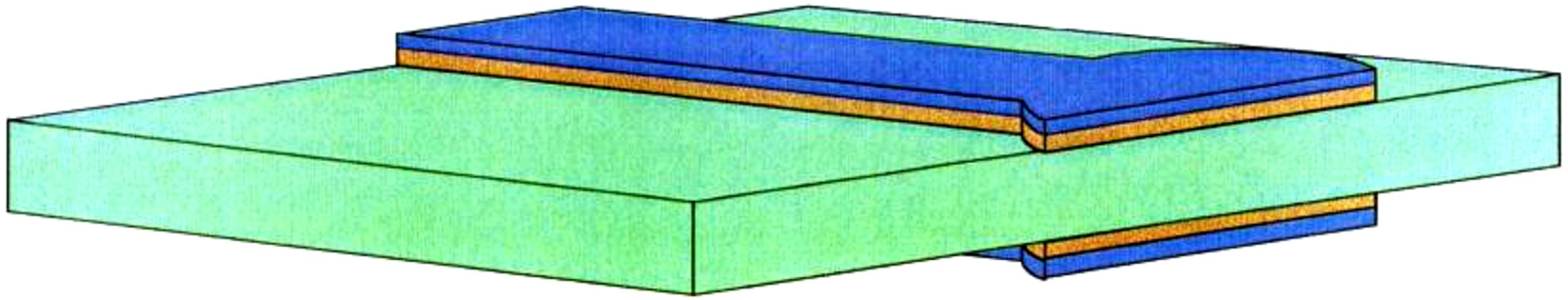
The core is chemically cleaned to remove any copper tarnish. It then passes through a cut sheet laminator where, through heat and pressure, a layer of dry film is placed on both sides of the core. This film will act as an etch resist later in the process, and will be removed after it has served its purpose.

Image and Develop



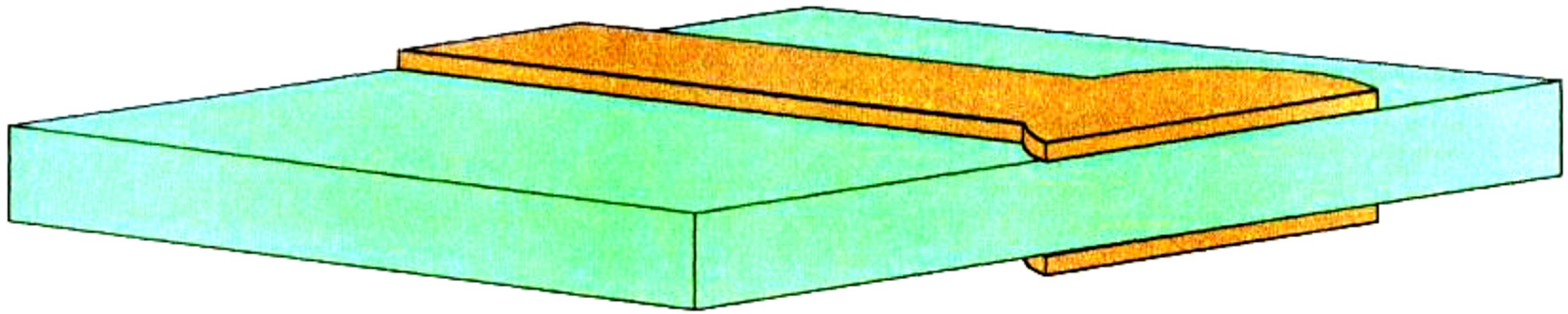
The resist-covered cores are placed into exposure frames where artwork is already in place. UV light is passed through silver halide artwork on both sides of the core simultaneously to expose the resist. This creates the circuit image in the dry film. The clear areas of the artwork through which light is allowed to shine on the film, are polymerized (hardened). Where light is blocked by artwork features, the film underneath stays soft. The soft, non-polymerized film is removed in the first section of the DES (Develop-Etch-Strip) line using a potassium carbonate solution, exposing only the unwanted copper for each layer.

Etch



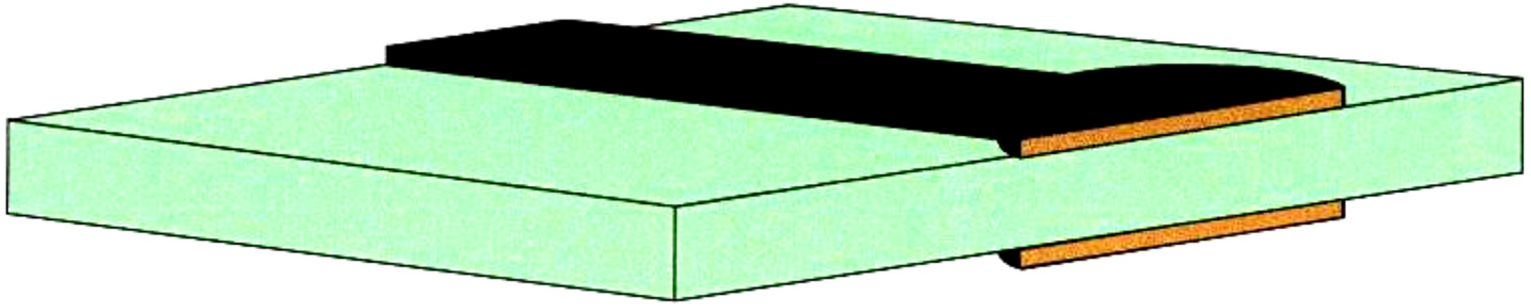
The core continues on through the DES line, passing through an ammoniacal etch, where the exposed, unwanted copper is attacked. The speed of the conveyor through etching is determined by the thickness of the copper being etched.

Strip Etch Resist



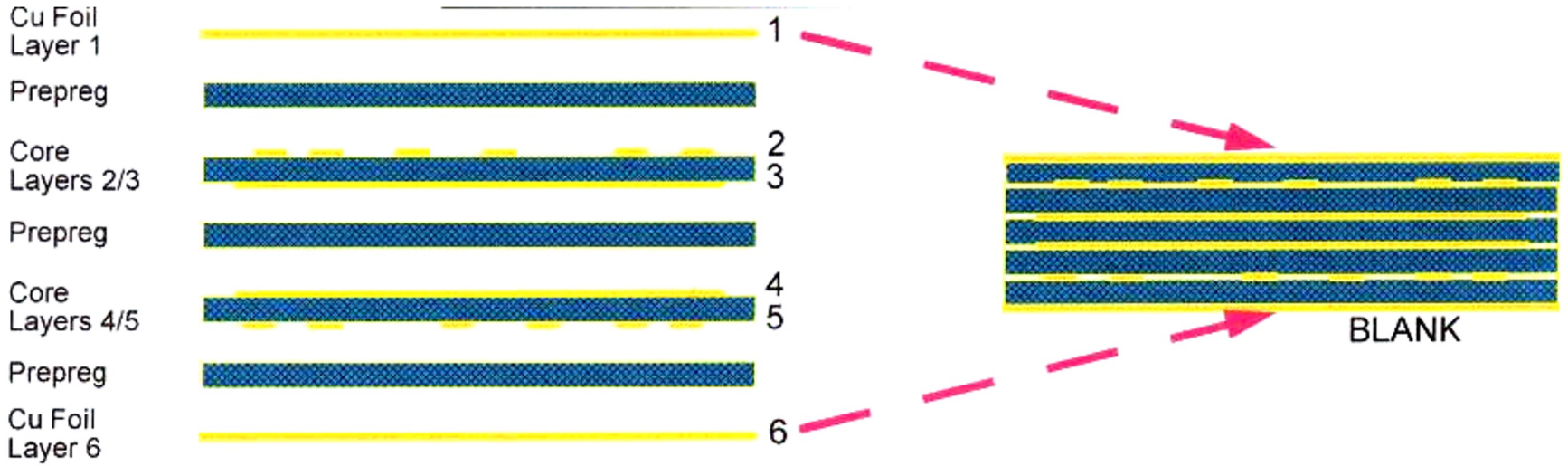
The dry film etch resist has completed its job. It is now removed in the final section of the DES line - the Stripper. Now a copper pattern for each layer can be seen. A Post-Etch Punch places a set of tooling slots in the core, by viewing targets placed precisely relative to the circuits and etched onto the core. These slots will be critical for proper registration of the cores used to construct the multilayer sandwich.

Black Oxide Coat



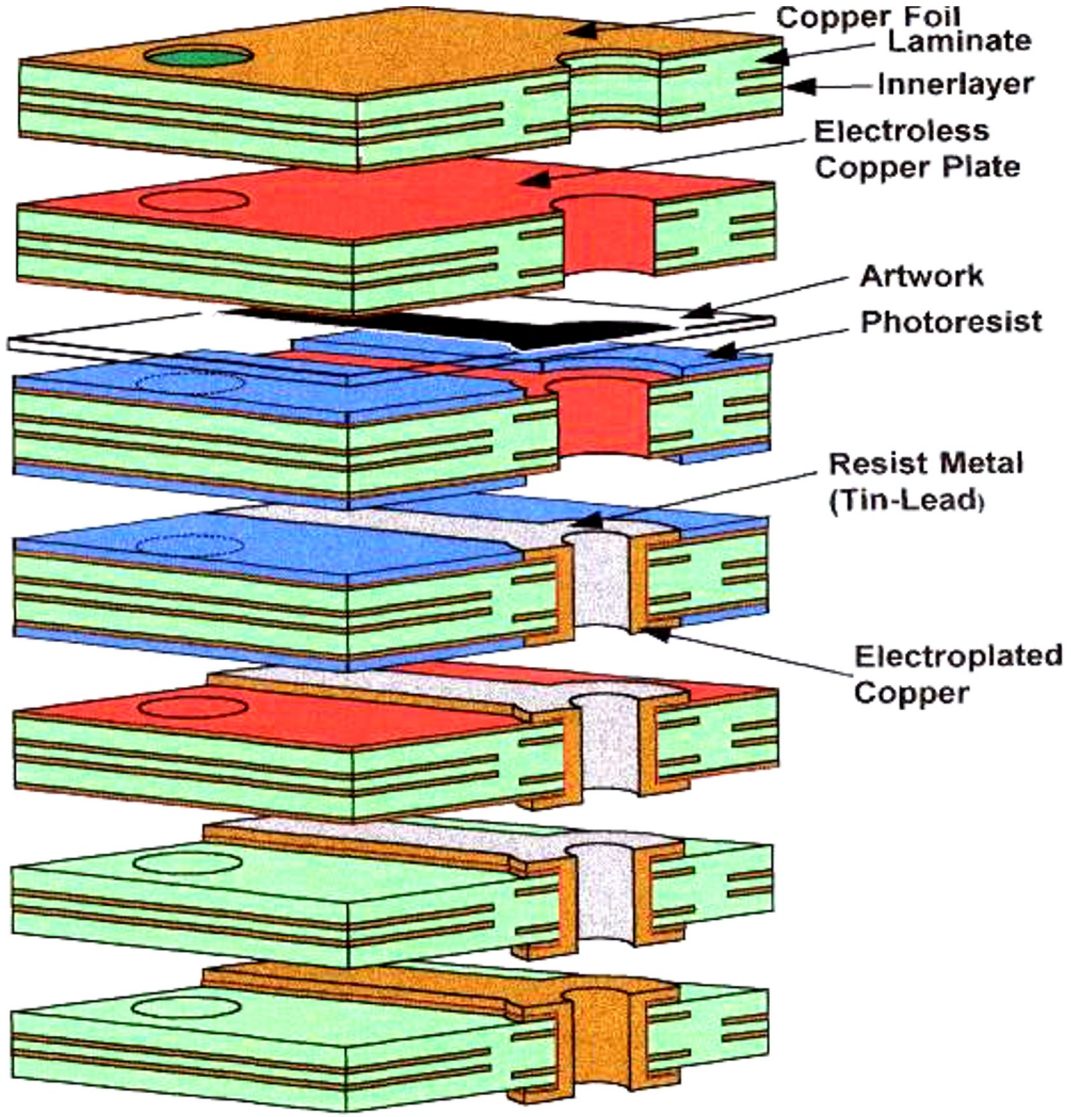
Prior to black oxide, the cores have undergone inspection using sophisticated AOI (Automated Optical Inspection) equipment. The inspected cores are then coated with an oxide in a programmed wet process line. The copper is changed to copper oxide, which has a crystal surface and will allow for better bonding when the multilayer is pressed together. The cores are then baked to remove any moisture.

KIT/ Laminate/ FAB



Once all the cores that go into the finished board are ready, they get released to kitting, where all the materials are put together to make a "blank". Copper foil will be placed on top and bottom, with the cores properly layered on the inside between sheets of prepreg ("B"-stage, fiberglass cloth impregnated with partially cured resin). This prepreg will act as the "glue" that holds the multilayer blank together, and will form the necessary dielectric between adjacent cores. All materials are placed over pins on registration plates to insure that the layers are perfectly lined up. Several boards laid up together separated by aluminum foil become a "book" with a top registration plate placed over the book. The books are placed in vacuum presses, where air is removed, and pressed together under heat and pressure. After pressing, pins are removed, "flash" is trimmed, and the blanks are separated, ready for drilling.

Outer Layer Process



DRILL & DEBURR

DESMEAR & COPPER DEPOSITION

COAT , IMAGE & DEVELOP PHOTORESIST

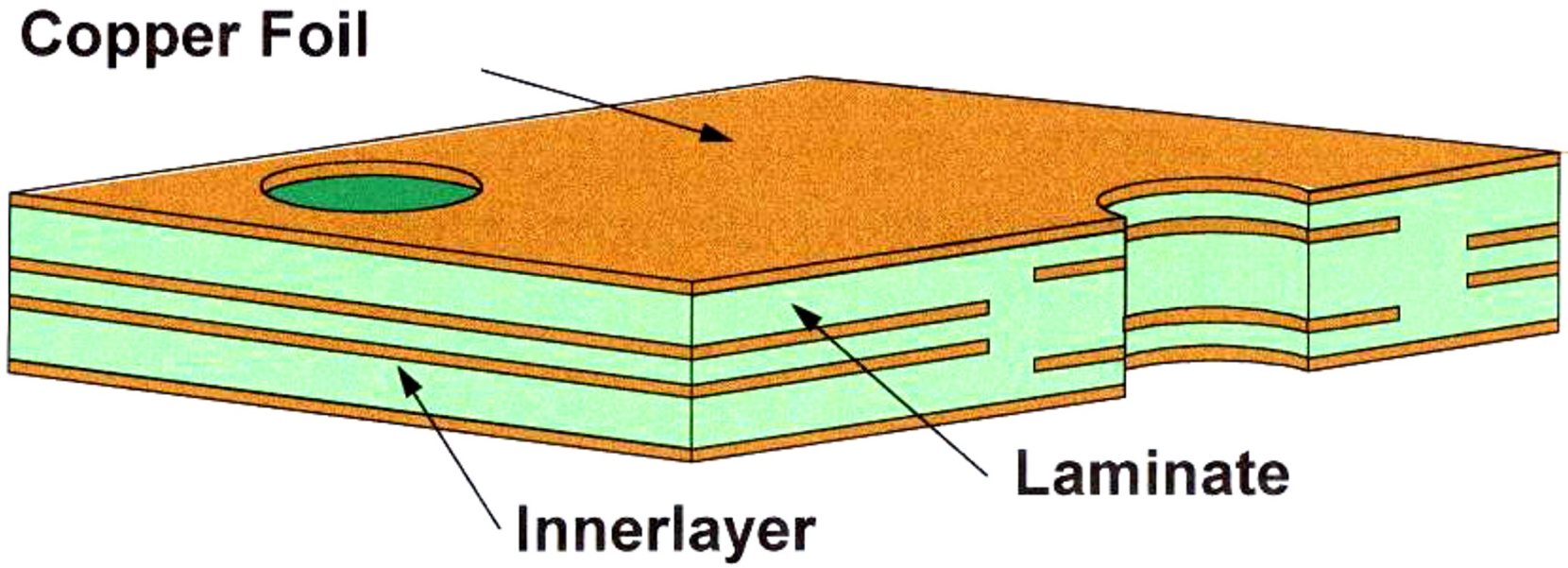
COPPER & SOLDER PLATE

STRIP PHOTORESIST

ETCH

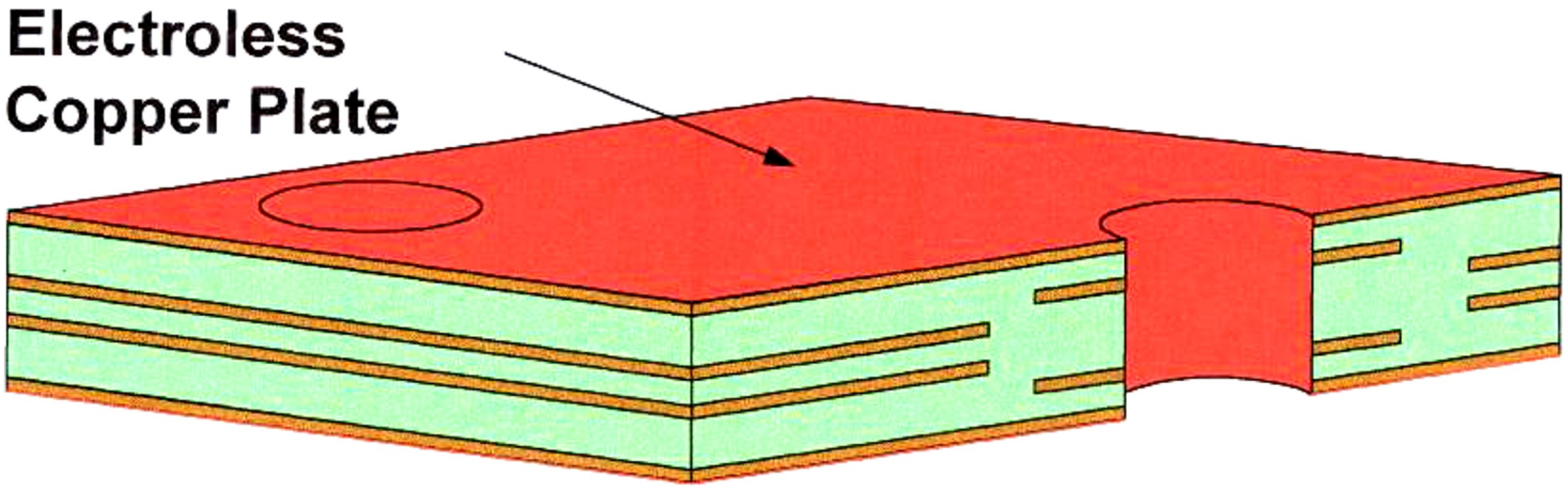
SOLDER STRIP

Drill and Deburr



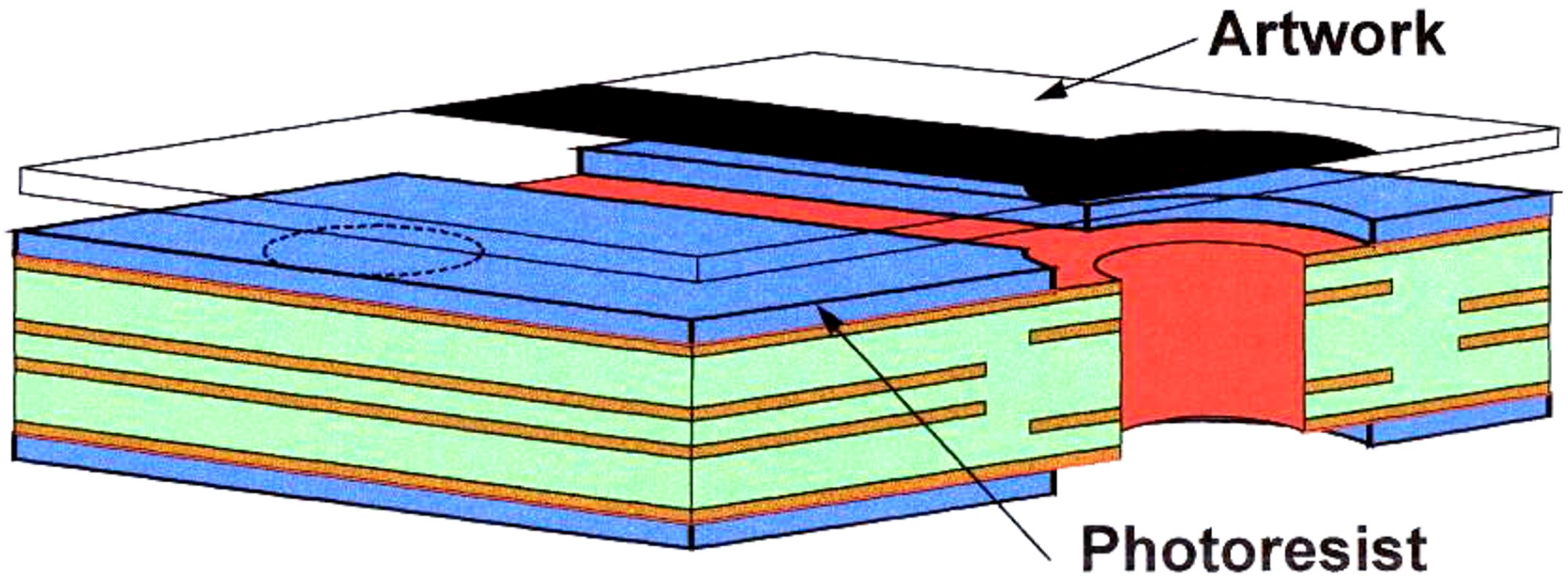
The blanks are pinned in stacks on tooling plates and drilled on multi-spindled drill machines. The computerized drill program determines where the holes are placed, and automatically changes drill sizes when each drill size has completed its path. Holes can be as small as .008” or as large as .250”. X-ray and visual inspection are used to verify that the holes are fully drilled and properly aligned to the inner layer pads. Deburring equipment removes any burrs that may have formed.

Desmear and Copper Deposition



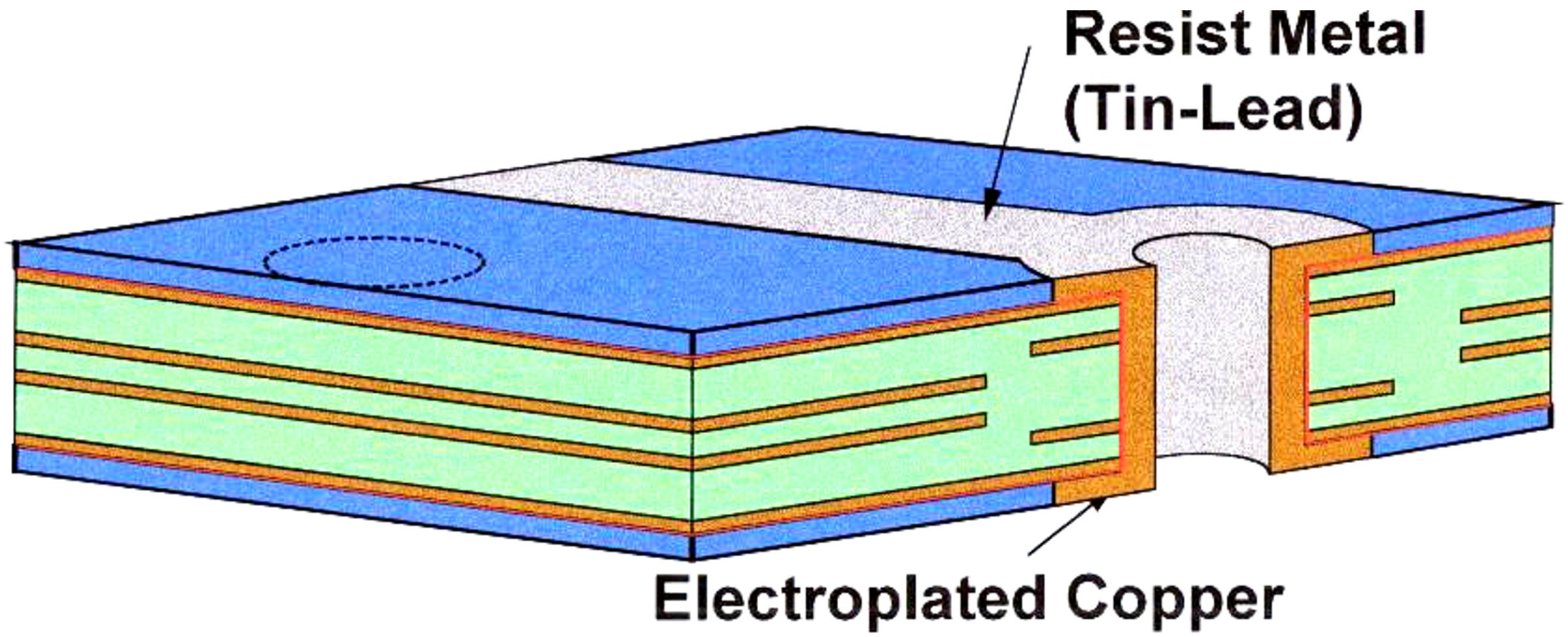
The holes undergo a process to remove any resin smear covering innerlayer connects and to slightly roughen the hole walls to allow for subsequent plating. The deposition process is an electroless plating process in which a very thin layer (80 to 100 millionths thick) of copper is deposited onto the surfaces of the hole wall (and incidentally on the copper foil surface). This will allow for subsequent electroplating of the holes.

Coat, Image and Develop Dry Film



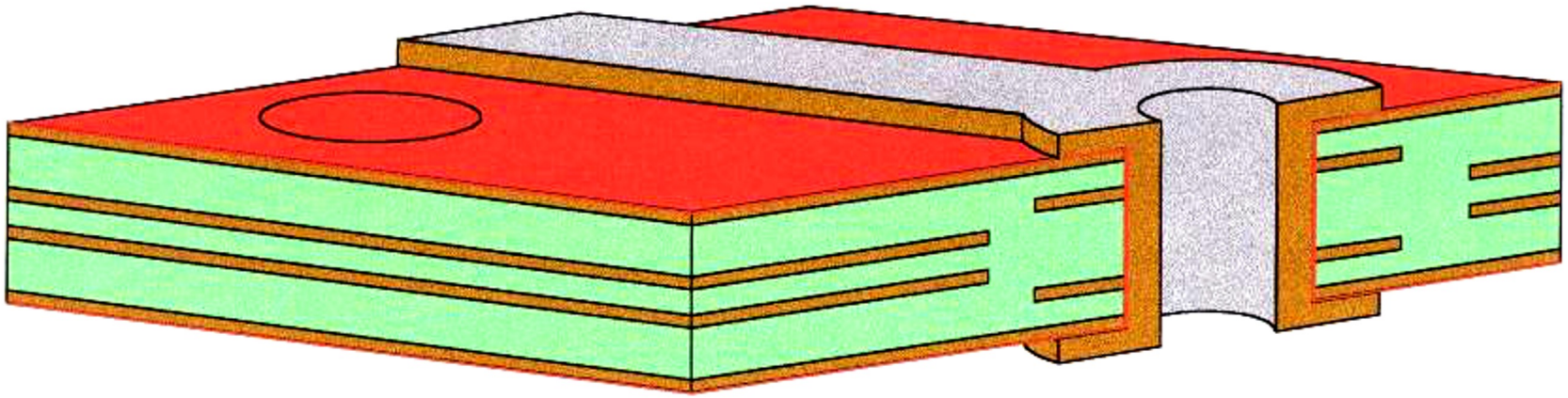
Dry film resist is applied to both sides of the panel under heat and pressure, similar to the cores in inner layers. The circuitry pattern of the artwork is aligned to the drilled holes and the panel is exposed to UV light from both sides. Where light is allowed to shine through, the film is polymerized. In the case of outer layers, a reverse artwork image is used, since the dry film is acting as a plating resist as opposed to the dry film being an etch resist in inner layer. The panels are developed, with the unexposed resist being washed away.

Copper and Solder Plate



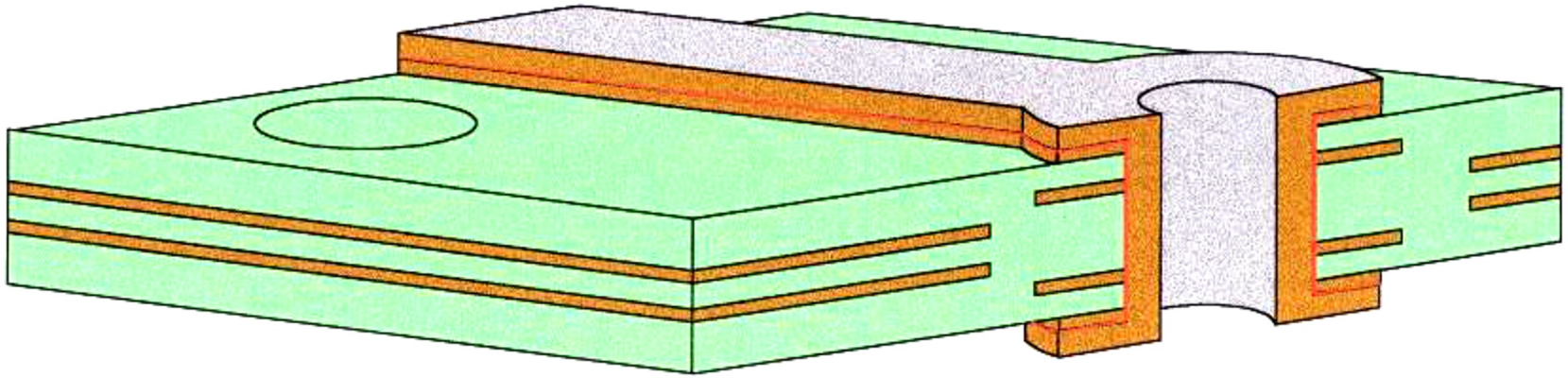
All copper exposed will be plated, with .001” nominal of copper in the hole barrels, followed by either tin or tin/lead, which will act as the etch resist further on. The panels are carried on racks by a hoist which is computer-controlled to repeat the same cycle time after time. The hoist places the racks of panels into the solution and rinse tanks for set time periods, so that the chemical solutions can deposit the metals to the traces, pads, and hole barrels electrolytically.

Strip Photoresist



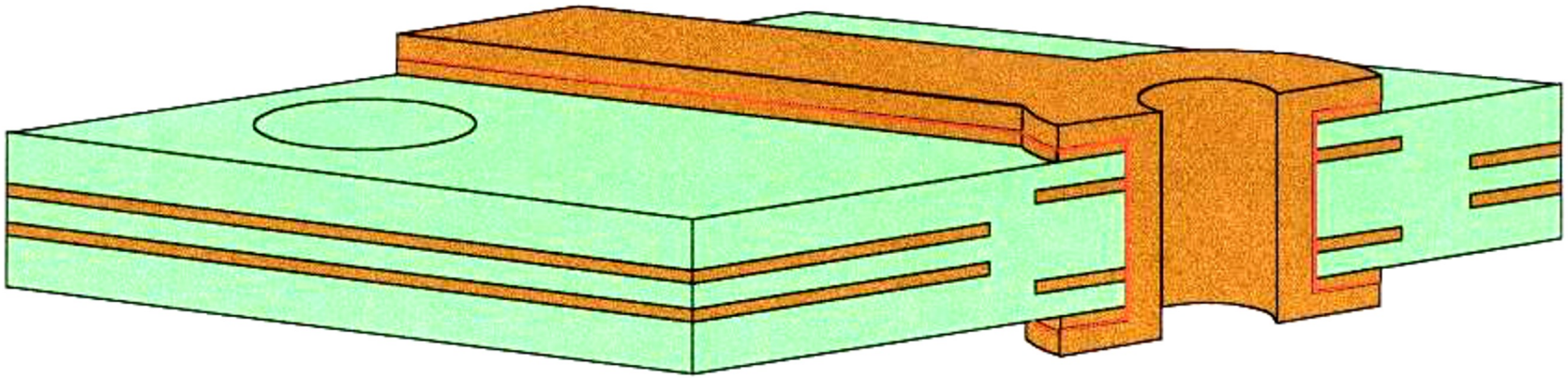
The dry film resist, which acted as a plating resist, is now stripped away with an alkaline solution in the Strip-Etch-Strip line. This exposed the unplated copper foil underneath on the surface. Any holes that were “tented” (covered) with dry film will have copper barrels from the electroless copper process.

Etch



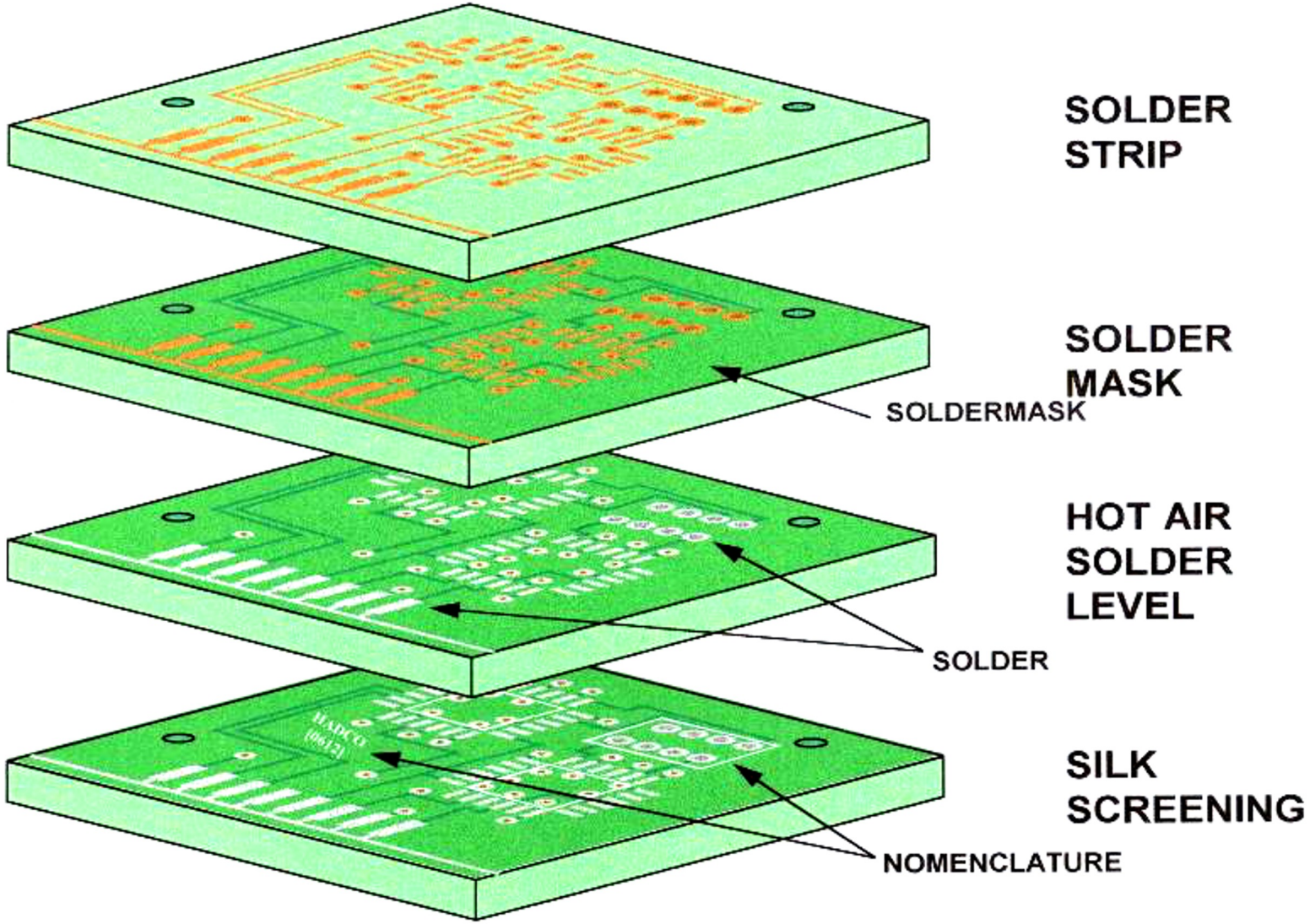
The copper foil is now etched away, using an ammoniacal solution. It is here where “a circuit is born,” since the board is electrically functional at this point. There are still, however, several more steps.

Solder Strip

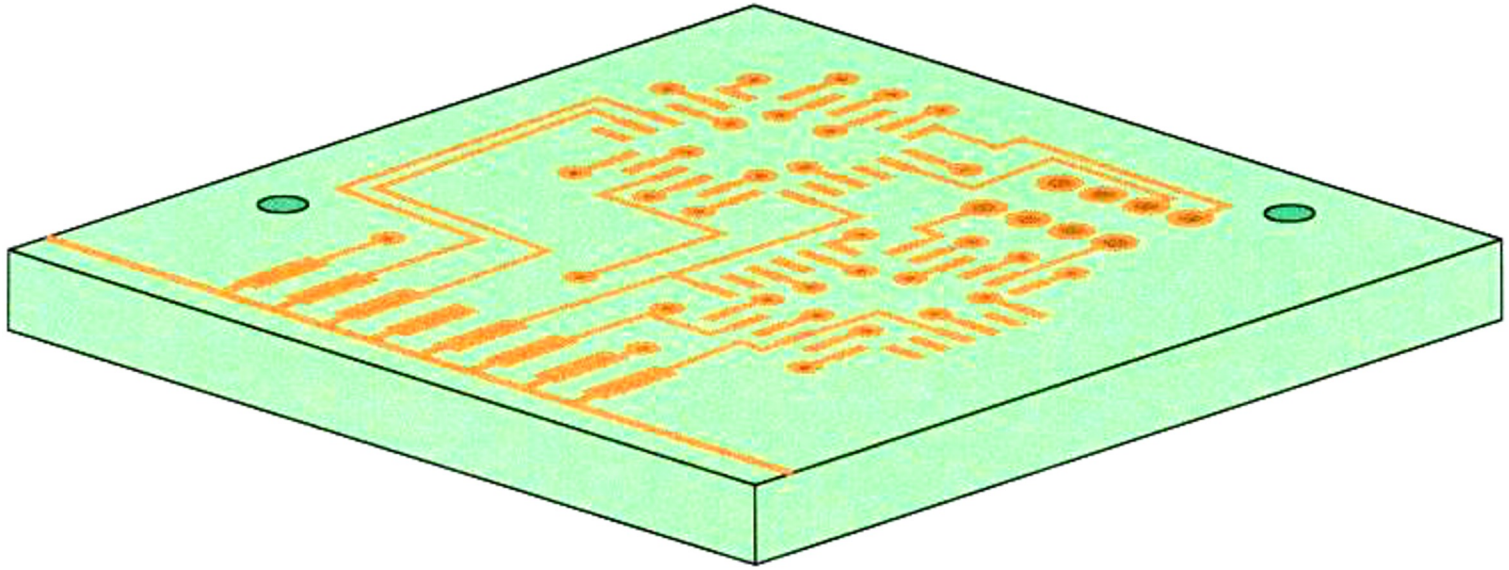


The tin or tin/lead that was protecting the traces, pads, and hole barrels from being etched is chemically stripped away at the end of the S/E/S line, leaving bare copper circuitry.

Outer Layer Process Steps

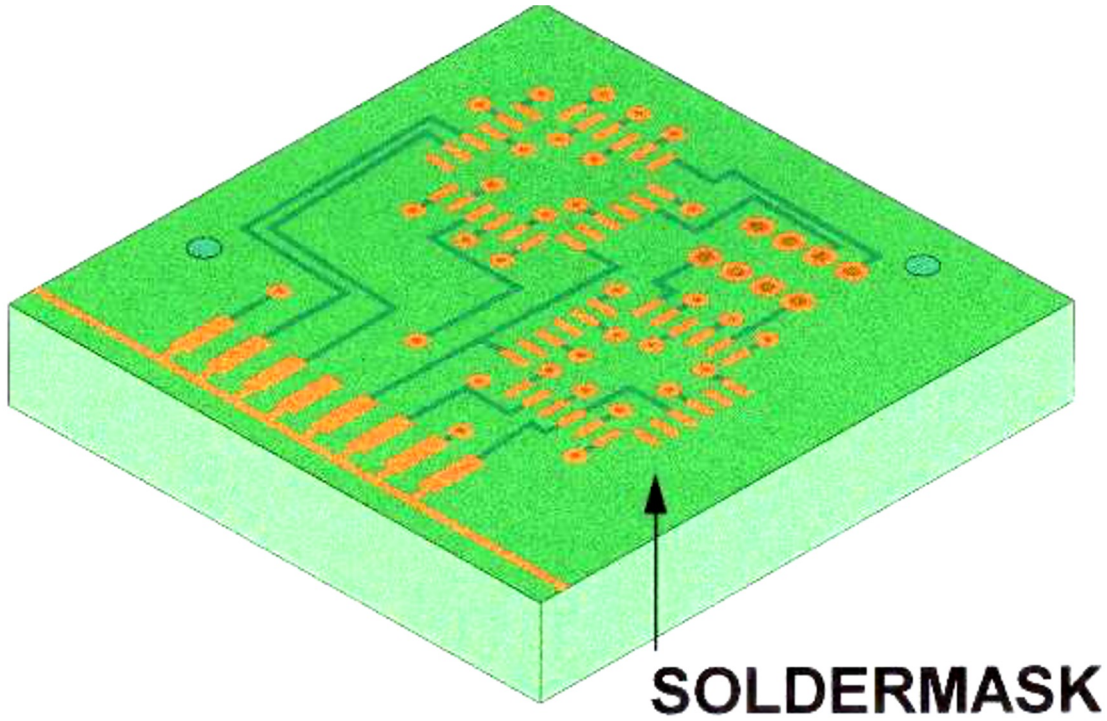


Solder Strip



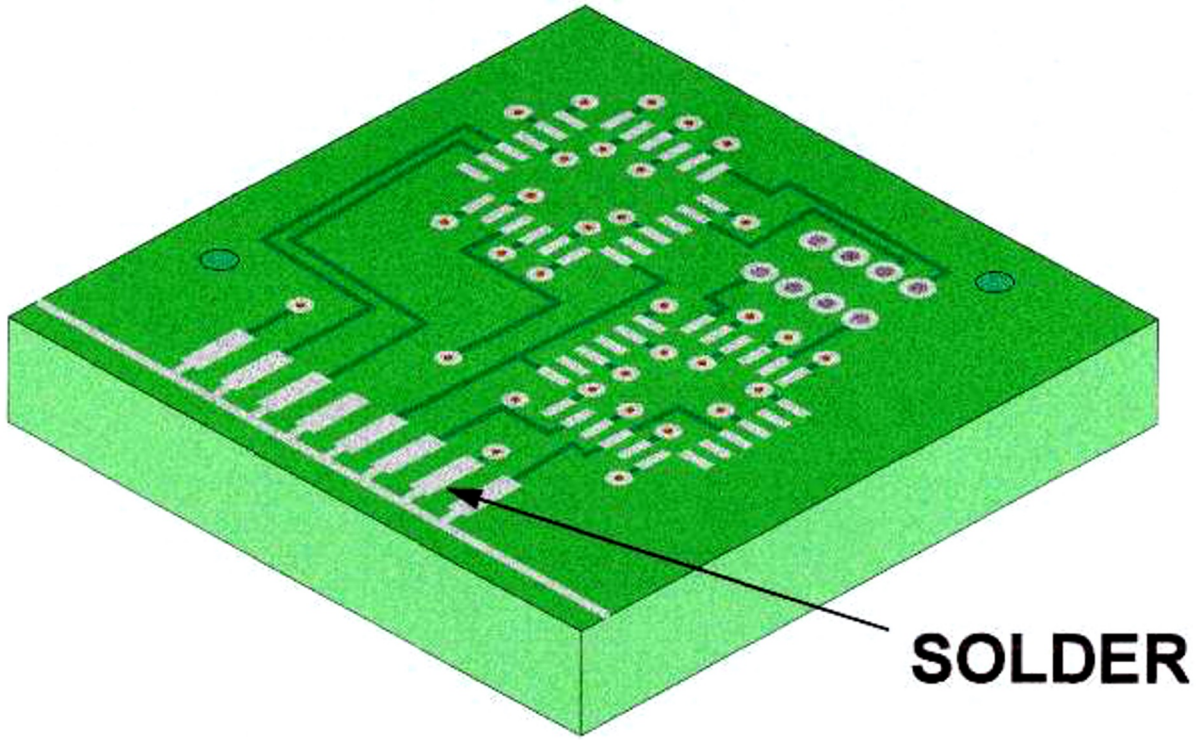
This details of this process, already discussed, involves the removal of the tin or tin/lead protecting the traces, pads, and hole barrels from being etched.

Soldermask



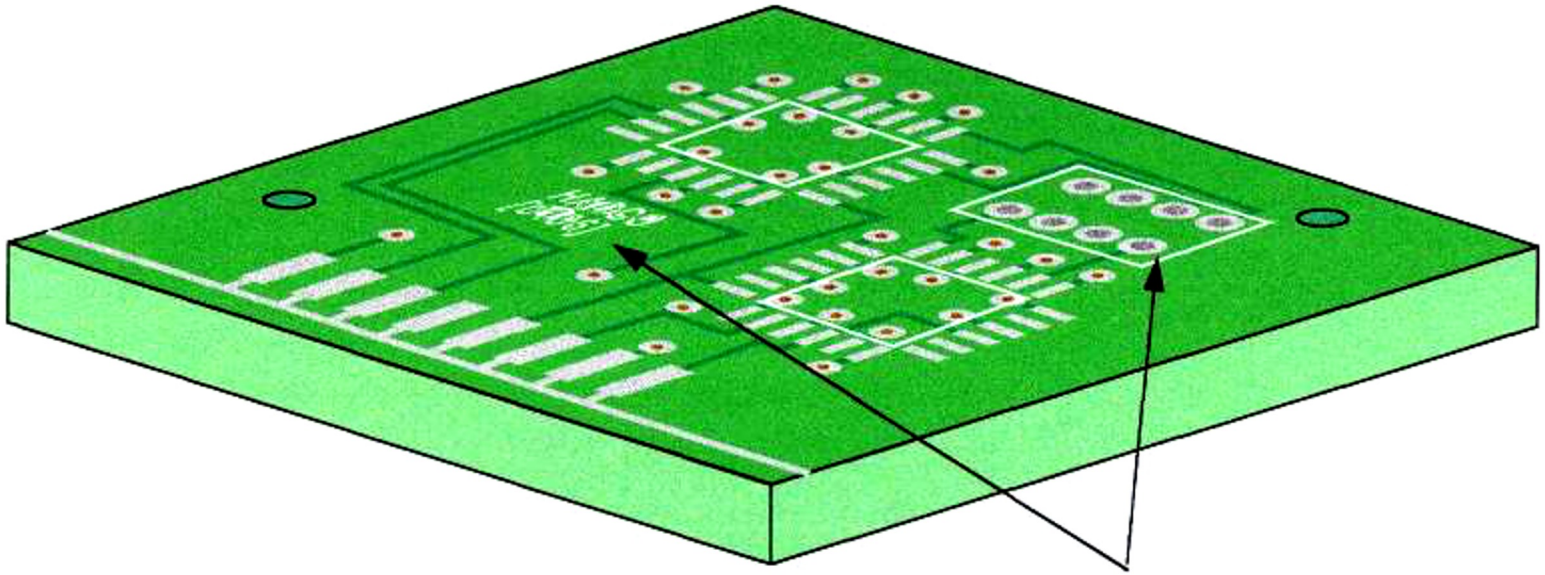
Soldermask is applied to protect and insulate the circuitry. The panels are cleaned, preheated, and coated with soldermask. Several stages of drying are performed to solidify the mask. The mask now acts much like the dry film in inner and outer layers. Artwork is exposed onto both sides of the panel, and the soft mask is removed where it is not wanted (pads). The panel is then baked for final curing.

Hot Air Solder Level



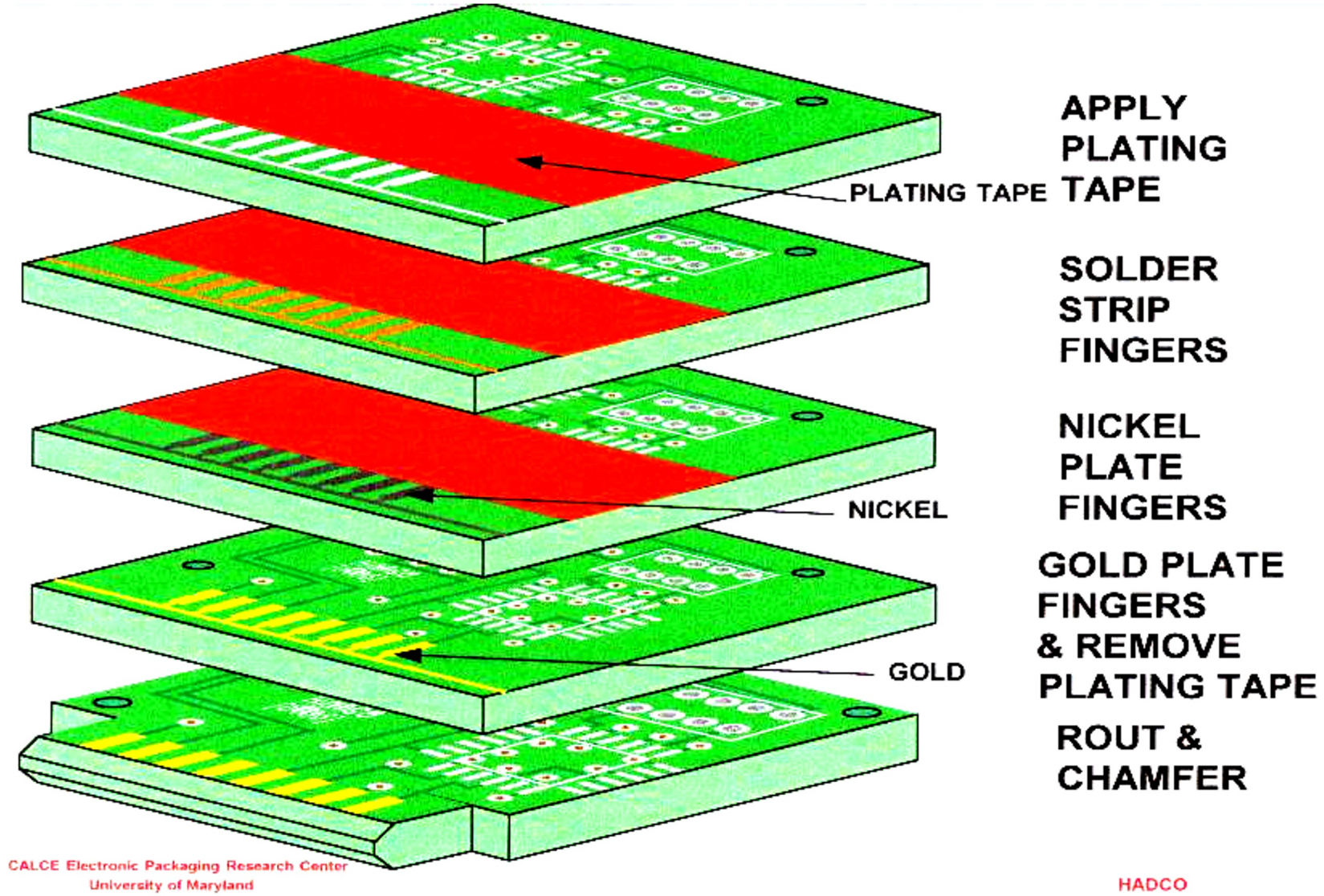
Hot Air Solder Level (HASL) involves the application of solder to selected board features, wherever copper was left exposed after soldermasking. The copper is cleaned and microetched in a preclean unit, preheated, and fluxed to promote solder wetting. The panel is horizontally immersed in the solder pot, and then excess solder is blown off with air knives. A cool down and cleaning stage follows.

Silk Screen

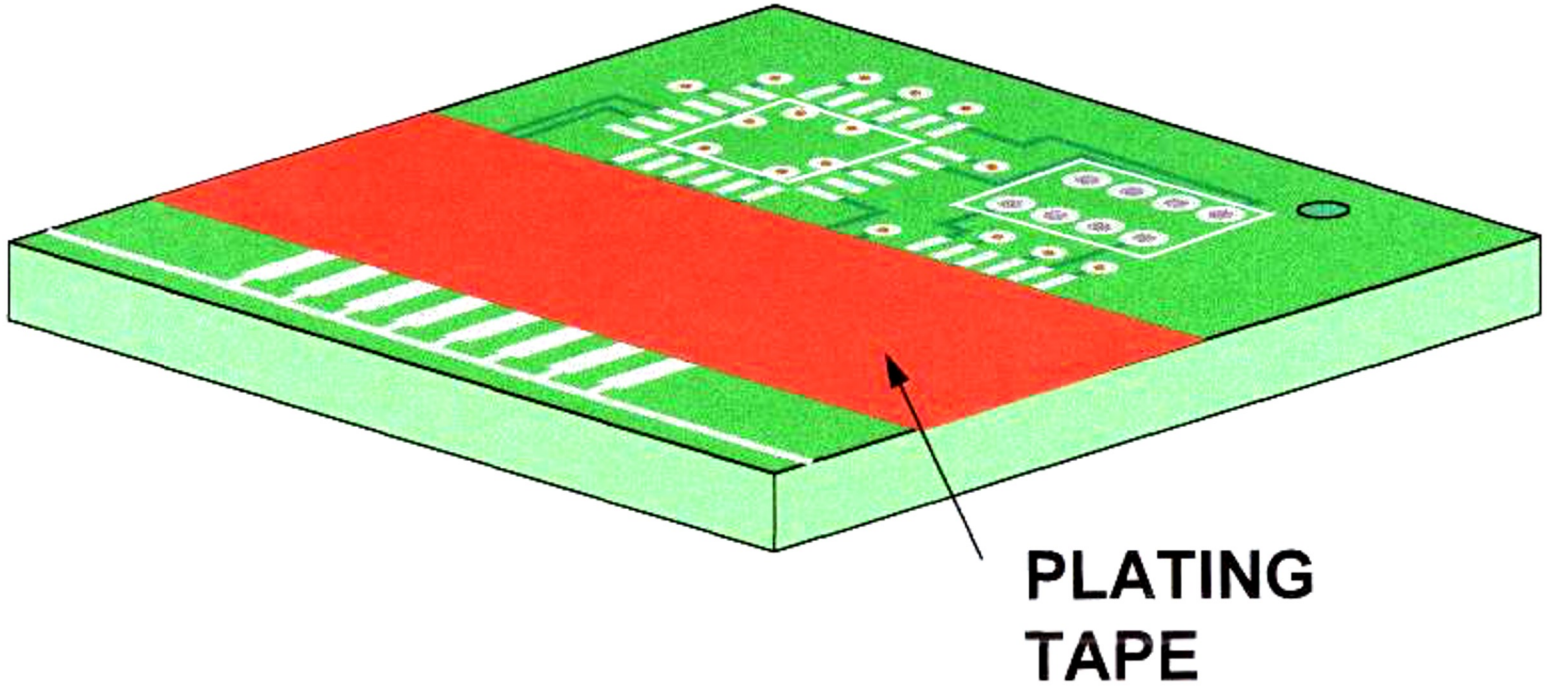


Information needed by the customer for assembly or troubleshooting is screen-printed onto the board. An epoxy ink is applied to the stenciled screen. Using a squeegee, the ink is forced through a screen fabric with a stencil image. The ink is then baked in order to cure the resin. Once baked, the ink is not easily removed.

Outer Layer Process Steps

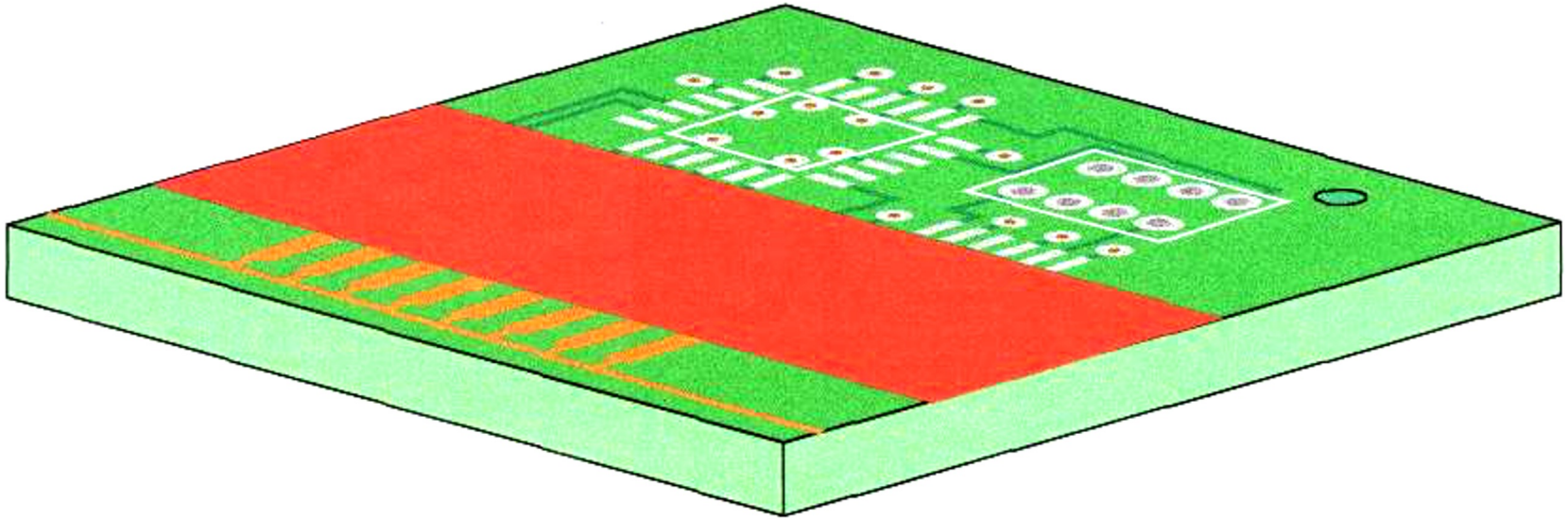


Apply Plating Tape



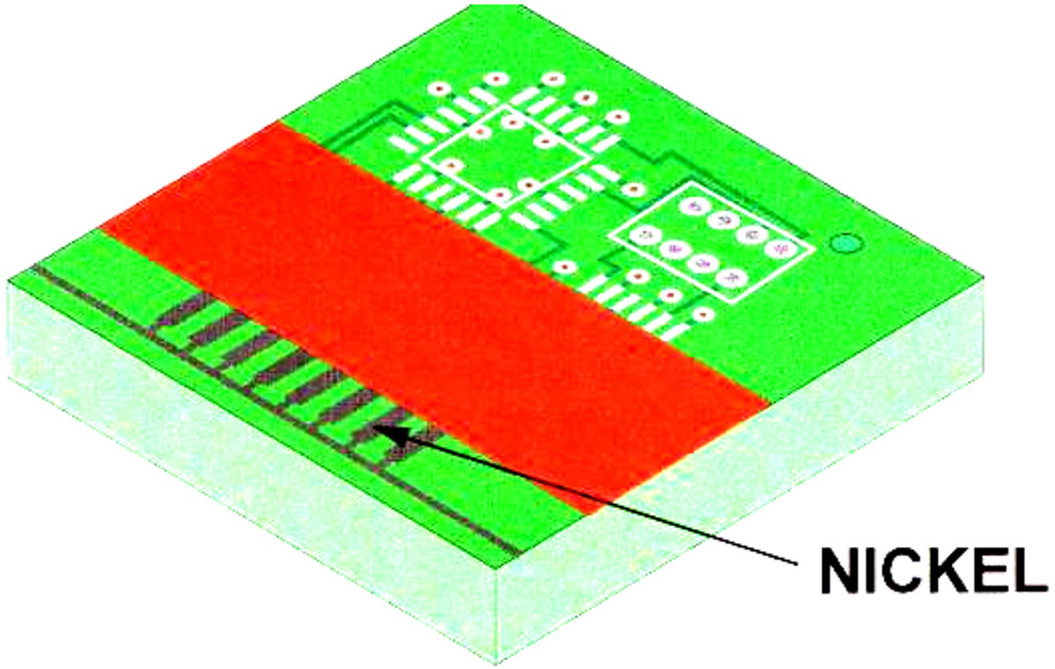
This nickel/gold plating process is used for edge connectors and critical contacts. A pressure tape is applied below the finger area in order to permit solder strip and nickel/gold plating in the finger area only.

Solder Strip Fingers



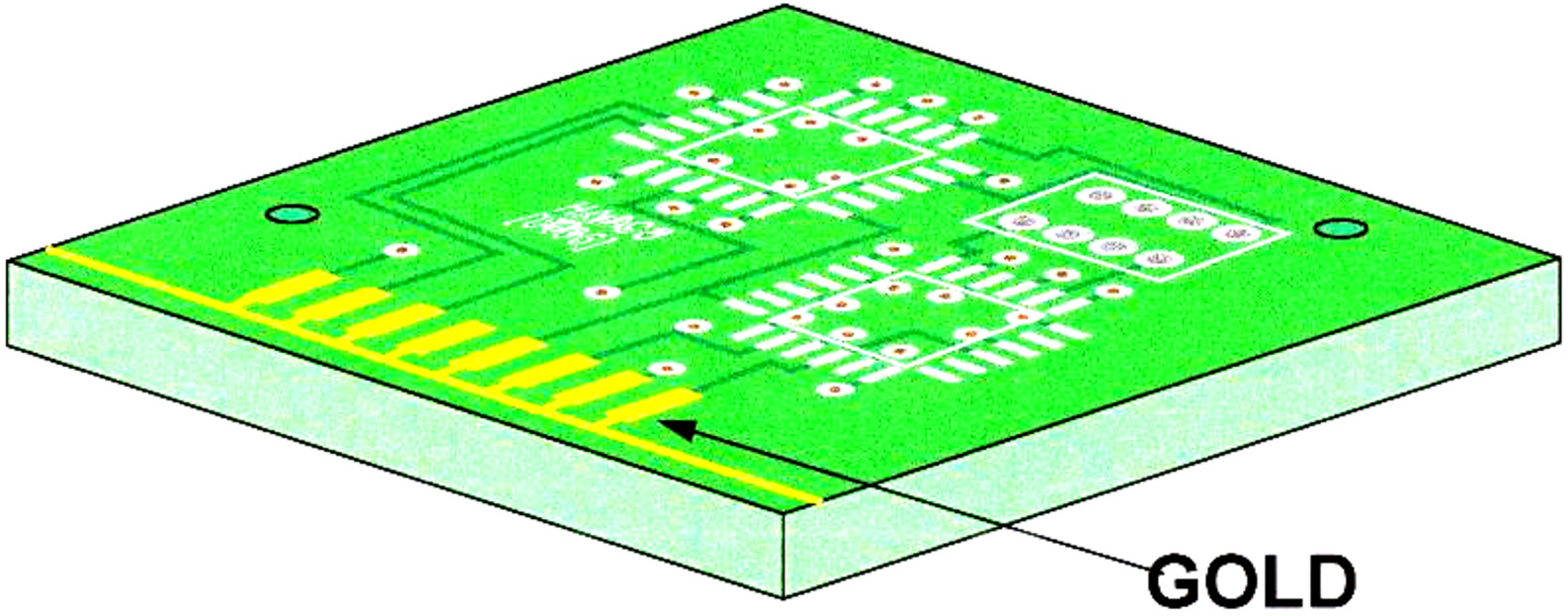
The boards travel within a conveyorized belt through shallow solution tanks. Solder, which had been leveled onto the connector fingers, is chemically stripped off.

Nickel Plate Fingers



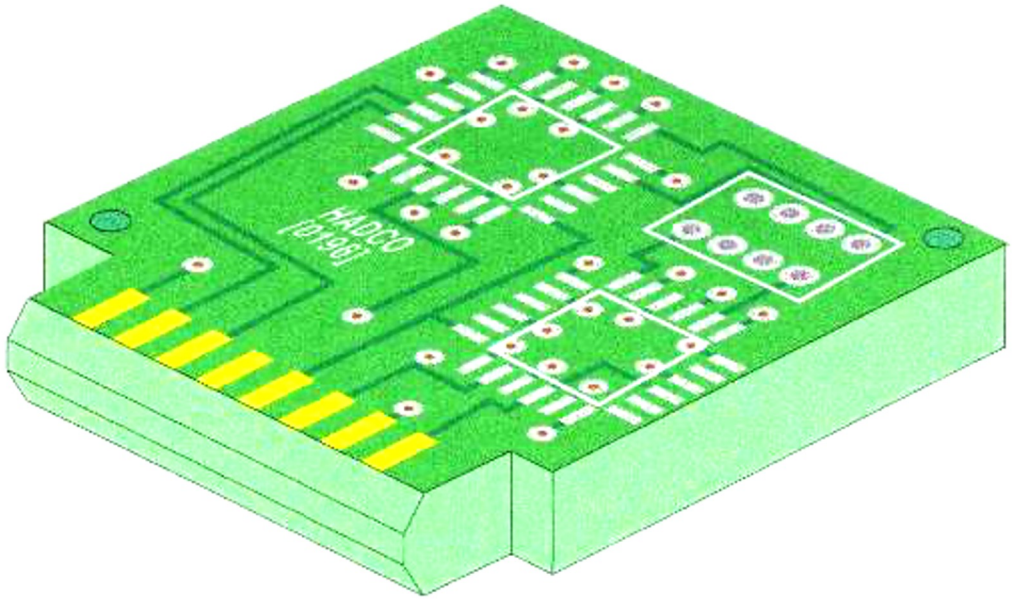
The nickel/gold plating process is electrolytic. As the board edges pass through plating solutions, brushes have made contact with blocks attached to a buss bar feeding to the fingers. This buss bar provides electrical continuity to the fingers and allows for plating. First, a layer of nickel about 100 - 150 microinches thick is plated onto the copper. This nickel increases wear-resistance. It also serves as a barrier to copper migration into the gold.

Gold Plating Fingers and Plating Tape Removal



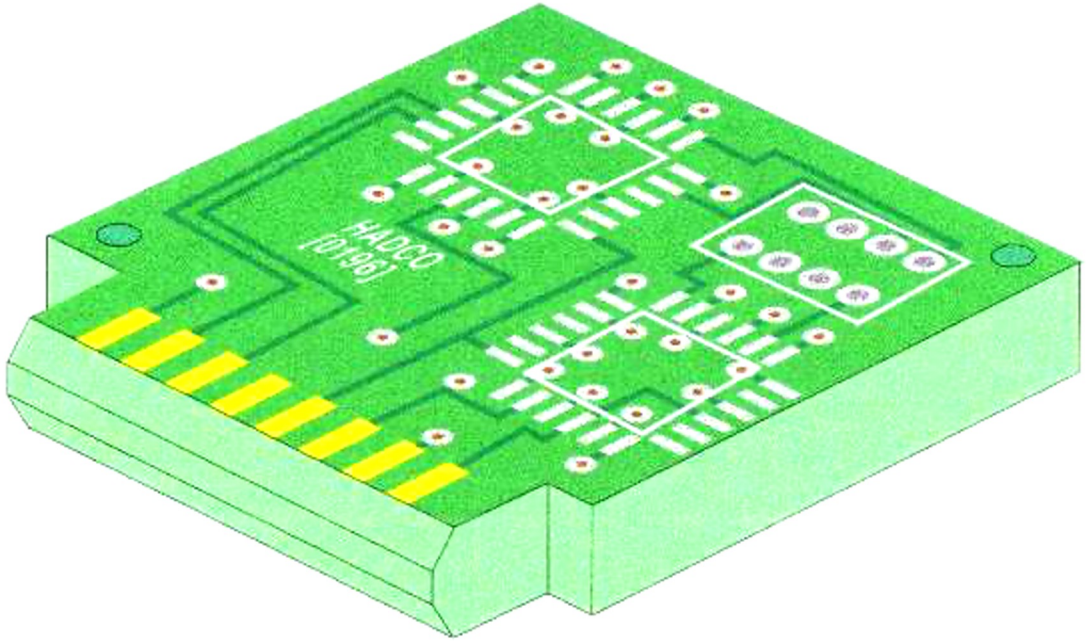
Gold, usually from 30 to 50 micro-inches thick, is plated directly over the nickel. Gold is used on the connector fingers because it is highly conductive and resists tarnishing. The plating tape is then pulled from the board, and the board is degummed.

Rout and Chamfer



Here the board is depanelized. The rout process is similar to the drill process, with the panels being stacked and pinned onto the tooling plates of a multiple spindle router. Utilizing a numerically controlled computer program, specialized carbide router bits are used to machine the edges, slots, and any required internal cutouts. The boards are removed and dimensionally verified to blueprint and shop traveler provided with the job. A bevel, or chamfer, is placed along the finger edge of the board, to remove the buss bar and allow for easier insertion of the card. Some boards with straight edges perpendicular to one another are scored, or V-grooved. The boards undergo a final clean of warm water and high-pressure rinse.

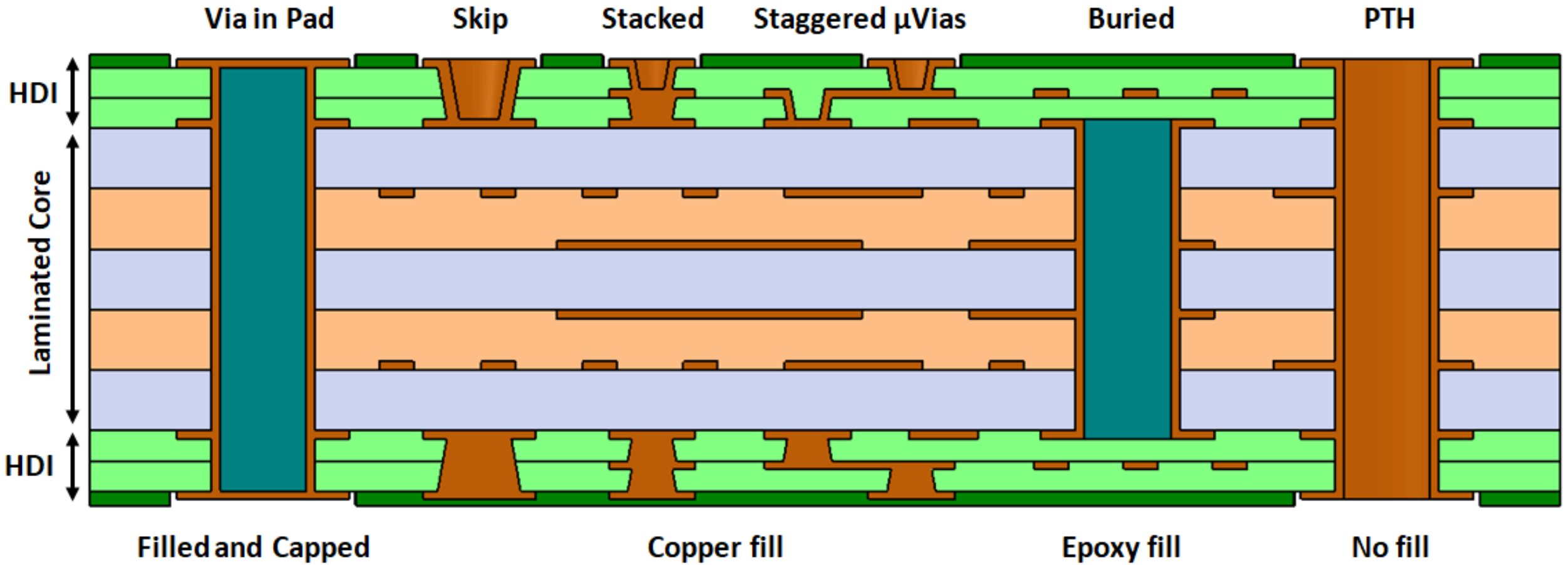
Electrical Testing, Final Inspection and Shipping



The boards undergo 100% electrical test on sophisticated simultaneous testers, to parameters set by the customer. This equipment runs from a downloaded program developed from net list or Gerber data. Final inspection looks for cosmetic flaws and performs dimensional checks. The shipping department then packages the boards for shipment to the customer.

Finished PCB – Via Types[1]

Vias are used to create the vertical, or layer-to-layer connections in a printed circuit board.

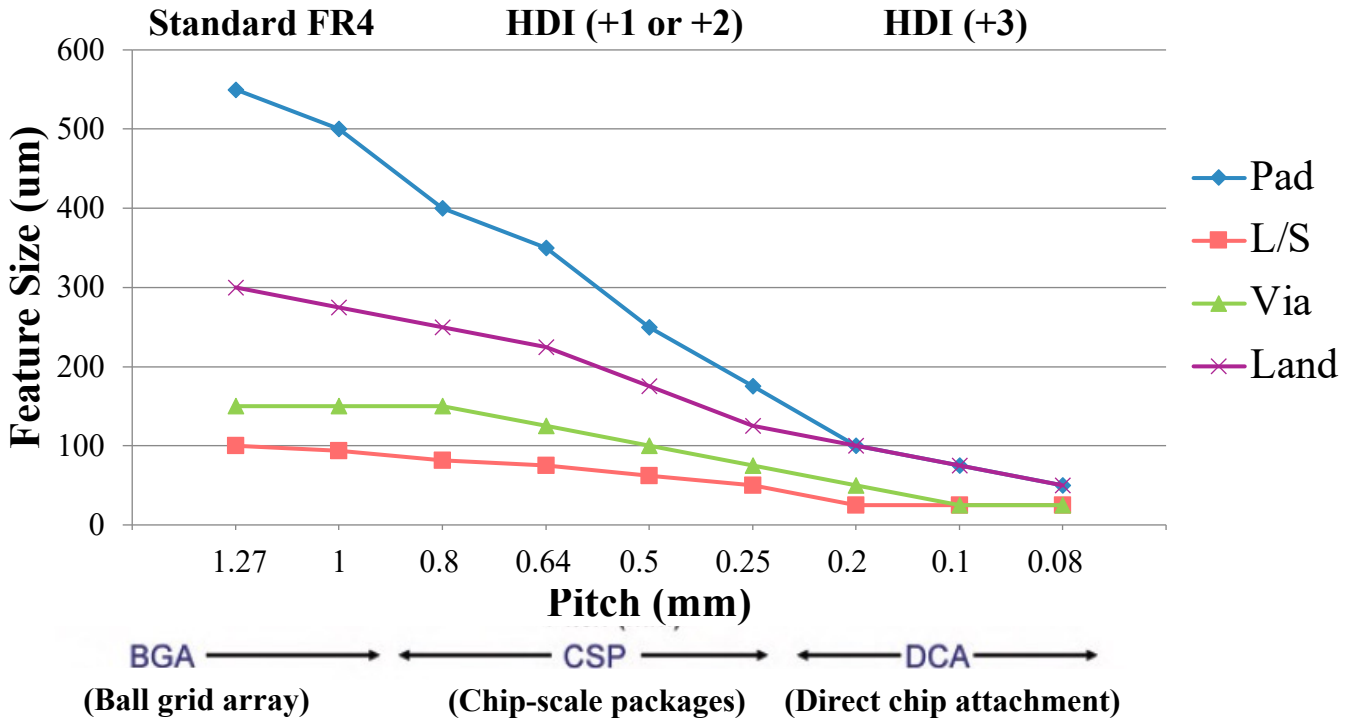


1 – An In-Depth Guide to PCB Vias and PCB Design, Available at: https://www.epiccolo.com/articles/pcb-vias-guide, accessed July 22, 2022

Microvia Assurance Methodology

Background

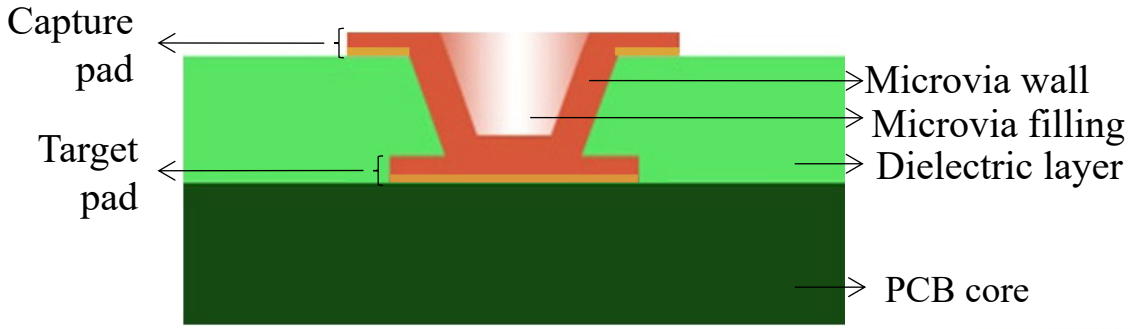
- The continuous increase in component performance and lead density and reduction in package sizes, has driven the need for high density µvias (or high-density interconnects HDIs).



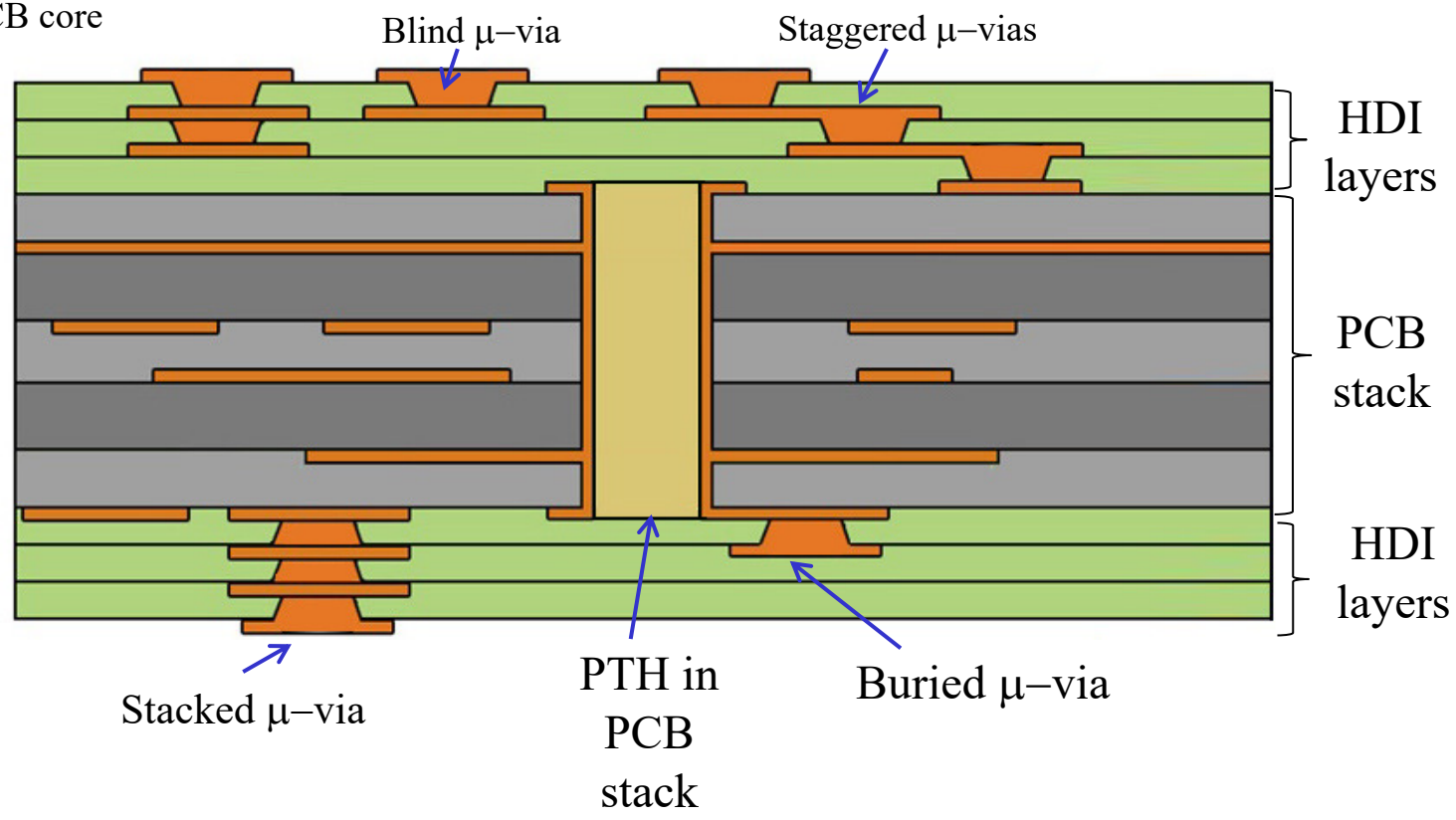
IC packaging feature roadmap with via size, via-pad size, lines and spaces (L/S), and SMT land size [1]

[1] Happy Holden et al., The HDI Handbook, 1st Edition. Available from: http://www.hdihandbook.com/

Illustration of Microvia and HDI Board



Microvias are blind or buried vias that are equal to or less than 150 µm in diameter and have a target pad equal to or less than 350 µm [1,2].



1. *IPC/JPCA-2315, "Design Guide for High Density Interconnects (HDI) and Microvias," June 2000*
2. *IPC-2226, "Sectional Design Standard for High Density Interconnect (HDI) Printed Boards," April 2003*

Assurance Requirements for Microvia and HDI Boards

For microvias, GSFC uses IPC-6012 requirements.

- Microvia plating integrity and interconnection integrity are inspected after microsection at a magnification of 200X ± 5%. Referee examinations are accomplished at a magnification of 400 - 500X.
- Inspections are dependent on grinding and polishing accuracy of the microsection, IPC-6012 specifies this accuracy shall be such that the viewing area of the microvia is within 10% of the drilled hole diameter.

- IPC-2221 specifies the copper plating thicknesses for microvias.

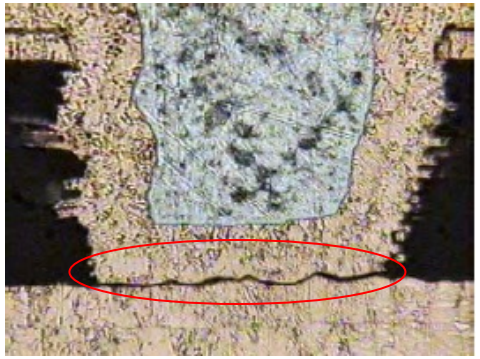
Table 4-4 Surface and Hole Copper Plating Minimum Requirements for Microvias (Blind and Buried)[1]

Copper - average[2]	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
Thin areas	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
Wrap[3]	AABUS	5 µm [197 µin]	6 µm [236 µin]

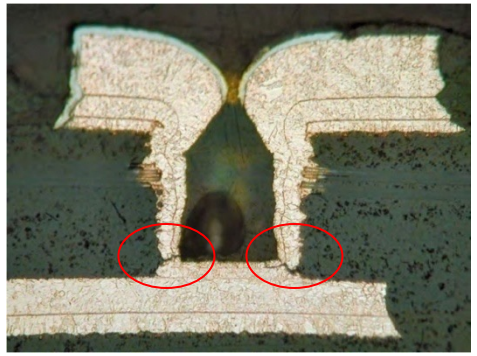
Note 1. See 1.5.1 for definition of microvia.
Note 2. Copper plating thickness shall be continuous and wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.
Note 3. Wrap copper plating for filled microvias shall be in accordance with IPC-6012.

Known µvia Failures in the Literature

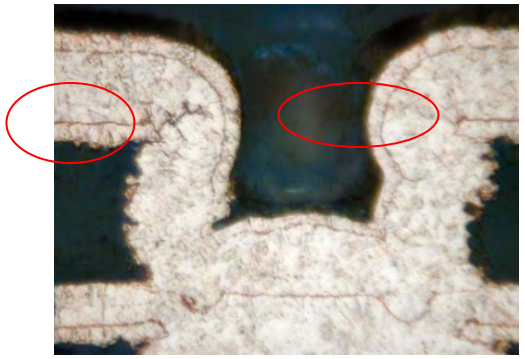
- Failure modes:



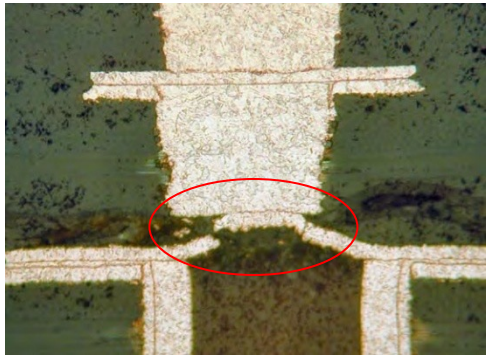
Interfacial separations [1]



Barrel cracks [3]

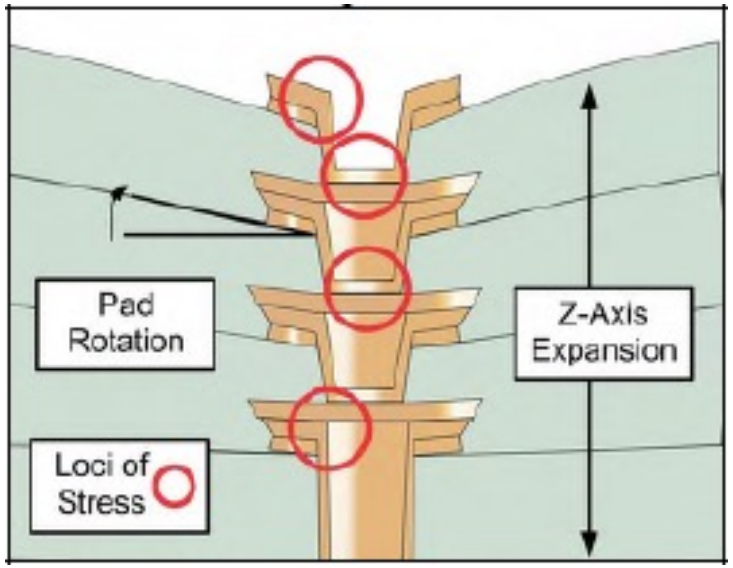


Corner/knee cracks [1]



Target pad cracks [2]

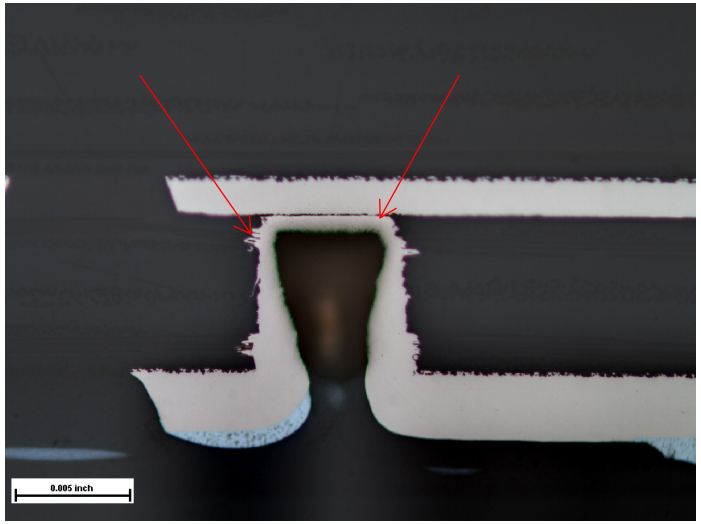
- Failures result from the thermomechanical stresses caused by CTE mismatch between metallization in the microvia structure and the dielectric materials in the board thickness direction (Z-axis). Typical CTE of copper = 17 ppm/°C; CTE of dielectric in Z-axis > 50ppm/°C.



[1] B. Birch, "Reliability Testing for Microvias in Printed Wire Boards", Circuit World, Vol 35, No. 4, pp.3 – 17, 2009
[2] Heer, Hardeep, and Ryan Wong. "Reliability of stacked microvia." Proc. IPC APEX Technical Conference. 2014.
[3] Lesniewski, Thomas. "Effects of dielectric material, aspect ratio and copper plating on microvia reliability." Proc. IPC APEX Technical Conference. 2014.

Issues with Current Approach

- Micro-sectioning and inspection does not reveal fine-line separations between target pad and electroless copper.
  - Extremely small feature, small sample sizes.
  - Opens occur after reflow.
- There are a number of variables to microvia fabrication: laser drilling, design, chemistry, target pad cleanliness and process – all of which can contribute to microvias quality.
  - Microvias which have passed electrical tests after bare board fabrication can fail after assembly or rework. Separations can occur between a target pad and electroless copper interface.



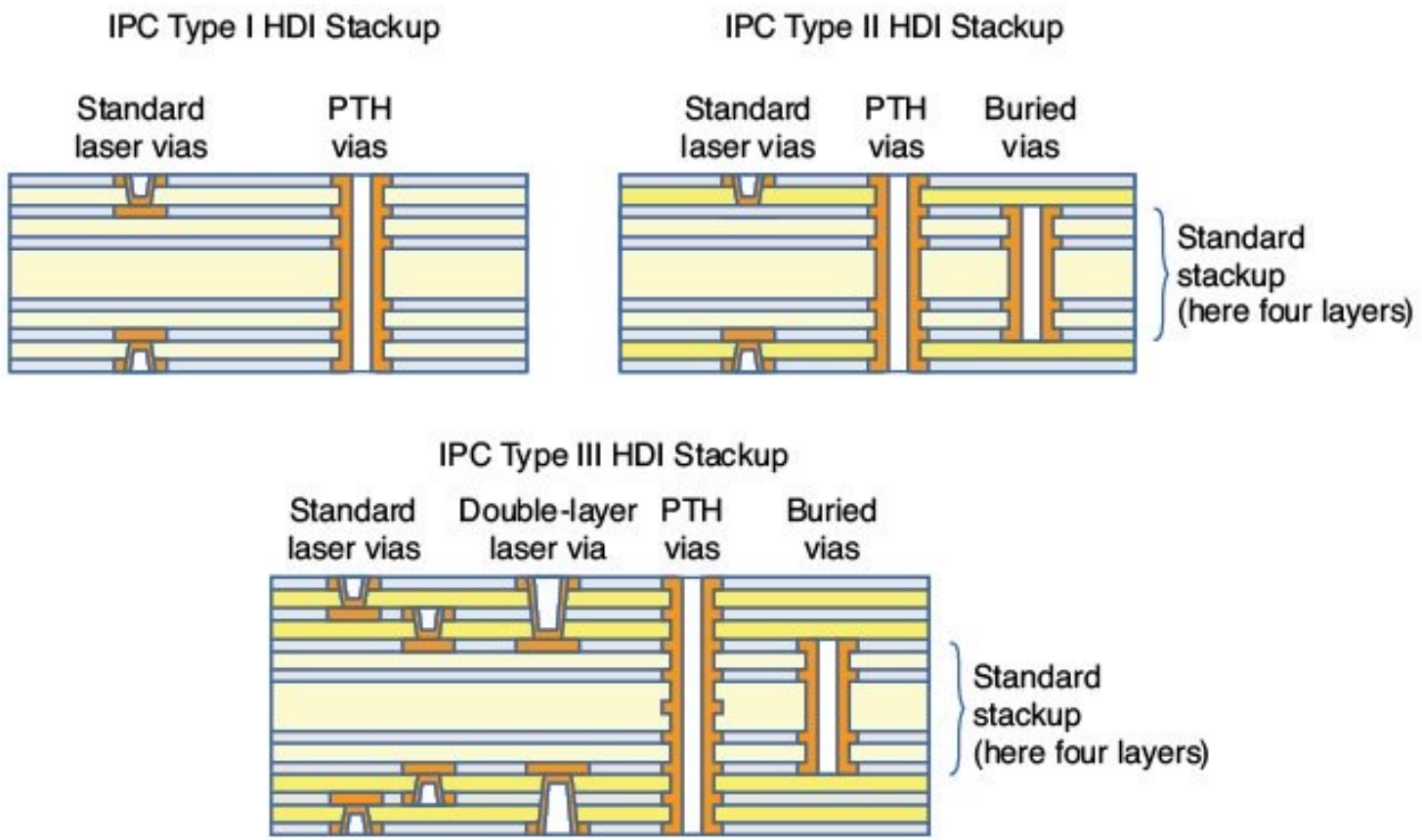




- Assurance approaches that focus on an understanding of the combinatorial effects of design, material and process, supplemented with analytical modeling are required.

IPC HDI Via Classification[1, 2] (Most Common Types)

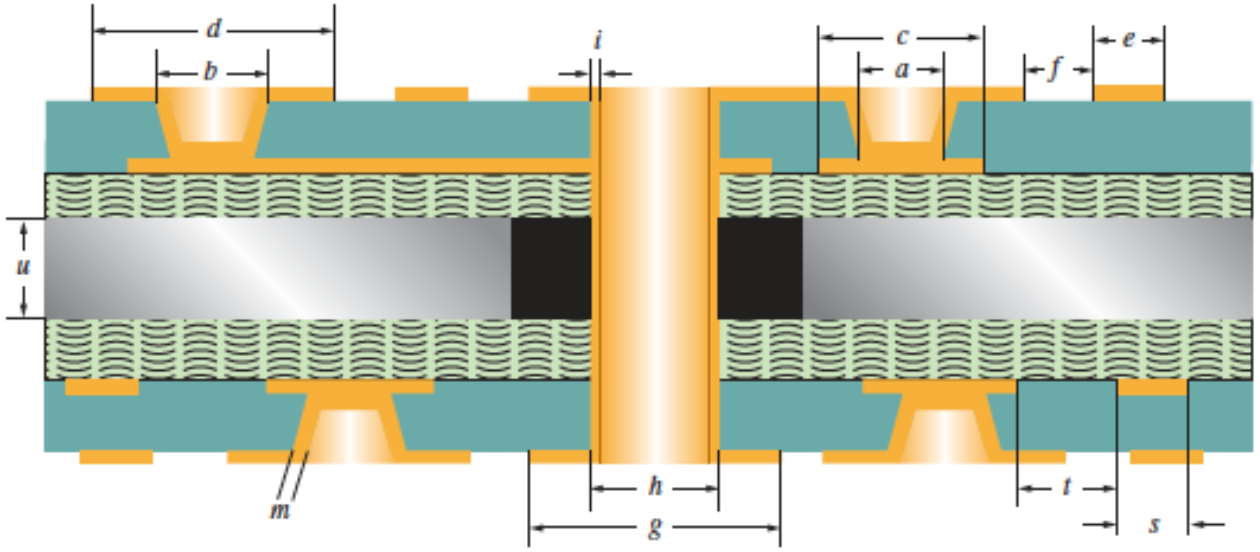
1. HDI Type I contains both microvias and conductive vias.
2. HDI Type II contains plated microvias, plated buried vias (two or more layers), and may have PTHs. The buried vias may be prefilled with a conductive/non-conductive paste.
3. HDI Type III contains plated microvias, plated buried vias (two or more layers), and may have PTHs.



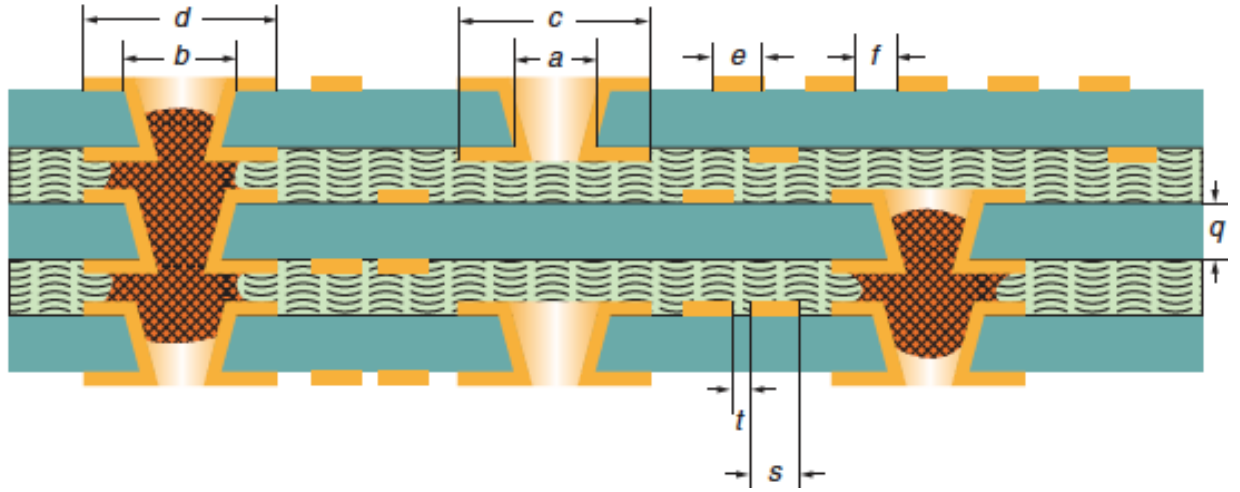
1 - Understanding Proper PCB Design, Available at https://circuitcellar.com/research-design-hub/basics-of-design/understanding-proper-pcb-design-part-2/, accessed July 22, 2022
2 – IPC-2226, Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

IPC HDI Via Classification[1] (Less Common Types)

- HDI Type IV Constructions contains microvia layers over an existing predrilled passive substrate. Additional microvia layers can be added sequentially. The core substrate is usually manufactured using conventional printed board techniques.



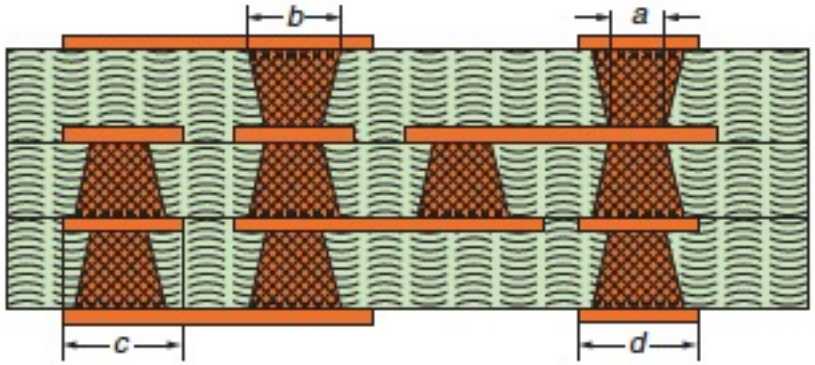
- Type V Constructions contains both plated microvias and conductive paste interconnections through a co-lamination process. There is essentially no core to this type of construction since all layer pairs have the same characteristics.



1– IPC-2226, Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

IPC HDI Via Classification[1] (Less Common Types)

- Type VI Constructions contains electrical interconnection and mechanical structure that are formed simultaneously. The layers may be formed sequentially or co-laminated, and the conductive interconnection may be formed by means other than electroplating (i.e., anisotropic films/pastes, conductive paste, dielectric piercing posts, etc.).



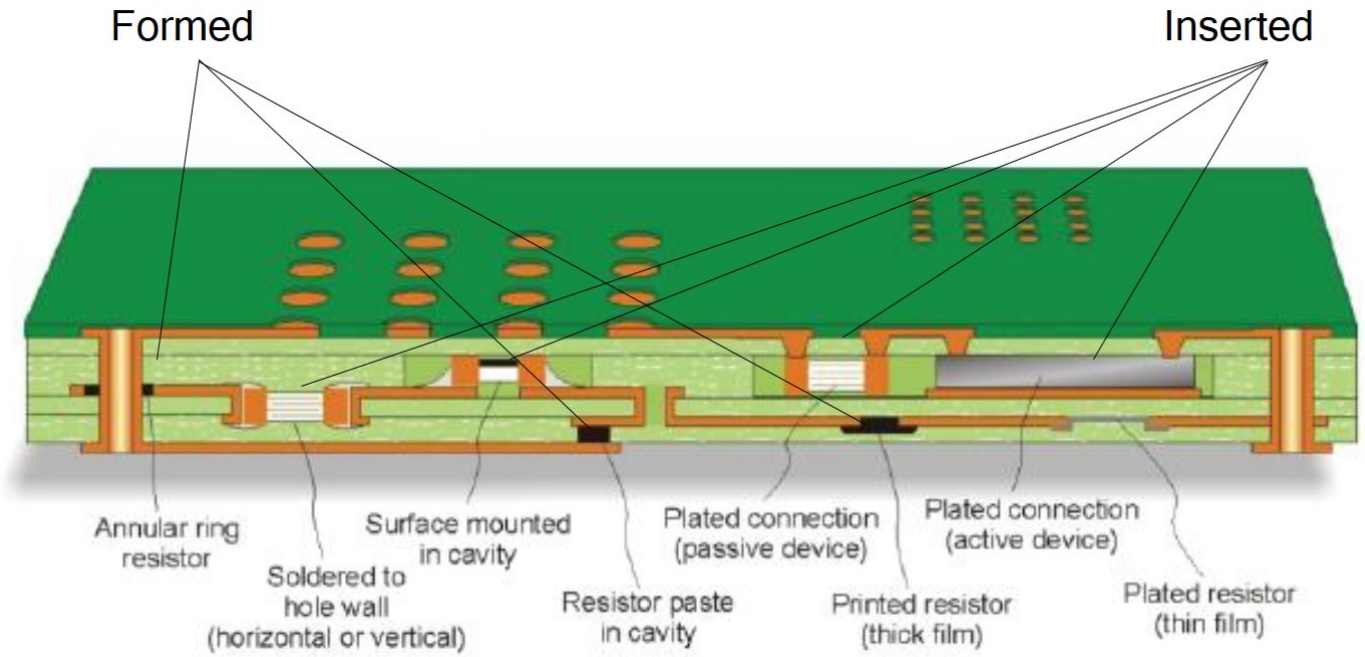
1– IPC-2226, Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

Overview of Design and Assembly Process Implementation for Embedding Passive and Active Components

- Introduction
- Evolution of Embedded Circuitry Standards and current status
- Selection criteria for embedding components
- Embedding passives and actives
- Embedding active semiconductors
- Closure

Introduction – Embedded Circuitry[1]

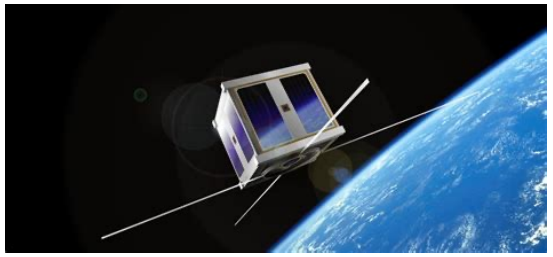
- Printed circuits have traditionally served as the platform for mounting and interconnecting active and passive components on the outer surfaces-
- Embedding a broad range of components within the circuit structure is undertaken to improve functionality and minimize usage of surface space.
- Both uncased active and passive component elements are candidates for embedding.
- The decision to embed components within the multilayer circuit structure, however, must be made early in the design process.

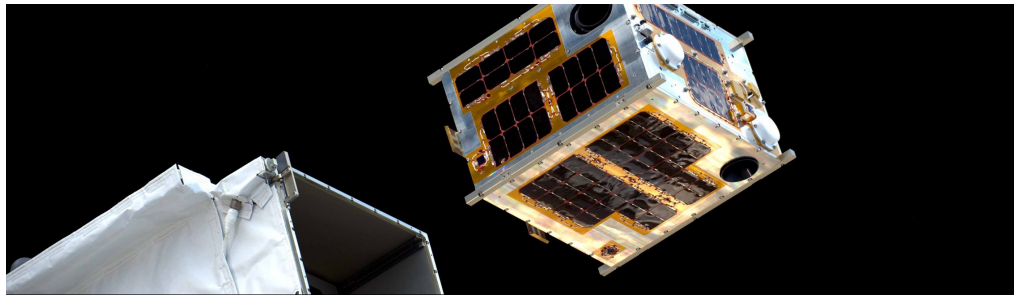


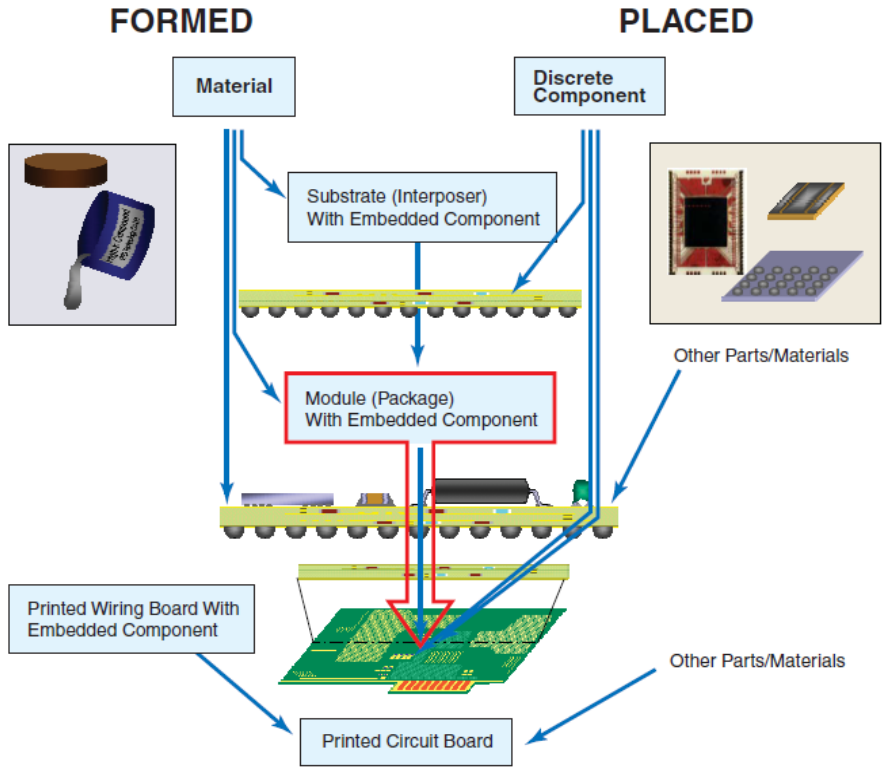
1– IPC-7092 - Design and Assembly Process Implementation for Embedding Passive and Active Components

Drivers for Embedding Components

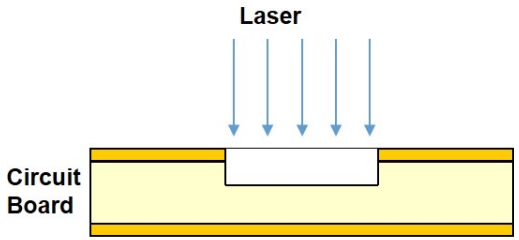
– Smaller board for same functions.
– Enable higher component density.
– Improve performance
    • Shorter circuit paths
    • Expanding bandwidth
    • Increasing signal speed
    • Minimizing noise
– Reducing total assembly costs.



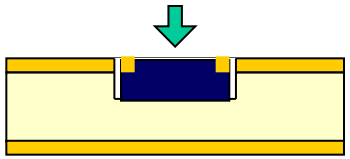




Embedding Parts/Power Sources into PCBs is Not New[1]

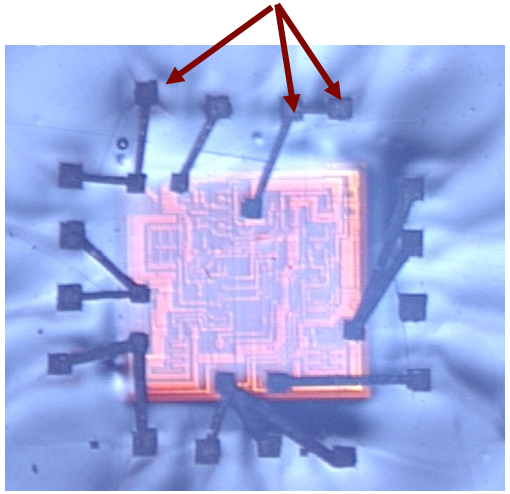


Use Laser Micromachining to Shape the Circuit Board



Place Device Inside Trench

Contacts From Die Pads to PCB

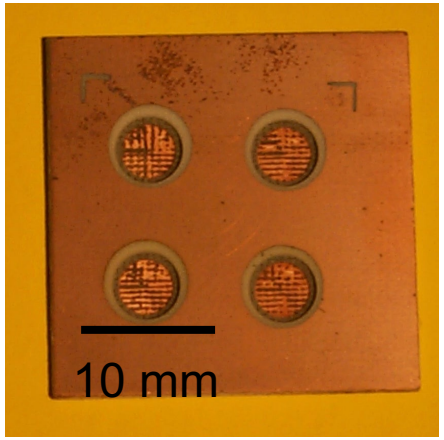




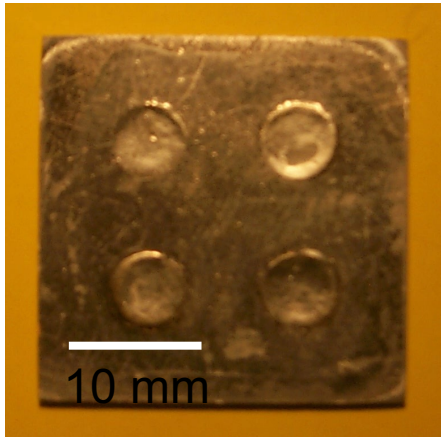
Encapsulate and Make Contacts

Laser Direct-Write Technique is capable of embedding virtually any type of die or surface mount component within any type of substrate

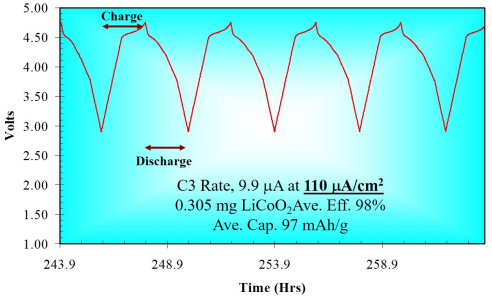
Laser Machined PCB

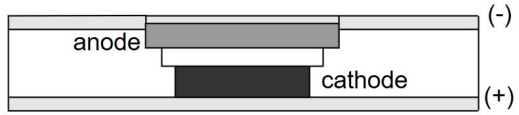


Sealed Structures



RO 4350 Circuit board





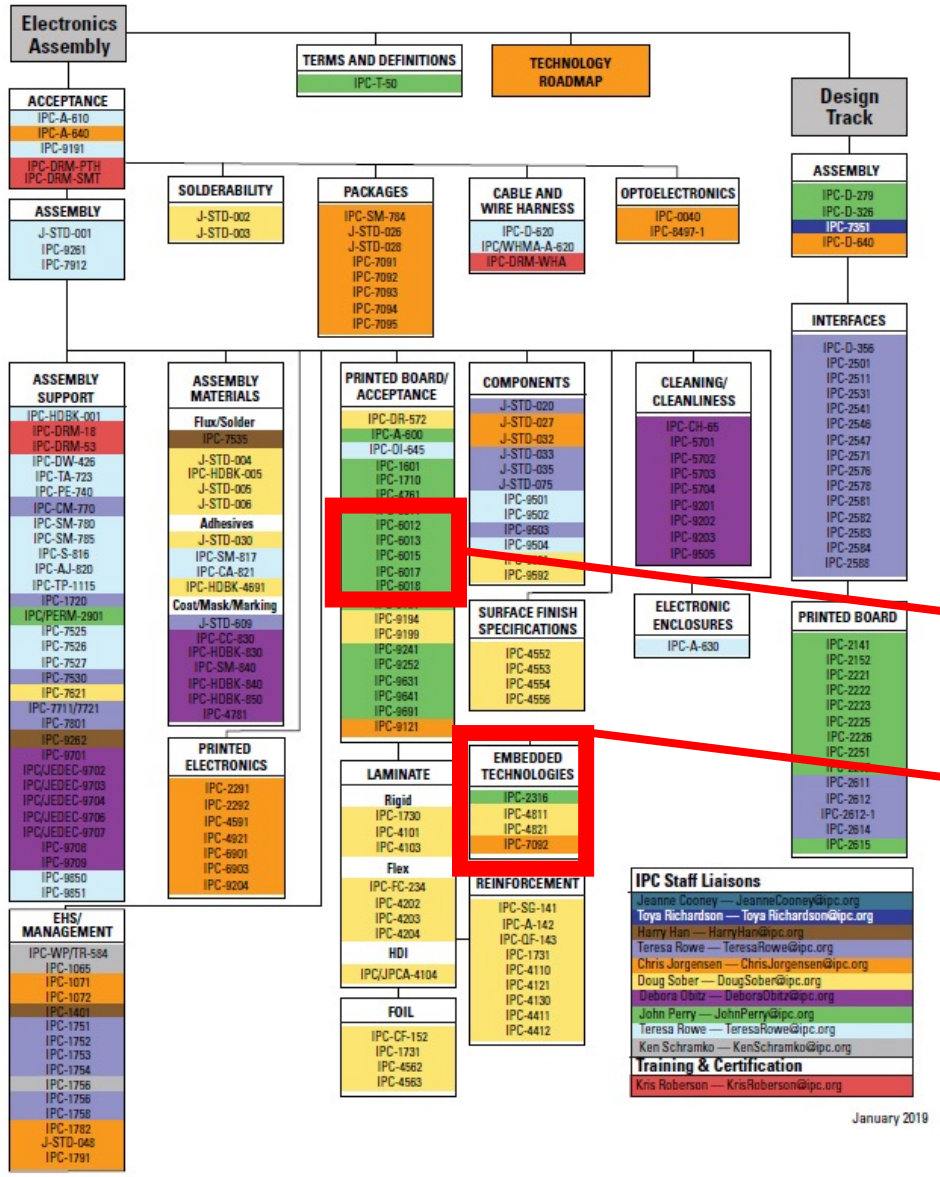
Fully Embedded and Concealed 1.5 Volt Alkaline Microbattery (4 cells in parallel)

Sood et al. "Laser-based technique for the transfer and embedding of electronic components and devices." U.S. Patent 8,056,222, issued November 15, 2011.

Evolution in Embedded Component Standards: Overview of current and evolving standards

- **IPC-2316** Design Guide for Embedded Passive Device Printed Boards (2007)
- **IPC-4811** Specification for Embedded Passive Device Resistor Materials for Rigid and Multilayer Printed Boards (2008)
- **IPC-4821** Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards (2006, Am 1 – 2010)
- **IPC-4101** Specification for Base Materials for Rigid and Multilayer Printed Boards.(Rev E, 2017)
- **IPC-6012** Qualification and Performance Specification for Rigid Printed Boards (Rev E, 2020)
- **IPC-6017** Qualification and Performance Specification for Printed Boards Containing Embedded Passive Devices (Published August 2021)
- **IPC-7092** Design and Assembly Process Implementation for Embedded Components (Published May 2022)

IPC Standards Tree



IPC-601X

Embedded Technologies

http://www.ipc.org/4.0_Knowledge/4.1_Standards/SpecTree.pdf

IPC-7092: Design and Assembly Process Implementation for Embedded Components

SCOPE

- IPC-7092 describes the design and assembly challenges for implementing passive and active components, in either formed or inserted methodology, into a printed board.
- The completed structure including internal electronic components is ready for surface mount and/or through-hole component attachment.
- The multilayered structure becomes a complete product ready for further processing in an assembly process and be made from organic, inorganic (ceramic) or both types of material.

Purpose

- The target audiences for this document are managers, design and process engineers, and technicians who develop electronic assemblies that include an embedded component printed board as a part of the product.
- The purpose is to provide useful and practical information to those who are involved in the decision making of either formed or inserted, passive or active components and to help establish inspection techniques, testing processes, and reliability validations.

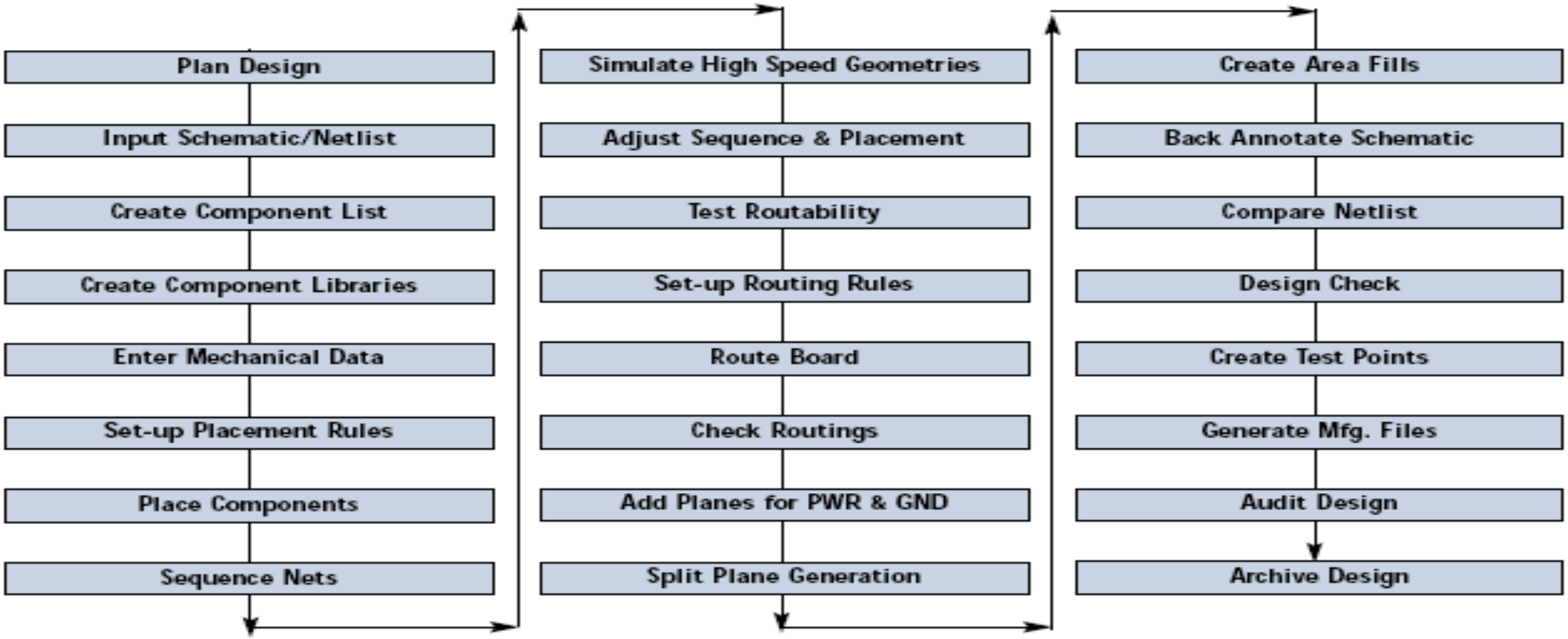


IPC-7092A is currently in draft

Embedded PCB – Planning

- The first decision that must be made is whether or not to adopt an embedded component solution.
- Depending on the application, cost, performance, or some other metric may influence the decision.
- Several factors must be considered:
  - Value range of passive components selected for embedding (formed or inserted).
  - Availability of discrete passive components suitable for inserting.
  - Procurement of bare ‘tested’ die prepared for embedding.

Embedded PCB Planning

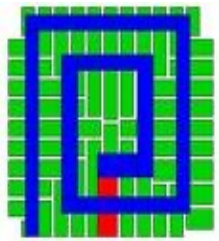


Design Layout Steps Prior to Embedded Component Board Assembly Density Feasibility

Formed Passive Components

- Formed resistors
  - Several companies have developed material sets and fabrication processes for thick-film resistors, requiring only a conventional screen-printing process. (Slide 26) Thick Film Resistor Forming Process
- Formed capacitors
  - The capacitor dielectric separating the copper surfaces of the power and ground plane an organic polymer thick film or ceramic thin film composite. (Slide 33) Formed Capacitors
- Formed inductors
  - A specific inductance can be developed using thin circuit trace patterns configured in spiral like geometry. (Slide 36) Formed Inductors

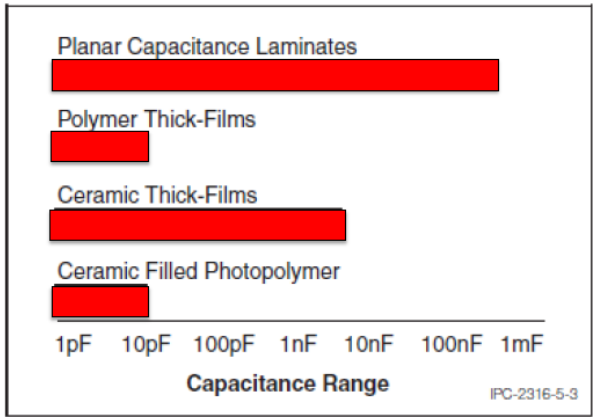




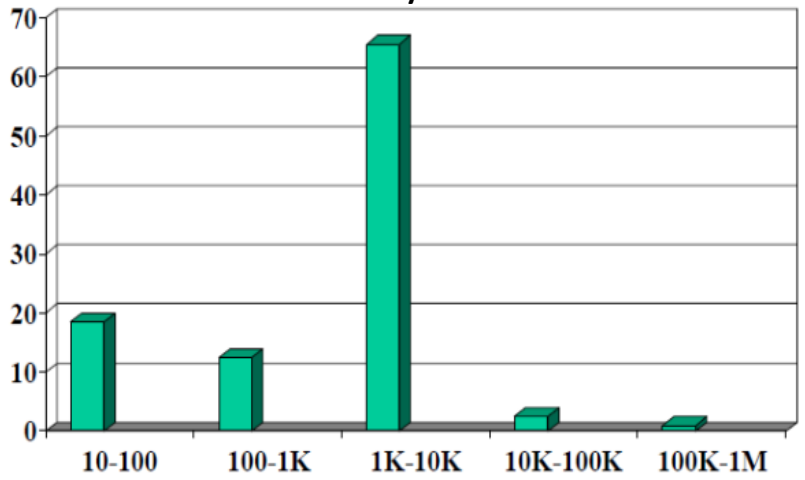


Inserted Passive Components

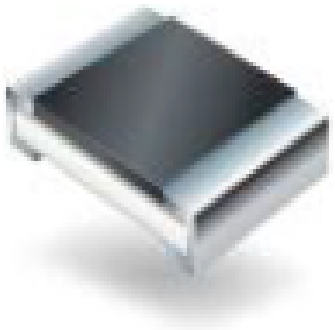
Formed capacitor materials: Technology v/s Capacitance Range



Selecting Resistors for Embedding : % Distribution by Resistor Value



- As an alternative to forming component parts, many designs are inserting discrete passive components within the multilayer circuit.
- The smallest discrete resistor is furnished in a standard 01005 package outline in all standard values.
- The capacitor family includes the 01005 package outline as well, but value range will be limited.
- Small outline inductors are available from limited sources with values ranging up to 100nH.





Selection Criteria in IPC-7092

- Available tolerance of the embedded parts and aging behavior.
- Drift limits following thermal shock or humidity exposure.
- Temperature coefficient impact on capacitance or resistance.
- Power handling capacity, breakdown field and leakage currents.
- Parts that will need circuit tuning or active trimming.
- Special requirements e.g., low noise metal film resistors.
- Available space for embedded parts, especially large capacitor values.
- Density of embedded parts – the cost effectiveness of embedding components may be maximized at some intermediate component density.

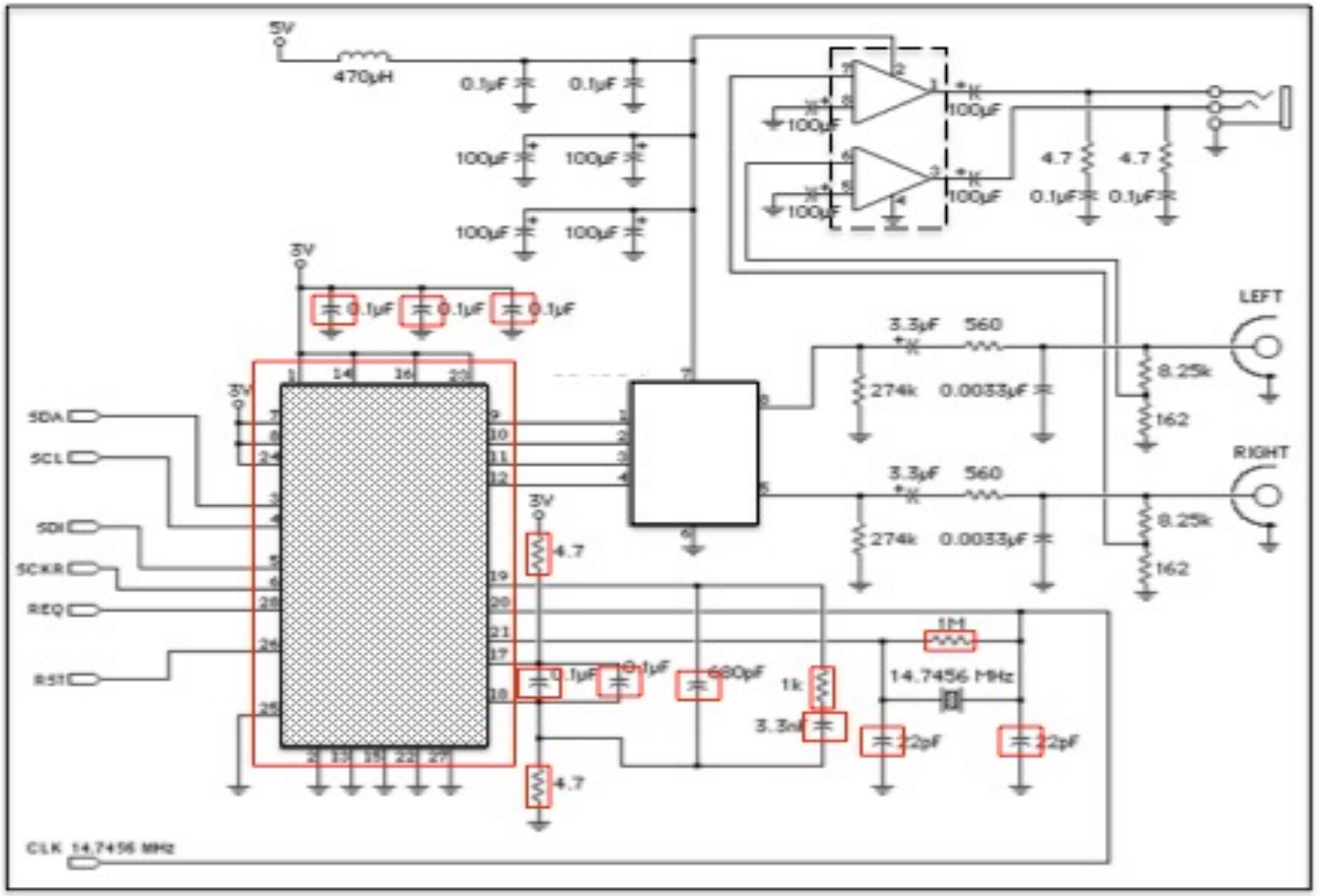
Perhaps the more difficult question to answer is ***Which embedding methodology will be used- formed passive or inserted discrete passive devices or a combination of both?***

The most common approach is to perform an analysis of embedded passive components:

1. Estimate the board size by the sum of the layout areas associated with the replaced discrete passives and determine the new number of boards on the production panel.
2. Determine the new board cost based on a higher per unit area cost for the embedded passive panel fabrication and the new panel yield computed.
3. Define the available manufactured components intended for insertion or the materials required for producing formed passive components.

Selecting Components for Embedding

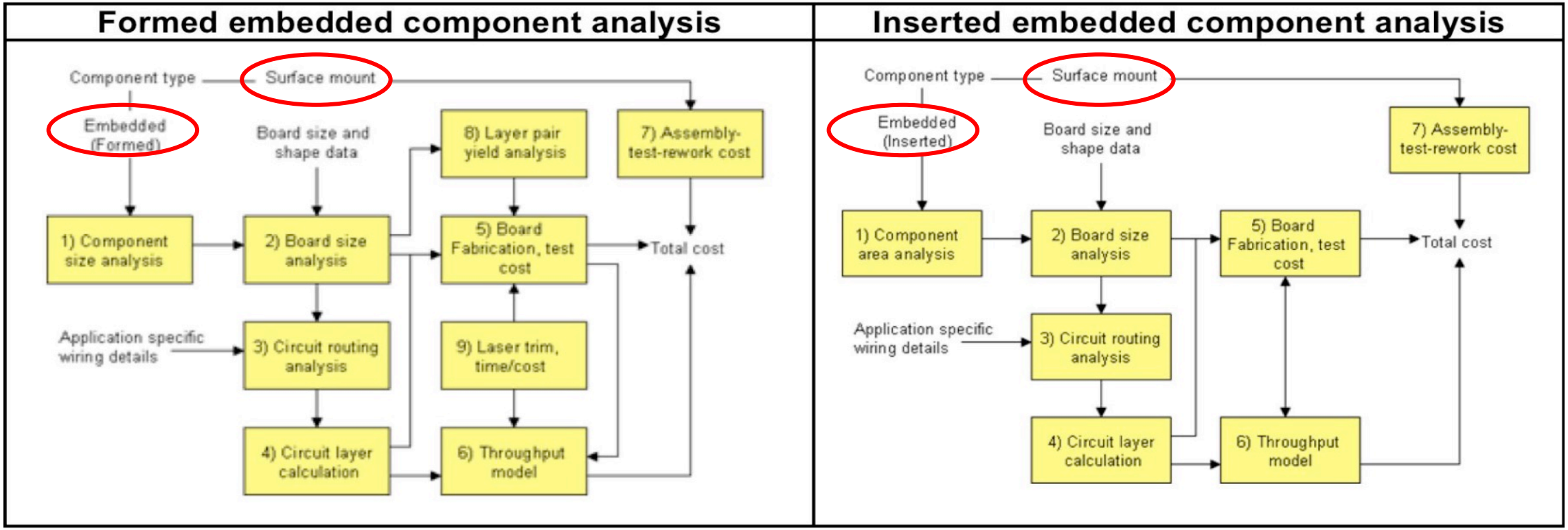
- Select passive components closely coupled to active device.
- Formed passive devices will have broad tolerance range.
- Inserted passive device values enable closer tolerances.
- Identify embedded component elements with a unique reference designator that is related to a specific layer of a PCB with embedded circuitry.



IPC-7092

Embedded Circuitry Cost Analysis for Passive Components (IPC-7092)

- The analysis focuses on differences in system cost between embedded passive and discrete passive solutions and assembly costs associated with non-embeddable parts.



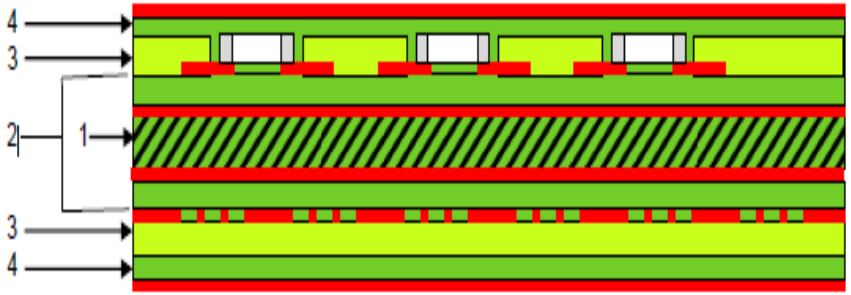
Defining Embedded Circuitry PCB Structure Groups

- IPC-7092 furnishes common Embedded Circuitry PCB structure groups (A-F)
  - The grouping is intended to identify some of the precision and control needed in the manufacturing processes.
  - The component handling, positioning, and attachment method are determined based on the manufacturers' capability and the completed base-core's ability to withstand multiple processing procedures and exposures.

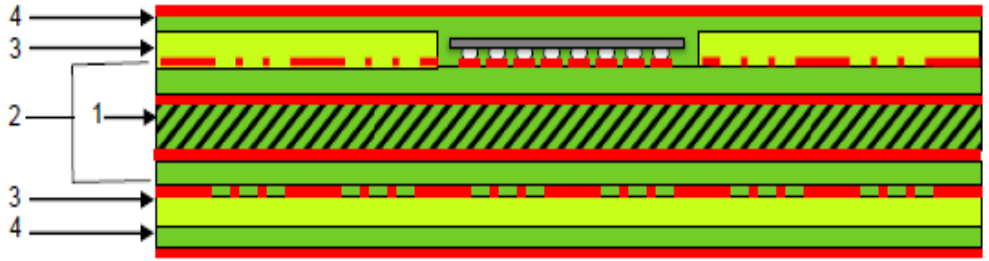
Defining Structure Groups

Type	Config	Description	Comments
A	1	Passive chip components "placed" on one side of a mounting base	Applications include developing a base-core ready for additional layers
	2	Active semiconductor chip components "placed" on one side of a mounting base	
	3	Passive chip and active semiconductor chip components "placed" on one side of a mounting base	
B	1	Passive chip components "placed" on both sides of a mounting base	Applications include developing a base-core ready for additional layers or component mounting
	2	Active semiconductor chip components "placed" on both sides of a mounting base	
	3	Passive chip and active semiconductor chip components "placed" on both sides of a mounting base	
C	1	Passive chip components "placed" on one side of a mounting base with formed components within the base	Applications include developing a base-core ready for additional layers or component mounting or a completed electronic assembly
	2	Active semiconductor chip components "placed" on one side of a mounting base with formed components within the base	
	3	Passive chip and active semiconductor chip components "placed" on one side of a mounting base with formed components within the base	
D	1	Passive chip components "placed" on both sides of a mounting base with formed components within the base	Applications include developing a base-core ready for additional layers or component mounting or a completed electronic assembly
	2	Active semiconductor chip components "placed" on both sides of a mounting base with formed components within the base	
	3	Passive chip and active semiconductor chip components "placed" on both sides of a mounting base with formed components within the base	
E	1	Passive formed components within a base-core intended for further layering	Applications include base-core ready for additional layer and/or component mounting or both
	2	Passive formed components within a base-core intended for component mounting	
	3	Passive formed components within a base-core intended for further layering and component mounting	
F		A coreless structure adopting build-up processing and plated via interface to interconnect circuit layers	

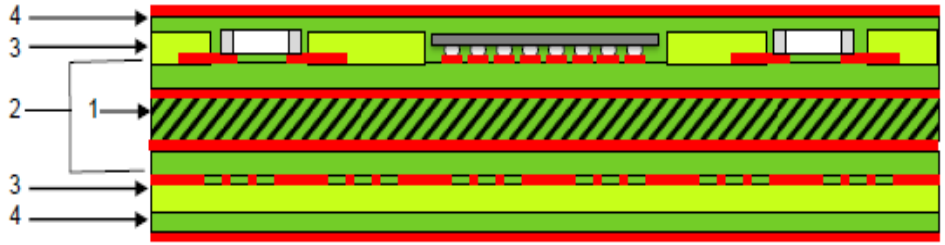
Type A



A1 Base-core example with inserted passive components on one side



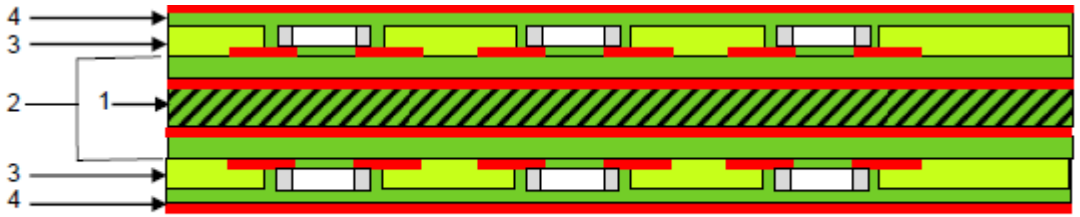
A2 Base-core example with inserted active components on one side



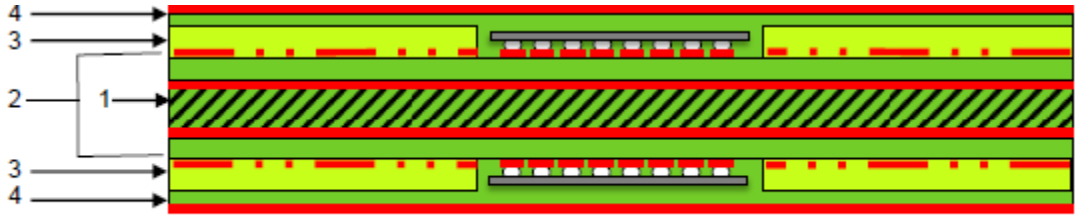
A3 Base-core example with inserted passive and active components on one side

1-Copper clad (2 side) core; 2- Component mounting base; 3-Cavity modified prepreg; 4-Copper clad dielectric

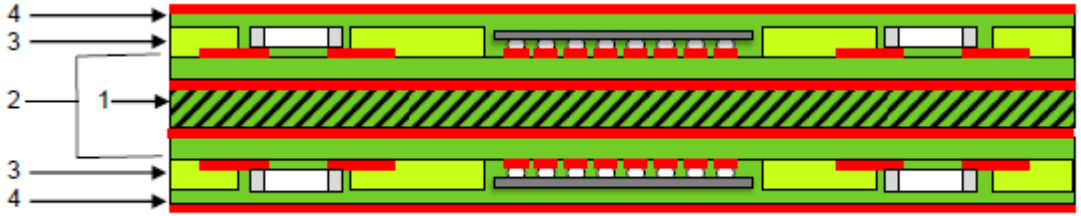
Type B



B1 Base-core example with inserted passive components on two sides



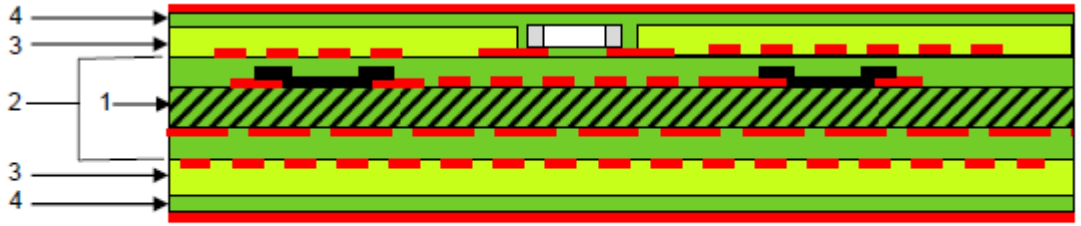
B2 Base-core example with inserted active components on both sides



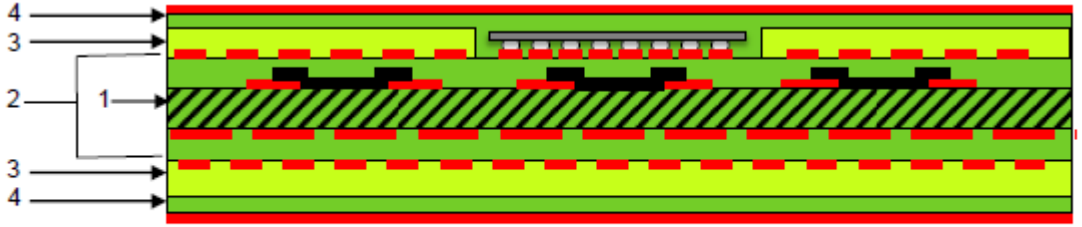
B3 Base-core example with inserted passive and active components on both sides

1-Copper clad (2 side) core; 2- Component mounting base; 3-Cavity modified prepreg; 4-Copper clad dielectric

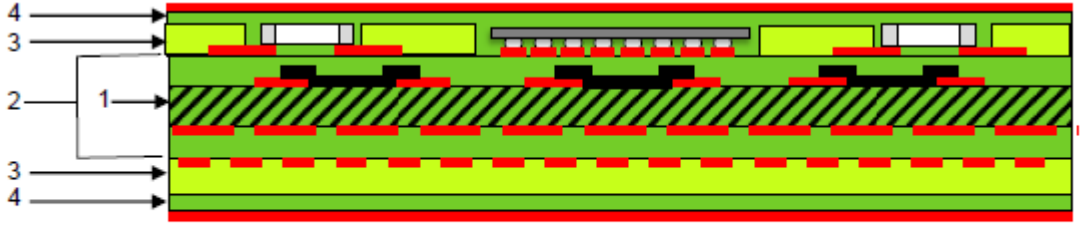
Type C



C1 Base-core example with formed passive components in the mounting base and inserted passive components on one side



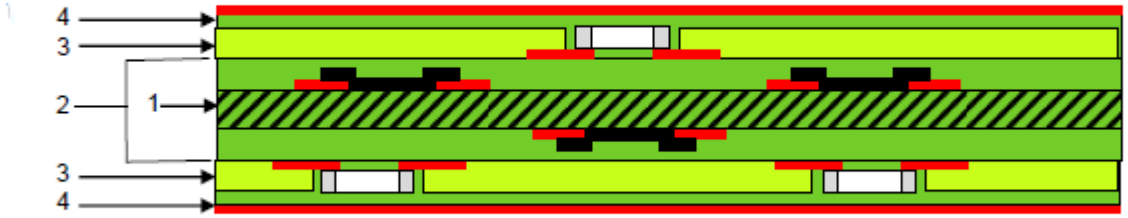
C2 Base-core example with formed passive components in the mounting base and inserted active components on one side



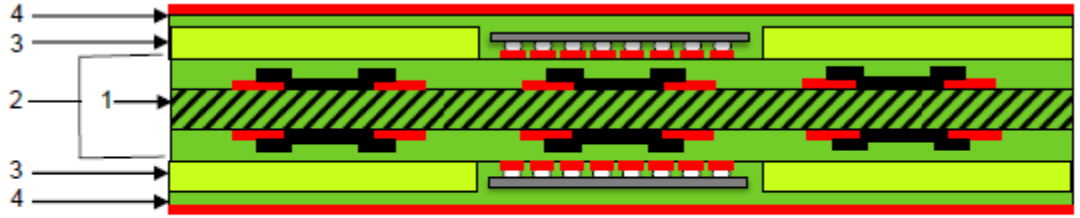
C3 Base-core example with formed passive components in the mounting base and inserted passive and active components on one side

1-Copper clad (2 side) core; 2- Component mounting base; 3-Cavity modified prepreg; 4-Copper clad dielectric

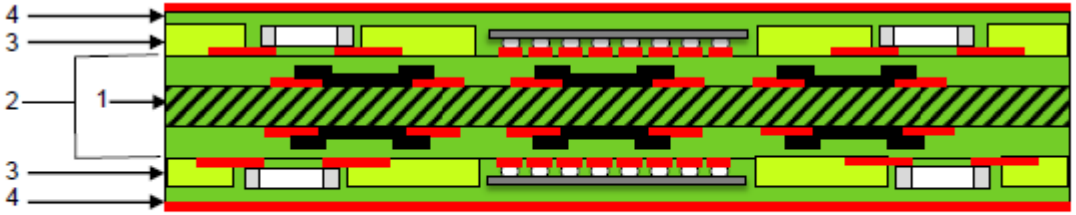
Type D



D1 Base-core example with formed passive components in the mounting base and inserted passive components on both sides



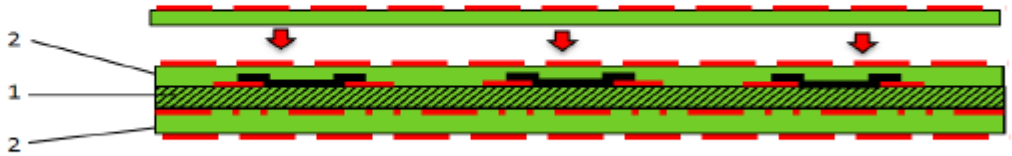
D2 Base-core example with formed passive components in the mounting base and inserted active components on both sides



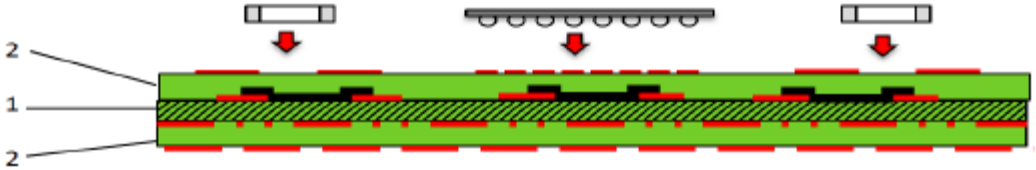
D3 Base-core example with formed passive components in the mounting base and inserted passive and active components on both sides

1-Copper clad (2 side) core; 2- Component mounting base; 3-Cavity modified prepreg; 4-Copper clad dielectric

Type E



E1 Mounting base example with formed passive components inside the mounting base plus additional layering added to one or both sides



E2 Mounting base example with formed passive components inside the mounting base turning the product into an base-core

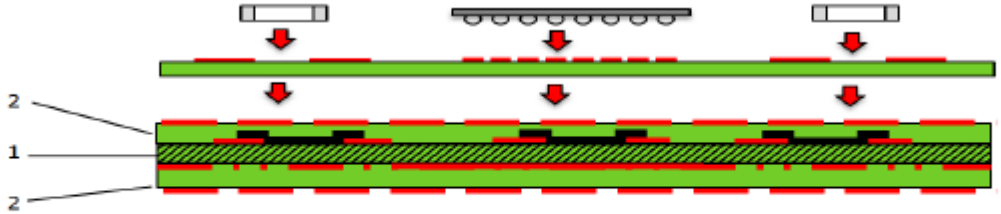
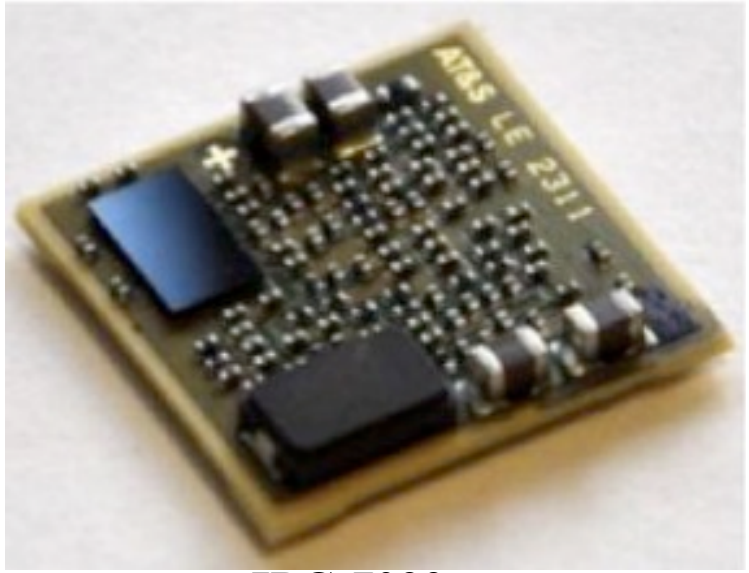


Figure 7-21 E3 Mounting base example with formed passive components inside the mounting base plus additional layering added to one or both sides

1-Copper clad (2 side) core; 2-Copper clad dielectric

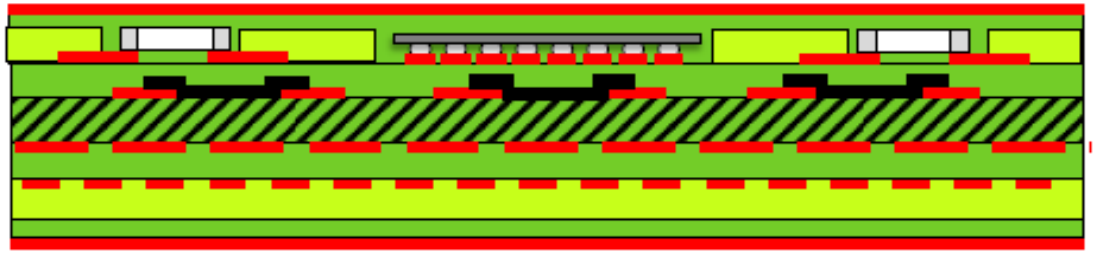
Structure Type F: Embedded Core Technology

- The process description for the F embedded core structure is based on a ‘face down’ semiconductor element mounting and laser ablated and plated via interface technology.
- Type F is a combination of HDI micro via and ultra-fine line process based on a modified semi-additive Cu plating technology and precise component assembly methodology .

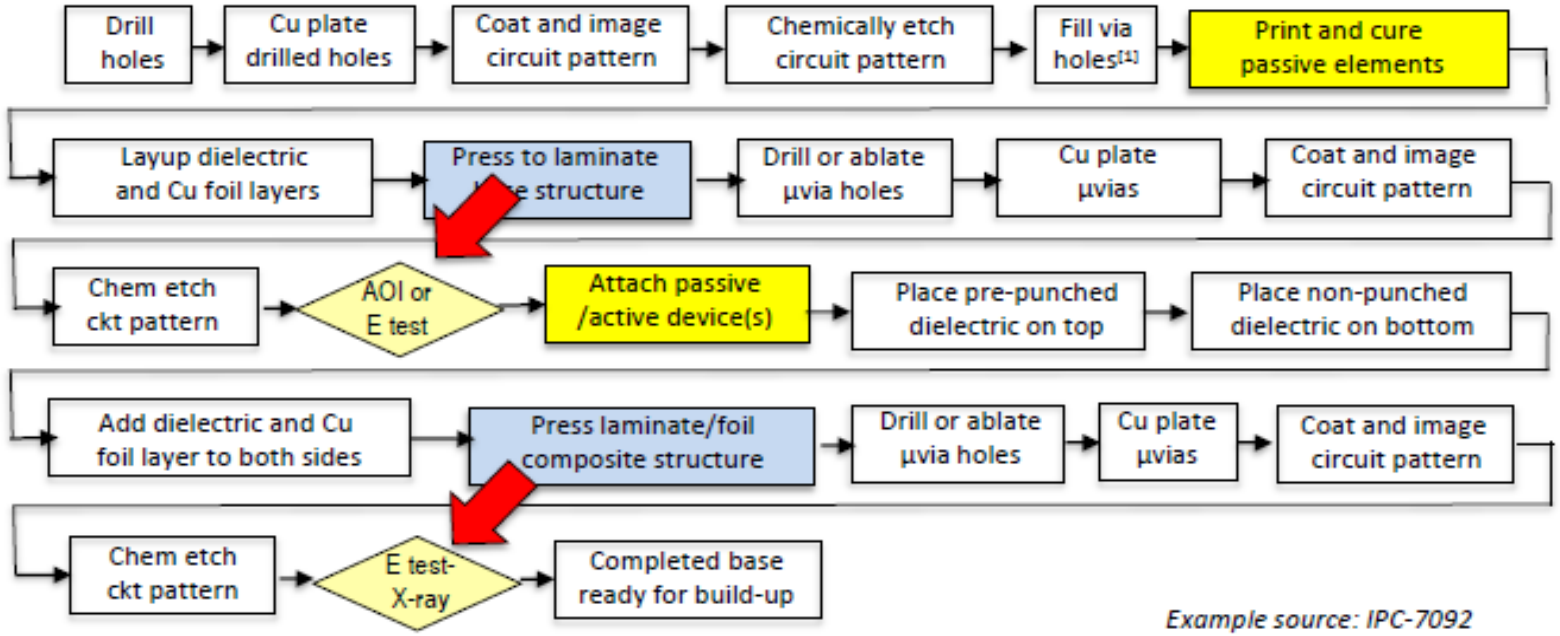


IPC-7092

Planning Embedded Circuitry PCB Fabrication Process Flow



C3 Base-core example with formed passive components in the mounting base ***and*** **inserted passive and active components on one side**



Example source: IPC-7092

Embedded Circuitry PCB Base Material Selection

- Industry roadmaps consistently point to materials and process refinement as the key enablers for improving product performance and manufacturing efficiency.
- Likewise, the conversion to lead-free solder technologies has forced the laminate industry to make significant refinement to all packaging and substrate related materials.
- The substrate methodologies being used for embedded semiconductor and passive component packaging will likely utilize one of the following dielectric systems:
  - FR-4 or FR-5 Epoxy/Glass – Primary PCB base material
  - BT Epoxy/Glass – Semiconductor substrate
  - Polyimide film (PI) – Used for environments requiring higher uptime and availability

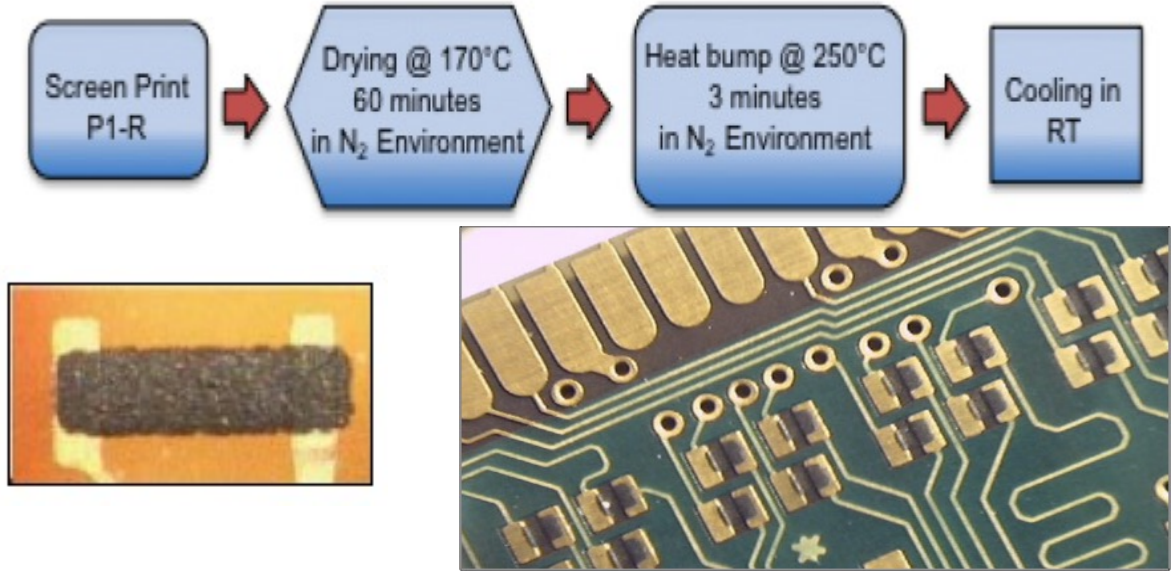
Type	Resin	Reinforcement	T_g (°C)
FR-4	Epoxy	Woven E Glass	130-170+
B-T	Bismaleimide triazine/epoxy	Woven E Glass	170-230
PI	Polyimide	Woven E Glass	250-265

Data source: IPC-4101

- Although many material systems can furnish excellent functional capability they do not all have a broad supply base.
- Because BT and PI may have more limited applications, fabrication costs are somewhat higher than the more common FR-4 based substrate.

Thick Film Resistor Forming Process

- Polymer thick-film (PTF) resistors can be printed directly onto the laminate surface.
- The application of these materials require only conventional screen printing processing to provide the resistor pattern.
- The paste-like PTF material is available in resistance values that range between 1 ohm and 1meg ohm per square while the CTF materials value range between 10 ohms and 10K ohms.
- Photo sensitive emulsion is applied onto the screen surface, photo-imaged and developed to provide the resistor pattern



Carbon Thick Film Resistor example.

Screen printing is typically adopted for applying resistive paste or ink patterns, variables-

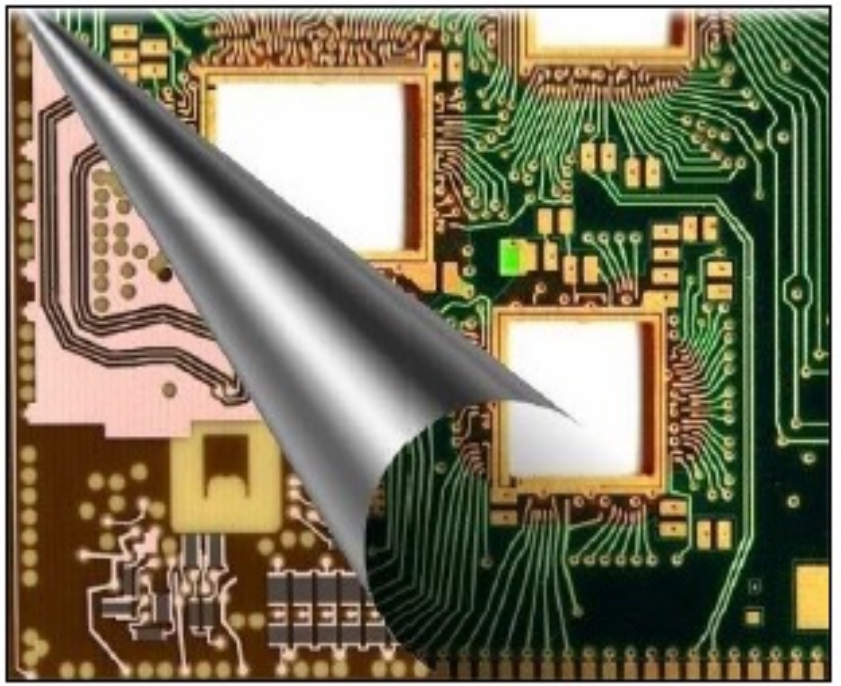
- Screen material stretch or shrinkage.
- Emulsion exposure variation.
- Affects of screen cleaning process.

Thick Film Resistor Issues and Concerns

- Resistance ranges and process variations.
- Expectation for resistor value stability.
- Affect of environment conditions-
  - Thermal stability
  - Moisture
  - Time (age affect)
- Material adhesion.
- Laser trim accessibility.
- Suitable coatings for protecting element.

Design Criteria for Sheet Film Resistor Elements

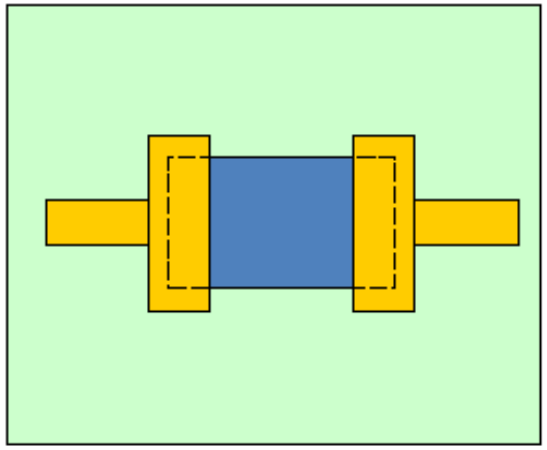
- The resistive foil is an integrated part of the system and should not be considered as an isolated element when designing the Embedded Circuitry PCB .
- Factors that effect system performance are:
  - Circuit configuration
  - Circuit thickness and material type
  - Thermal conductivity of the dielectric
  - Proximity to power or ground planes
  - Ambient operating temperature range
  - System cooling or heat sinking
  - Resistor size (total resistor area)



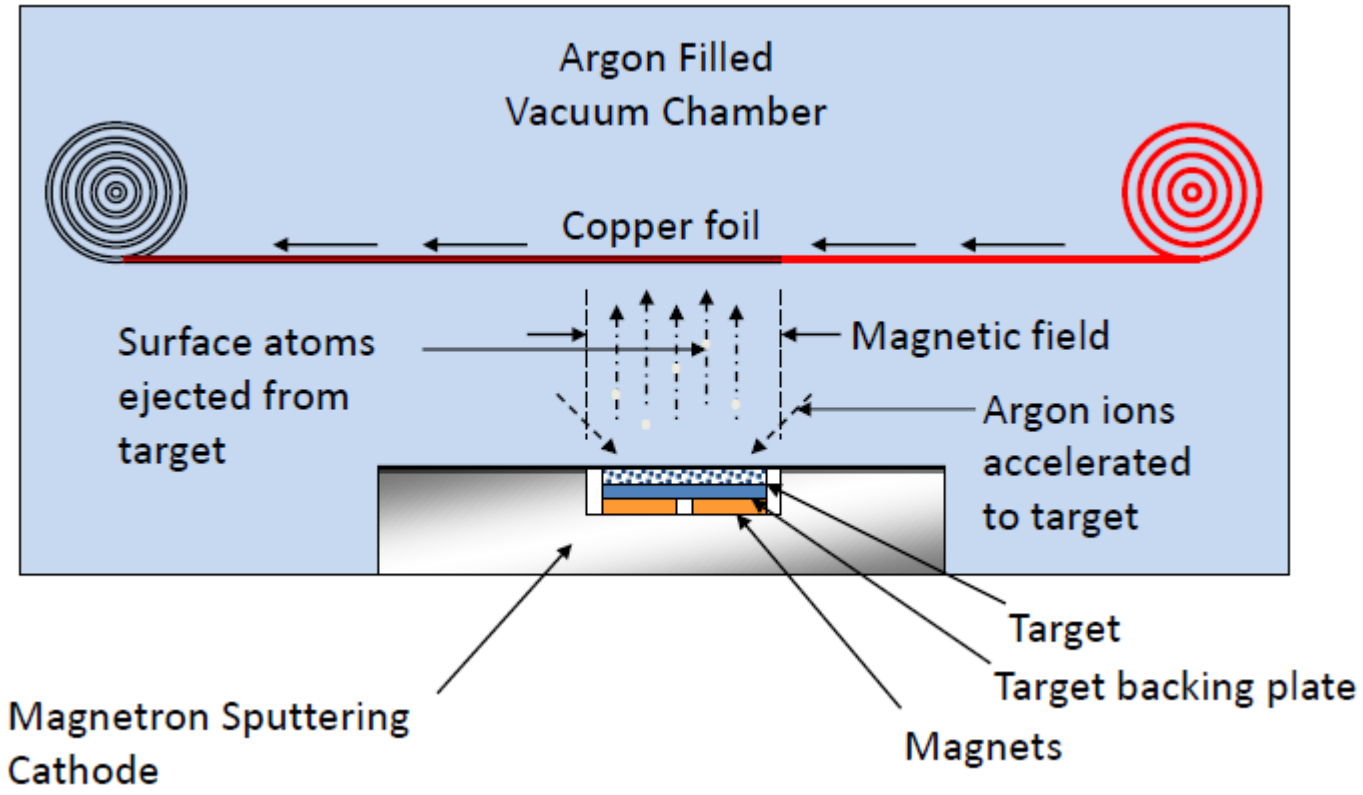
Example source: Ohmega Technologies

Foil Based Thin-Film Resistor Material

- Thin-film nickel chromium (Ni-Cr) or Nickel Chromium Aluminum Silicon (NiCrAlSi) is sputter coated onto Cu foil sheet stock,
- Furnished in 25, 50, 100 and 250 ohms/square sheet resistivity.
- Basic sheet resistor tolerance is +/- 5% but, laser trimming can be used to improve resistor tolerance.

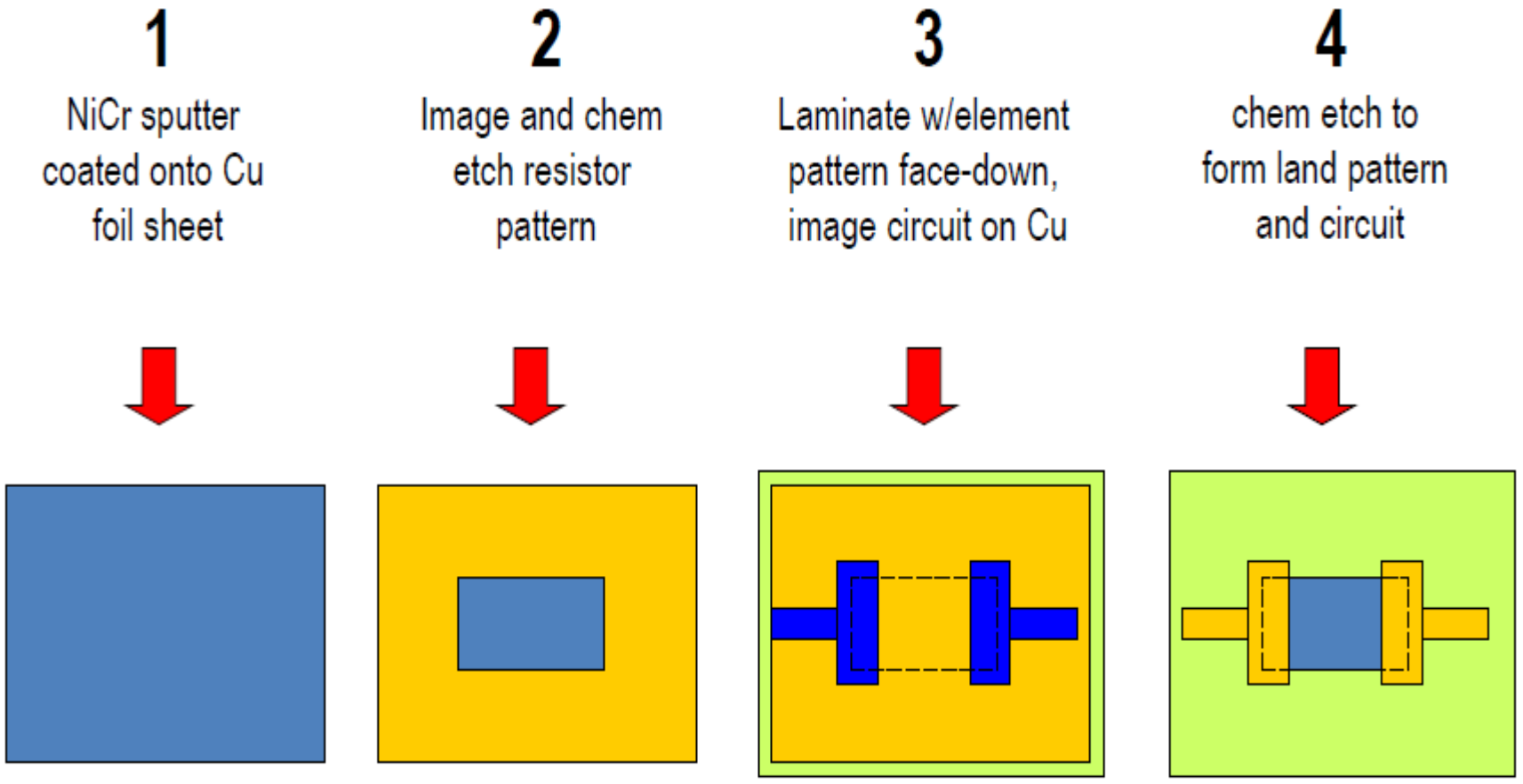


Thin-Film Deposition Process



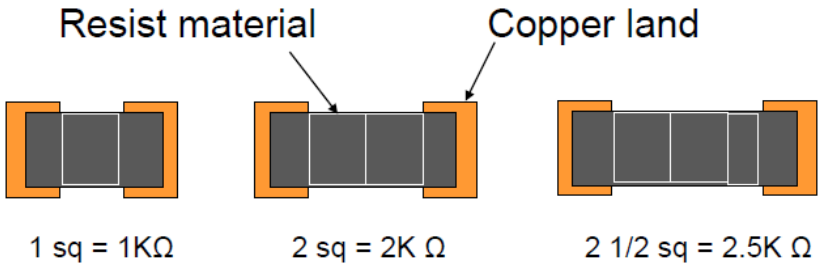
Thin-Film Resistor Forming Process

- Resistor elements are formed using a two step chemical etch process
- Compensation must be made for etching process tolerance.
- Finished resistor tolerance in the range of +/- 8% to +/- 10%
- Laser trimming can be used to improve resistor tolerance.
- Minimum recommended feature size is 0.25mm

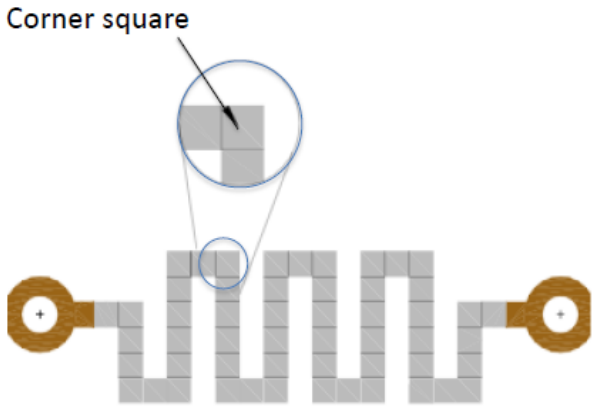


Basic Value Planning for Formed 'Bar' or Serpentine Resistors

The value of the bar resistor element (thick-film or thin-film) is determined by the basic value of the paste, ink or sheet composition and the number of square segments between land pattern features.



- A serpentine resistor can be designed as a bar resistor with the exception of the corner squares (right-angle bends).
- Due to the change in current density at right-angle path, the effective number of the corner square is 0.56.



Example:
Sheet resistance (RS) = 100 Ω/sq
No. of squares = 37
No. of corner squares = 16

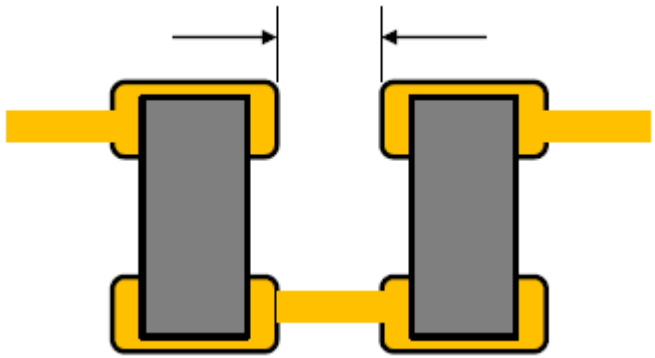
Total No. of effective squares =
37 + (16 @ 0.56) = 45.9 ≈ 46

Resistance value = 46 x 100 = 4.6 KΩ

Data and example source: Ohmega Technologies

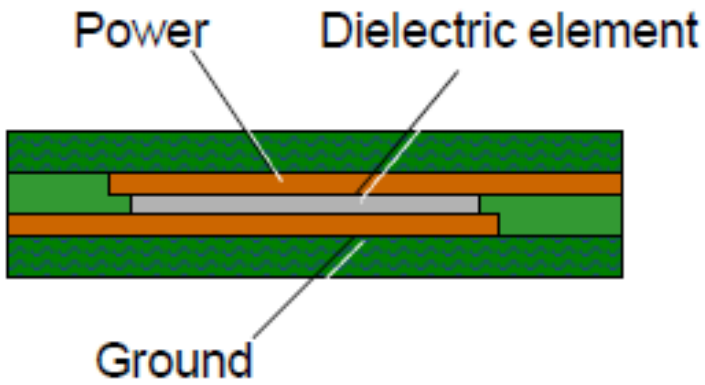
General Formed Resistor Layout Guidelines

- Establish optimum base value for resistors-
  - Refer to material suppliers dimension guide for details.
- Determine min/max resistor feature sizes needed-
  - Recommend maintaining basic rectangular shapes.
  - Printed patterns should be greater than 0.30mm wide.
- Allow 125µm spacing between copper features for test probe access and laser trim.
- Back to Formed Passive Components

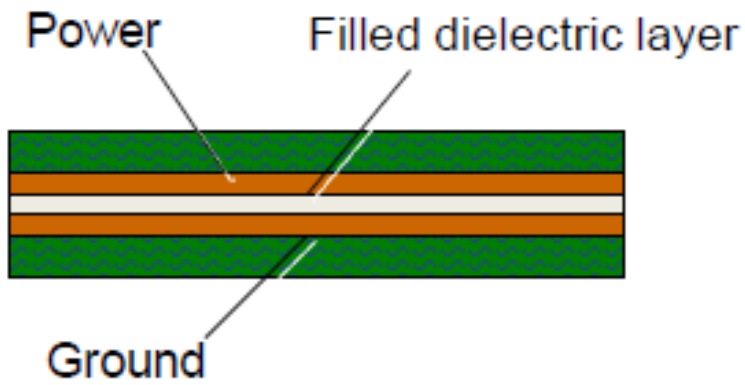


Formed Capacitors

- There are two techniques commonly adopted for embedded capacitor forming:
  - Dielectric material deposited directly onto a Cu foil or the circuit layers using a thick-film screening process.
  - Dielectric layer laminated between opposing copper circuit layers.



Discrete Form



Planar Form

Formed Capacitor Material / Process Variations

- Process variations-
  - – Etched copper planes on two sides of a filled or unfilled dielectric layer (Planar)
  - – Printed or photo-imaged
    - • Polymer thick film
    - • Ceramic thick film
    - • Ceramic filled polymer
- Monetary impact-
  - - Minimal for all photo-print products
  - - Precision screen-printing may be required
  - - Precision photo-imaging commonly required
  - - Some material may need high temperature curing

Capacitor Value Range Limitations

- The discrete SMT capacitor family includes the 01005 and 0201 outline capacitors as well but the dielectric type, working voltage and value range for the smaller device outlines may be somewhat limited from traditional sources.

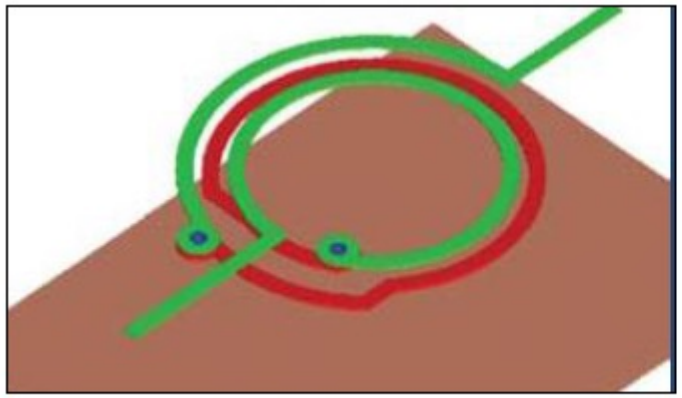
EIA	Size (mm)			Capacitance					
	L	W	T	1nF	10nF	100nF	1uF	10uF	100uF
0201	0.6	0.3	0.3						
0402	1.0	0.5	0.5						
0603	1.6	0.8	0.8						
0805	2.0	1.25	1.25						
1206	3.2	1.6	1.6						
1210	3.2	2.5	2.5						
1812	4.5	3.2	2.5						

Example source: Murata Mfg. https://www.murata.com/en-us/products/capacitor/mlcc/lineup#smd

Back to Formed Passive Components

Formed Inductors

- Formed inductors are current loops configured in the Cu foil to induce a magnetic field for short term storing and controlling inductive energy.

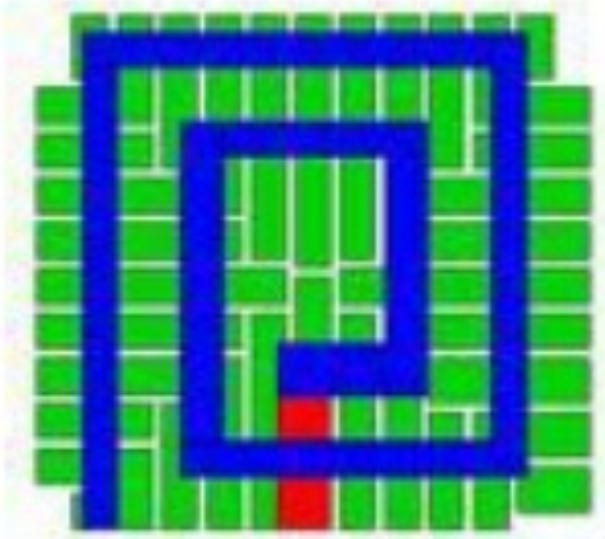


Example source: IPC-2316



Formed Inductor Design

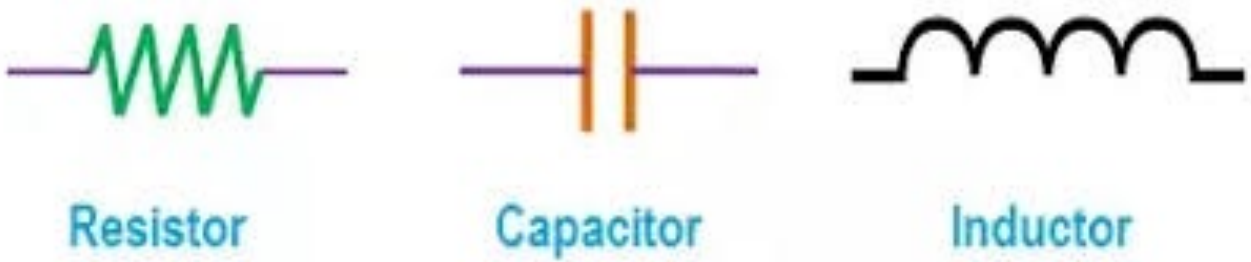
- The inductance is determined by the length of the spiral and number of turns.
- The spacing between turns will control the resonant frequency of the inductor.
- A wider spacing will typically reduce capacitance and raise the inductance frequency.



Back to Formed Passive Components

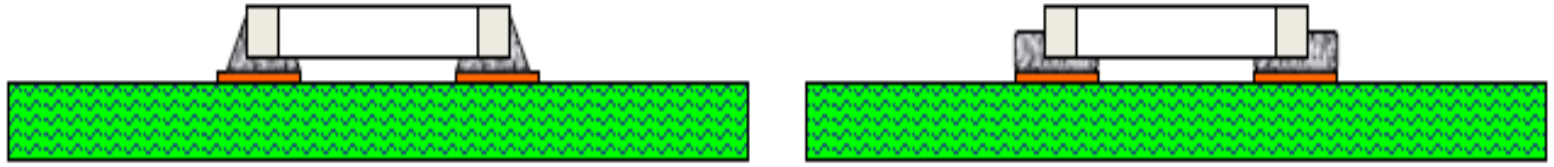
Inserted Passive Devices

- Resistors
  - Small outline, thin profile
  - Broad value range, wide tolerance choice
- Capacitors
  - Small outline, varying profile
  - Limited value range and tolerance
- Inductors
  - Small outline, varying profile
  - Very limited value range



Component Termination Variations

- Interconnection can be made using deposited solder paste and reflow processing or secured using a anisotropic conductive polymer and a thermal cure process.



- Miniature pass placement systems with a

Alternative Termination Process

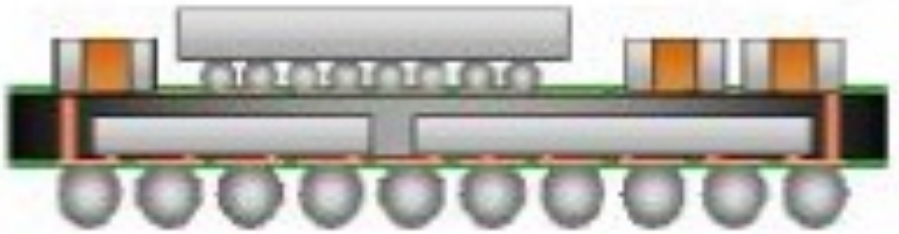
- Rather than relying on solder or conductive polymer for electrical interface, passive devices can be mounted onto the substrates surface with a non-conductive adhesive.
- Electrical termination can then be made directly onto the component terminals with micro-via ablation and copper plating process.



- To achieve the most reliable micro via to component interface the user should specify copper plated terminals when ordering passive components.

Embedding Active Components

- Progress in developing high density embedded component substrate capability has accelerated through the cooperation and joint development programs between a number of government, industry and technical universities.
- In addition to these joint development programs, several independent laboratories and package assembly service providers have developed a number of proprietary processes for specific applications.



Semiconductor Die Quality Classification[1]

- It is strongly recommended that the embedded die candidate be at least a 'Level 2' before use.

Quality Level	Visual Inspection	Electrical Characteristics	Early Failures	Long Term Reliability
Level 1 Known Good Die	Sampling specified on product spec.	All test items Assured [1]	Detection Assured	Assured ✔
Level 2 Known Tested Die	Sampling specified on product spec.	All test items Assured [1]	Not Assured	Not Assured
Level 3 Probed Die	Sampling specified on product spec.	Some tests Skipped [2]	Not assured	Not assured

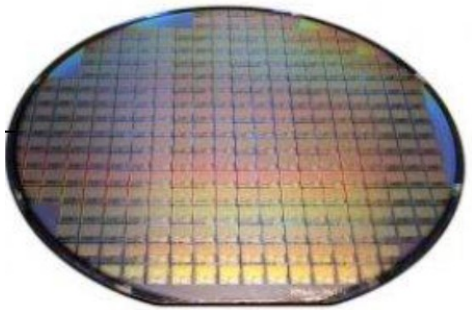
1Corresponding to the specified criteria for packaged products
2 The same criteria level as packaged products with burn-in

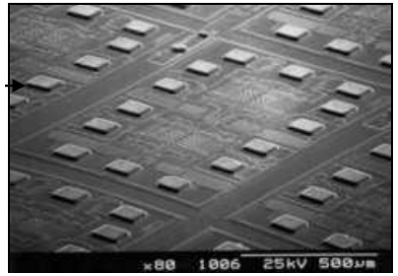
1 – IPC-7092

Die Interface Prep and Terminal Face-Down Assembly

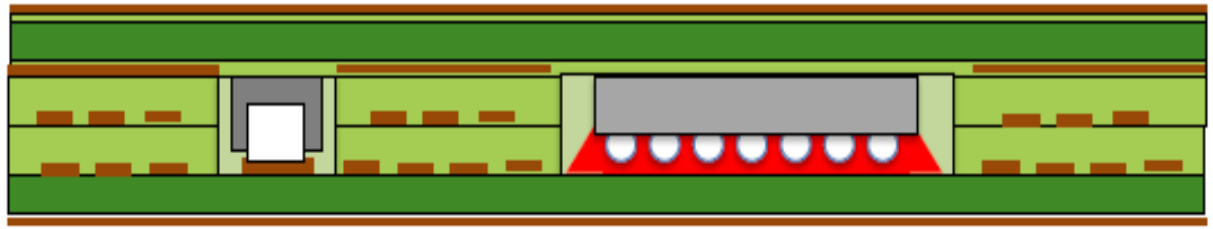
Semiconductor Interface Preparation

- Mounting the semiconductor (face-up or face-down) will require additional metallization processing while in the wafer format-
  - The aluminum bond sites must be over-plated with Cu.
  - A Cu redistribution layer (RDL) will be required for die elements having less than 100µm bond pitch.



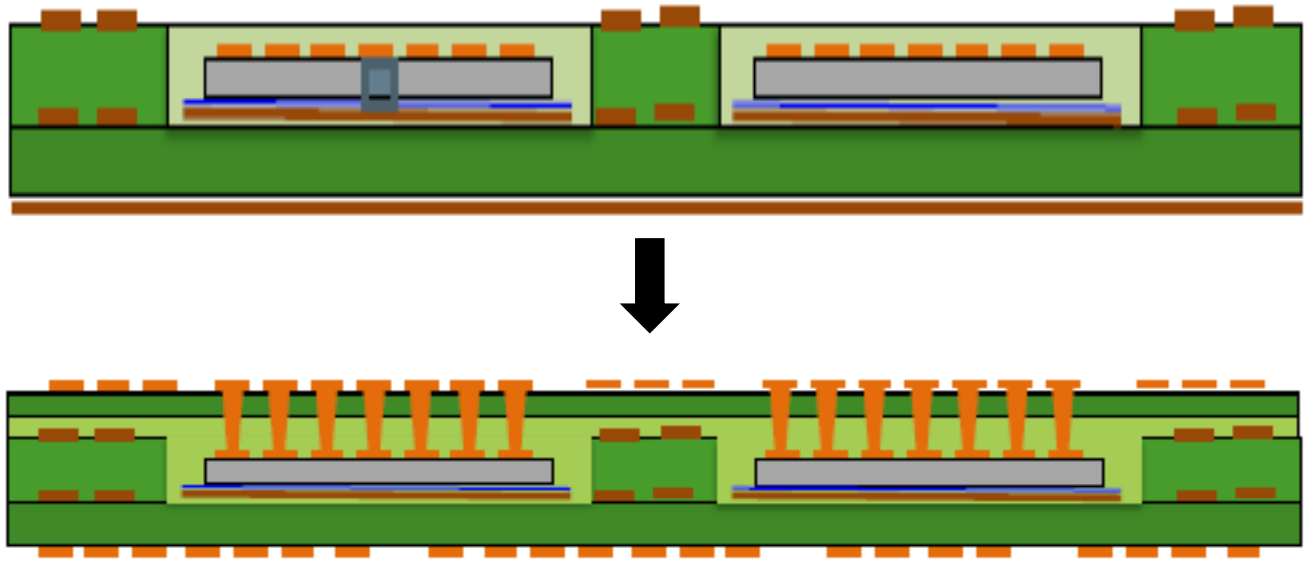


- Develop substrate with cavity feature to accommodate component thickness.
- Place component onto prepared land pattern features.
- Cure or reflow attachment material, clean, apply underfill and cure.
- Laminate cap layer to complete component encapsulation.

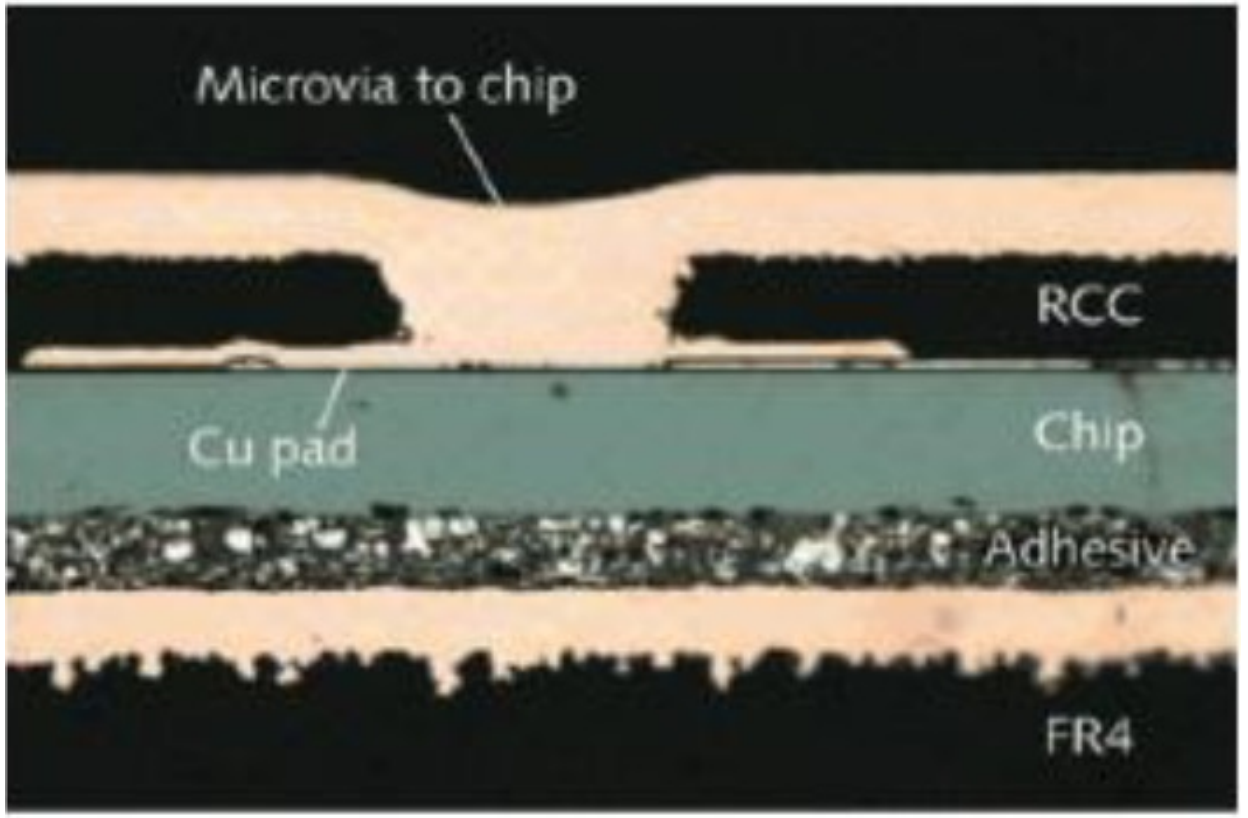


Terminal Face-Up Assembly

- Develop substrate with cavity feature to accommodate component thickness.
- Place component face-up onto prepared Cu pattern features.
- Cure attachment material and laminate cap layer to complete component encapsulation.
- Ablate vias at terminal sites and Cu plate to complete interface with upper layer circuit.



Via-to-Semiconductor Interface

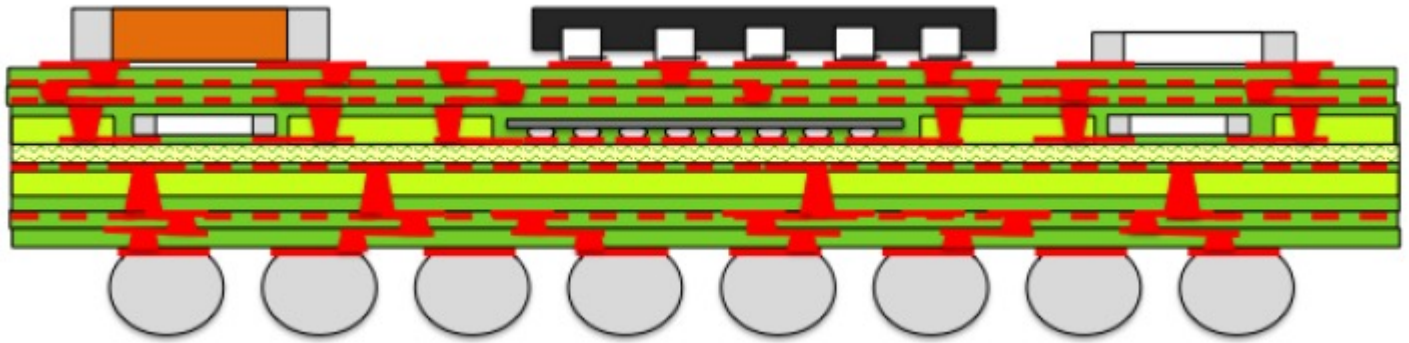


Example source: ASE Global

SMT/BGA Embedded Circuitry PCB Assembly Sequence

Surface mount assembly follows the sequential build-up and electrical test of the Embedded Circuitry PCB structure-

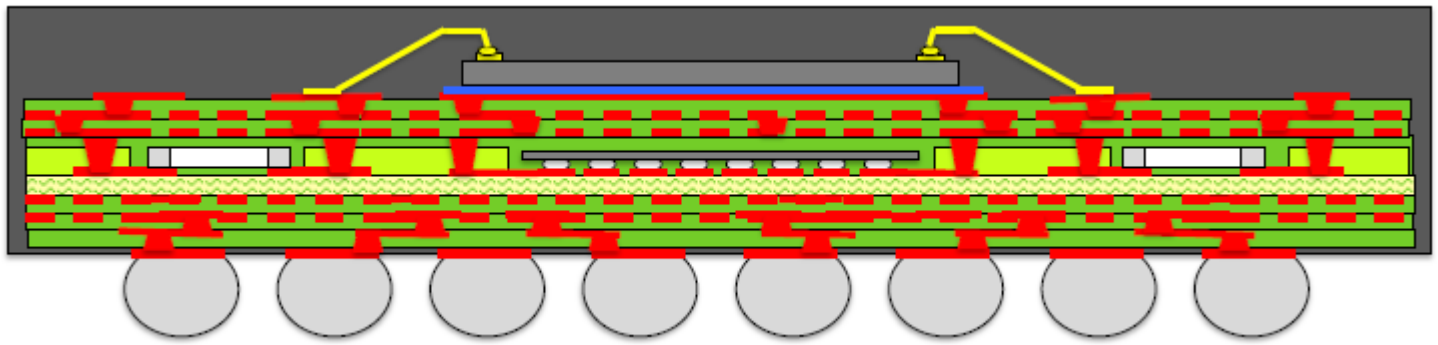
- Print solder paste onto land patterns on top surface.
- Place components onto lands, reflow solder, clean.
- Print tacky flux on array pattern on lower side of Embedded Circuitry PCB .
- Place alloy spheres onto flux, reflow solder, clean, test.



BGA/Microelectronic Assembly Sequence

Microelectronic assembly follows the sequential build-up and electrical test of the basic Embedded Circuitry PCB structure-

- Apply die attach film to top surface of structure.
- Place die element and perform wire-bond process.
- Encase wire-bonded die element with mold compound.
- Print tacky flux on array pattern on lower side of Embedded Circuitry PCB .
- Place alloy spheres onto flux, reflow solder, clean, test.



Positive Factors

Increase	Decrease
Number of printed boards fabricated on a panel due to decreased board size.	Printed board area can be smaller due to a reduction in the number of surface mounted passive components.
Surface mounted component density resulting in shorter coupling between devices.	Wiring density simplified due to the integration of resistors and bypass capacitors within the substrate.
Potential for higher second level assembly process yields	Reduction in overall assembly costs, solder process defects and rework

Negative Factors

Increase	Decrease
Greater printed board cost per unit area due to greater fabrication process complexity.	Printed board fabrication throughput may be impacted by process variables.
Higher wiring density requirements due to the reduced printed board area.	Lower printed board fabrication yield due to process related defects.

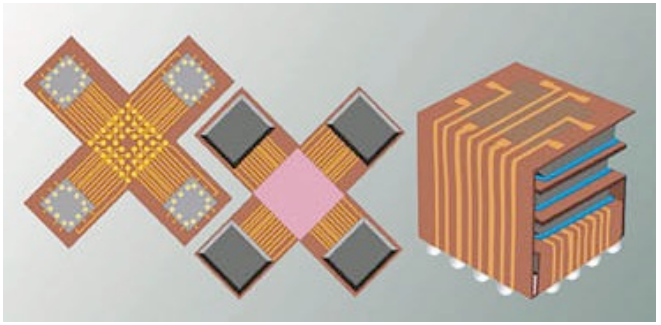
Summary

- Embedding both passive and active components is a mature process in the PCB industry.
- Although ‘formed’ resistor and capacitor processes are very mature, physical stability and wide tolerance range remain a concern.
- With the availability of smaller and thinner passive device outlines, there are some advantage for embedding discrete passive elements.
  - Less restrictive value selection.
  - Wide resistor and capacitor value range.
  - Acceptable tolerance and stability.
- Embedding the semiconductor element is where significant roadblocks exist.
  - Procurement of semiconductors in a wafer format.
  - Outsourcing wafer metallization and thinning.
  - Testing - what to test and features needed to enable testing etc.
- There is a need to develop partnerships between the two primary suppliers - the PCB fabricators and the embedded circuitry assembly service provider.

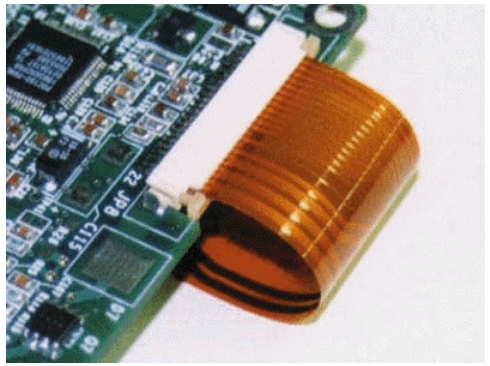
Flex and Rigid-Flex Circuits

- Flex Circuits are thin, lightweight, bendable signal traces built on flexible dielectric substrates. Flex circuit technology enables 3D configurations, smaller, lighter and faster products, and can lower total applied cost.

- Characteristics
  - Meet dynamic flexing requirements: active and passive components can be added directly to the flex.
  - Impedance control
  - EMI control



Chip to chip connection



Board to board connection

Types of Flex Circuits*

- **Type 1:** One conductive layer, either bonded between two insulating layers or uncovered on one side. (Stiffeners, pins, connectors, components, are optional).
- **Type 2**: Double sided, two conductive layers, PTHs, with or without stiffeners.
- **Type 3:** Multi-layer flexible, three or more conductive layers, PTHs, with or without stiffeners.
- **Type 4**: Multi-layer rigid and flex, three or more conductive layers, PTHs.
- **Type 5:** Flex or rigid-flex, two or more conductive layers, no PTHs.

*** - IPC-6013C- Multi-layer rigid and flex, three or more conductive layers, PTHs, Nov 2003.**

Flex, Rigid-Flex Circuits - Materials

Base Material

- Polyester
- Polyimide
- Polyethylene napthalate (PEN)
- Liquid crystal polymer
- Flouropolymers

*** - Flexible Circuit Technology, Third Edition, J. Fjelstad, BR Publishing Inc, Sept 2006**

Flex, Rigid Flex - Base Materials

Substrate Material	Dielectric Constant	Dissipation Factor	Dielectric Strength (v/mil)	**Moisture Absorption**	Tensile Strength (kpsi)	Elongation
FEP	2	0.0002	5000	**< 0.01%**	2-3 kpsi	~ 300%
PTFE	2.5	0.0002	5000	**< 0.01%**	15- 25 kpsi	N/A
Polyester	3.2	0.005	7000	**< 0.08%**	25 kpsi	~ 120%
LCP	2.9	0.003	6000	**0.02 - 0.1%**	15-25 kpsi	~ 15%
PVC	4.7	0.093	500	**< 0.5%**	5 kpsi	~ 120-500%
Polyimide	3.5	0.003	7000	**1.3 – 3%**	25 kpsi	~ 60%
PEN	2.9	0.004	7500	**1%**	30-35 kpsi	~ 75%
Aramid Paper	2	0.007	380	**3%**	11 kpsi	~ 10%

Flex, Rigid-Flex Circuits - Materials

Bonding Adhesives

- Polyester
- Acrylic
- Epoxy
- Polyimide
- Butyl phenolic
- Polythermides

Flex, Rigid Flex - Adhesive Materials

Adhesive Type	Peel Strength (post-solder) N/mm	Adhesive Flow mils/mil	**Moisture Absorption max %**	Surface Resistivity min M W	Dissipation Factor @1MHz	Dielectric Constant @1 MHz
PTFE	> 1 N/mm	125 mm max	**0.01**	1012	0.0007	2.2 nom
Polyester		250 mm max	**2**	104	0.02	4.0 max
Butyral-Phenolic	1.0 N/mm	125 mm max	**2**	104	0.025	3.0 max
Polyimide	1.0 N/mm	125 mm max	**3**	105	0.01	4.0 max
Epoxy	1.4 N/mm	125 mm max	**4**	104	0.06	4.0 max
Acrylic	1.6 N/mm	125 mm max	**6**	107	0.02	3.5 nom

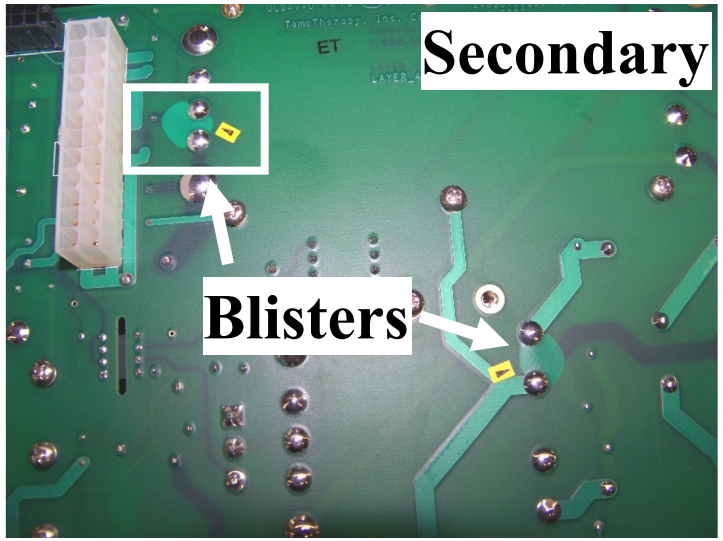
Flex, Rigid-Flex Circuits - Materials

Conductors

- Copper foil or electrodeposited
- Annealed copper
- Electroplated copper
- Sputter deposited copper
- –Aluminum
- –Stainless steel
- –Beryllium copper
- –Polymer thick film

Case Study and Discussion

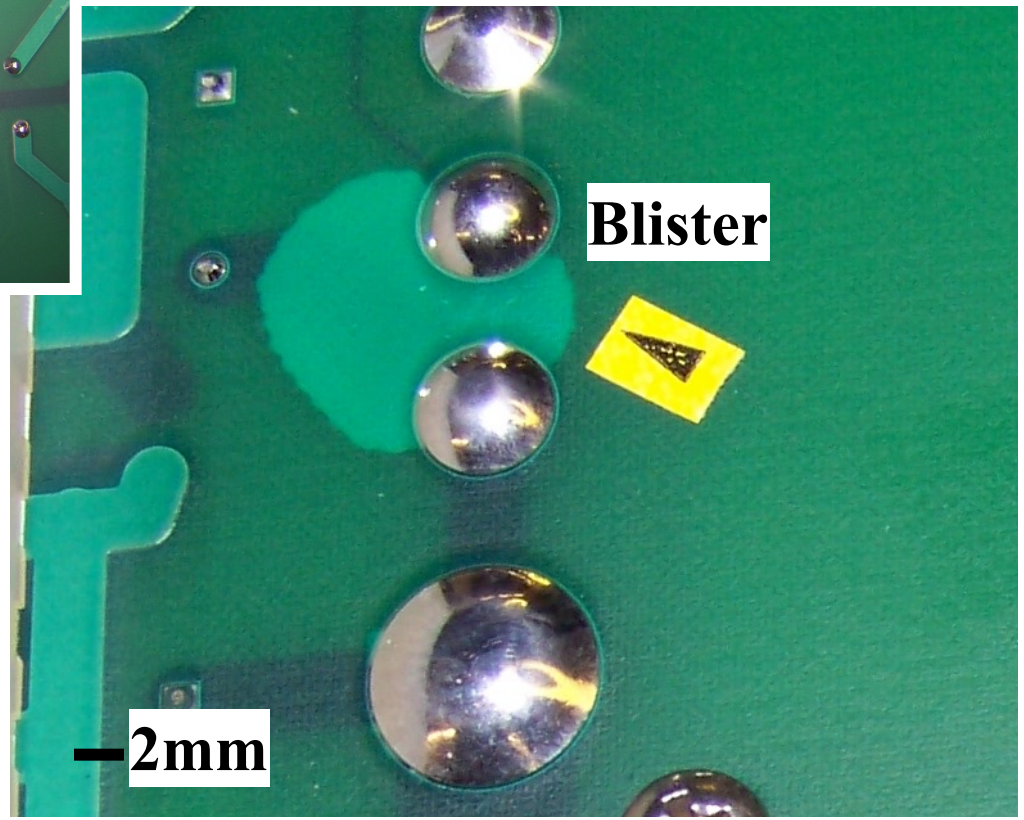
Blistering



IPC-A-600 Section 3.1.4, Class 3:

- **Target – no blisters**
- **Acceptable**
  - **Max two per side**
  - **Not exceeding 0.25mm**
- **Nonconforming**
  - **More than two per side**
  - **Larger than 0.25mm**

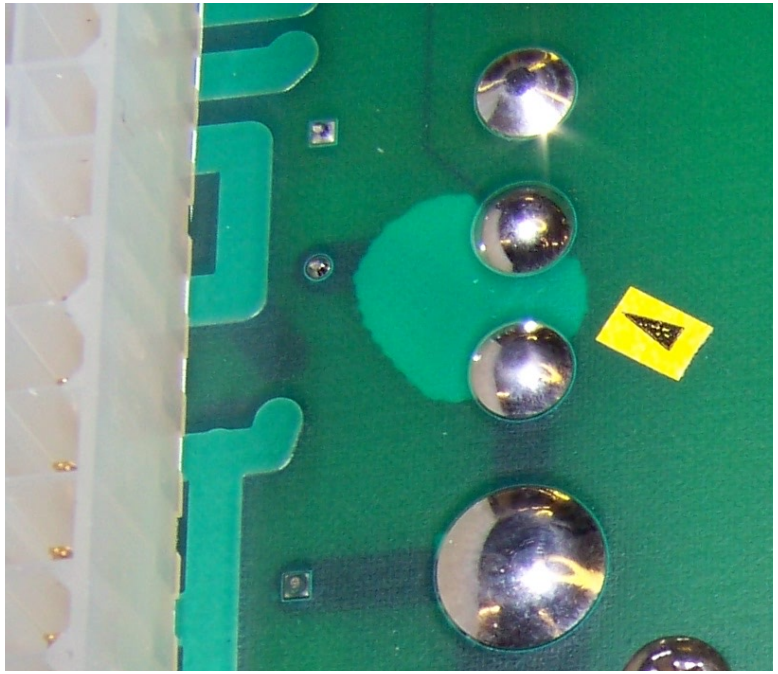
Blistering [1]



1 – Eric Their

Blistering

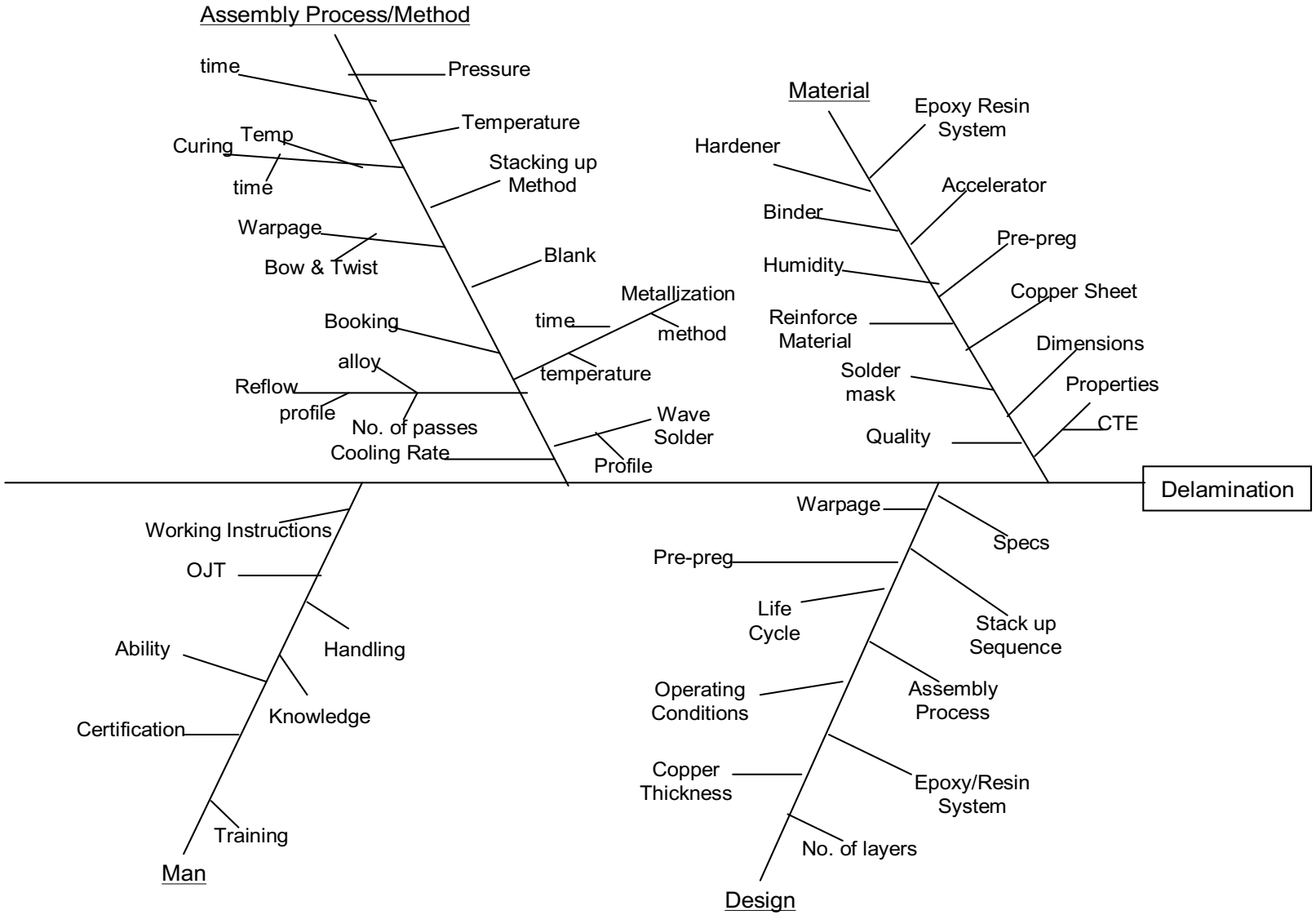
- Absence of, or poor hole wall treatment
- Poor drill tool quality
- Incompletely cured laminate
- Improper PCB storage or handling.
- Excessive copper plating rates during PTH wall plating



Blistering [1]

1 – Eric Their

Fishbone – Delamination



Delamination

- Multilayer boards are a stack up composite system
- Bonding strength depends on the strength of the thermo set material
  - Which in turn is a function of the thermo-mechanical properties such as Tg, CTE, and stiffness
- Bonding capacity will also depend upon
  - Curing time
  - Temperature
  - Presence and efficiency of the accelerators, binders, and catalyst in the epoxy system
- Failure to hold the stacked layers in the out of plane “z” direction results in delamination

Section - 3

Failure Mechanisms in PCBs and PCBAs

Review: Failure Definitions

Failure	A product no longer performs the function for which it was intended
Failure Mode	The effect by which a failure is observed.
Failure Site	The location of the failure.
Failure Mechanism	**The physical, chemical, thermodynamic or other process that results in failure.**

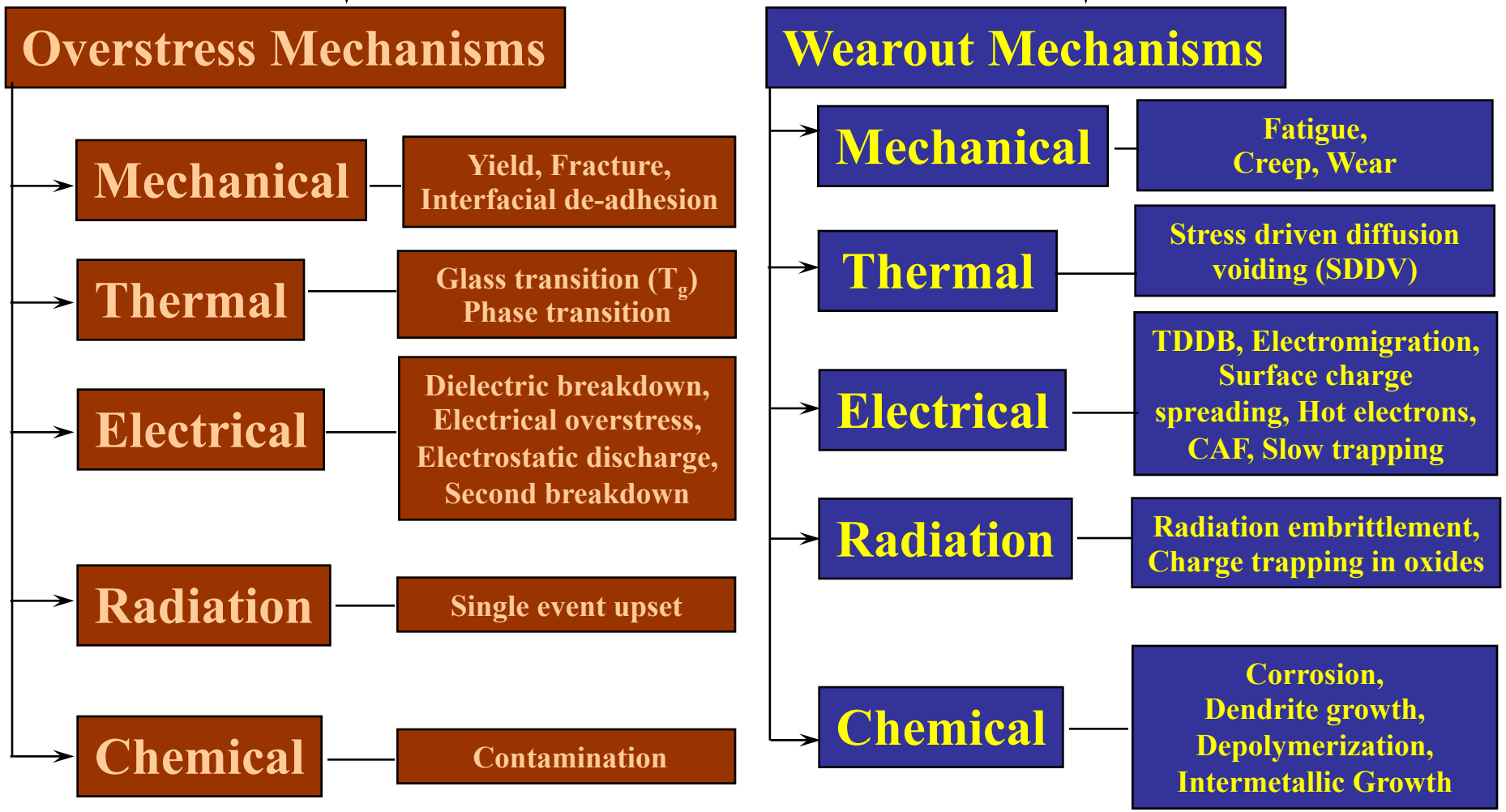
In principle, it should be possible to develop a **failure model** for a specific failure mechanism, expressing the likelihood of failure (time-to-failure, probability of failure, strength, etc.) as a function of the stresses and characteristics of the material.

Review: Classification of Failures

Key classes of failure:

- ***overstress*:** use conditions exceed strength of materials; often sudden and catastrophic
- ***wearout*:** accumulation of damage with extended usage or repeated stress
- *infant mortality*: failures early in expected life; typically related to quality issues.

Some Common Failure Mechanisms

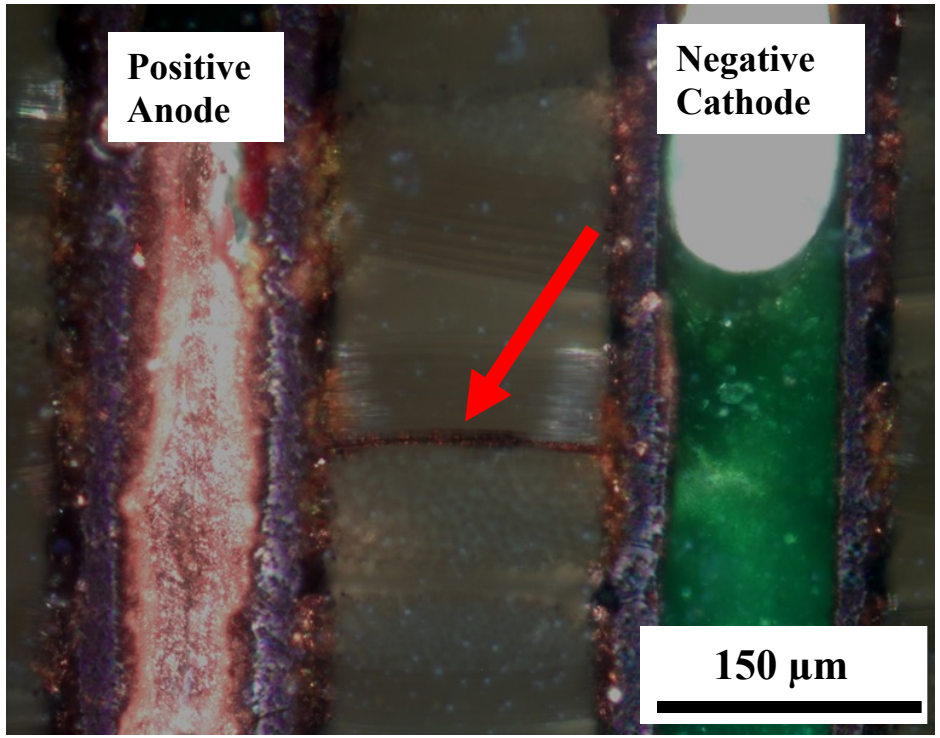


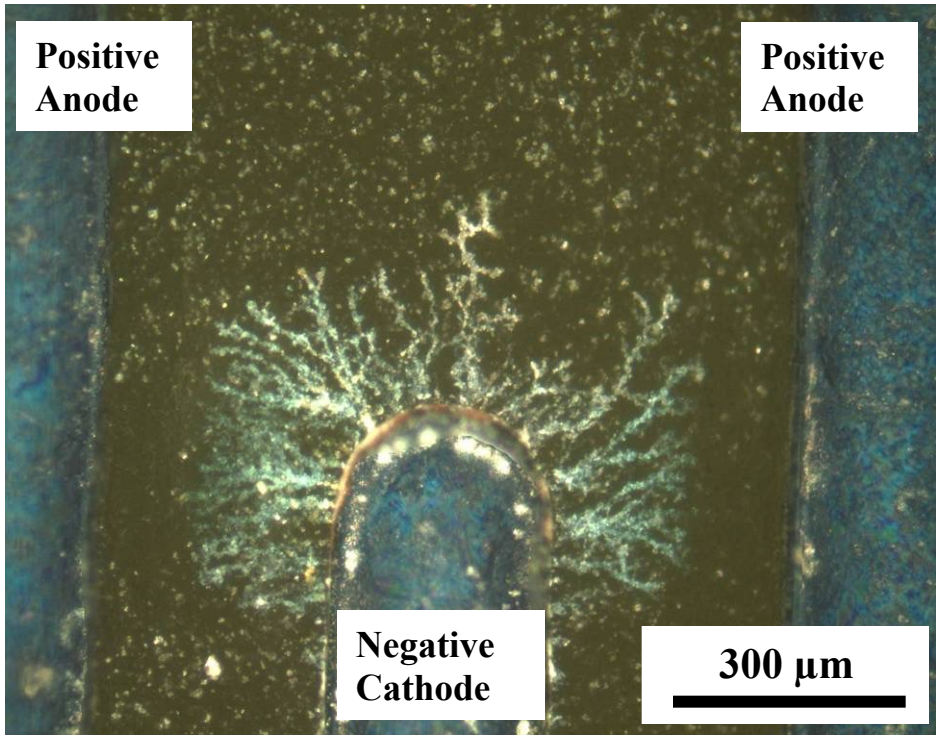
Examples of Failure Models

Failure Mechanism	Failure Sites	Relevant Stresses	Sample Model
Fatigue	Die attach, Wirebond/TAB, Solder leads, Bond pads, Traces, Vias/PTHs, Interfaces	Cyclic Deformations (Δ T, Δ H, Δ V)	Nonlinear Power Law (Coffin-Manson)
Corrosion	Metallizations	M, ΔV, T, chemical	Eyring (Howard)
Electromigration	Metallizations	T, J	Eyring (Black)
Conductive Anodic Filament Formation	Between Metallizations	M, ΛV	Power Law (Rudra)
Stress Driven Diffusion Voiding	Metal Traces	σ, T	Eyring (Okabayashi)
Time Dependent Dielectric Breakdown	Dielectric layers	V, T	Arrhenius (Fowler-Nordheim)

Δ:	Cyclic range	V:	Voltage
Λ:	gradient	M:	Moisture
T:	Temperature	J:	Current density
H:	Humidity	σ:	Stress

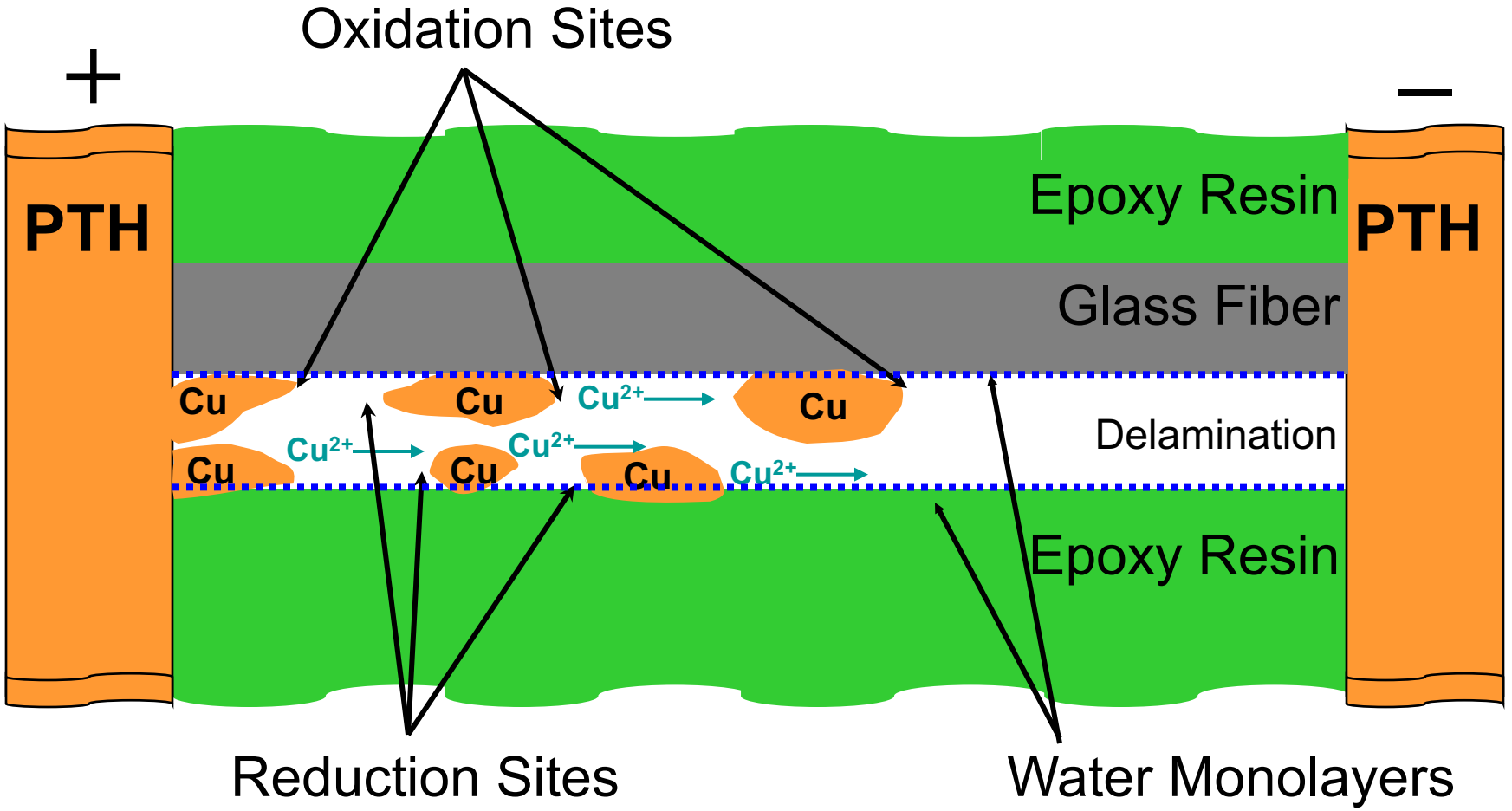
ECM: Surface and Sub-surface Mechanisms





ECM	Conductive Anodic Filament (CAF)	Dendritic Growth
Growth Direction	Anode to cathode	Cathode to anode
Filament Composition	Metallic salt	Pure metal
Growth Position	Internal	Surface

Formation of Conductive Filaments [1] [2]

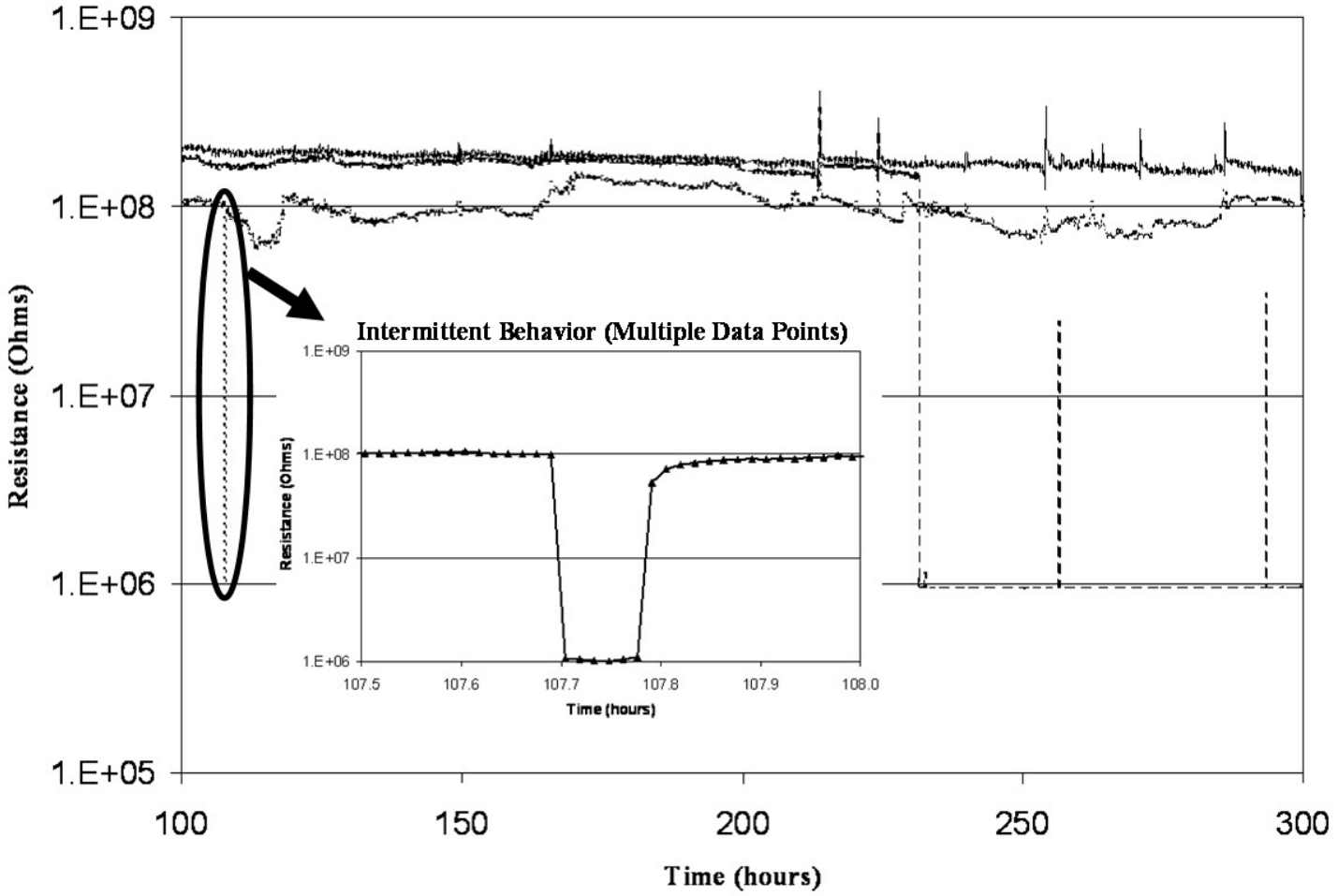


Factors that influence CAF include conductor spacing, hollow fibers, drill defects, poor epoxy wet-out, bias, moisture and ion concentration.

1.Rogers, K., "An Analytical and Experimental Investigation of Filament Formation in Glass/Epoxy Composites." (2005).

2.Sood, B., and Pecht M., "Conductive filament formation in printed circuit boards: effects of reflow conditions and flame retardants." Journal of Materials Science: Materials in Electronics 22.10 (2011): 1602-1615.

PTH-PTH (6 mil) 10V, 85°C/85% RH



Factors

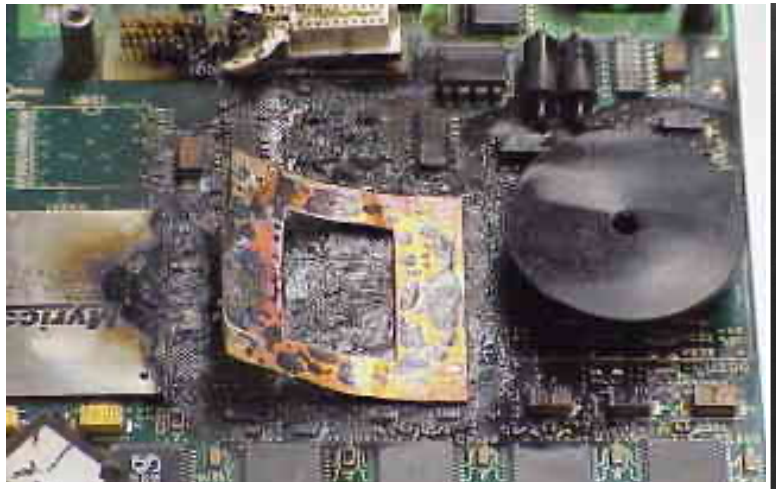
- Voltage
- Moisture
- Conductor spacing
- Ion concentration in epoxy resin

Defects

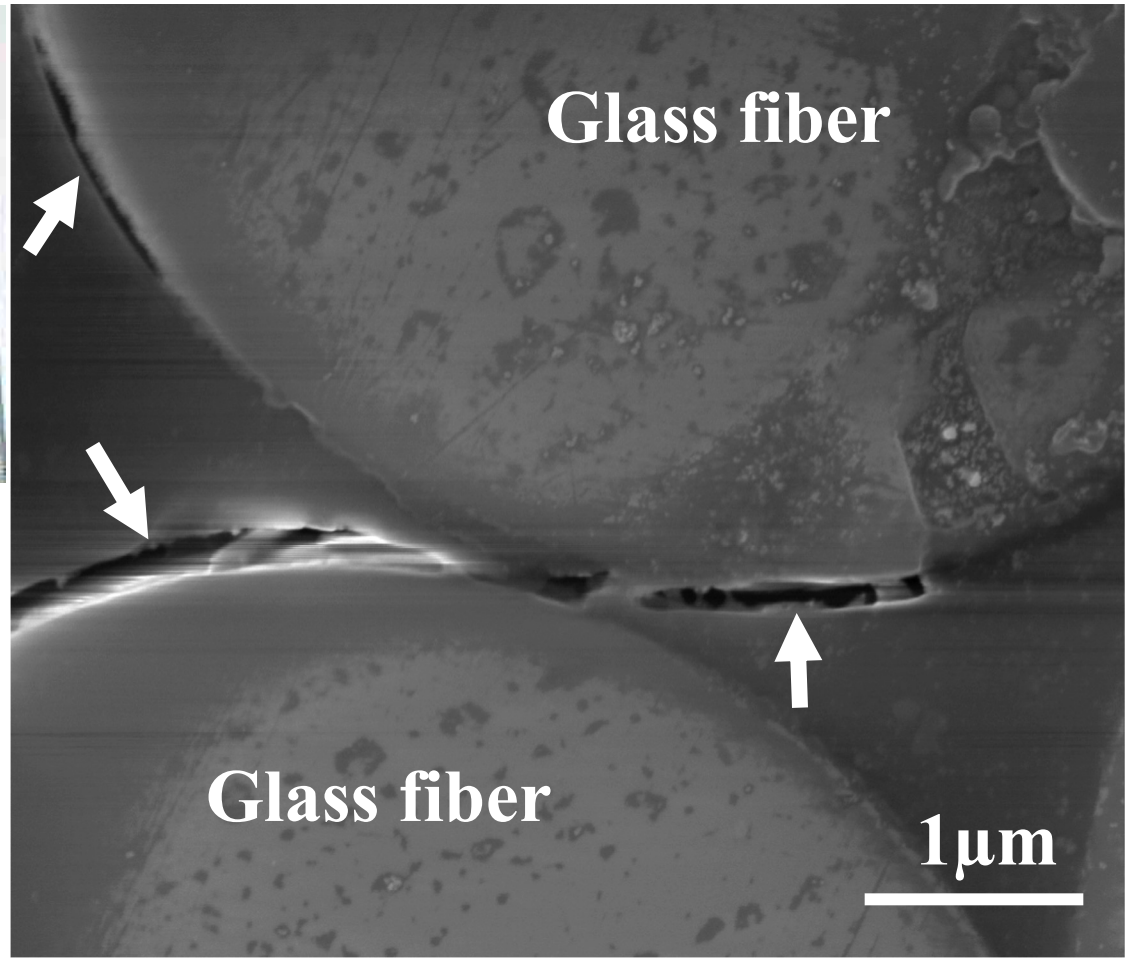
- Fiber/resin separation
- Hollow fibers
- Misregistration
- Wicking
- Drilling damage
- Poor wetout

Importance of the Epoxy/Glass Interface

Path formation for CAF is often along the glass fiber to epoxy matrix interphase (this step is eliminated with hollow glass fibers).



Example of CAF Failure



Fiber/resin interphase delamination occurs due to CTE mismatches (shear) or bond degradation.

Glass Fibers and Coupling Agents

Coupling agents are functionally graded materials that act as adhesion promoters. [1] [2] [3]

- Coupling agents are typically composed of antistats, lubricant, surfactant, silanes and film formers (collectively also called sizing).
- Silane act as molecular bridges between two chemically different materials (glass and epoxy matrix).
- Prior to application of coupling agents, fibers are first heat cleaned at 538C to remove oil coats.
- Organo-functional group bonds to the organic resin.
- Inorganic groups bond to the glass surface.

1.Mishra, Debasmita, and Alok Satapathy. "An Investigation on The Dielectric Properties of Epoxy Filled With Glass Micro-Spheres and Boron Nitride." (2012)

2.Mack, H. "Choosing the Right Silane Adhesion Promoters for SMP Sealants," Adhesive and Sealant Council Meeting, Orlando, Fl, Spring 2001.

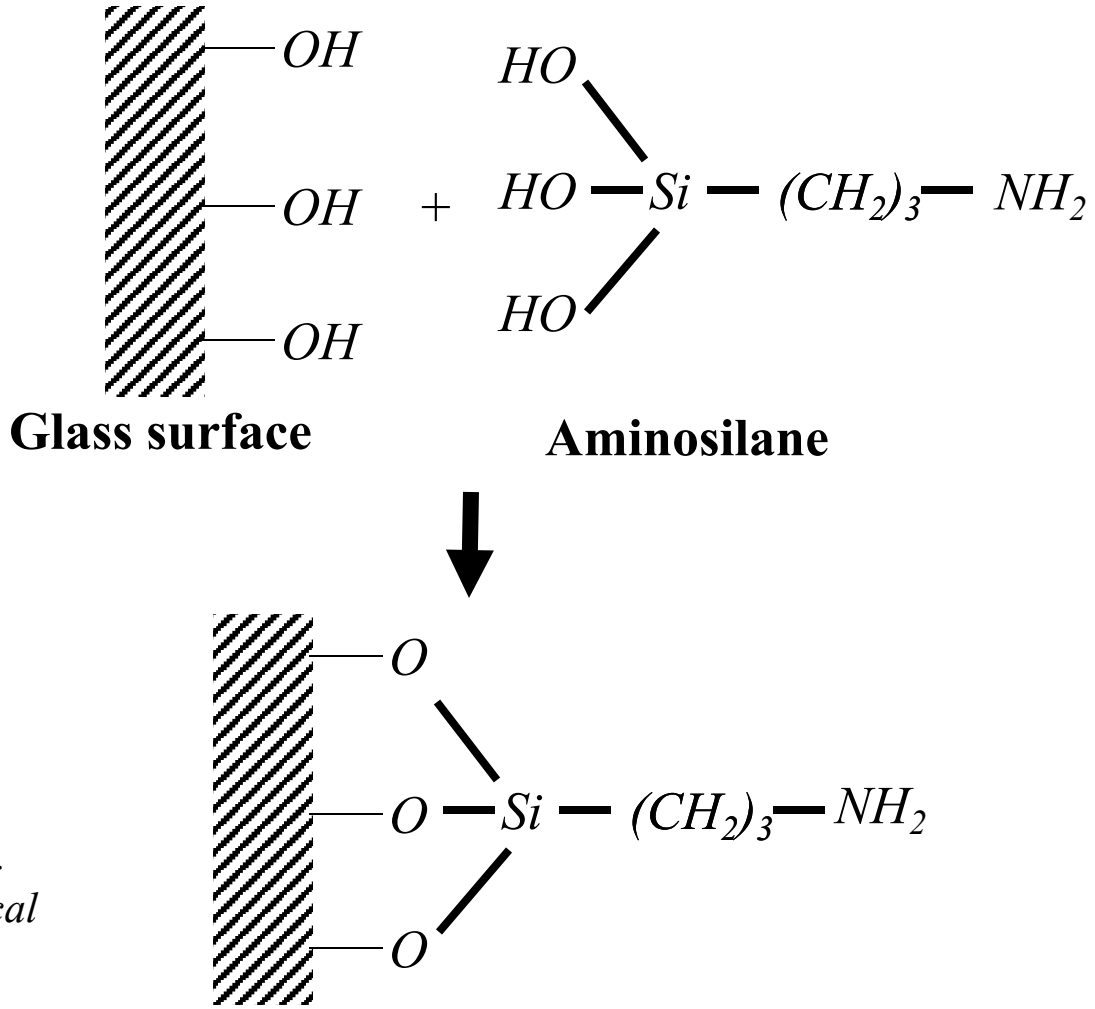
3.Gelorme, Jeffrey Donald, and Joseph Kuczynski. "Silane Coupling Agents for Printed Circuit Boards." U.S. Patent Application 12/694,005.

Coupling Agents Used in FR4

Dow Corning, BGF, Gelest are key suppliers.

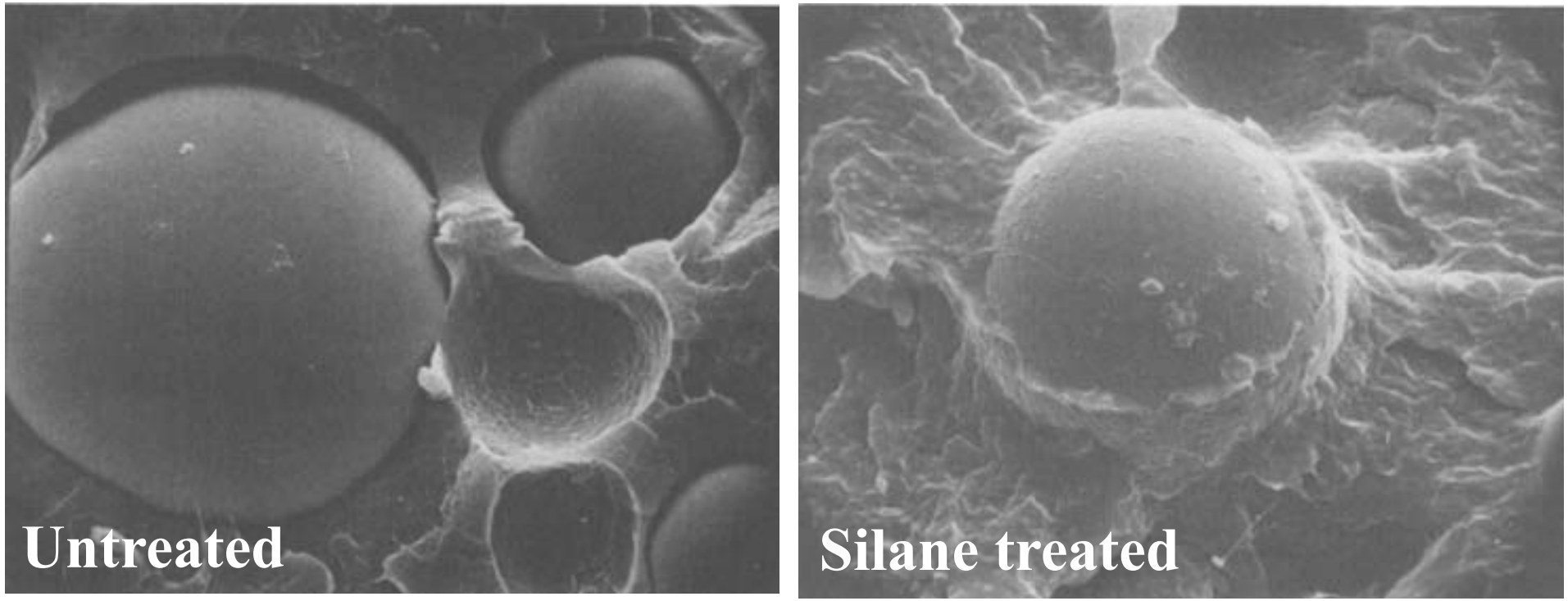
Main silane types are:

- Aminosilanes
- Epoxy Silanes
- Vinyl Silanes
- Methacryl Silanes
- Alkylsilane
- Phenyl Silane
- Chlorosilane



Mittal, Kashmiri Lal, and Antonio Pizzi, eds. Adhesion promotion techniques: technological applications. CRC Press, 1999.

Visualizing the Effects of Coupling Agents

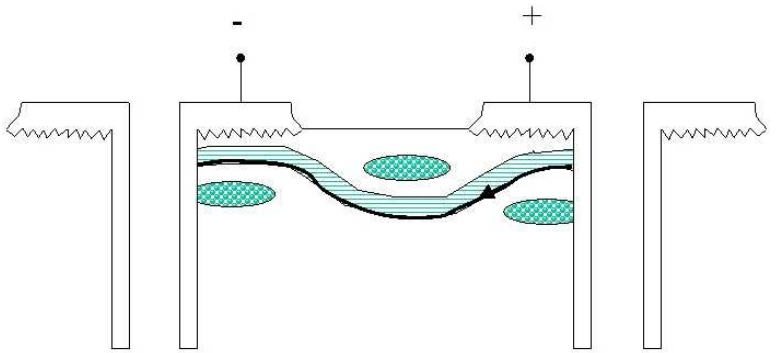


SEM images of fracture surfaces shows silane treated and untreated fillers [1] in a polyimide composite.

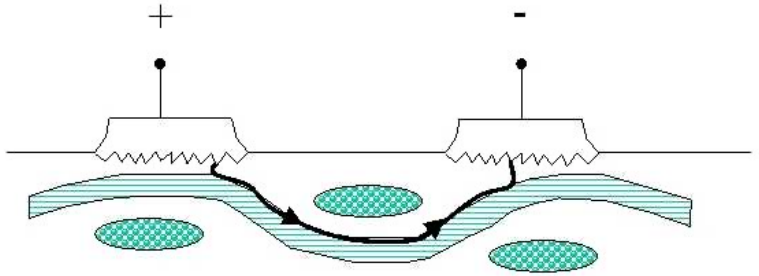
1. *Vanderbilt Minerals, Product Information Document, accessed April 2014.*

CFF Paths

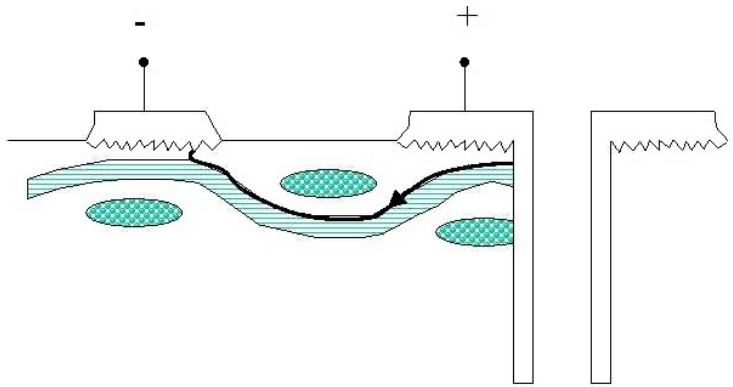
A. Between two plated-through holes (PTHs)



B. Between two traces

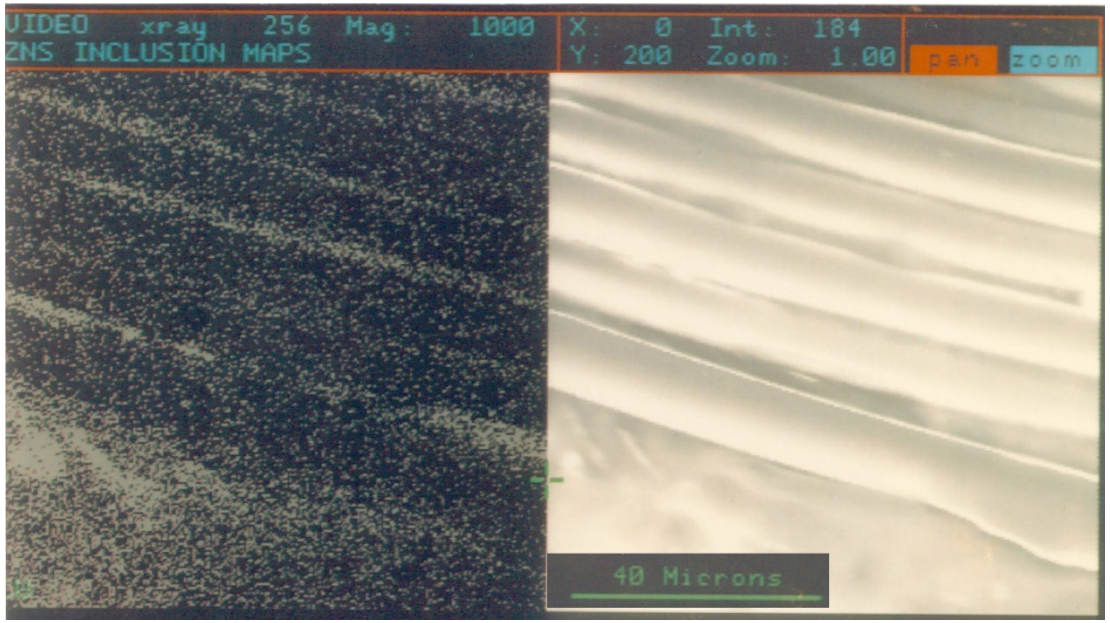


C. Between a trace and a plated-through hole (PTH)



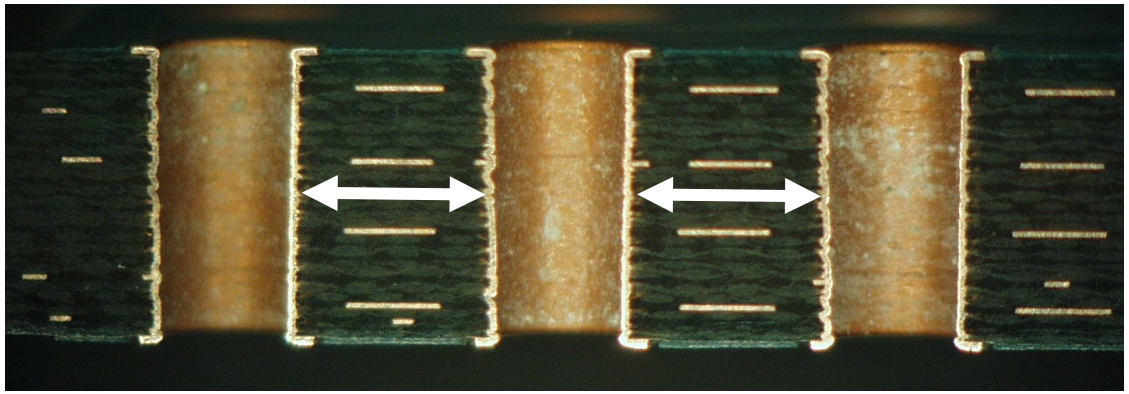
Evidence of Filament Formation

X-ray Map of Cu

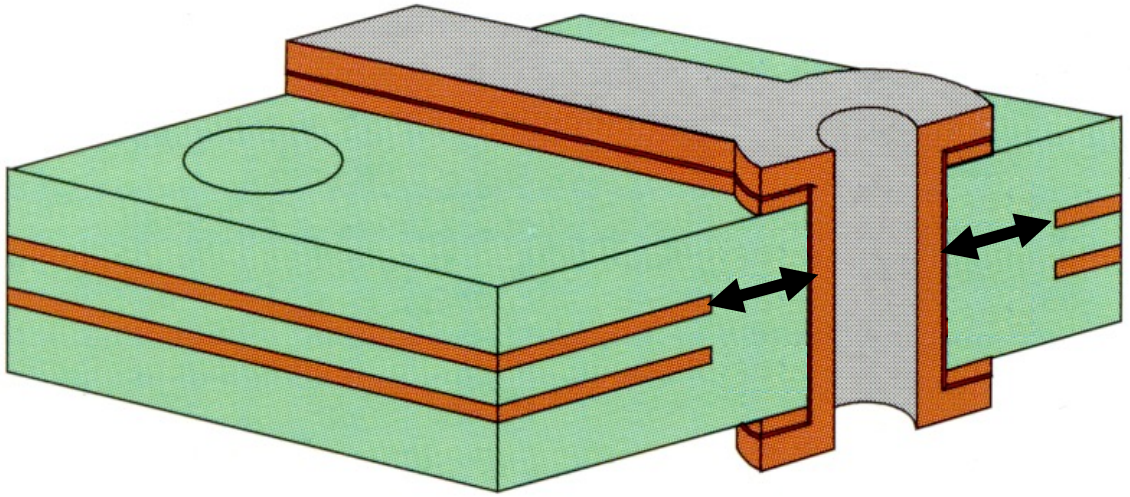


Electron micrograph of area of fiber/resin delamination. EDS shows evidence of copper filaments.

Factors Affecting CAF: PCB Internal Conductor Spacings

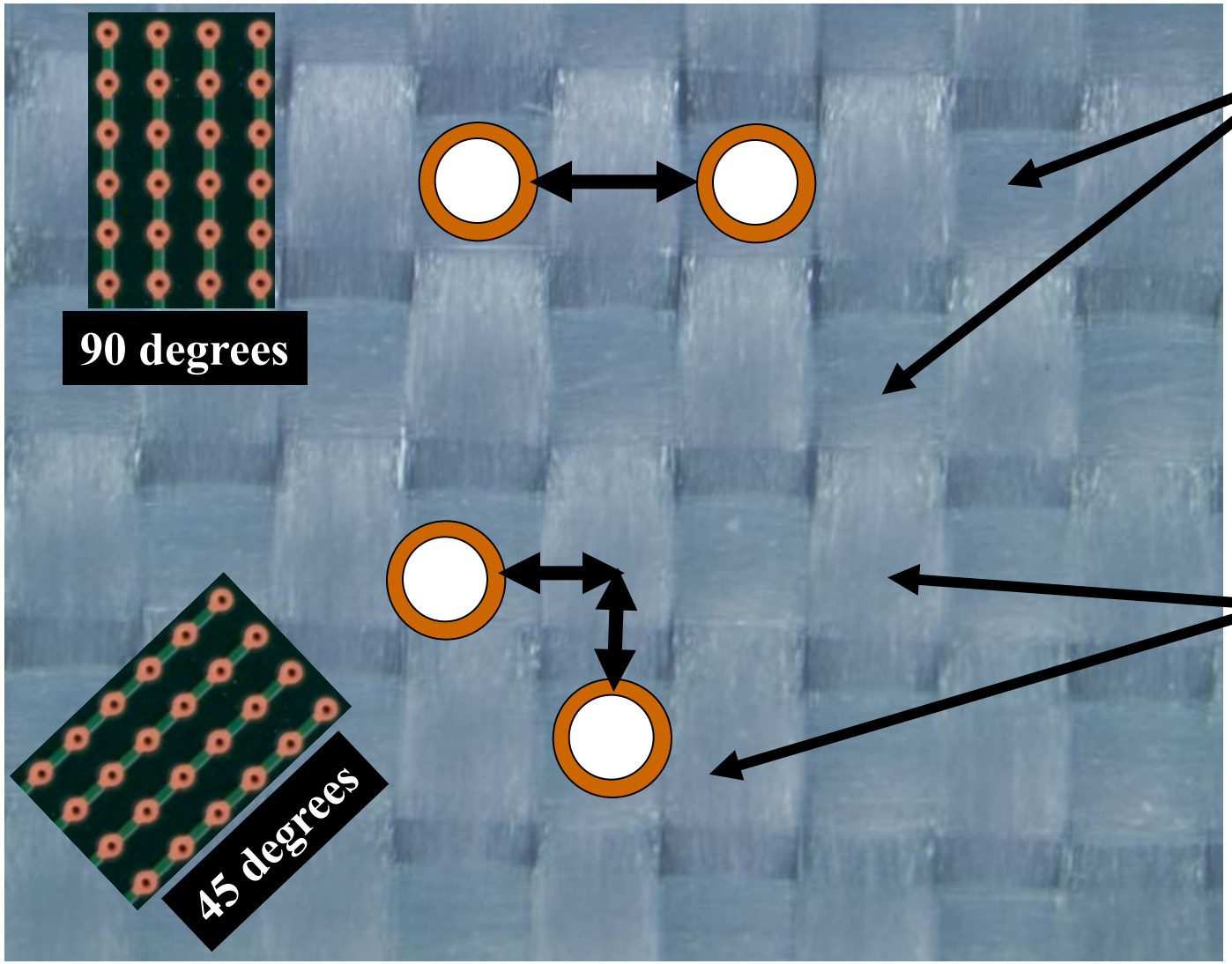


PTH-to-PTH spacings



PTH to plane spacings

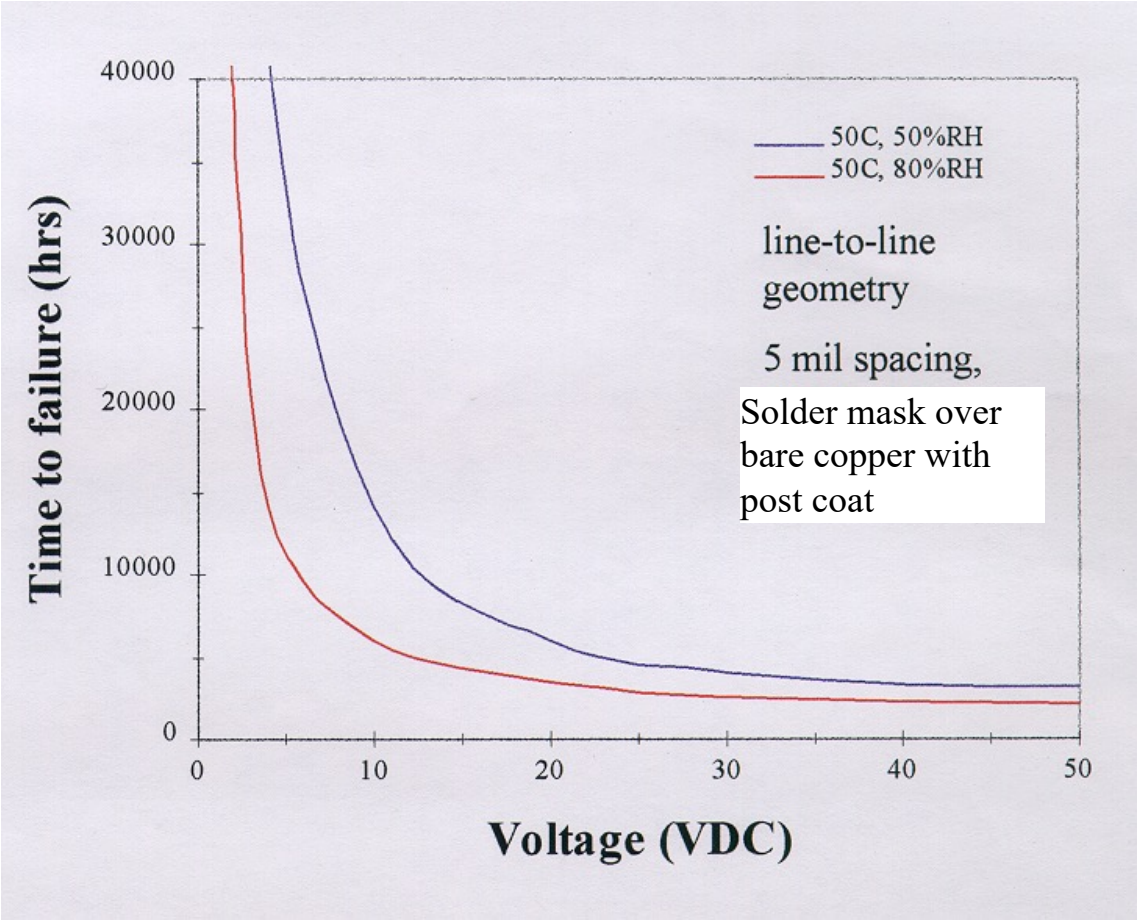
Factors Affecting CAF:
Board Orientation Respective to Fabric Weave



The initial set of parallel fiber bundles is known as the warp, and lie in the machine direction

A second set of parallel fiber bundles known as the fill or weft, is woven through the first set

Effect of Voltage and Humidity on Time to Failure



Failure Accelerators of CAF

Decrease in Strength

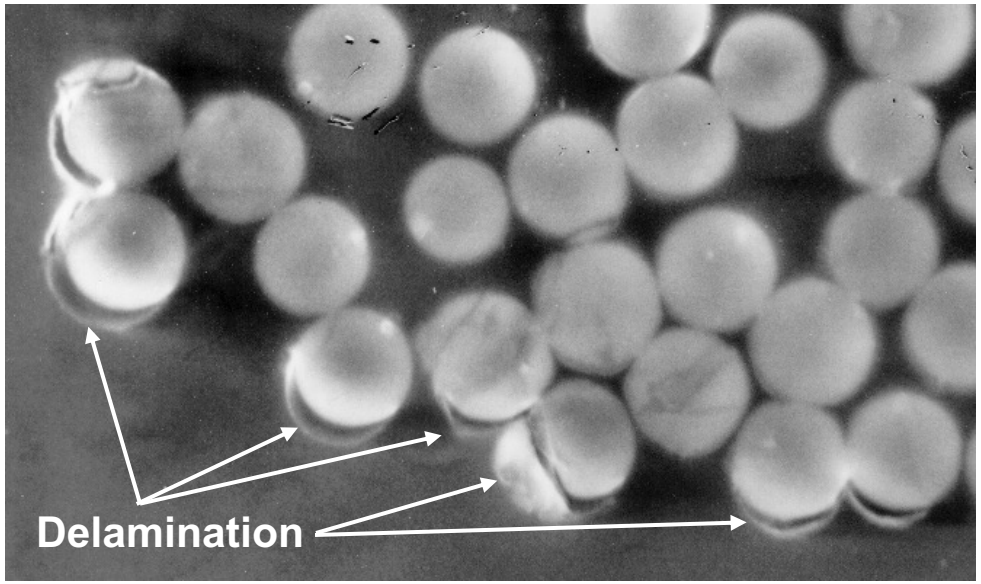
- Fiber/resin separation
- Copper/resin separation
- Hollow fibers
- Misregistration of PTHs/Vias
- Copper wicking
- Drilling damage
- Separation of PTH wall from epoxy resin

Increase in Stress

- Higher voltage
- Higher moisture concentration
- Tighter conductor spacing
- Higher ion concentration in epoxy resin

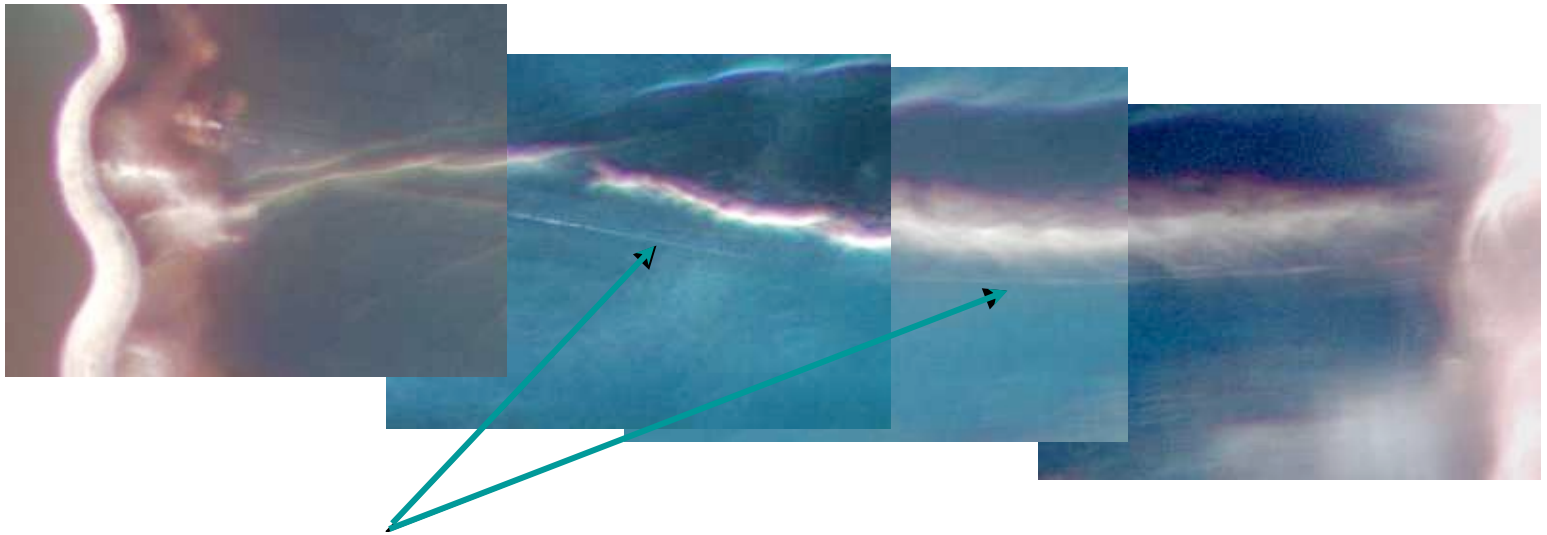
Fiber/Resin Interface Delamination

Fiber/resin interface delamination occurs as a result of stresses generated under thermal cycling due to a large CTE mismatch between the glass fiber and the epoxy resin (ratio of 1 to 12).



Delamination can be prevented/resisted by selecting resin with lower CTE's and optimizing the glass surface finish. Studies have shown that the bond between fiber and resin is strongly dependent upon the fiber finish.

Hollow Fibers



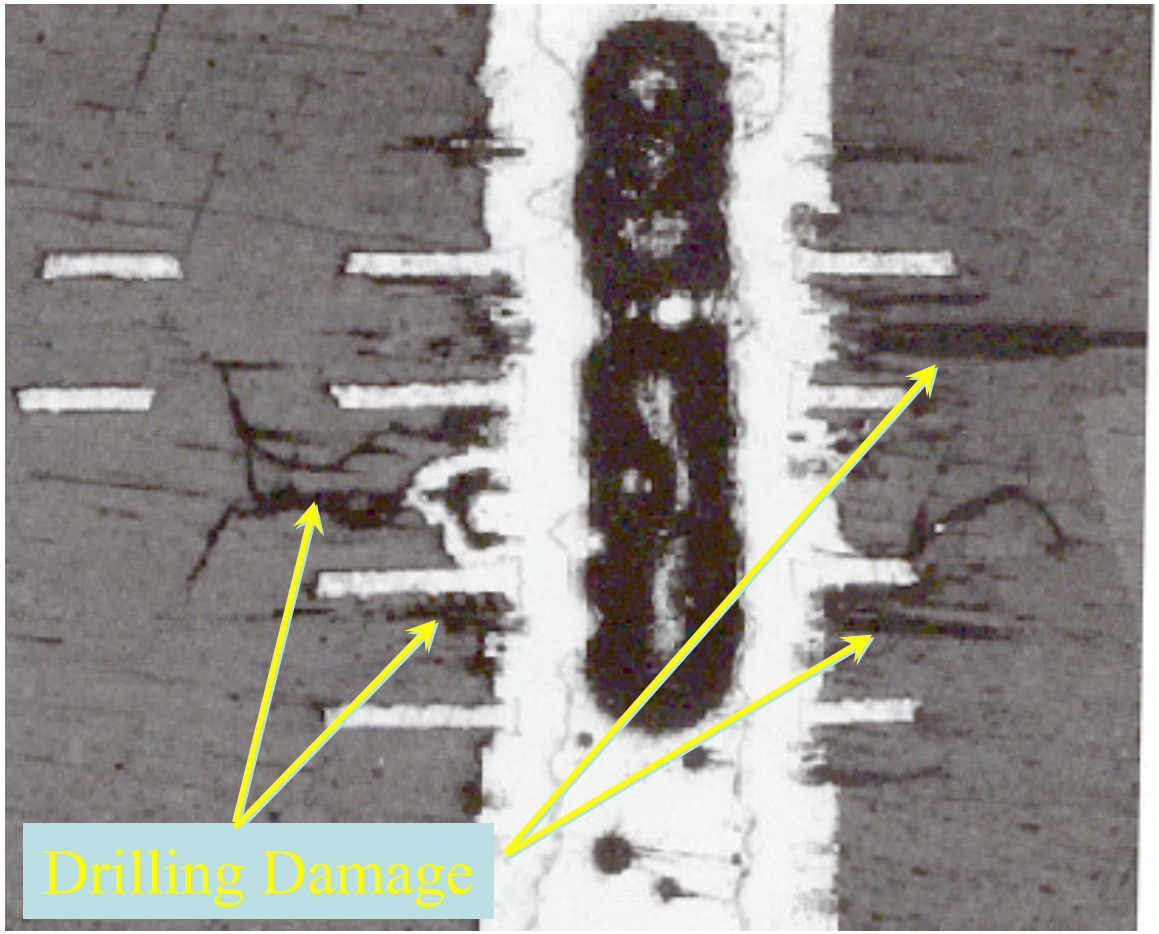
Hollow fibers are vacuous glass filaments in E-glass laminates which can provide paths for CAF.

With the appearance of hollow fibers inside the laminates, CAF can happen as a one step process. In this case, the number of hollow fibers inside the laminates is most critical to reliability.

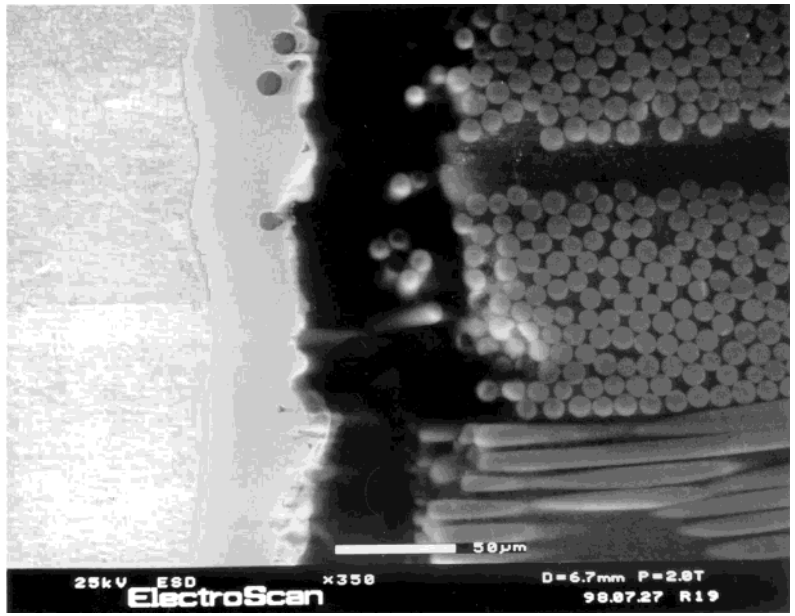
Drilling

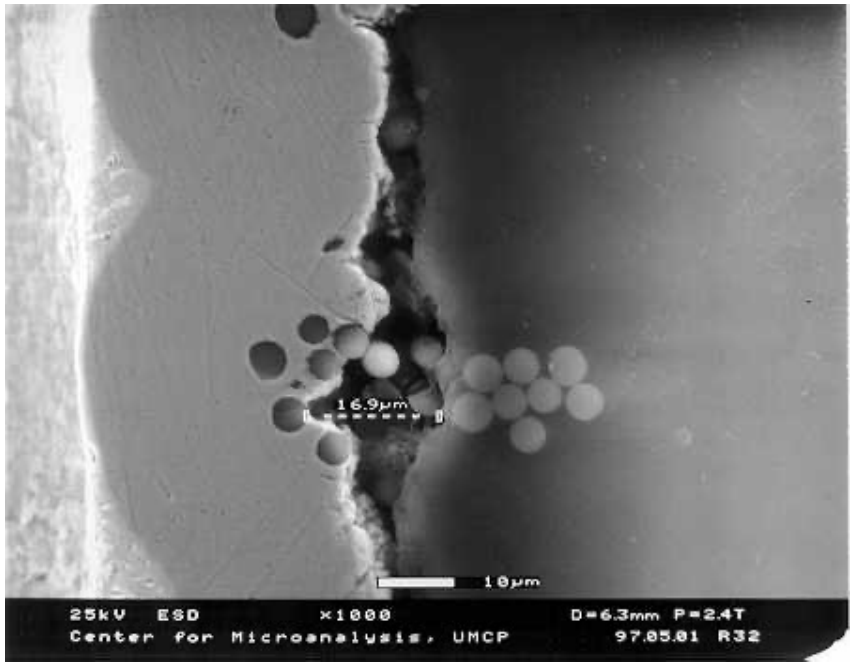
Drilling damage can accelerate CAF through

- Fiber/resin delamination,
- Creation of paths for moisture to accumulate
- Wicking due to cracking of the board material



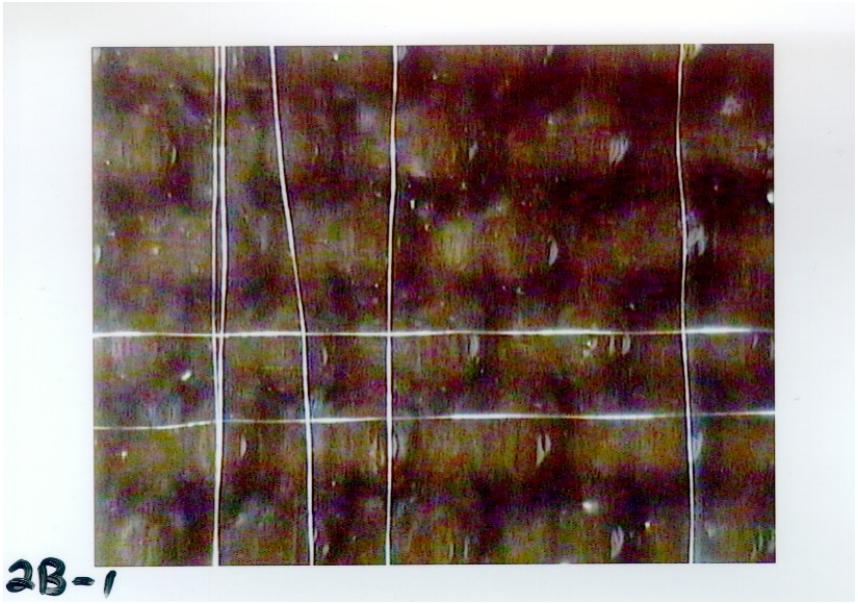
PTH-Resin Separation

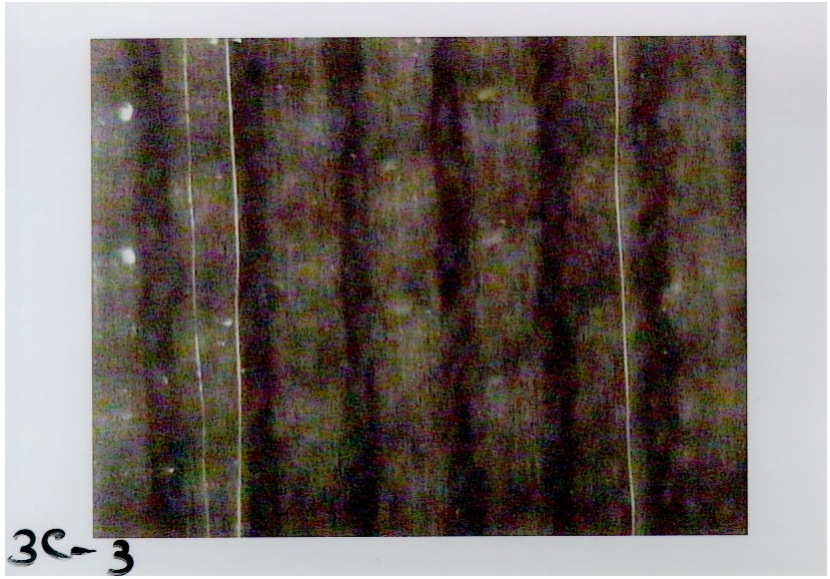




In both of these SEM pictures, a separation can be seen at the copper plating to fiber epoxy resin board interface. These gaps provide an accessible path for moisture to accumulate and CAF to initiate. These voids can be adjacent to inner-layer copper foil or to the PTH barrel and normally result from contraction of the epoxy (resin recession) due to the heat of thermal stress.

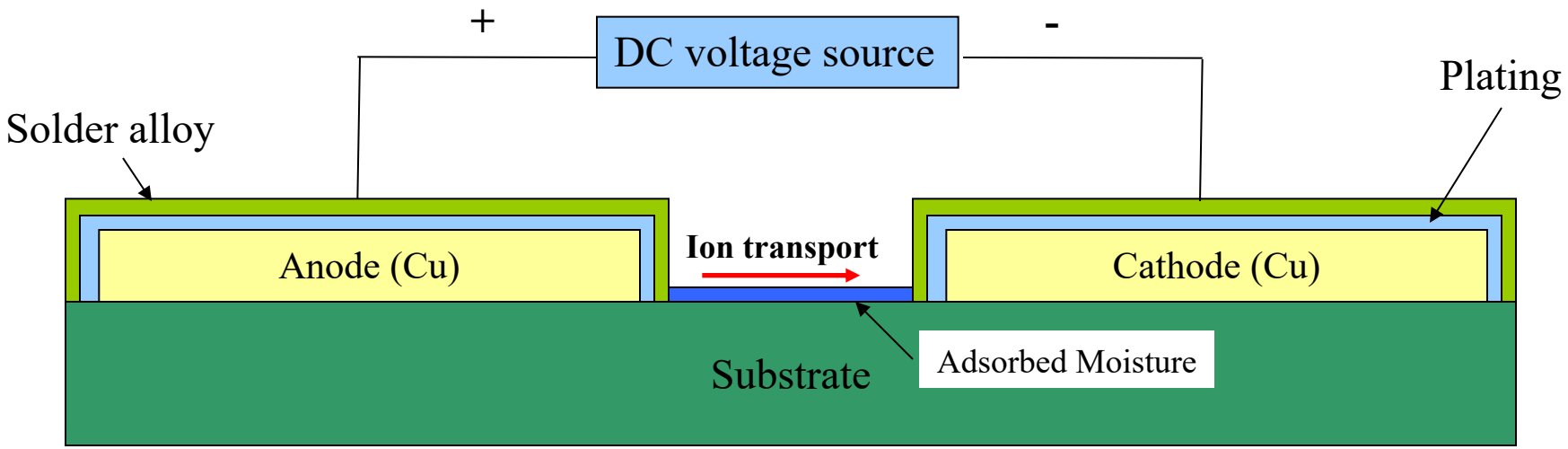
Images of Hollow Fibers





Background on Dendritic Growth

Dendritic Growth is a form of electrochemical migration (ECM) involving the growth of conductive filaments on or in a printed circuit board (PCB) under the influence of a DC voltage bias. [IPC-TR-476A]



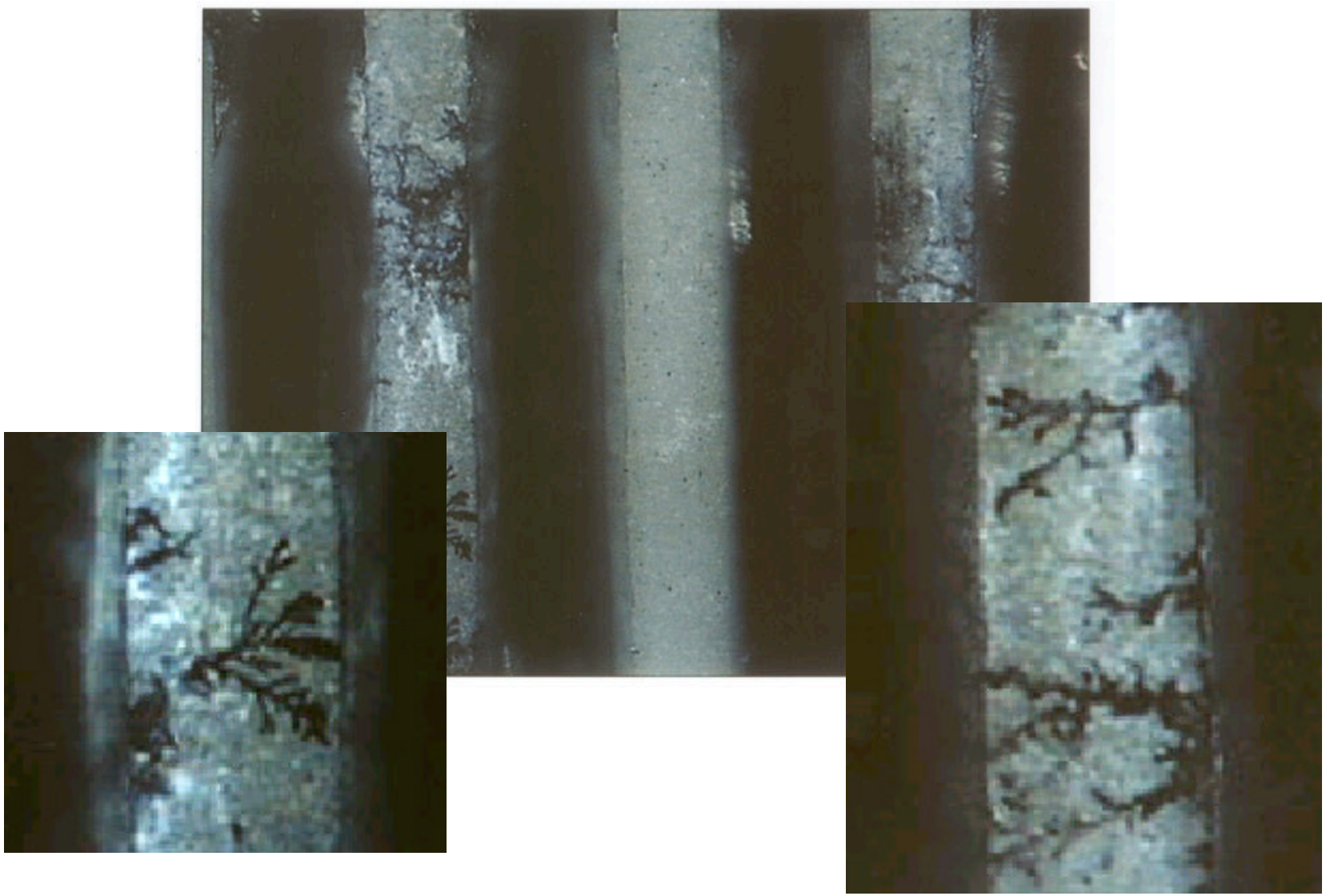
Necessary Conditions for ECM

- Electrical carriers (ions).
- A medium, usually water, to dissolve the ionic materials and sustain them in their mobile ionic state.
- Electrical potential between the electrodes to establish an ionic current in the liquid medium.

Stages of ECM

- Path formation
- Electrodissolution
- Ion transport
- Electrodeposition
- Filament growth

Electrochemical Migration



Contaminants

- Halide residues, such as chlorides and bromides, are the most common accelerators of dendritic growth.
- Chlorides are more detrimental, but easier to clean
- Bromides can resist cleaning; often require DI water with saponifier
- In general, an increased risk of ECM will tend to occur once the levels of chloride exceed 10µg/in^2 or bromide exceeds 15µg/in^2
- Rapid failure can occur when contaminant levels exceed 50µg/in^2

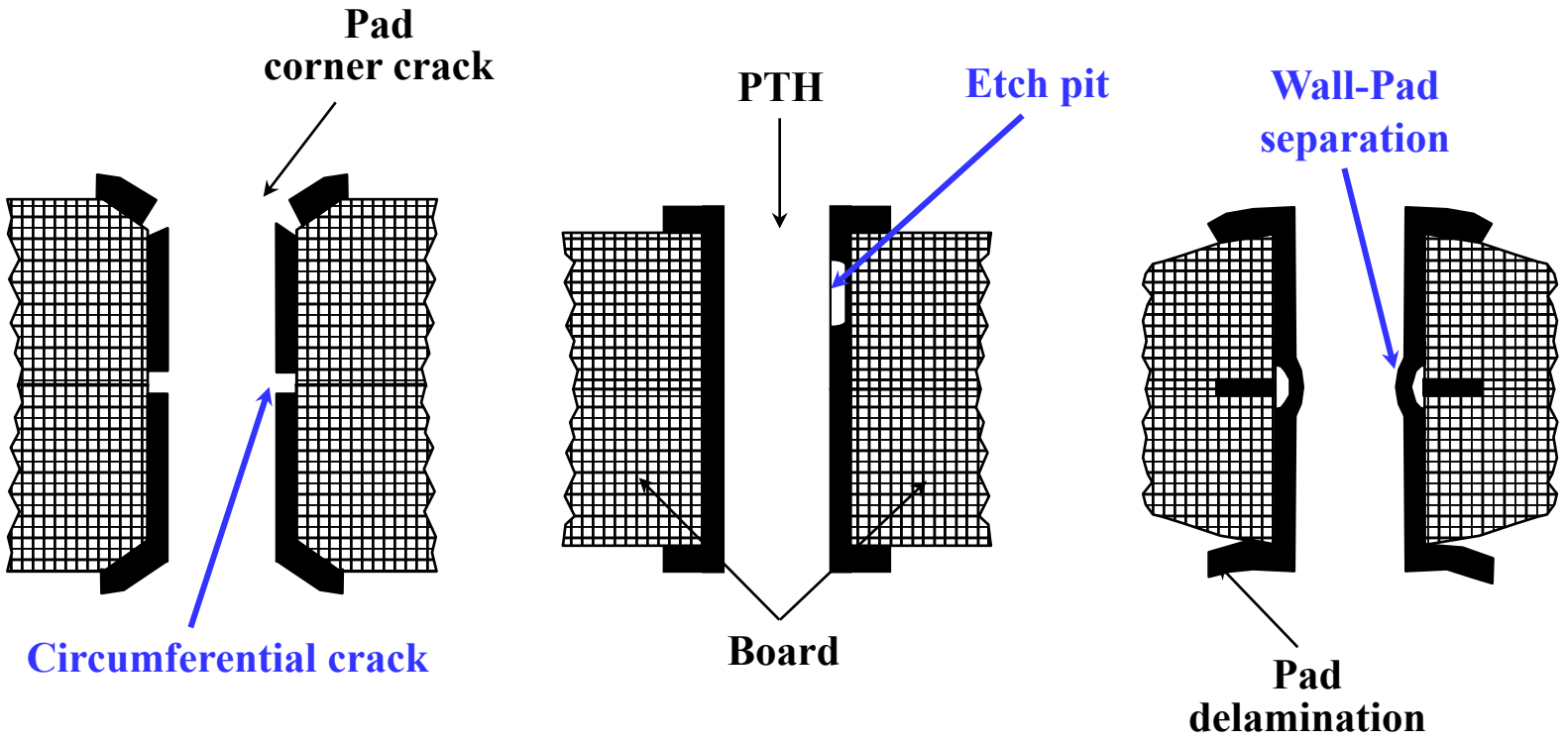
What Are the Sources of Contaminants?

- Board Manufacturing
  - Flame-proofing agents
  - Copper plating deposits
  - Etchants
  - Cleaners
  - Fluxes (for HASL coatings)
  - Poorly polymerized solder masks
  - “Fingerprints”
- Assembly
  - Fluxes
  - Solder paste residues
  - “Fingerprints”
- Environmental
  - Liquid (i.e., salt spray)
  - Gaseous (i.e., Cl_2)

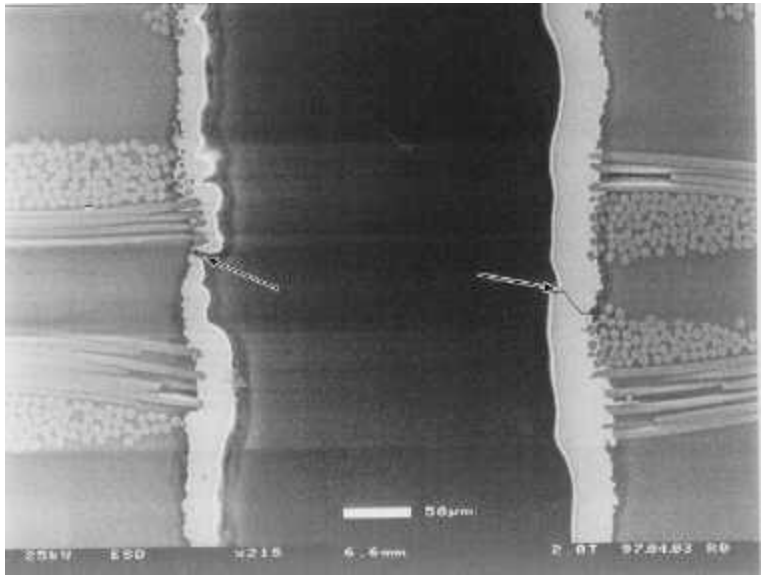
Plated Through Hole (PTH) Failures

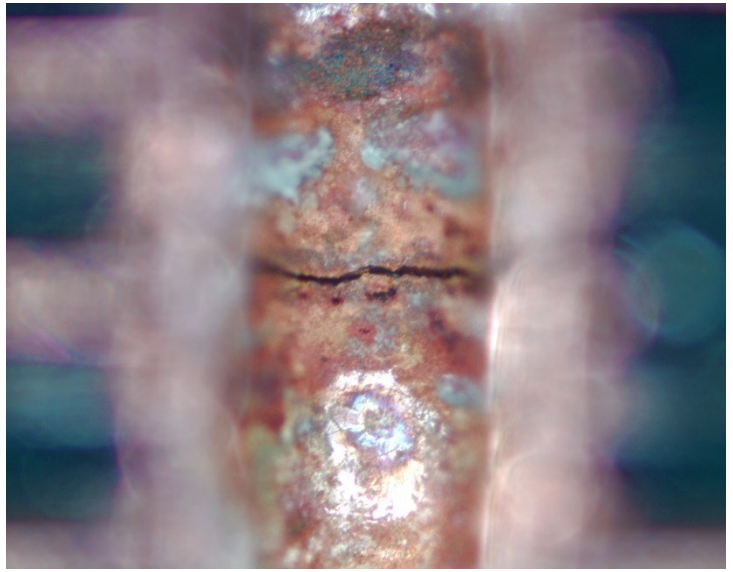
- Circumferential cracking
  - Single event overstress
  - Cyclic fatigue
- Openings (voids, etch pits)
  - Accelerate circumferential cracking
- Wall-Pad Separation
  - Also known as “breakout of internal lands” or “plated-barrel separation”

PTH Failures (cont.)



Circumferential Cracking – Single Event Overstress





Since the difference in the coefficient of thermal expansion (CTE) of the copper plating and the resin system in the PWBs is at least a factor of 13, stress exerted on the plated copper in the plated-through holes in the z-axis can cause cracking.

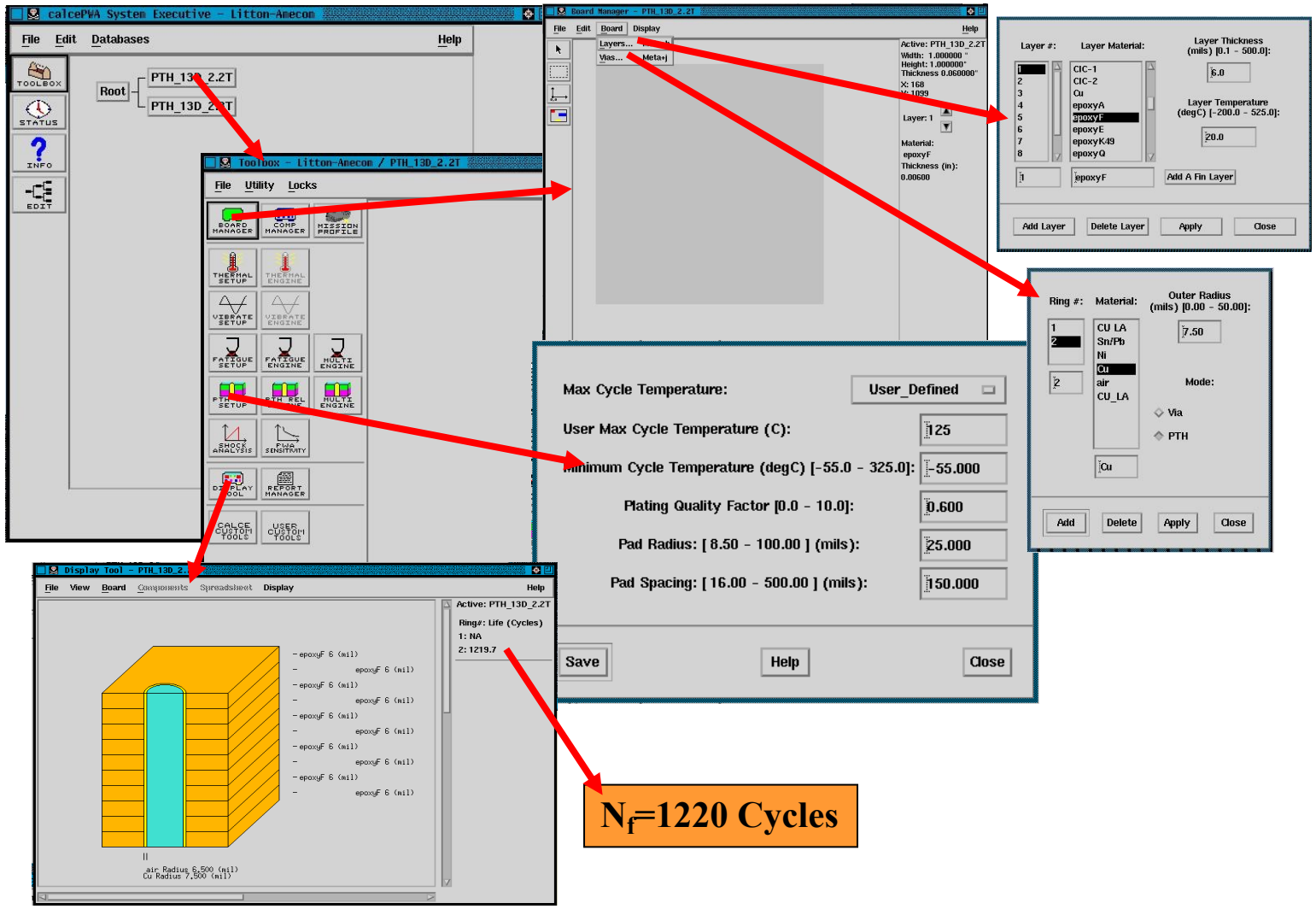
Single Event Overstress (cont.)

- Failure Mode
  - Complete electrical open
- Failure History
  - Primarily occurs during assembly; may not be detected until after operation
- Root-Causes
  - Excessive temperatures during assembly
  - Resin Tg below specification
  - Insufficient curing of resin
  - Outgassing of absorbed moisture
  - Plating folds
  - PTH wall recession
  - Resin-rich pockets adjacent to PTH
  - Insufficient mechanical properties of deposited copper
  - Plating voids
  - Etch pits
  - Insufficient PTH wall thickness

Design Considerations to Avoid Fatigue Damage in PTHs

- PTH Spacing
  - Decreasing spacing improves mechanical reliability
- Aspect Ratio
  - Decreasing board thickness more effective than increasing hole diameter
- Plating Thickness
  - Increasing leads to increasing in fatigue strength
- Nonfunctional Internal Pads
  - Minimal effect. Results in localized stress relief; most effective when results in elimination of resin-rich areas

A Sample PTH Fatigue Damage Model*

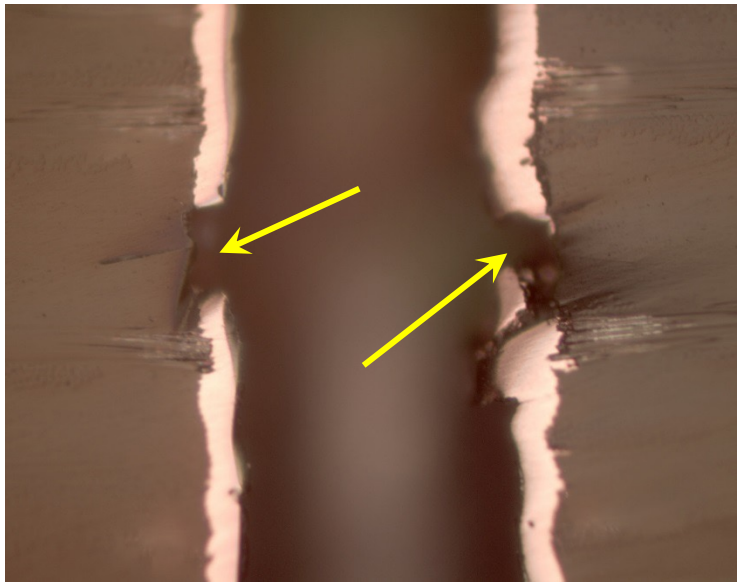


* - http://www.calce.umd.edu/software/online/

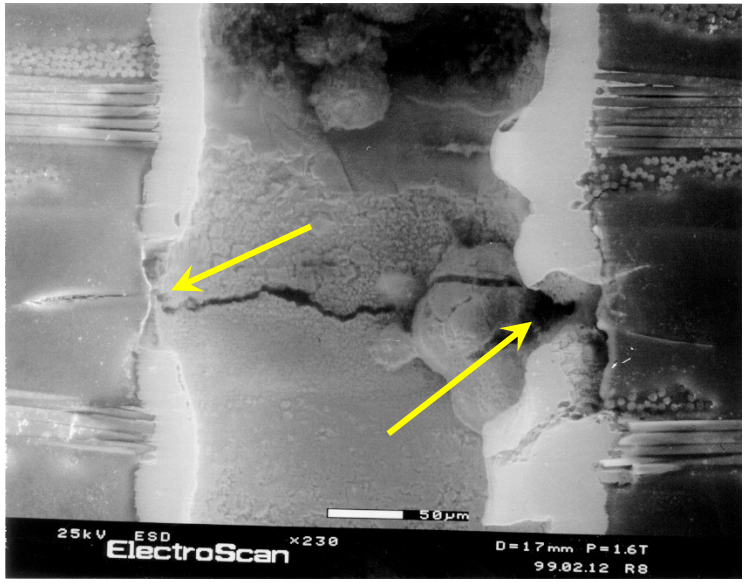
Root-Cause Analysis of Circumferential Fatigue Cracking

- Failure Mode
  - Intermittent to complete electrical open
- Failure History
  - Requires an environment with temperature cycling; often occurs after extended use in the field (“child” or “teenage” mortality)
- Root-Causes
  - Resin CTE below specification
  - Plating folds
  - PTH wall recession
  - Resin-rich pockets adjacent to PTH
  - Customer use exceeds expected environment
  - Insufficient mechanical properties of deposited copper
  - Presence of overstress crack
  - Plating voids
  - Etch pits (“mouse bites”)
  - Insufficient PTH wall thickness

Openings in PTH Walls



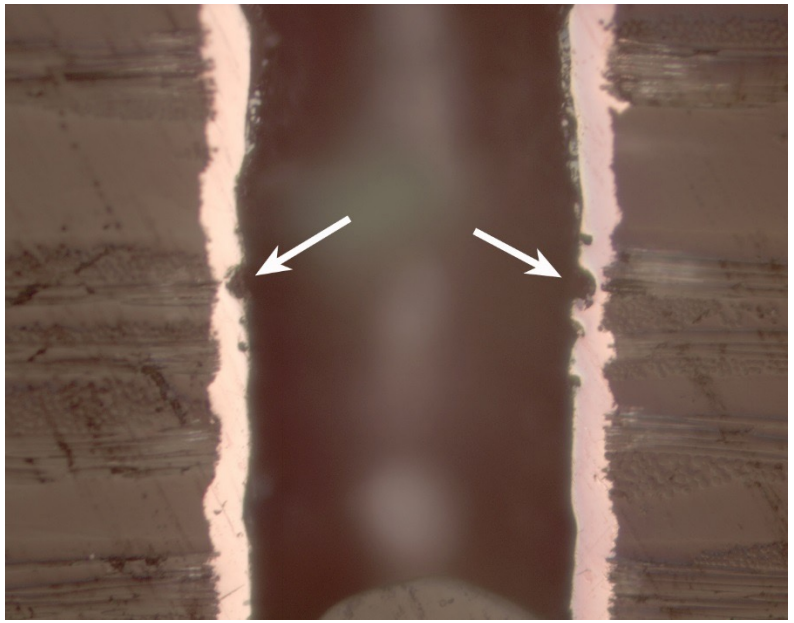
Optical micrograph of cross section of PTH with etch damage



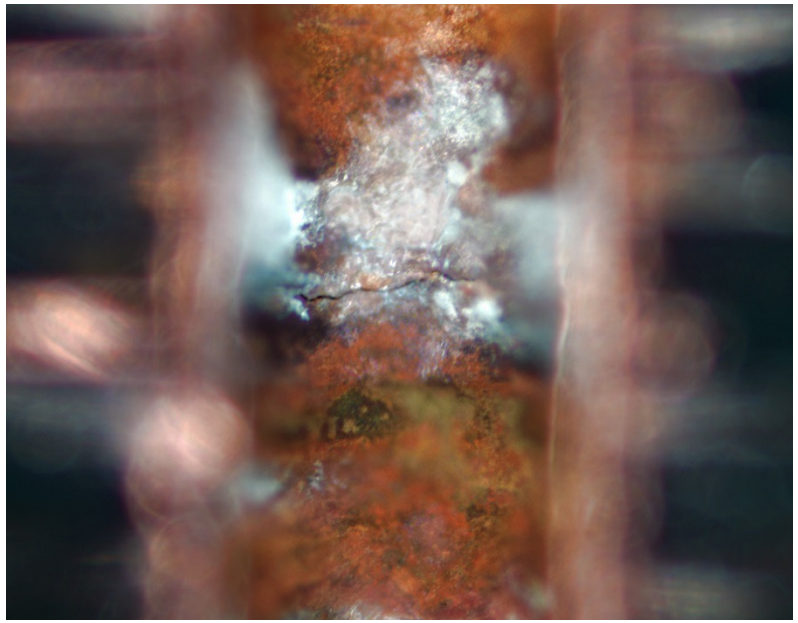
Electron micrograph of same PTH shown on left

Overetching can cause electrical opens or induce overstress circumferential cracking

Evidence of Overetching



Optical micrograph of cross section of PTH with etch damage (bright field)



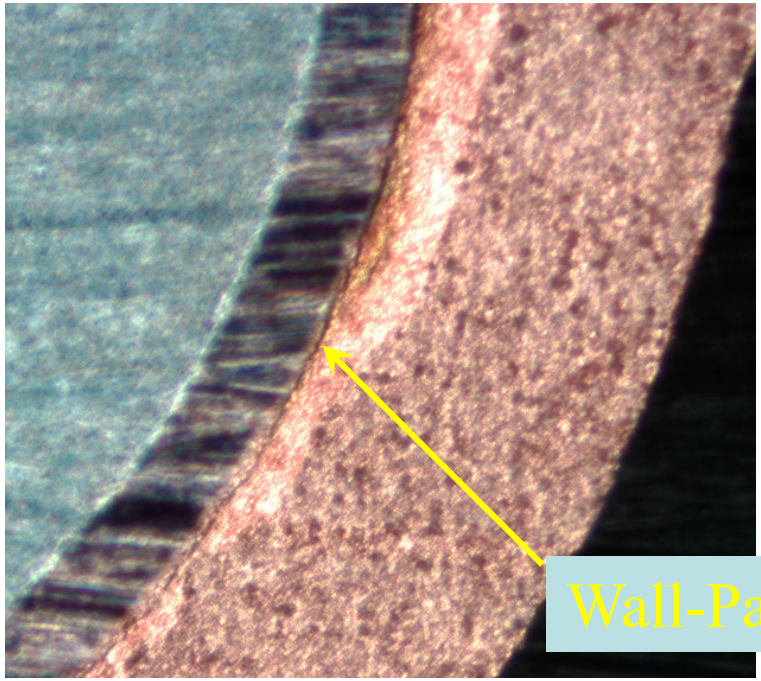
Optical micrograph of cross section of PTH with etch damage (dark field)

Evidence of overetching can include reduced plating thickness and discoloration of PTH barrel walls

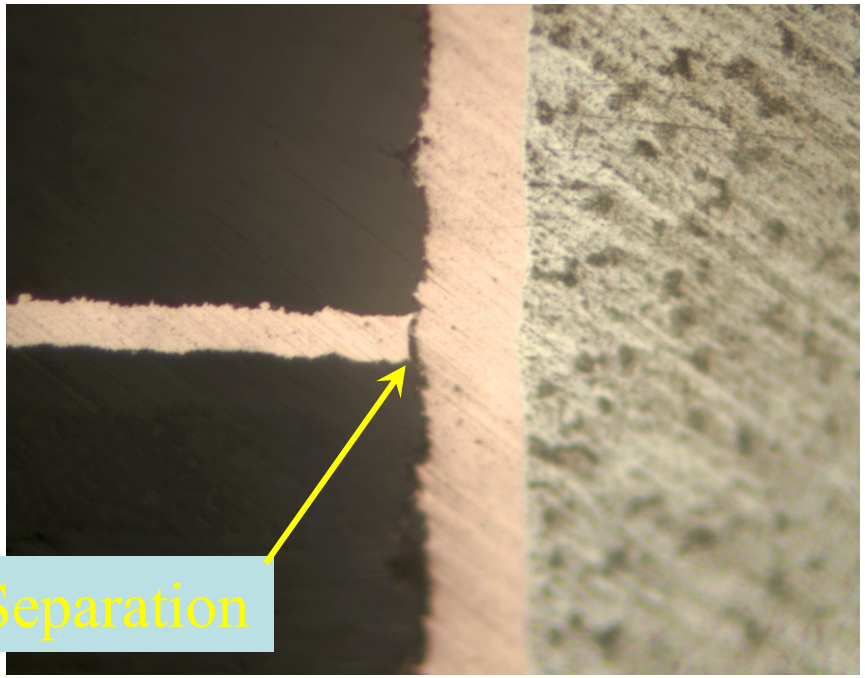
Opening in PTH/Via

- Failure Mode
  - Complete electrical open
- Failure History
  - Often occurs during assembly; may not be detected until after operation
- Root-Causes
  - Openings in PTH's/Vias are etch pits or plating voids and often occur because the following manufacturing processes are not optimized:
    - Drilling
    - Desmear/Etchback
    - Electroless copper plating or direct metallization
    - Electrolytic copper plating
    - Tin resist deposition
    - Etching
  - Openings can also occur due to poor design (i.e., single-sided tenting of vias, resulting in entrapment of etchant chemicals)

PTH/Via Wall-Pad Separation



Optical micrograph of cross section perpendicular to the PTH axis



Optical micrograph of cross section parallel to the PTH axis

PTH/Via Wall-Pad Separation

- Failure Mode
  - Intermittent or complete electrical open
- Failure History
  - Will primarily only occur during assembly
- Root-Causes
  - Insufficient Curing of Resin.
  - Outgassing of absorbed moisture
  - Excessive temperatures during assembly
  - Resin CTE or Resin Tg below specification
  - Number of nonfunctional lands (only useful for failures during assembly)
  - Drilling process resulting in poor hole quality
  - Insufficient desmearing process.
  - Substandard processes or materials in electroless copper plating

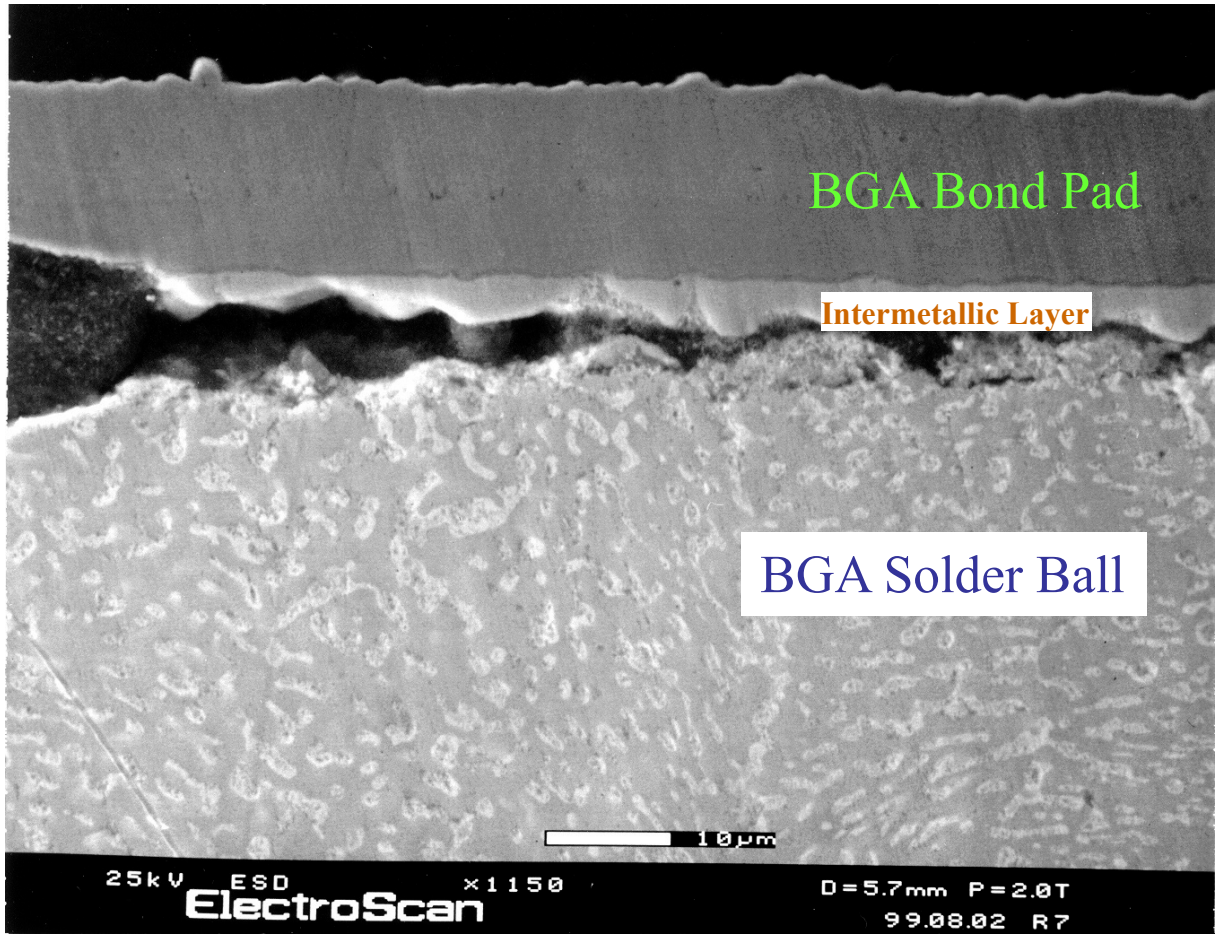
Failure Mechanisms due to Handling

- Affects leadless components
  - Ball grid arrays (BGAs), Flip Chip on Board
- Affects brittle components
- Insidious
  - Failures due to handling tend to difficult to screen and intermittent in nature
  - Often occur after testing

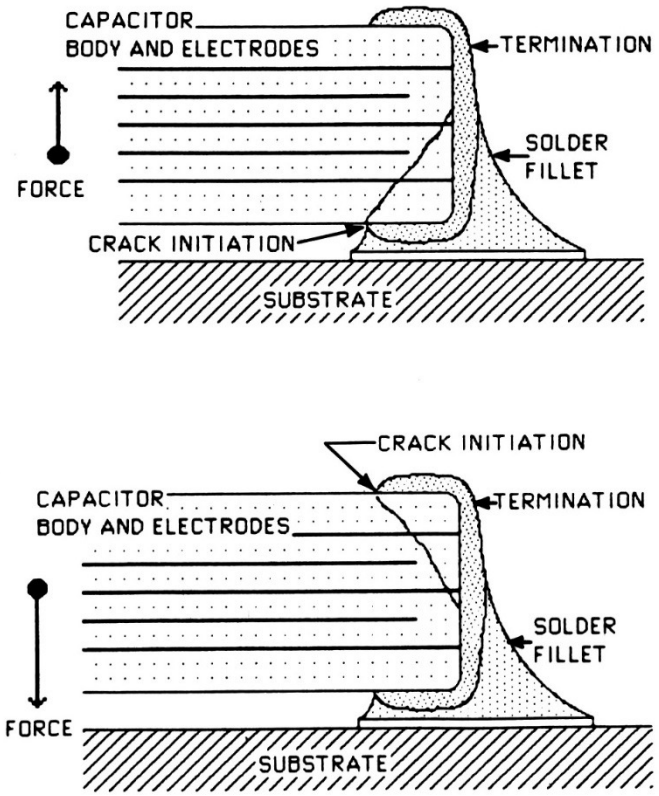
When Do Handling Failures Occur?

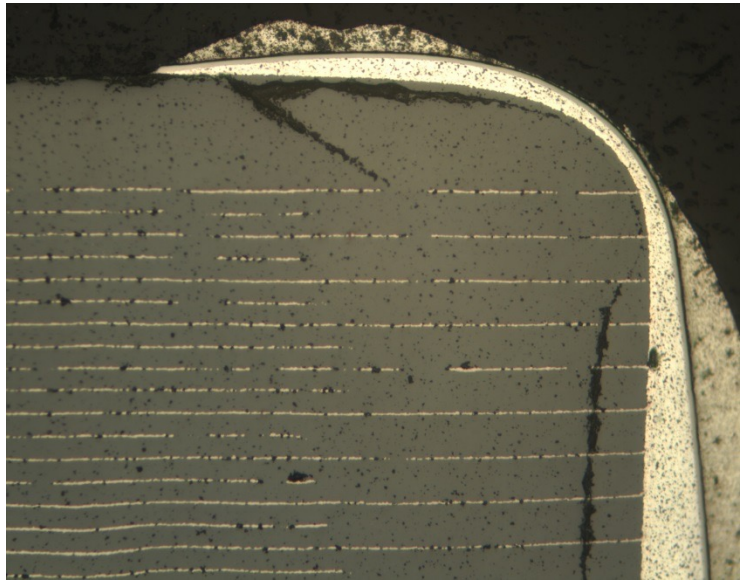
- Assembly
  - Transfer of product between lines; during rework
- Heatsink Attachment
  - Use of screws
- Connector Insertion
  - Large press-fit connectors; daughter boards into mother boards
- Electrical Testing
  - Bed-of-Nails testing can bend local areas
- Packaging
- Transportation
- Customer Site
  - Slot insertion

Evidence of Damage Due to Handling -- BGAs



Evidence of Damage – Ceramic Capacitors





Intermittent Failures

- An intermittent failure is the loss of some function in a product for a limited period of time and subsequent recovery of the function.
- If the failure is intermittent, the product's performance before, during, or after an intermittent failure event may not be easily predicted, nor is it necessarily repeatable.
- However, an intermittent failure is often recurrent.

No Fault Found

- No-Fault-Found (NFF): Failure (fault) occurred or was reported to have occurred during product's use. The product was tested to confirm the failure, but the testing showed "no faults" in the product.
- Trouble-Not-Identified (TNI): A failure occurred or was reported to have occurred in service or in manufacturing of a product. But testing could not identify the failure mode.
- Can-Not-Duplicate (CND): Failures that occurred during manufacture or field operation of a product cut could not be verified or assigned.
- No-Problem-Found (NPF): A problem occurred or was reported to have occurred in the field or during manufacture, but the problem was not found during testing.
- Retest-OK: A failure occurred or was reported to have occurred in a product. On retesting the product at the factory, test results indicated that there was no problem.

The Impact of Intermittents

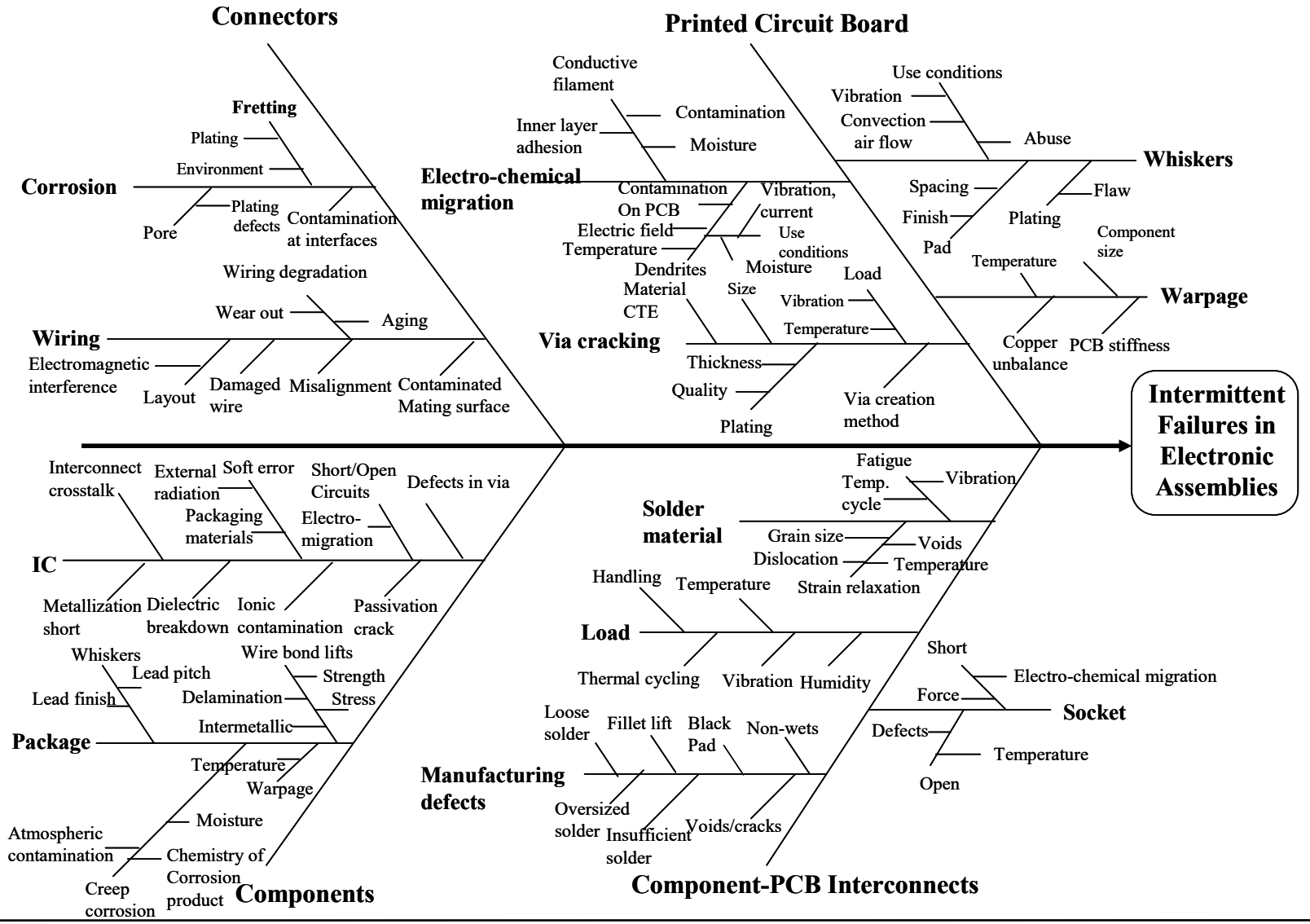
- Can not determine root cause and thus the reason for the failure (NFF)
- Reliability modeling analysis can be faulty
- Potential safety hazards
- Decreased equipment availability
- Long diagnostic time and lost labor time
- Complicated maintenance decisions
- Customer apprehension, inconvenience and loss of customer confidence
- Loss of company reputation
- Increased warranty costs
- Extra shipping costs

Common Examples of Intermittents

Some common examples of intermittent failures:

- Medical: asthma attacks, allergy attacks, angina, toothaches (especially if food- or temperature- dependent)
- Automotive: squealing sound or failure to charge battery due to loose fan belt
- Utility: brown-outs
- Cell phone or computer: multiple letter entries for a single keystroke, which may be due to bad contact or sticky keys on keypad
- Household: water ingress through leaky roof, especially if leak is wind-driven; running toilet, due to problems with mechanism or plunger seal

Intermittent Failures in Electronic Assemblies
Cause-and-Effect Diagram

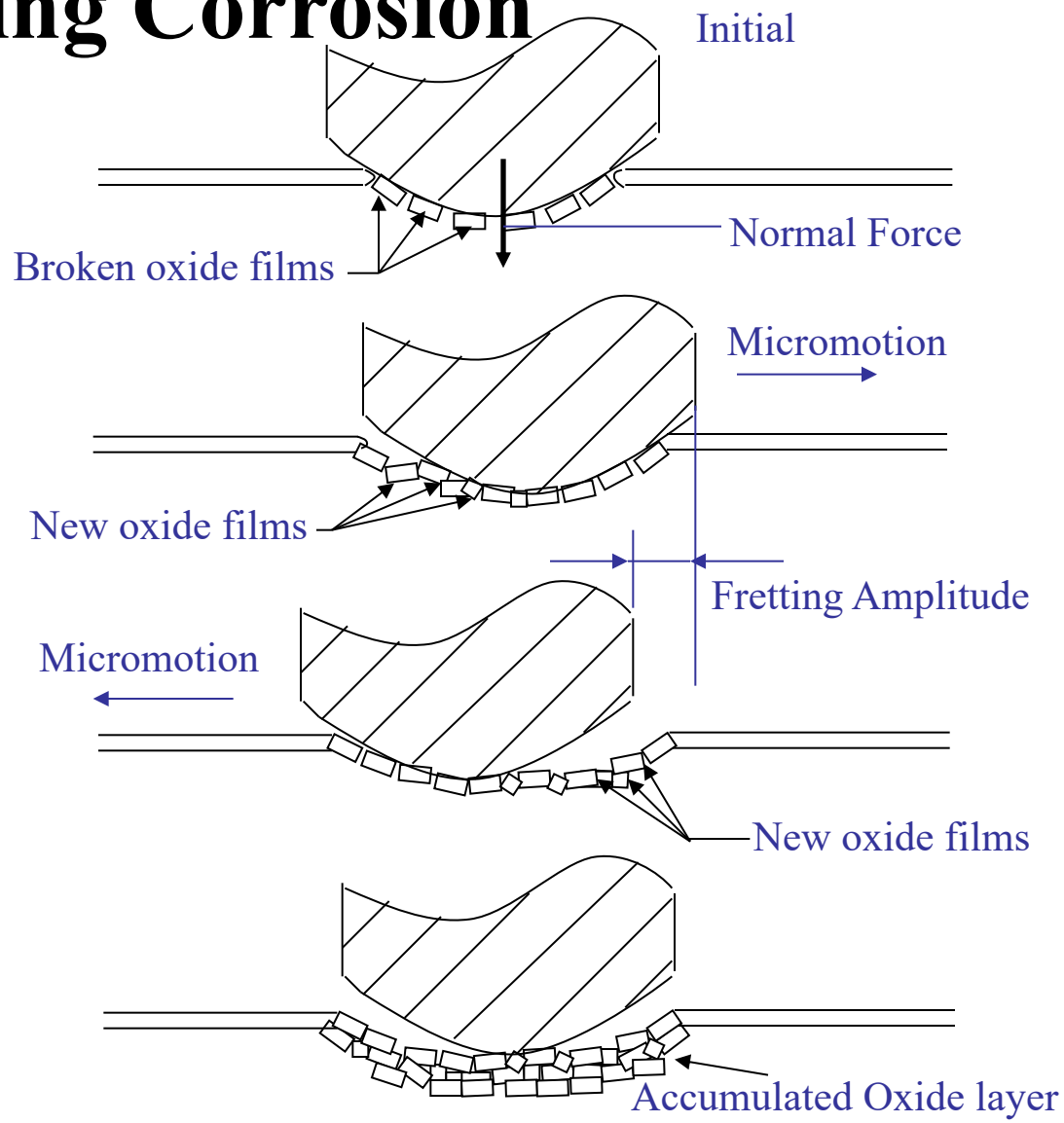


Characteristics of Intermittent Failures

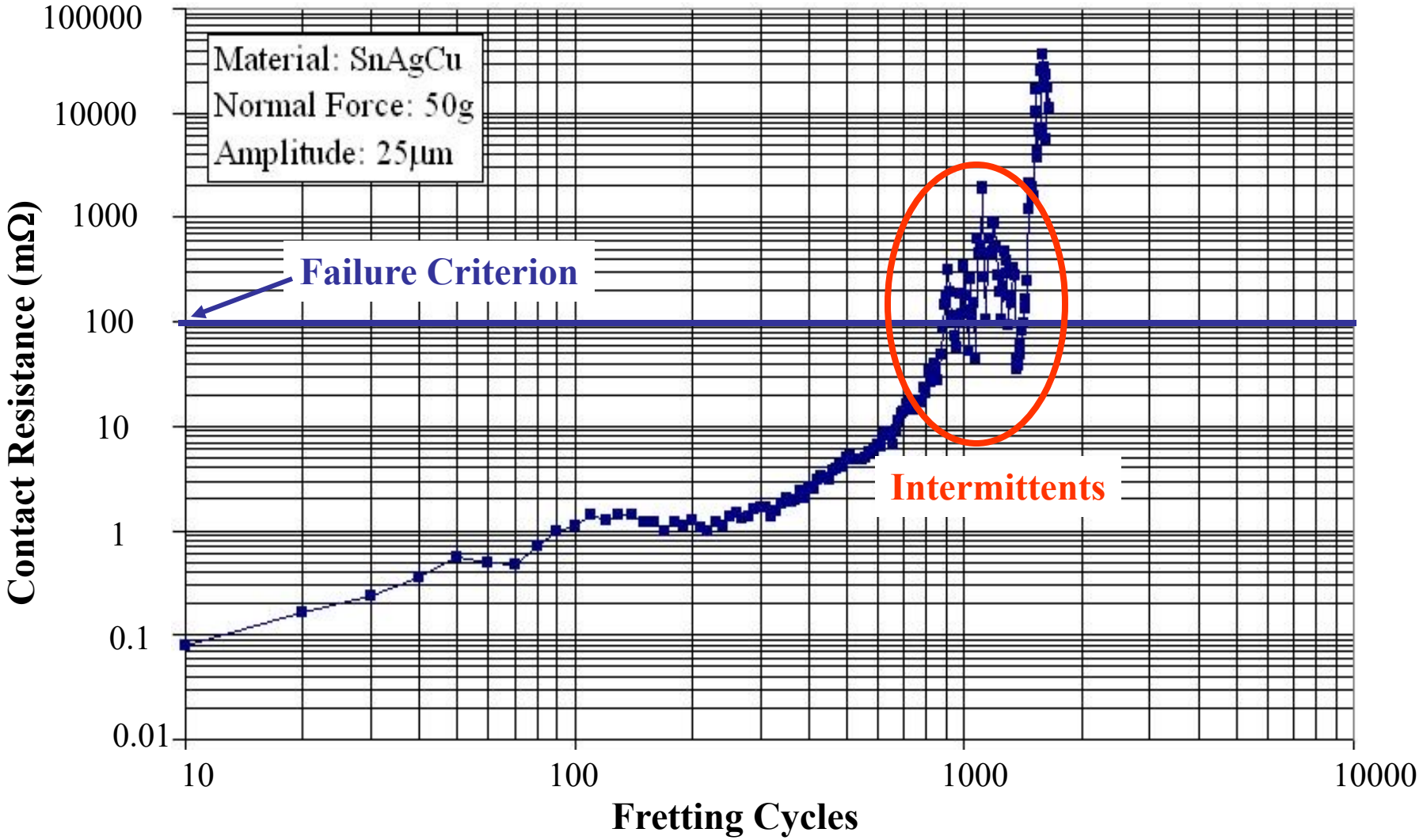
- May indicate that a failure has occurred. Intermittent failure may be due to some extreme variation in field or use conditions.
- May indicate the imminent occurrence of failure.
- May not leave a failure signature making it difficult to isolate the site.

Example: Intermittent Failures Due to Fretting Corrosion

- Tin alloys are soft metals on which a thin but hard oxide layer is rapidly formed.
- Being supported by a soft substrate, this layer is easily broken and its fragments can be pressed into the underlying matrix of soft, ductile tin-lead alloy.
- The sliding movements between contact surfaces break the oxide film on the surface and expose the fresh metal to oxidation and corrosion.
- The accumulation of oxides at the contacting interface due to repetitive sliding movements causes contact resistance to increase, leading to contact open.
- Tin based lead-free solders are expected to show similar fretting corrosion susceptibility as tin-lead solder coatings.

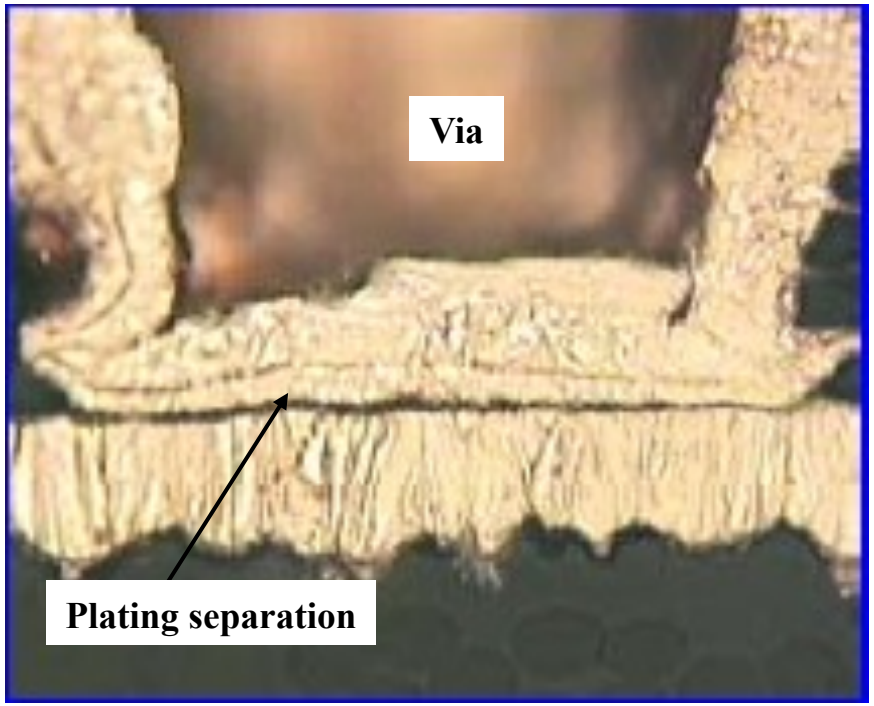


Electrical Contact Resistance vs. Fretting Cycles



Example: Intermittent Failure Due to Improper Micro-via Plating in PCB

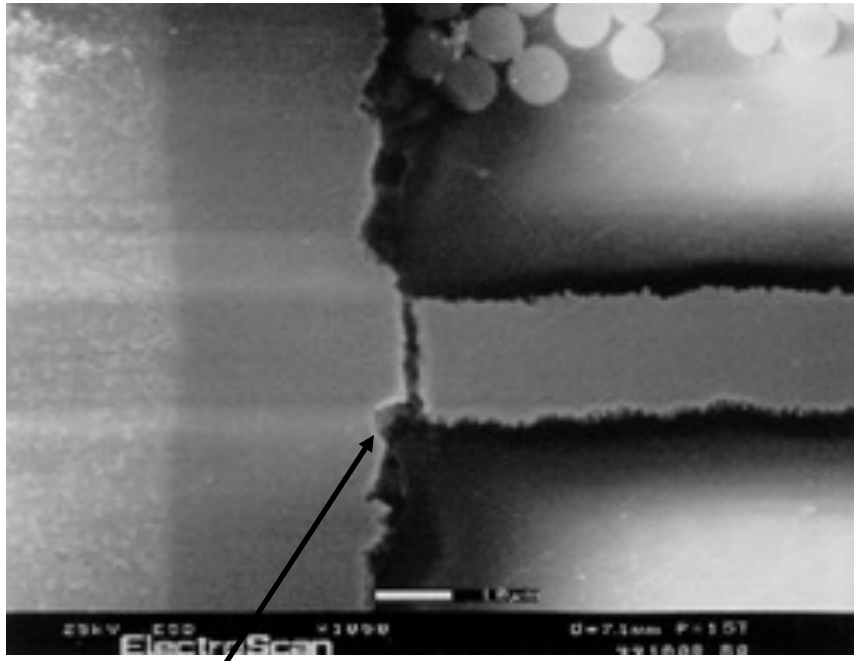
A computer graphics OEM was experiencing intermittent failures on printed circuit boards with chip scale packages (CSPs) and ceramic ball grid array packages (CBGAs). High magnification metallurgical microscope imaging of micro-etched cross sections of micro-vias in the printed circuit board showed a separation of the via plating from the capture pad [Nektek Inc. Service Report, 2004]. The plating separation was found to be the cause of intermittent failure.



Plating separation at base of micro via [Nektek Inc. Service Report, 2004]

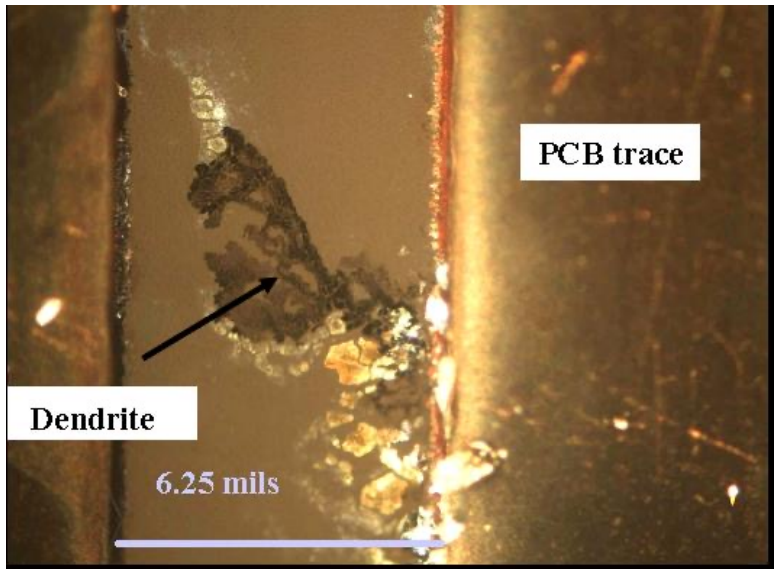
Example: Intermittent Failure Due to Open Trace in PCB

Open trace can also cause intermittent failures in PCB under environmental loading conditions. Under thermal cycling or vibration loading, the open trace may reconnect with intermittent electrical continuity observations.



Example: Intermittent Failures Due to Electro-chemical Migration (Surface Dendrites)

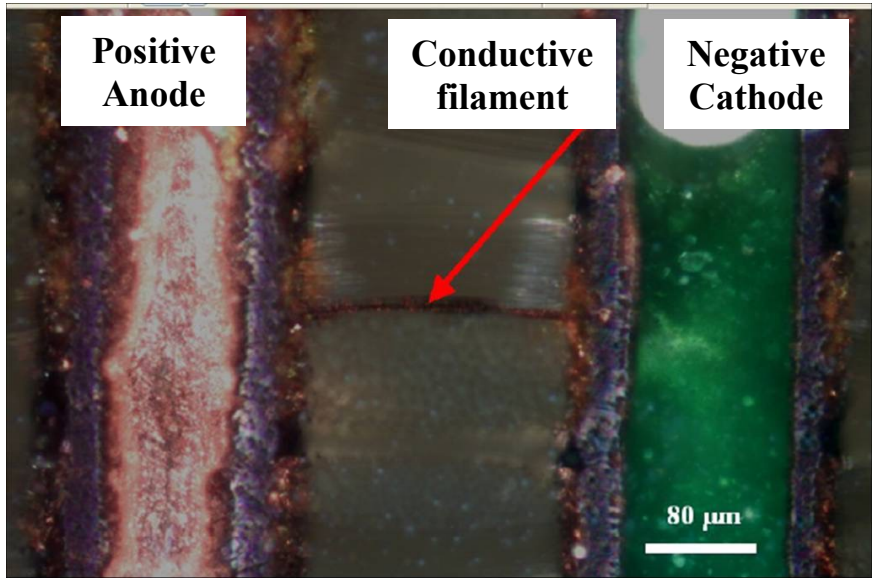
- Electrochemical migration (ECM) can cause shorts due to the growth of conductive metal filaments in a printed wiring board (PWB).
- Surface dendrites can form between the adjacent traces in the PWB under an applied voltage when surface contaminants and moisture are present.
- It is often difficult to identify the failure site because the fragile dendrite structure will burn upon shorting, often leaving no trace of its presence.



Dendritic growth during an ECM test

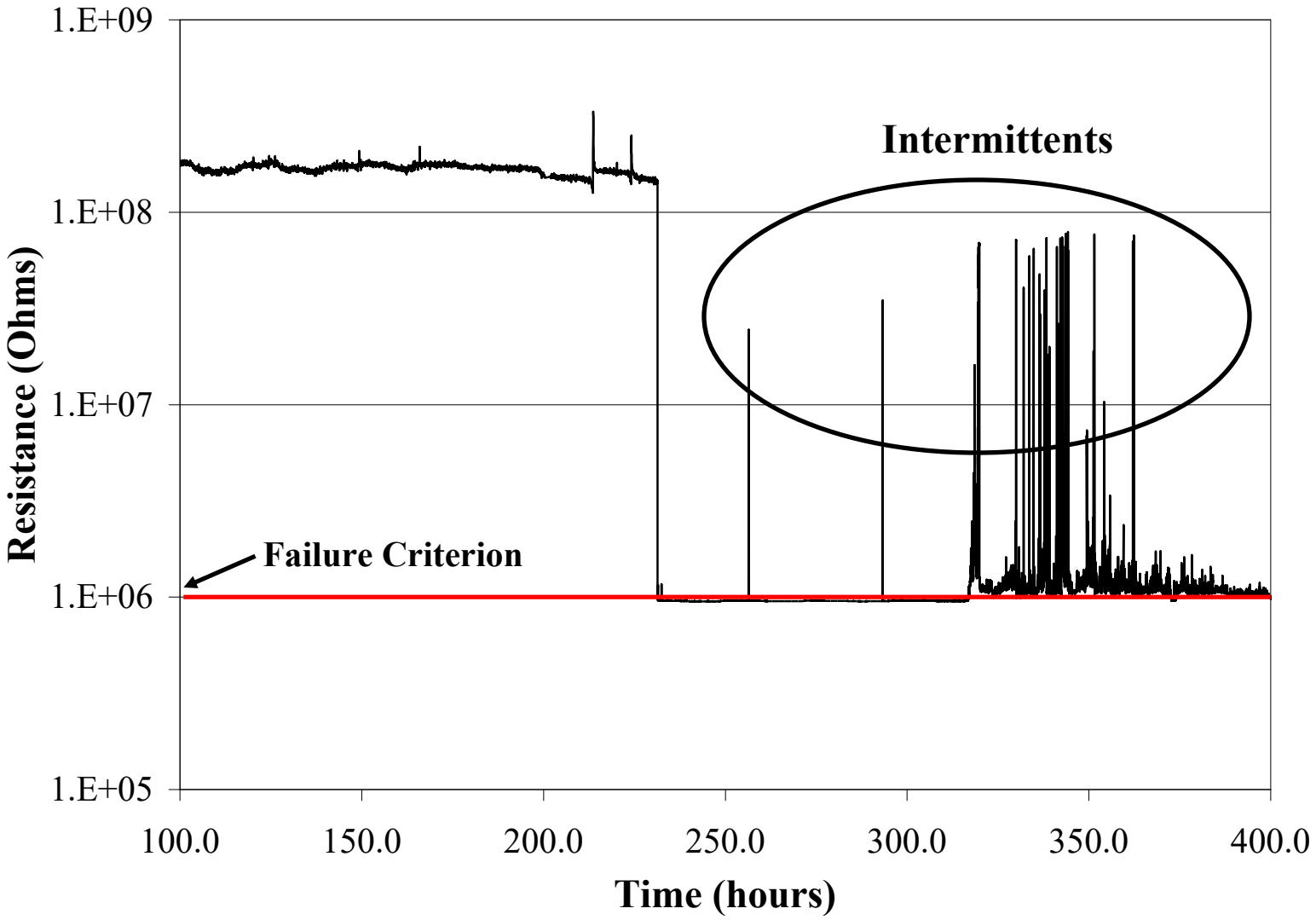
Example: Intermittent Failures Due to Electro-chemical Migration
(Conductive Anodic Filament Formation)

- Conductive filament is formed internal to the board structure.
- In CAF, the filament is composed of a metallic salt, not neutral metal atoms as in dendritic growth.
- One of distinct signatures of CAF failures is intermittent short circuiting. The conductive filament bridging the two shorted conductors can blow out due to the high current in the filament, but can form again if the underlying causes remain in place.



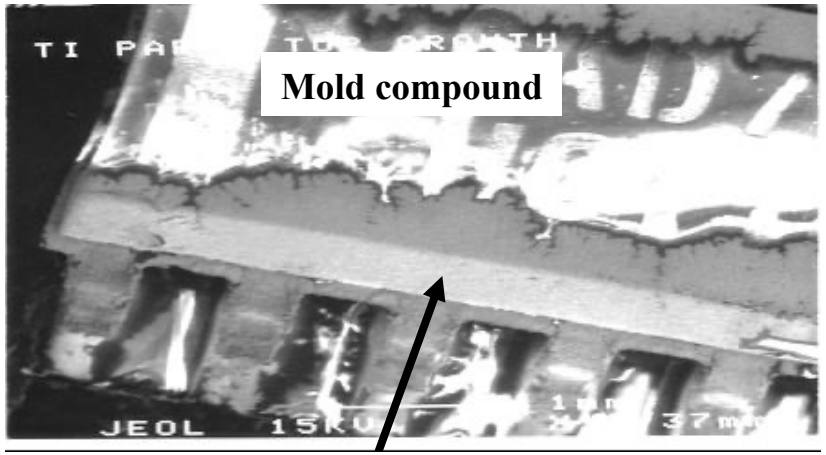
A conductive filament bridging two plated through holes in a PWB

Electrical Resistance vs. Time Due to CAF



Example: Intermittent Failures Due to Creep Corrosion

- Definition
  - Creep corrosion is a mass transport process in which solid corrosion products migrate over a surface.
- Failure mode
  - On IC packages, creep corrosion can eventually result in electrical short or signal deterioration due to the bridging of corrosion products between isolated leads.
  - Depending on the nature of the environment, the insulation resistance can vary and cause intermittents.



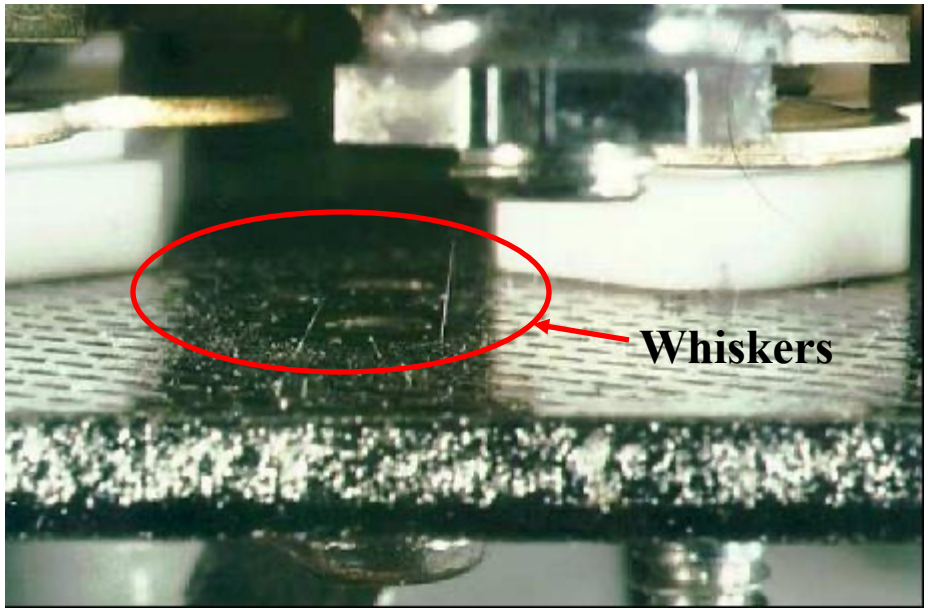
Creep corrosion

Field failure due to creep corrosion [Adtran, 2001]

Example: Intermittent Failures Due to Tin Whiskers



Failed relay due to tin vapor arcing



Whiskers on the armature of a relay

Photos Courtesy: Northrop Grumman

- Whiskers are elongated single crystals of Sn which grow spontaneously out of the surface. Internal stresses within the plated deposit drives growth
- Tin (and other conductive) whiskers or parts of whiskers may break loose and bridge isolated conductors, resulting in an intermittent short circuit. These field failures are difficult to duplicate or are intermittent because at high enough current the conductive whisker can melt, thus removing the failure condition. Alternatively, disassembly or handling may dislodge a failure-producing whisker.
- Failure analysis concluded that tin whiskers initiated the current surge to the ground. Once a whisker bridged a terminal stud to the armature, plasma arcing could occur with enough voltage and current to damage the relay.

Effects of Conformal Coating

- Prevent the whisker penetration
  - Block the electrical shorting caused by whiskers

  → *Measure the breakdown voltage of conformal coating*

  - Keep whiskers under the conformal coating

  → *Measure the mechanical properties(Young's modulus, hardness) and adhesion strength of conformal coating*

- Slow the whisker growth

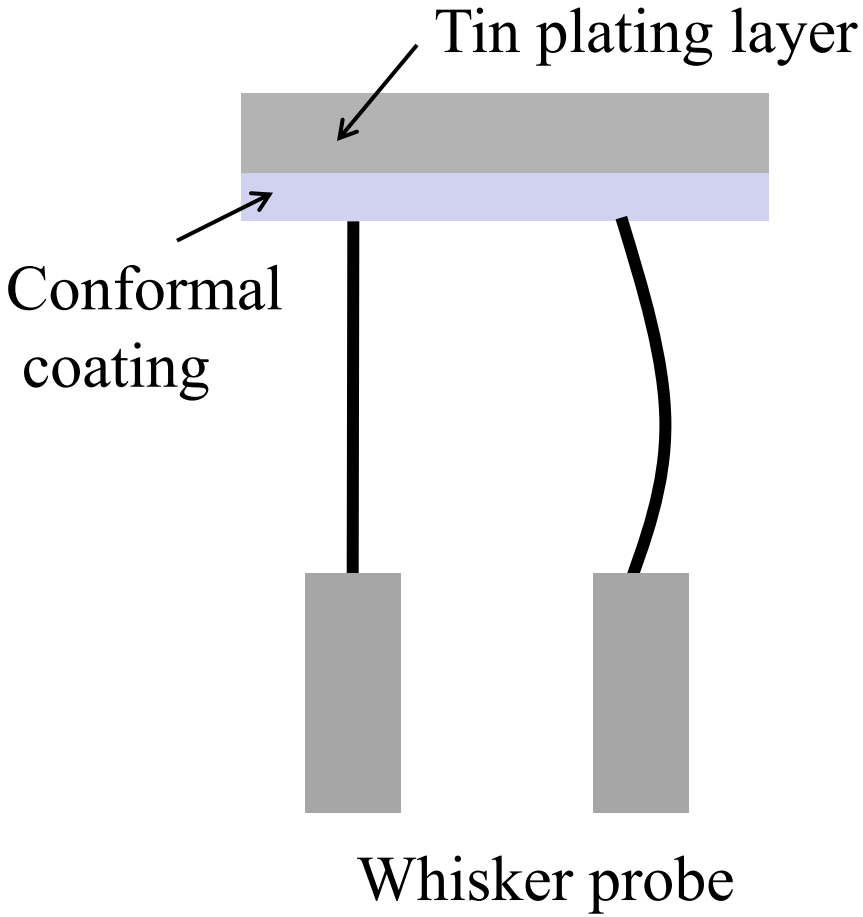
  → *Measure the preferred crystal orientation and residual stresses in tin layer*

Buckling Force 1/2*

- Measuring the buckling force using various length of whisker probes

$$F_B = \frac{\pi^2 EI}{(KL)^2} \approx \left(\frac{\pi^3 E}{32}\right)\left(\frac{d^4}{L^2}\right)$$

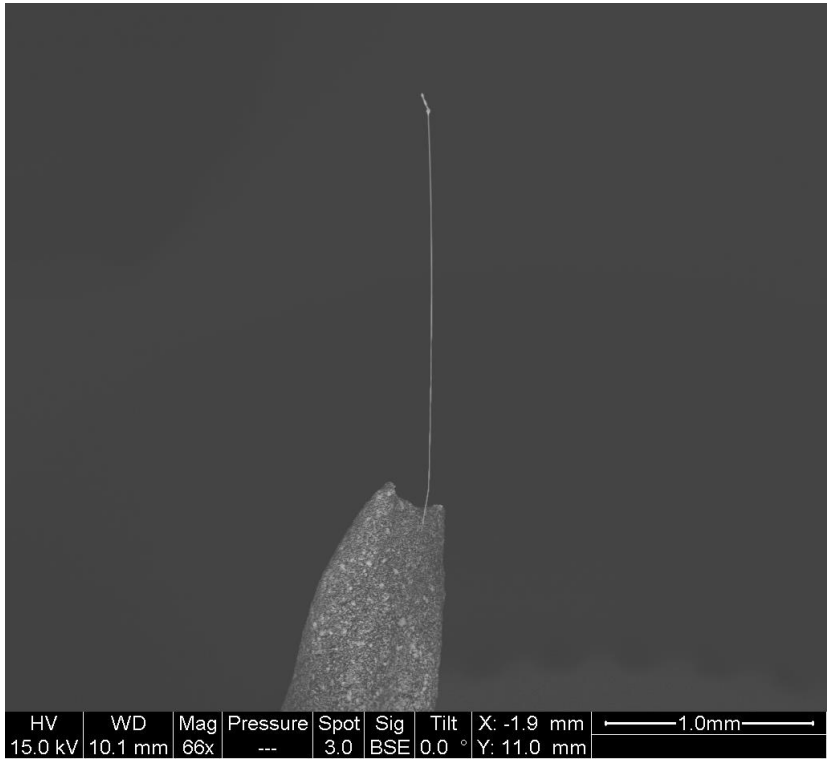
E=Young's modulus of whisker
I=Area moment of inertia
L=Length of whisker
K=Column effective length factor(0.7)

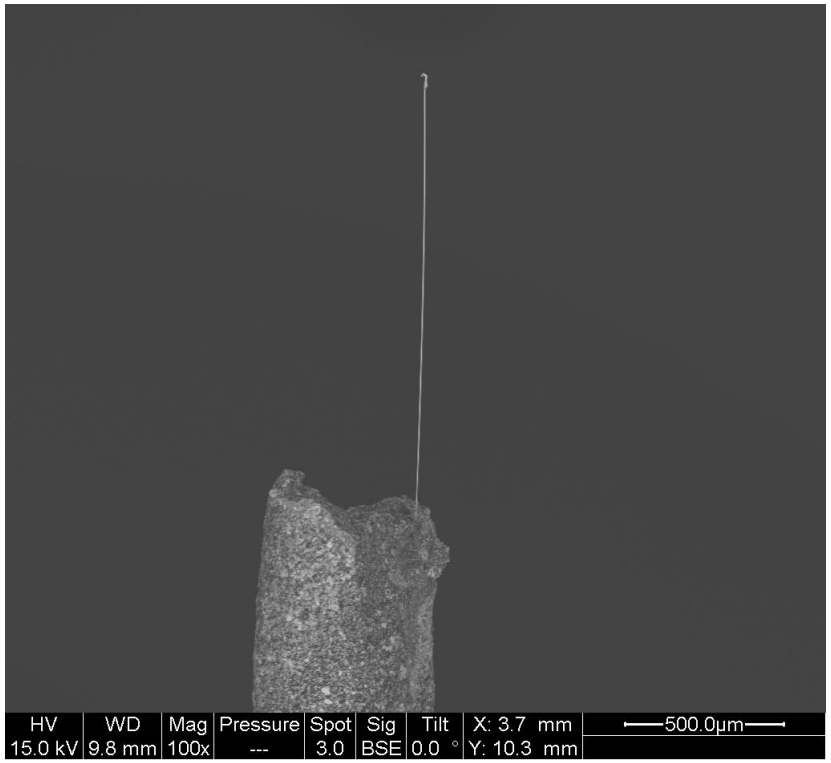


* - Han, Sungwon, et al. "Evaluation of effectiveness of conformal coatings as tin whisker mitigation." Journal of electronic materials 41.9 (2012): 2508-2518.

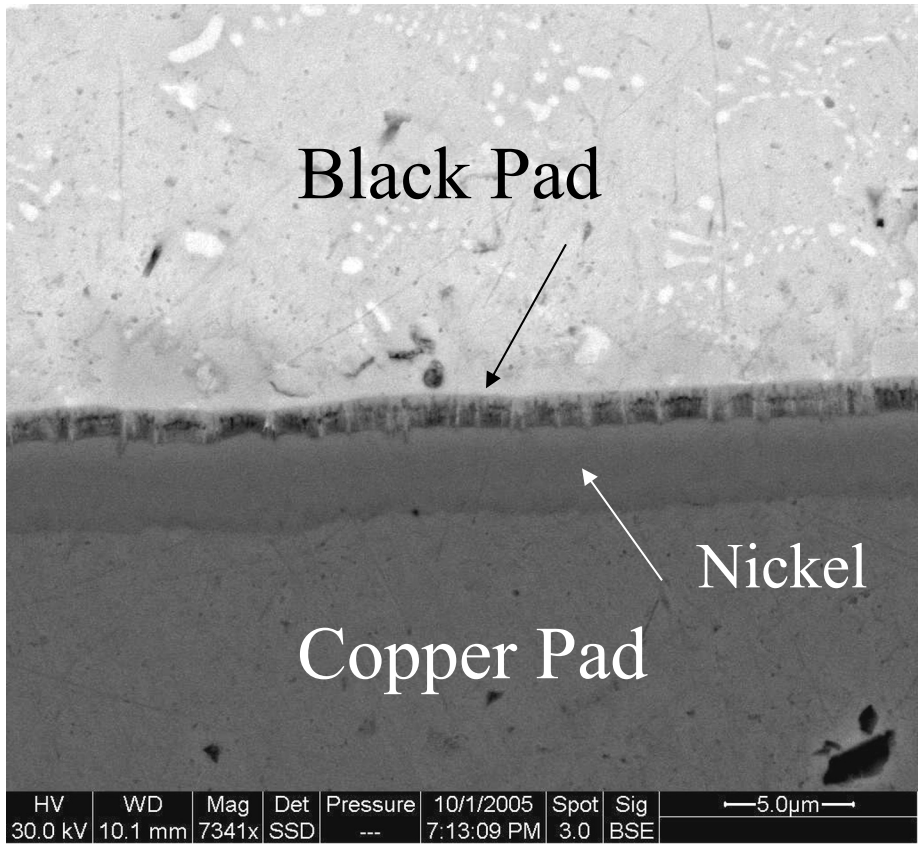
Buckling Force 1/2

- Challenge
  - Most of whiskers on whisker probe are already buckled.
  - Tip of whiskers were damaged during the cut-off process.





Example: Intermittent Failures Due to Black Pad



The 'Black Pad' phenomenon in Electroless Nickel over Immersion Gold (ENIG) board finish manifests itself as gray to black appearance of the solder pad coupled with either poor solderability or solder connection, which may cause intermittent electrical 'opens.'

Bulwith et al. [2002] identified numerous Ball Grid Array (BGA) package intermittent electrical open failures to be black pad related.

Section – 4
Effects of Moisture on PCB Technology

Effects of Moisture in PCB

- Swelling and inner layer delamination
- Blistering
- Reduces glass-transition temperature (Tg) – increases stresses on features like PTHs
- Increases dielectric constant (D_k) and dissipation factor (D_f) – reducing circuit switching speed
- Oxidation of copper surfaces – leading poor wettability of finishes and solder
- Ionic corrosion – leading to electrical opens or shorts
- Interfacial degradation – leading to conductive filament formation

Inner Layer Delamination – 1

- Delamination occurs at the interface of adhering materials.
- Work required to separate the interfaces and extend the crack includes:
  - Work necessary for de-adhesion, and
  - Work required to deform, elastically or inelastically, the separating bulk phases.



Delamination between copper conductors, core and prepreg [1]

1 – Reid, PWB Interconnect Solutions

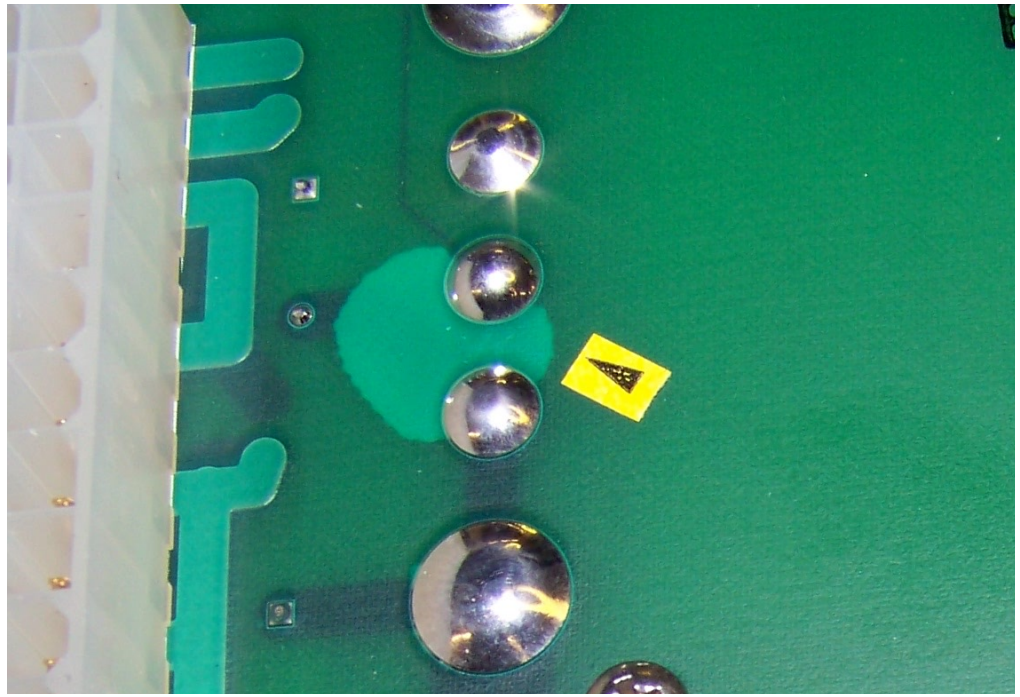
Inner Layer Delamination – 2

- Partially polymerized or uncured resin, at reflow temperatures, forms shorter chains
  - Unbound water molecules exert internal pressure by turning to steam – causing localized delamination
  - Regions away from PTHs are more prone to delamination
  - Moisture can escape more easily close to PTHs
- Additional causes:
  - Using prepregs from uncontrolled storage.
  - Board lamination in uncontrolled humidity environments.

Blistering

Typically caused by high vapor pressure exerted by

- Moisture trapped between the solder mask and board surface
- Volatiles, retained solvents or resin decomposition products



Blistering [1]

1 –edn.com

Effect of Lead-free Soldering Exposures on PCB Laminates – 1

- Lead-free soldering reflow temperatures are much higher than the T_g of FR-4 laminates and as the material is heated above T_g, relative motion of the polymer chains increase
- If the thermal exposures are sufficiently high, it could lead to the cleavage of bonds (at the chain ends, leading to further curing; or in the polymer backbone, leading to a degraded structure) in the polymer network and as the material is cooled below T_g, the resulting polymer matrix could be either:
  - **an 'enhanced-cure' structure**
    - More curing, leading to increase in the cross-linking density
  - **a 'degraded' structure**
    - At approximately 240°C, thermal degradation of epoxy network begins through homolytic scission of chemical bonds, which influences its physical properties but does not cause a large weight loss[1]
    - At approximately 300°C, elimination of secondary alcohol groups as water molecules takes place leading to the formation of less stable allylic C-O linkages[2]

1- . J. Macan, I. Brnardic, S. Orlic, H. Ivankovic, M. Ivankovic, "Thermal degradation of epoxy-silica organic-inorganic hybrid materials", *Polymer degradation and stability*, vol. 91, pp. 122-127, 2006

2- S. Levchik, E. Weil, "Thermal decomposition, combustion and flame-retardancy of epoxy resins-a review of the recent literature", *Polymer International*, vol. 53, pp. 1901-1929, 2004

Effect of Lead-free Soldering Exposures on PCB Laminates – 2

- **If the material is cured due to lead-free soldering exposures**
  - Cross-linking density increases due to further curing of the polymer, resulting in a **reduction of CTE**
  - Increase in cross-linking density enhances the free-volume in the polymer structure, allowing for **increase in water absorption** [water absorption could increase due to increase in polarity of the molecules or due to the presence of more free-volume]
  - This increase in water absorption **increase the plasticity** of the polymer matrix

    [water acts as a plasticizer]
  - The plasticizing effect of water significantly **reduces the T_g** of a material

    [plasticizers typically work by embedding themselves between the chains of polymers, spacing them apart, further increasing the free-volume]
  - The plasticizing effect also results in softening of the material or a **reduction in hardness**
- But, with increase in cross-linking density, T_g and hardness of the material could increase
- T_g of polymers is dependent on several parameters such as molecular weight of the material, its tacticity, the degree of cross-linking, and entrapped plasticizers[1]

Katrin Wondraczek, Jorg Adams, Jurgen Fuhrmann, "Effect of Thermal Degradation on Glass Transition Temperature of PMMA", *Macromolecular Chemistry and Physics*, vol. 205, issue 14, pp. 1858-1862, 2004

Effect of Lead-free Soldering Exposures on PCB Laminates – 3

- Thus there exist two possible competing mechanisms taking place due to increase in cross-linking, the effects of which counteract each other
  - Reduction in T_g with increase in water absorption leading to reduction in hardness
  - Increase in T_g and hardness
- Overall, the variation in properties due to lead-free soldering exposures can be correlated to the degree of cross-linking and the extent of water absorption in the exposed sample
- DICY cured systems are more hydrophilic to start with, compared to Phenolic cured systems.

Effects of Moisture on T_g

- A decrease in T_g of an epoxy system is usually associated to the entrapped plasticizers.
- Water typically acts as a plasticizer in the epoxy systems resulting in a reduction of T_g.

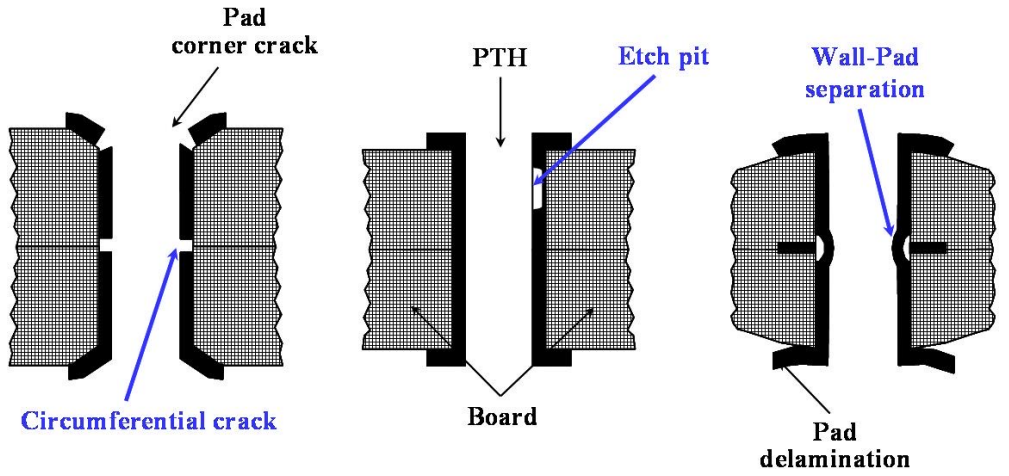
Effects of Moisture on CTE

Exposure to humidity has no obvious effect on z-CTE values (below 100ºC and above Tg).

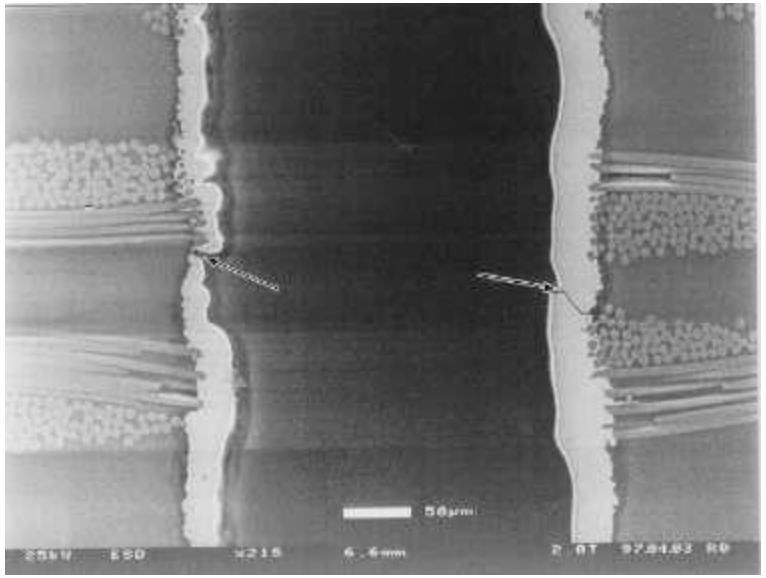
- However, moisture causes swelling in PCB laminates between 100ºC and the Tg point
- Increases z-axis expansion rates.

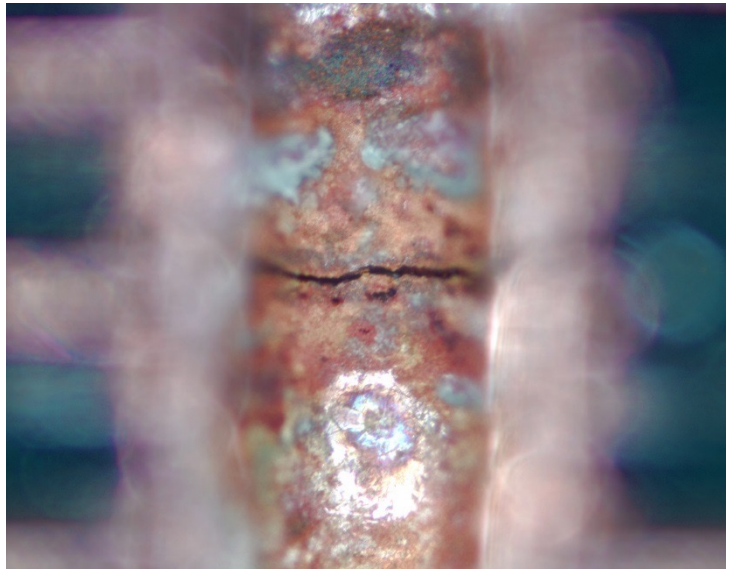
Increased Z-Axis Expansion

- Excessive out of plane expansion can lead to stress build up at PTH
- Circumferential cracking
  - Single event overstress
  - Cyclic fatigue
- Openings (voids, etch pits) can accelerate circumferential cracking.



Circumferential Cracking – Single Event Overstress

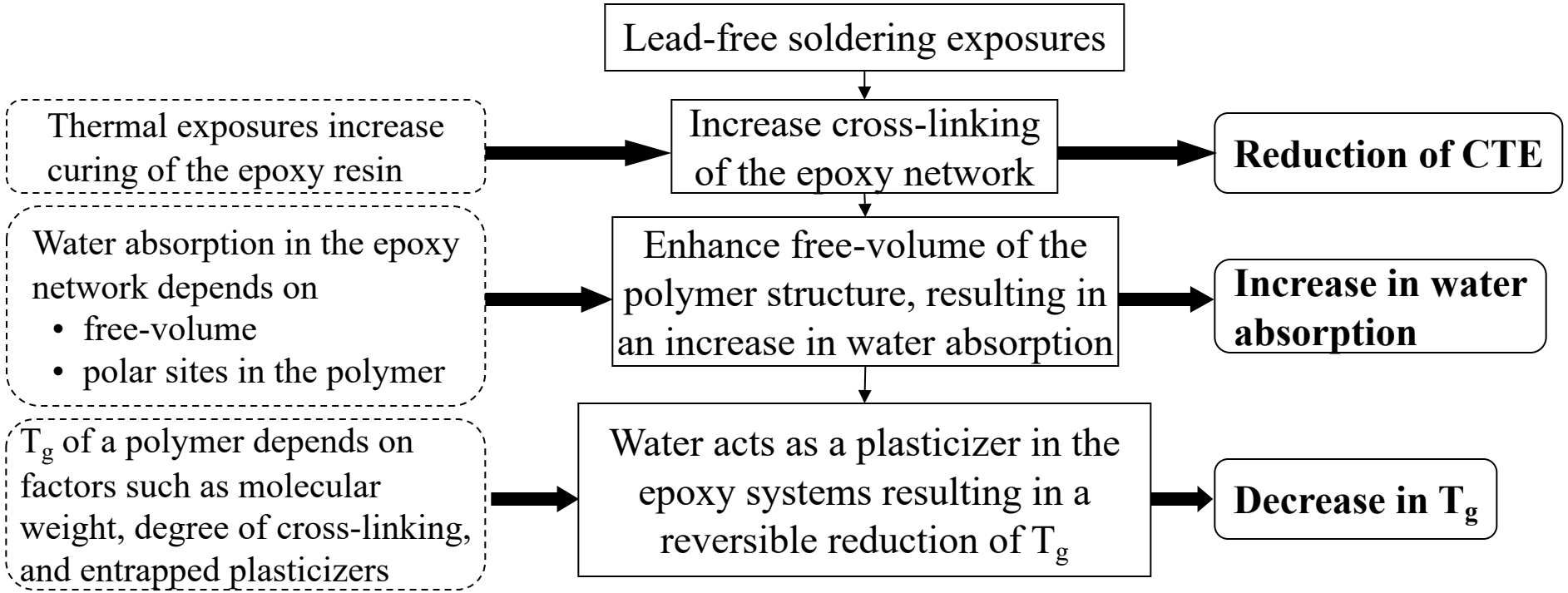




- CTE difference between copper plating and the resin system is at least a factor of 13

- Stress exerted on the plated copper in the plated-through holes in the z-axis can cause cracking.

PCBs After Lead-free Reflow – Effects of Moisture



Property	Observed variation*	Magnitude of variation*
CTE (z)	Decrease	>15%
Water absorption	Increase	>25%
T_g	Decrease	>5°C

FR4 Materials Compared

#	T_g	Curing agent	Fillers present	Halogen free
1	170°C	DICY	Yes	Yes
2	148°C	Phenolic	Yes	No

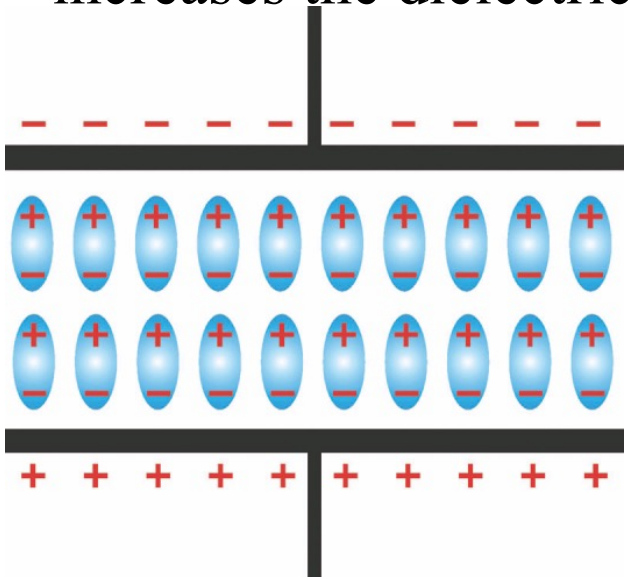
Effect of Moisture on D_k and D_f

- Exposure to humidity impacts PCB materials' dielectric properties
  - D_k and D_f increase linearly with an increase in the moisture content of the PCB materials. With specimen moisture content increasing from 0 to 0.98%, the D_k increased ~5.13% and the D_f increased ~74.5% [1].
- The two most important phenomena are
  - Dipole polarization due to polar molecules and;
  - Interfacial polarization caused by inhomogeneities in the material.

L. Ma, B. Sood, and M. Pecht, ECS Transactions Vol. 27, Iss. 1, pp. 227-236; China Semiconductor Technology Int'l Conf. 2010: Metrology, Reliability and Testing, Shanghai, China, March 18-19, 2010.

Effect of Moisture on D_k and D_f

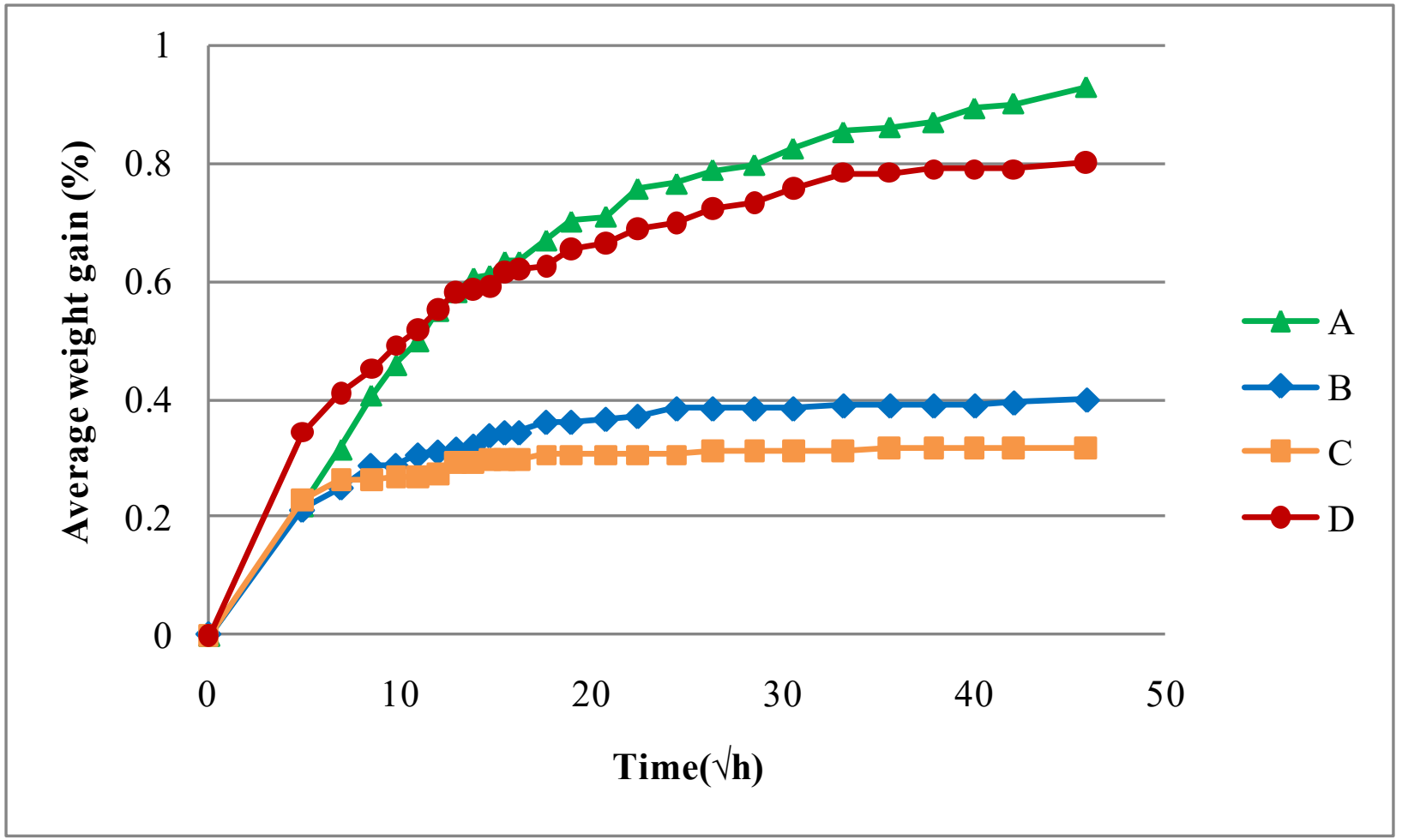
- Water has extremely polar O-H bonds and a D_k value close to 80. Water molecules will increase the dipole polarization due to polar molecules and interfacial polarization caused by inhomogeneities in the material.
- Even a small amount of absorbed moisture significantly increases the dielectric properties.



Schematic view of a capacitor

A capacitor with a dielectric medium of higher D_k will hold more electric charge at the same applied voltage. In other words, its capacitance will be higher.

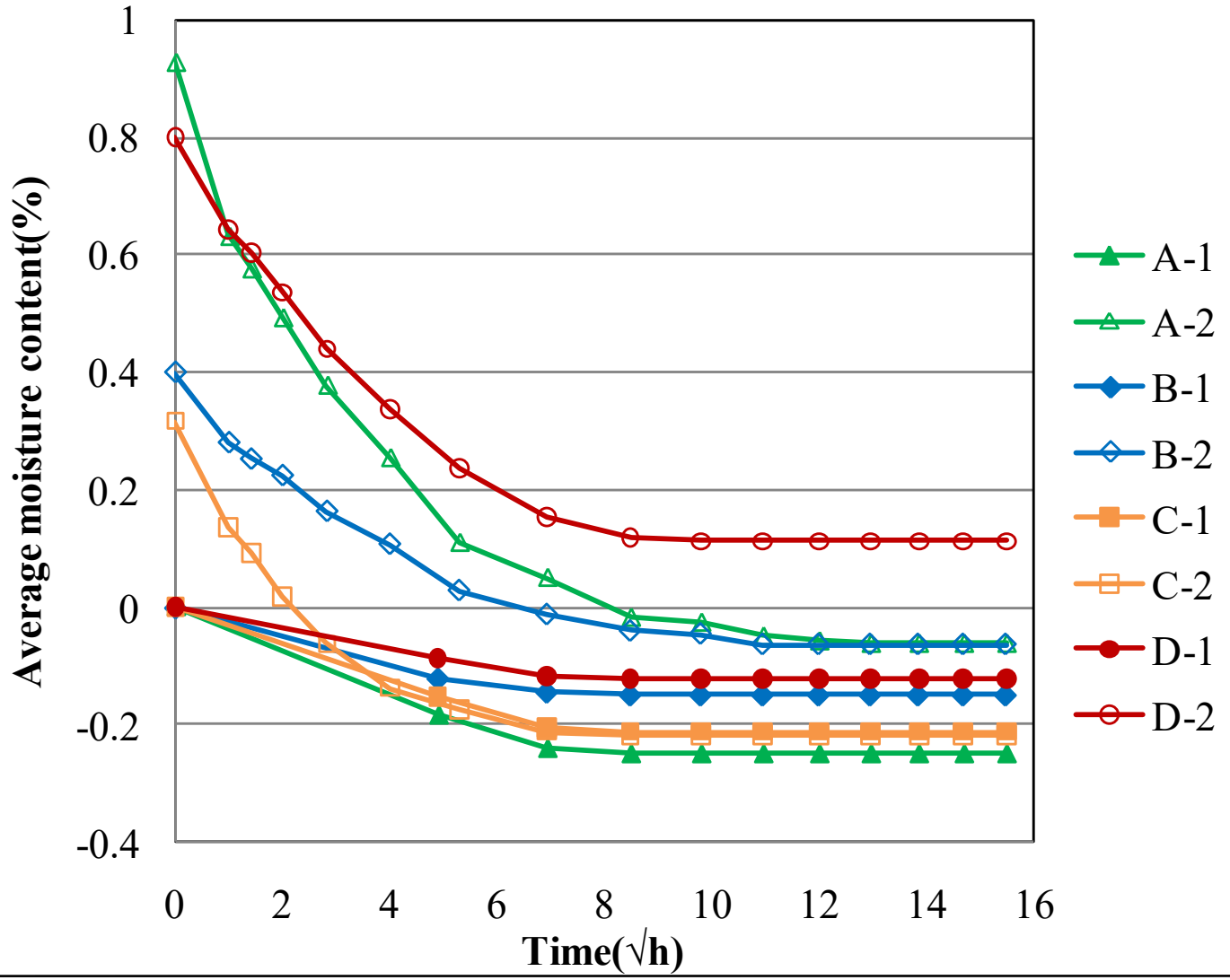
Moisture Absorption Experiment



Moisture absorption experiments were conducted on two coupons (10mm×10mm and 20mm×20mm) of each PCB material, which were exposed in 85ºC and 85% RH condition and the coupons were taken out of chamber to measure weight at increasing time intervals.

Moisture Desorption Experiment

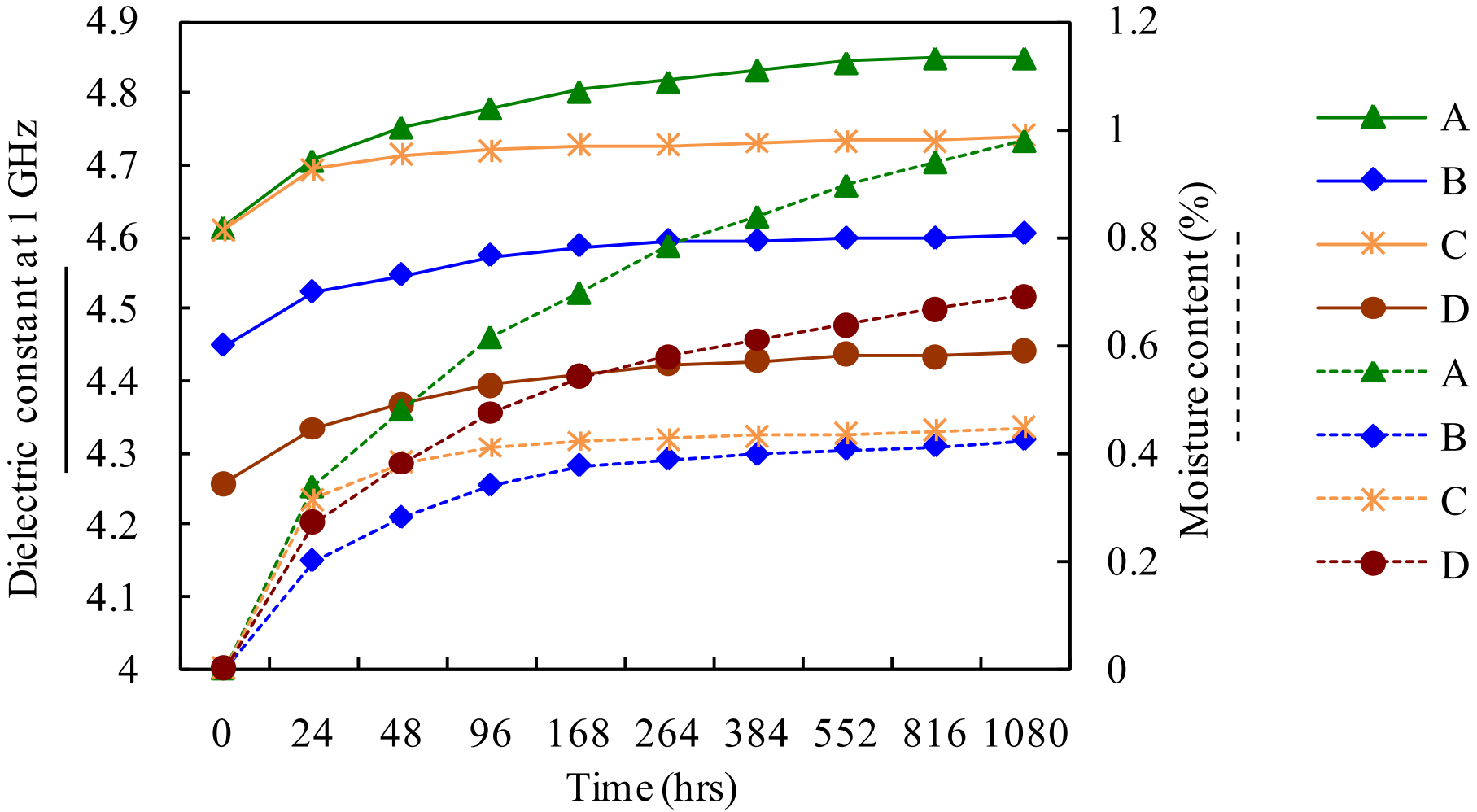
Upon bake, test coupons did not release the moisture absorbed during 85°C/85%RH.



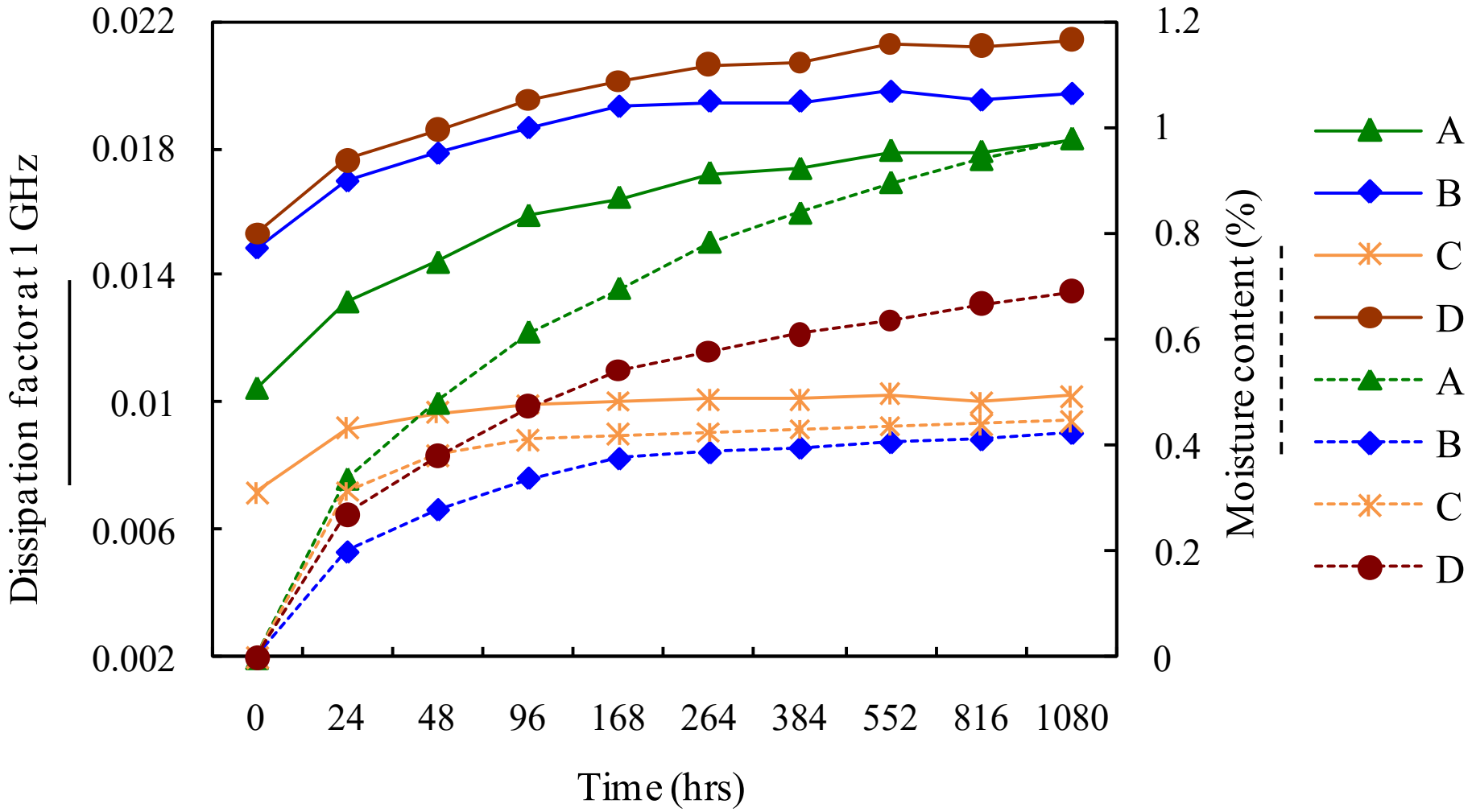
Samples for moisture desorption experiment were baked at 105°C, two initial conditions:

1. **Baked from room storage condition.**
2. **Baked after moisture absorption in 85/85 for 2112 hours.**

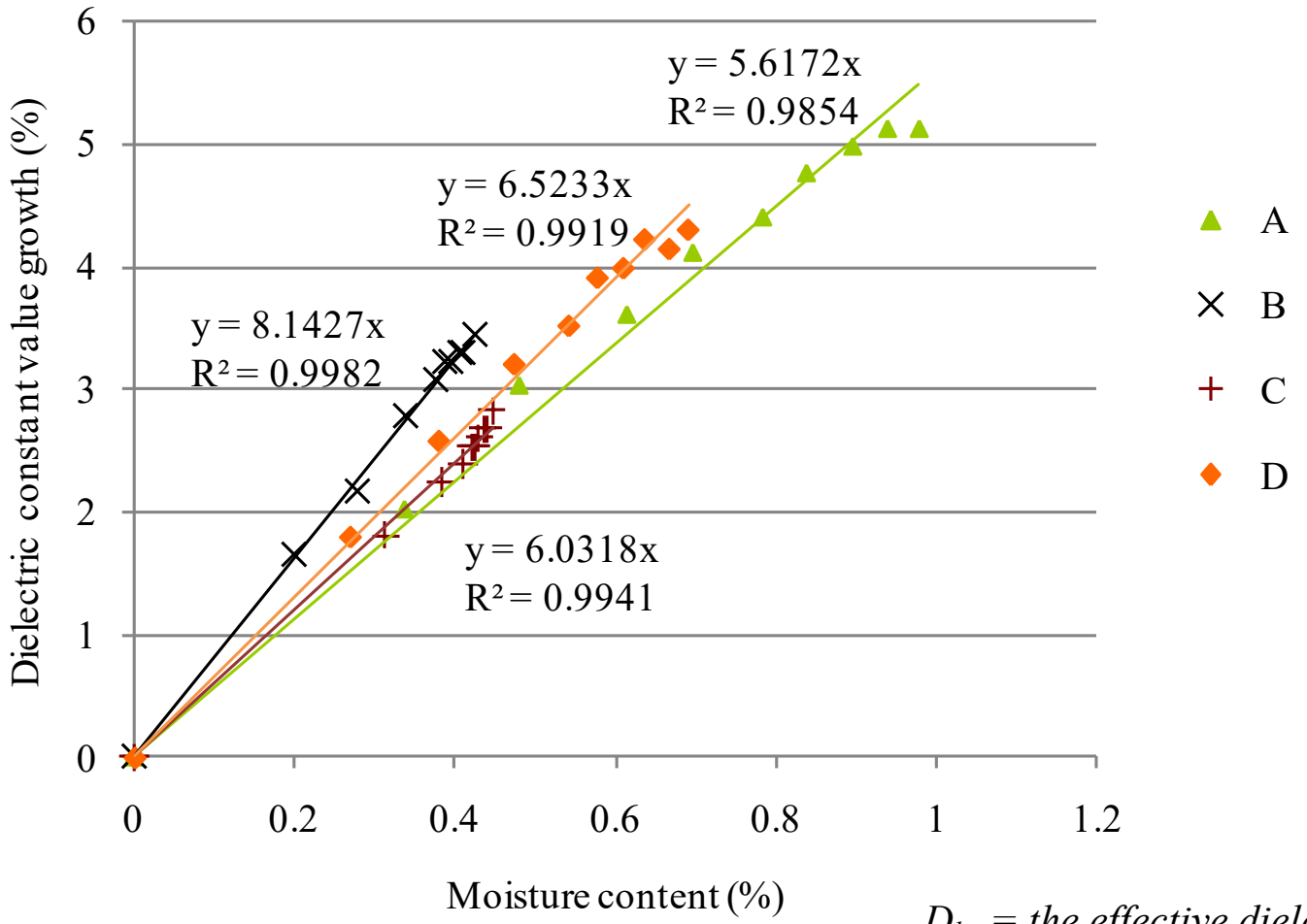
Effect of Moisture on D_k



Effect of Moisture on D_f



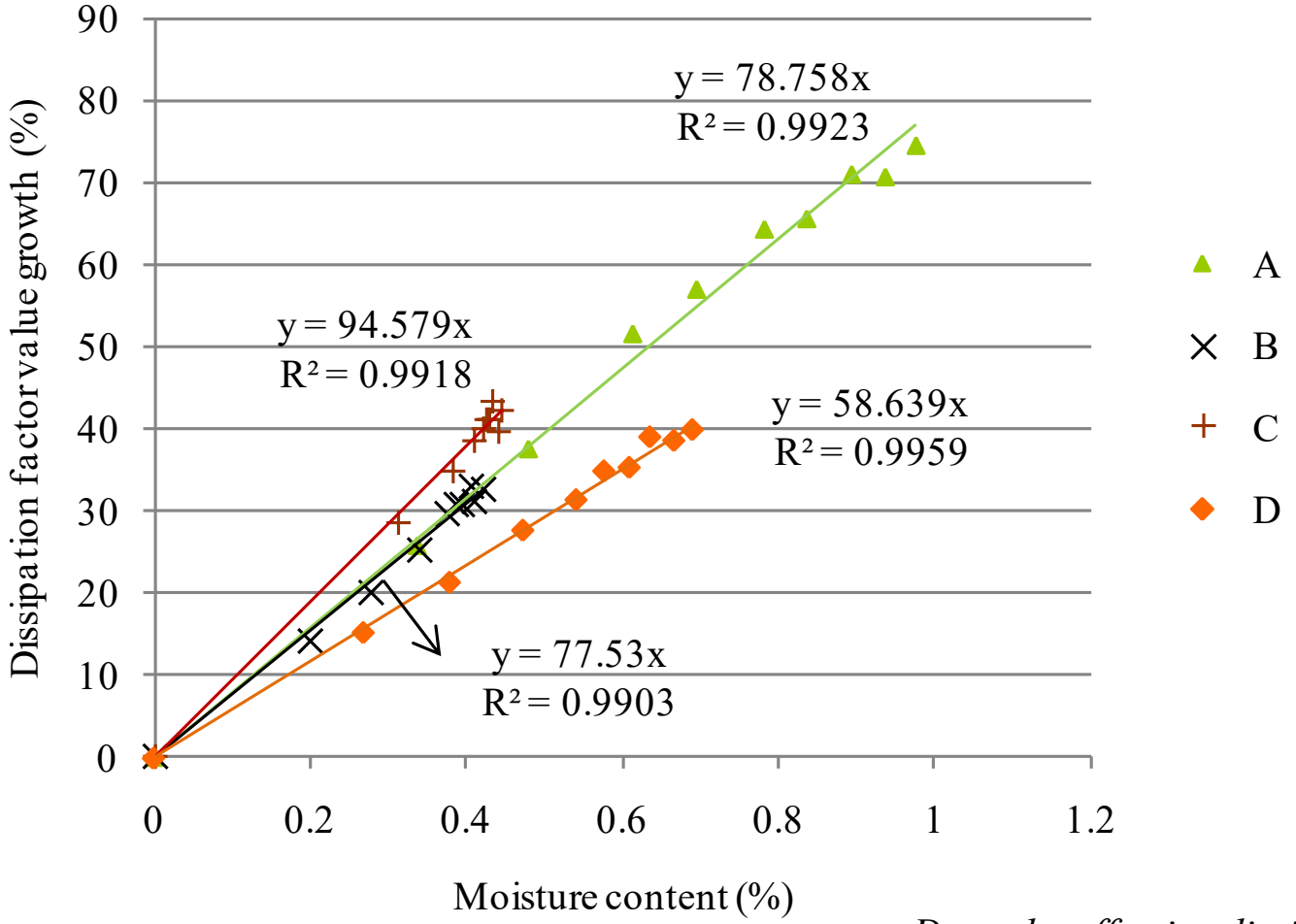
Effect of Moisture on D_k



$$\frac{D_{kn} - D_{k0}}{D_{k0}} = \alpha C_w \Leftrightarrow D_{kn} = D_{k0}(1 + \alpha C_w)$$

D_{kn} = *the effective dielectric constant*
D_{k0} = *the initial dielectric constant*
α = *factor*
C_w = *the moisture content*

Effect of Moisture on D_f

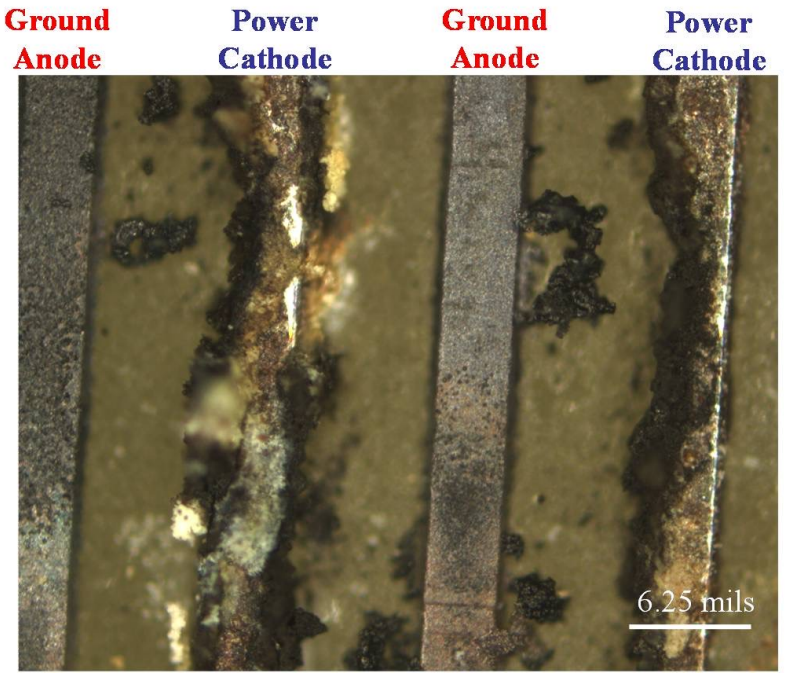


$$\frac{D_{fn} - D_{f0}}{D_{f0}} = \kappa C_w \Leftrightarrow D_{fn} = D_{f0}(1 + \kappa C_w)$$

D_{fn} = the effective dissipation factor
D_{f0} = the initial dissipation factor
κ = factor
C_w = the moisture content

Effects of Adsorbed Moisture on Traces

- Wet corrosion occurs when two metals/alloys connected by a layer of adsorbed moisture – one acts as anode and other act as cathode
  - Either due to different materials or same material with different potential bias.
- Ambient RH and temperature dictate amount water adsorbed.
- Ionic contamination enhances conductivity.
- Shorts occur when moisture creates a bridge across traces.



Corrosion of HASL (10 VDC)

Process of Corrosion

- Requirements
  - Aqueous medium (moisture)
  - Metal (solder)
  - Corrosive agent (flux)
  - Oxygen or carbon dioxide
- Outcomes
  - Continuous (corrosive agent is recycled)
  - Terminated (creation of a passivation layer on metal)
  - Terminated (presence of depolarization agent in flux)

Electrochemical potential of metals in contact with water

Red.	⇔	Ox.	+	e^-	E^0[Volt]
Mg	⇔	Mg^{2+}	+	$2e^-$	−2,37
Al	⇔	Al^{3+}	+	$3e^-$	−1,66
Mn	⇔	Mn^{2+}	+	$2e^-$	−1,19
Zn	⇔	Zn^{2+}	+	$2e^-$	−0,76
Cr	⇔	Cr^{3+}	+	$3e^-$	−0,74
Fe	⇔	Fe^{2+}	+	$2e^-$	−0,44
Cd	⇔	Cd^{2+}	+	$2e^-$	−0,40
Co	⇔	Co^{2+}	+	$2e^-$	−0,28
Ni	⇔	Ni^{2+}	+	$2e^-$	−0,23
Sn	⇔	Sn^{2+}	+	$2e^-$	−0,14
Pb	⇔	Pb^{2+}	+	$2e^-$	−0,13
H_2	⇔	$2H^+$	+	$2e^-$	0,00
Cu	⇔	Cu^{2+}	+	$2e^-$	+0,34
Ag	⇔	Ag^+	+	e^-	+0,80
Pd	⇔	Pd^{2+}	+	$2e^-$	+0,99
Pt	⇔	Pt^{2+}	+	$2e^-$	+1,20
Au	⇔	Au^{3+}	+	$3e^-$	+1,50



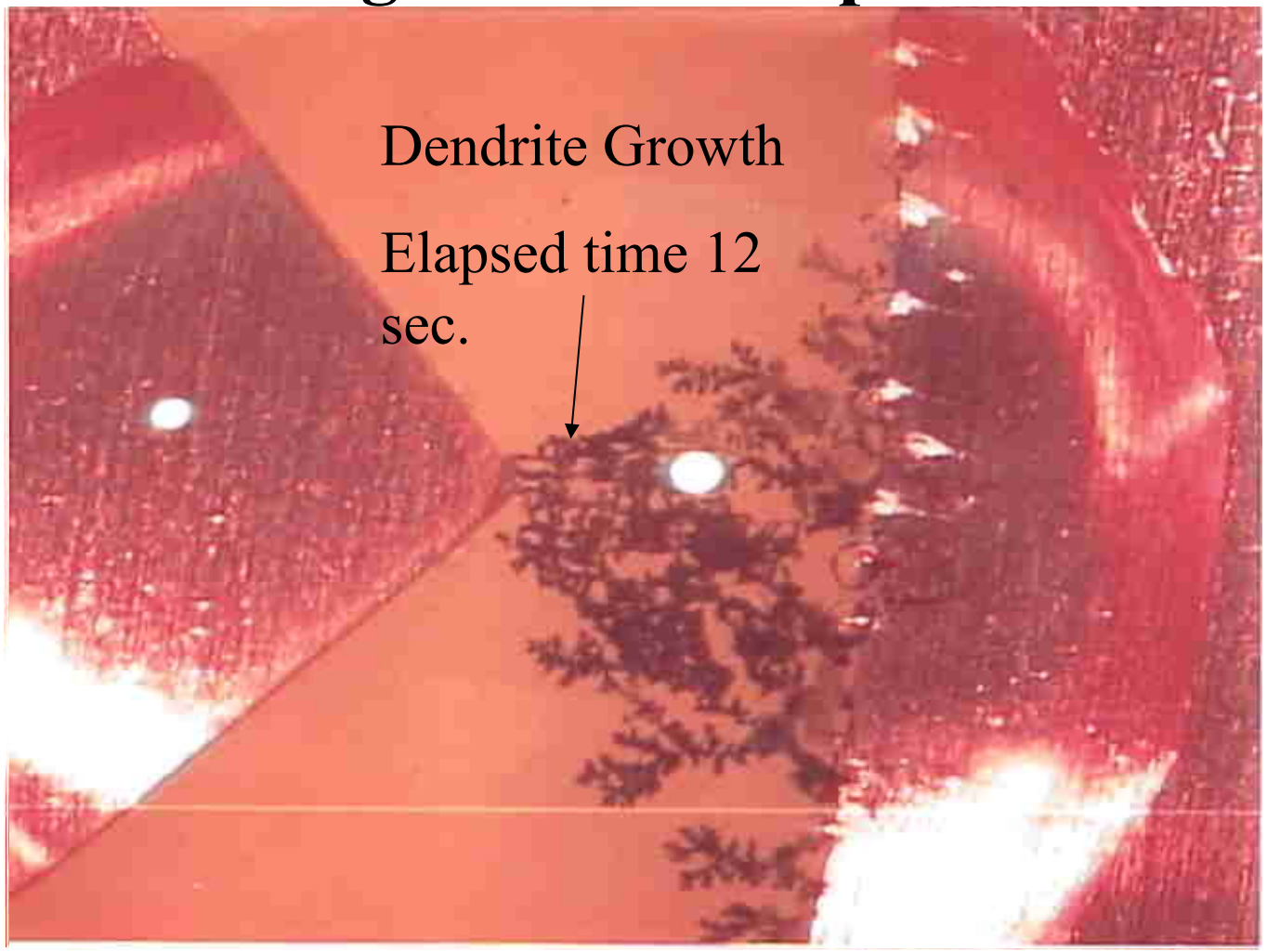
Electro-Chemical Migration

- **Electrochemical migration** (ECM) is the growth of conductive metal filaments (dendrites) on or through a printed circuit board (PCB) through an electrolytic solution (usually H_2O) under the influence of a DC voltage bias [1].
- **Surface Insulation Resistance** (SIR) is the resistance between two electrical conductors separated by some dielectric material(s) [2].

- Failure mechanism: ECM through electrodissolution, ion transport, and electrodeposition
- Failure modes: electrical shorts and drops in SIR
- Failure sites: wherever moisture, oppositely biased conductors, and contamination exist simultaneously; e.g., between the traces on a printed circuit board

1. IPC Publication IPC-TR-476A, "Electrochemical Migration: Electrically Induced Failures in Printed Wiring Assemblies," Northbrook, IL, May 1997.
2. IPC Publication IPC-9201, "Surface Insulation Resistance Handbook," Northbrook, IL, July 1996.

Dendritic Growth During a Water Drop Test *



*From Contamination Studies Laboratory, Inc., http://www.residues.com

Factors Influencing ECM

- Temperature
- Humidity
- Voltage Bias/Voltage Gradient
- Conductor Spacing
- Contamination (type and concentration)
  - Halide vs non-halide
  - Organics
- Conductor material (copper, silver, tin/lead, etc.)
- Conductor geometry
- Surface topology
- Conductor pre-treatment and surface condition
  - Conductor surface roughness, scratches/pits, presence of solder mask and conformal coatings
  - Permeability of coatings
- Substrate composition (FR-4, $BaTiO_3$, etc.)
- Electrolyte (e.g., water, rosin)
- Gaseous pollutants (Cl_2, H_2S, SO_2)
- Ambient air velocity
- Conductor configuration (comb)

Preventative Actions for ECM
Reduce Moisture

- Ensure proper solder mask coverage
- Conformal coatings
  - Barrier to external sources of contamination.
  - Reduce moisture absorption
  - Ineffective against intrinsic contaminants
  - Delamination of coating from board can accelerate ECM due to moisture condensation

Introduction to Conformal Coatings

Conformal Coating

- Conformal coating is defined as a thin polymeric layer.
- The application of conformal coating is to protect the components on PCB from the environments.
- The conformal coating is required not only to protect the circuit against the effects of environmental hazards, but also to provide good dielectric characteristics and moisture resistance.
- The selection of conformal coatings is rely on the protection requirement for PCB.

Required Performance for Conformal Coating

- Excellent dielectric characteristics
- High insulation resistance
- Excellent environmental resistance
- Tenacious adhesion to difficult substrates
- Excellent moisture and thermal shock resistance
- Non-slumping viscosities
- Excellent abrasion resistance

Some Conformal Coating Specifications

- MIL I-46058C: Insulating compound, electrical (for coating printed circuit assembles)

- IPC CC-830: Qualification and performance of electrical insulation compounds for printed board assembles

Common Coating Failure Mechanism (1/2)

- Capillary flow: Cause by low viscosity or high surface tension of the conformal coating, surface energy of substrate
- Delamination: Caused by contaminations on substrate, surface energies mismatch (poor adhesion), moisture permeation
- Cracking: Caused by too high cure temp, large CTE mismatch due to the excessive coating thickness
- De-wetting: Caused by residues or contaminatoins on substrate

* SCH Technologies, http://www.conformalcoating.co.uk/technicalbulletins.php

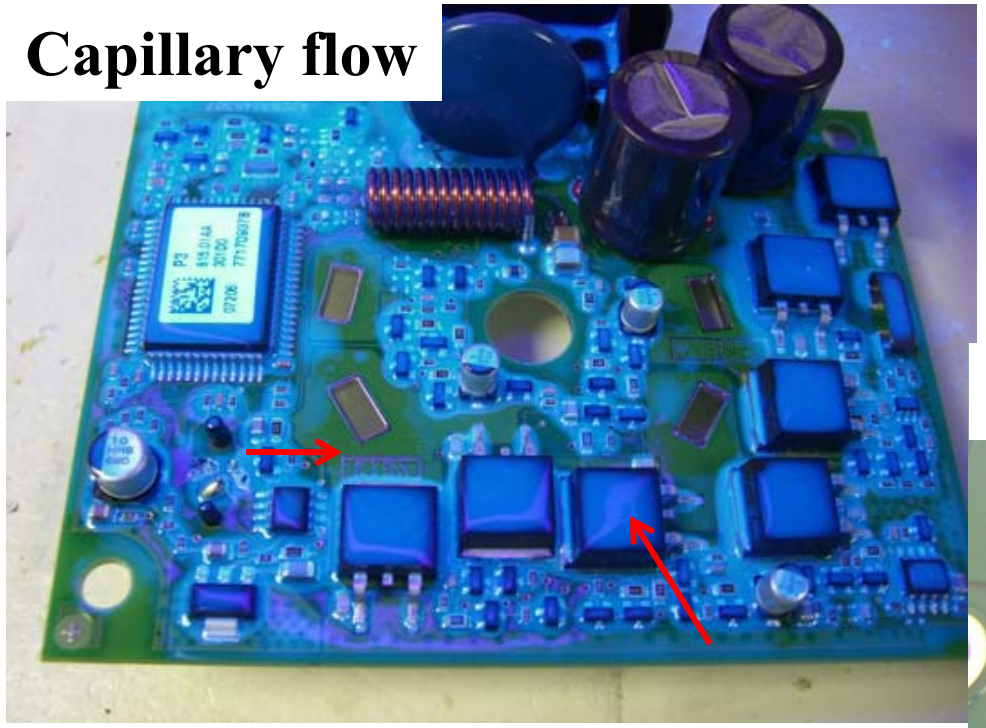
Common Coating Failure Mechanism (2/2)

- Corrosion: Caused by improper cleaning method or handling
- Orange Peel: Caused by incorrect thickness of the coating or cure profile

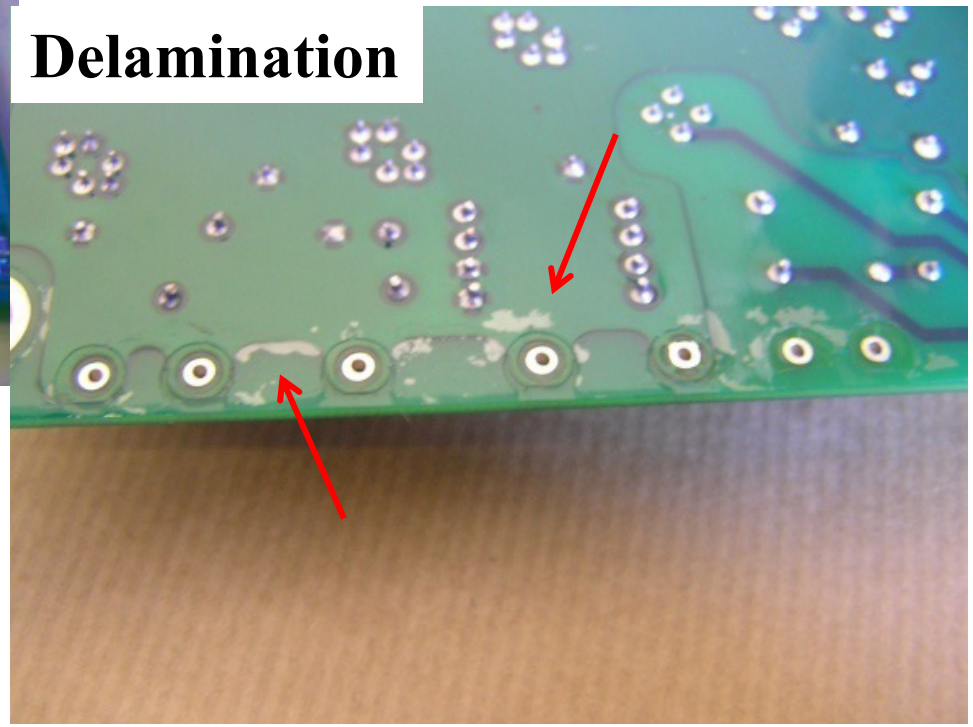
* SCH Technologies, http://www.conformalcoating.co.uk/technicalbulletins.php

Examples of Common Coating Failure 1/2

Capillary flow



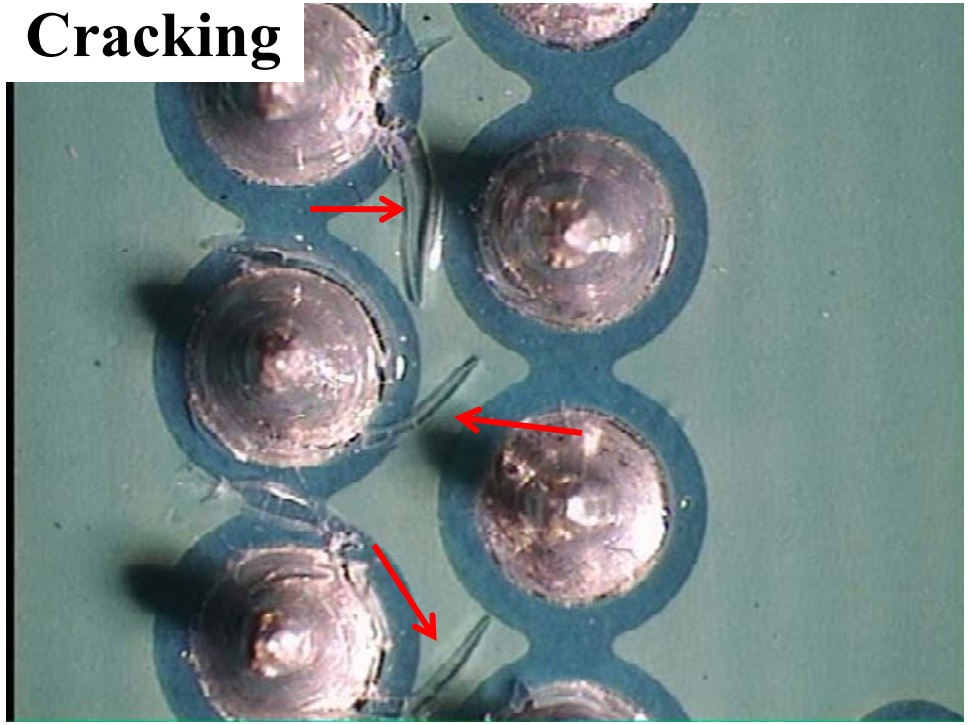
Delamination



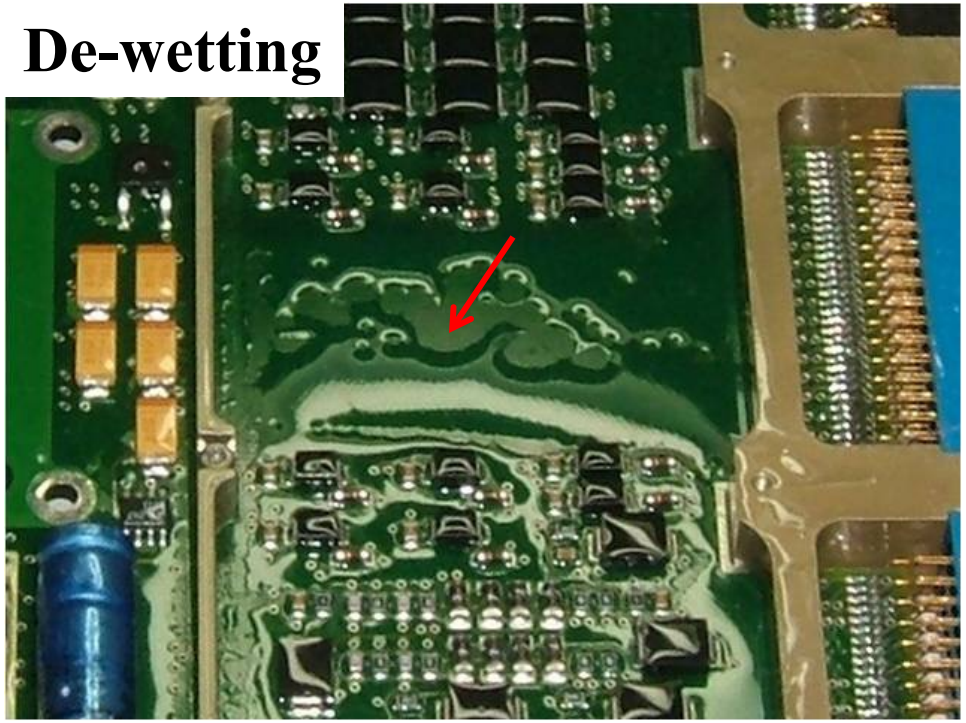
* SCH Technologies, http://www.conformalcoating.co.uk/technicalbulletins.php

Examples of Common Coating Failure 1/3

Cracking



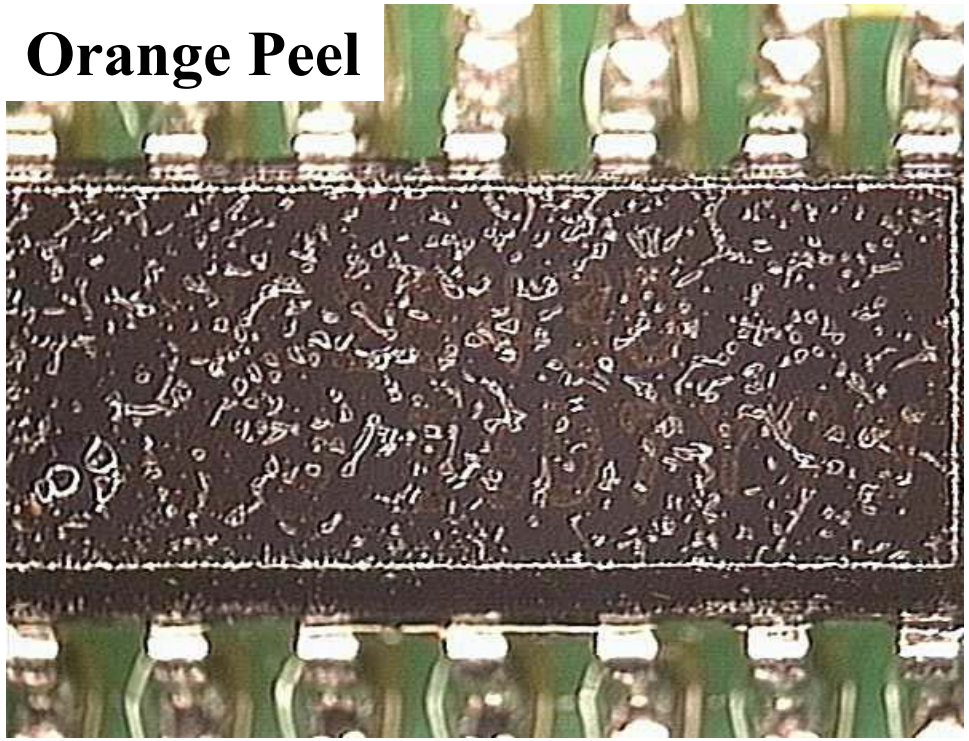
De-wetting



* SCH Technologies, http://www.conformalcoating.co.uk/technicalbulletins.php

Examples of Common Coating Failure 1/3

Orange Peel



* SCH Technologies, http://www.conformalcoating.co.uk/technicalbulletins.php

Conformal Coating Manufacturers

- Humiseal
- Dow Corning
- Dymax
- Tech Spray
- Cytec
- Emerson & Cuming
- Loctite

Physical Properties

- Viscosity
- Hardness
- Adhesion
- Modulus of Elasticity

Test Methods – Viscosity

Manufacturer	*Test methods*
Humiseal	ASTM D-4287
Dow Corning	-
Dymax	ASTM D-2556
Tech Spray	-
Cytec	
Emerson & Cuming	ASTM D-2393
Loctite	Not provided

1. ASTM D-4287 “Standard Test Method for High-Shear Viscosity Using a Cone/Plate Viscometer”
2. ASTM D-2556 “Standard Test Method for Apparent Viscosity of Adhesives Having Shear-Rate-Dependent Flow Properties”
3. ASTM D-2393 “Test Method for Viscosity of Epoxy Resins and Related Components”

Test Methods – Hardness

Manufacturer	*Test methods*
Humiseal	Not provided
Dow Corning	-
Dymax	ASTM D-2240
Tech Spray	ASTM D-3363
Cytec	Not provided
Emerson & Cuming	ASTM D-2240
Loctite	Not provided

1. ASTM D-2240 “Standard Test Method for Rubber Property—Durometer Hardness”
2. ASTM D-3363 “Standard Test Method for Film Hardness by Pencil Test”

Test Methods - Adhesion

Manufacturer	*Test methods*
Humiseal	ASTM D 2197
Dow Corning	Not provided
Dymax	Not provided
Tech Spray	ASTM D 3359-08
Cytec	MIL-I-46058C
Emerson & Cuming	Not provided
Loctite	Not provided

1. ASTM D2197 “Test Method for Adhesion of Organic Coatings by Scrape Adhesion”
2. ASTM D3359-08 “Standard Test Methods for Measuring Adhesion by Tape Test”
3. MIL-I-46058C “Insulating compound, electrical (for coating printed circuit assembles)”

Test Methods – Modulus of Elasticity

Manufacturer	*Test methods*
Humiseal	-
Dow Corning	Not provided
Dymax	ASTM D-638
Tech Spray	Not provided
Cytec	Not provided
Emerson & Cuming	Not provided
Loctite	Not provided

1. ASTM D-2240 “Standard Test Method for Rubber Property—Durometer Hardness”
2. ASTM D-3363 “Standard Test Method for Film Hardness by Pencil Test”

Electrical Properties

- Dielectric Breakdown Voltage
- Dielectric Constant & Factor

Test Methods – Dielectric Breakdown Voltage

Manufacturer	*Test methods*
Humiseal	ASTM D-149
Dow Corning	-
Dymax	ASTM D-1304
Tech Spray	ASTM D-149
Cytec	-
Emerson & Cuming	ASTM D-149
Loctite	IEC 60243-1

1. ASTM D-149 “Standard Test Method for Dielectric Breakdown Voltage and Dielectric Strength of Solid Electrical Insulating Materials at Commercial Power Frequencies”
2. ASTM D-1304 “Standard Test Methods for Adhesives Relative to Their Use as Electrical Insulation”
3. IEC 60243-1 “Electrical Strength of Insulating Materials - Test Methods - Part 1: Tests at Power Frequencies”

Test Methods – Dielectric Constant & Factor

Manufacturer	*Test methods*
Humiseal	ASTM D150-65T (1 MHz)
Dow Corning	100 Hz, 1000 kHz, 1 MHz
Dymax	Not provided
Tech Spray	-
Cytec	-
Emerson & Cuming	ASTM D150 (60 Hz)
Loctite	IEC 60250 (1 kHz)

1. ASTM D-150-65T "Standard Test Methods for AC Loss Characteristics and Permittivity (Dielectric Constant) of Solid Electrical Insulation"
2. IEC 60250 "Recommended Methods for the Determination of the Permittivity and Dielectric Dissipation Factor of Electrical Insulating Materials at Power, Audio and Radio Frequencies Including Metre Wavelengths"

Concerns with Rigid-Flex Circuits

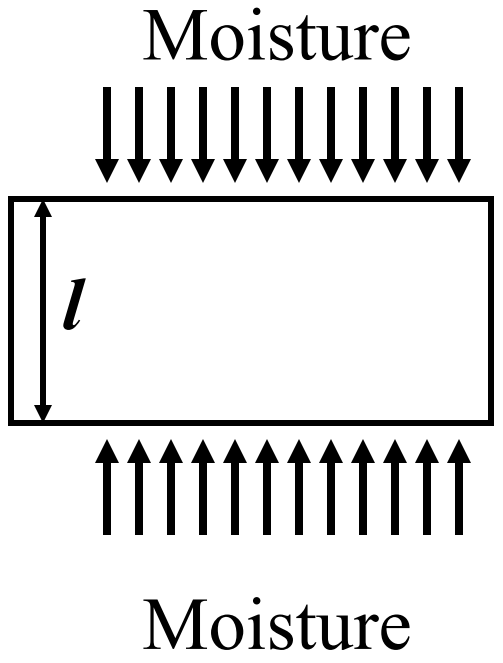
- Polyimide base material readily absorbs moisture at a faster rate than many other base materials (see slide on diffusion coefficients).
  - Absorbed moisture expand rapidly upon exposure to elevated temperature and cause separation, delaminations and blisters.
- Epoxy and acrylic adhesives between base material layers are also prone to excessive moisture absorption.
- Capillary wicking of moisture into pockets along conductor patterns in high density circuits.
  - Pockets are created due to expansion rate mismatches between acrylic and polyimide.
- Bulk moisture can expand rapidly upon exposure to elevated temperature and cause separation, delaminations and blisters.

Common Mechanisms of Moisture Transport

- Bulk diffusion (Fickian) – Bulk diffusion within the epoxy matrix.
- Wicking – Wicking interfaces is another mechanism for moisture transport.
- Capillary – Capillary action is associated with micro-cracks or channels present in the epoxy.

Bulk Diffusion

- Diffusion is the ability of a molecular, atomic, or ionic species to migrate into the bulk phase of a second material time-dependently.
- For many polymeric resin systems, diffusion can be classified as Fickian.
- Fick's law states that in presence of a uniform concentration gradient, the flux of diffusing atoms is proportional to the product of the diffusion coefficient and the concentration gradient (the driving force).

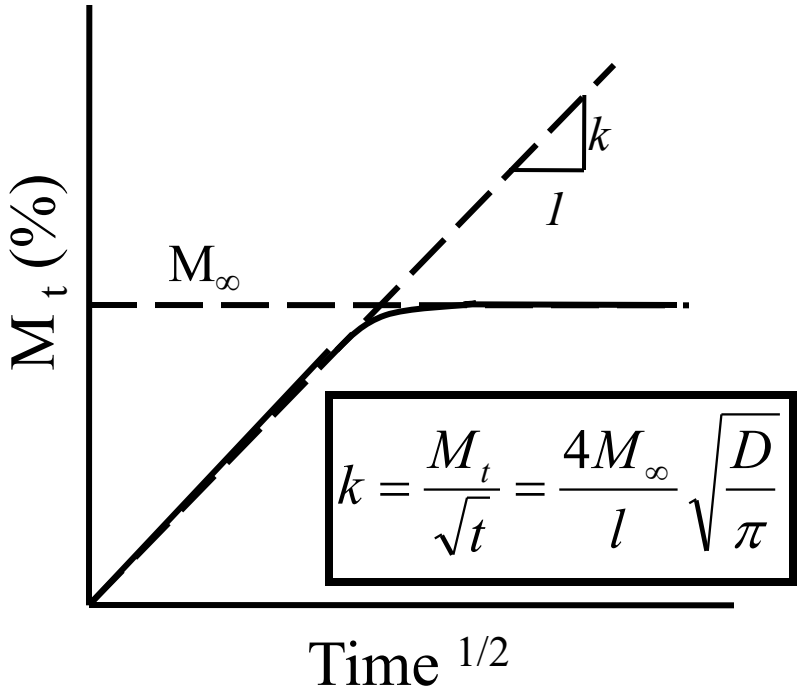


Fickian Uptake Model

For Fickian diffusion in a plane sheet with thickness *l* exposed on both sides to the same environment, the moisture content, Mt, at time t, is given by the expression:

$$\frac{M_t}{M_\infty} = \frac{4}{l}\left(\frac{Dt}{\pi}\right)^{1/2} \Rightarrow$$

$$\Rightarrow D = \pi\left(\frac{M_t l}{4\sqrt{t}M_\infty}\right)^2$$

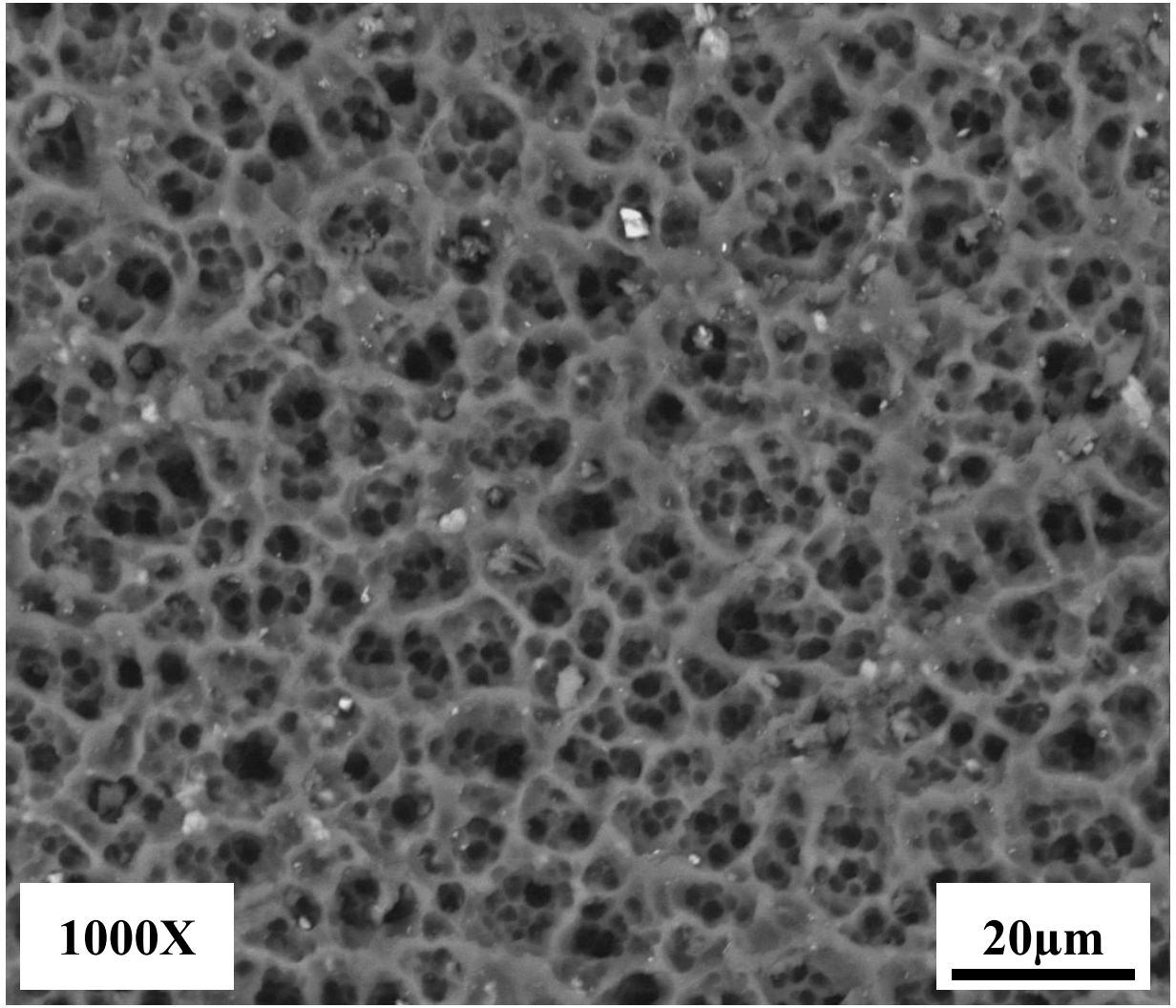


Diffusion Coefficients*

Laminate	Average D ($\times 10^{-8}$)			
	@50°C /50%RH	@50°C /85%RH	@85°C /50%RH	@85°C /85%RH
FR-4 – I	0.74	0.99	3.22	2.27
FR-4 - II	0.82	1.23	2.74	0.93
PI – I	3.30	1.64	8.17	4.65
CE – I	3.44	2.91	11.17	5.75
BT - II	1.22	1.65	4.75	3.03

* - Moisture Ingress into Organic Laminates, M. Pecht, H. Ardebilib, A. Shukla, J. Hagge, and D. Jennings, IEEE Transactions on Components and Packaging Technology, Vol. 22, No. 1, pp. 104-110, March 1999.

ESEM Image of Typical FR-4



Moisture Absorption – Dominant Sites

- Moisture diffusion primarily occurs in the epoxy, reinforcement glass does not readily absorb moisture [1].
  - As a result, the moisture absorption characteristics of PCB dielectric materials will vary by construction and glass fiber/epoxy resin content.
  - The glass reinforcement will act as a barrier to restrict flow and impact the diffusivity between different constructions.
  - Also, the varying glass/epoxy ratios between PCB of different constructions will result in a varying moisture concentration and maximum moisture uptake.
- Different epoxies inherently have different moisture content.

[1] Hamilton, P.; Brist, G.; Guy Jr, B.; and Schrader, J., "Humidity-Dependent Loss in PCB Substrates," Proceedings of IPC Printed Circuit Expo, February 2007.

Bound and Free Water Molecules

The water molecules absorbed into epoxy can be classified into two types [1, 2]:

- "bound" water, which is trapped at polar sites, that is usually bonded to hydroxyl groups in the epoxy network;
- "free" water, which is clustered in the free volume or voids inside the epoxy.

[1] Zhao, H.; and Li, Robert K.Y., "Effect of water absorption on the mechanical and dielectric properties of nano-alumina filled epoxy nanocomposites", Composites. Part A, Applied science and manufacturing, v 39, n 4, pp: 602-611, 2008.
[2] Maggana, C.; and Pissis, P., "Water sorption and diffusion studies in an epoxy resin system", Journal of polymer science. Part A, Polymer chemistry, v37, n 11, pp: 1165-1182, 1999.

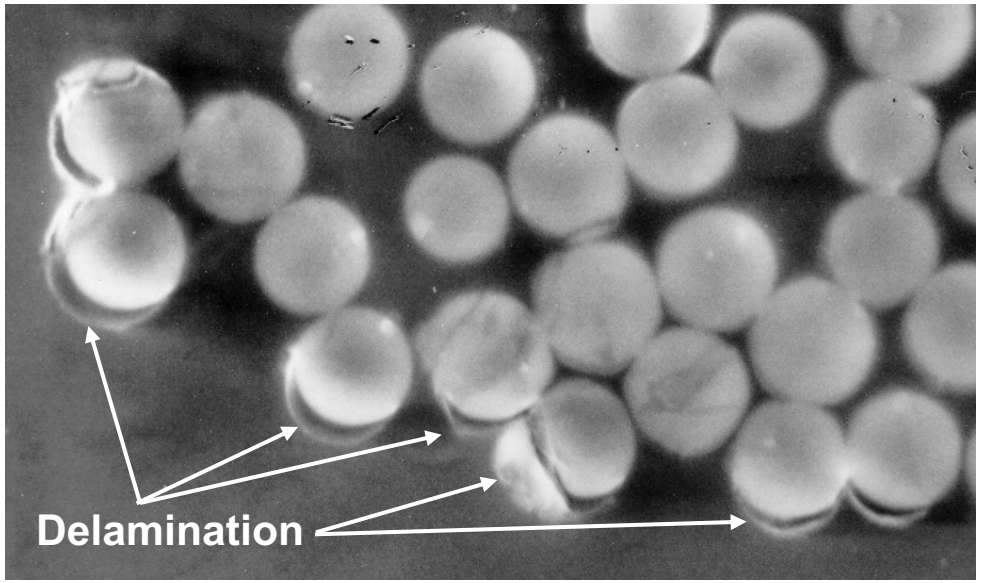
Wicking and Capillary Action

- Although the concept of capillary action is similar to wicking,
  - Distinction lies in that wicking is used to describe enhanced moisture absorption due to voids or cracks at the interfaces.
  - Capillary action is generally used to describe enhanced moisture absorption due to voids or cracks in the bulk.
- The sites for wicking and capillary action are present in the form of voids or cracks that may form by the addition of fillers.
- Bulk diffusion is dominant in the moisture transport.

Wicking

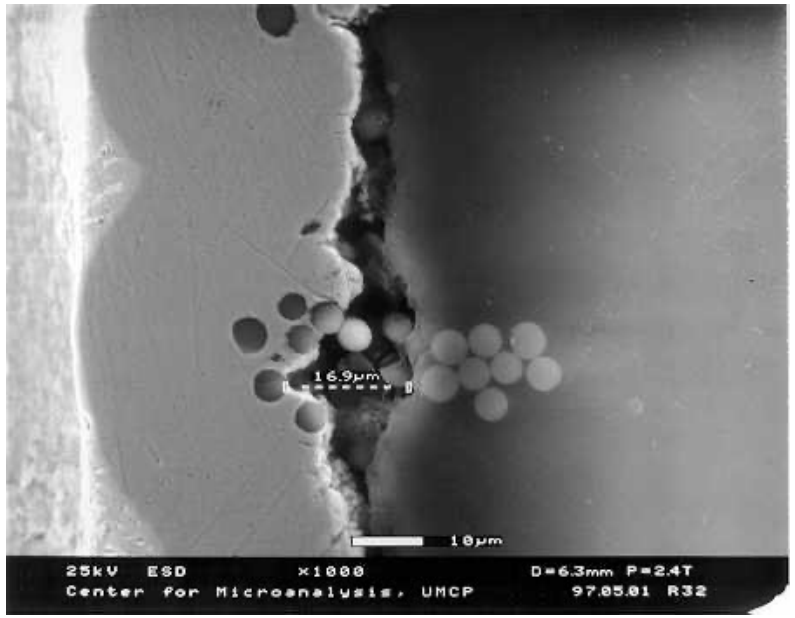
- Wicking involves ingress of moisture absorbed by epoxy glass at board edge.

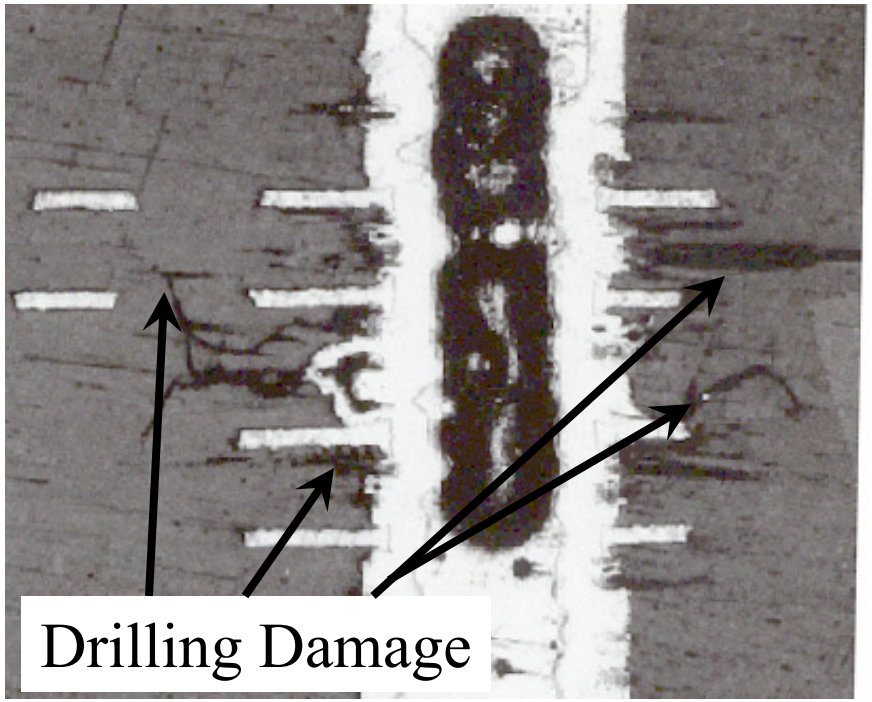
- Fiber/resin interface delamination occurs as a result of stresses generated under thermal cycling due to a large CTE mismatch between the glass fiber and the epoxy resin (approximately 5.5 ppm/°C and 65 ppm/°C.



Capillary Action

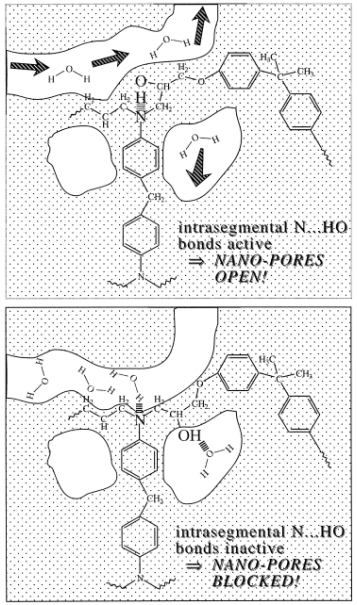
Capillary action is generally used to describe enhanced moisture absorption at cracks or voids.

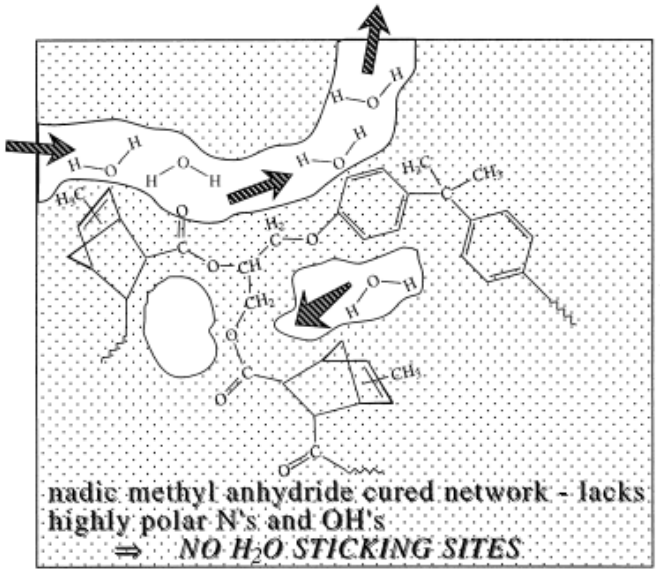




Wicking in PCBs

- Wicking occurs as a result of capillary action.
- Capillary action is a result of surface tension acting on the liquid's leading edge.
- Geometry, material properties, and environmental conditions can all affect how a fluid wicks.





Molecular Mechanisms of Moisture Transport

1. Oh. "EE428 BioMEMS and LOAC – Lecture 10: Capillary-Driven Microfluidics". University of Buffalo, The State University of New York. (2010).
2. Soles and Yee. "A discussion of the molecular mechanisms of moisture transport in epoxy resins"/ Journal of Polymer Science Part B: Polymer Physics 38.5. (2000).

Effects of Trapped Moisture

- Upon exposure to reflow, moisture trapped inside a PCB turns to steam.

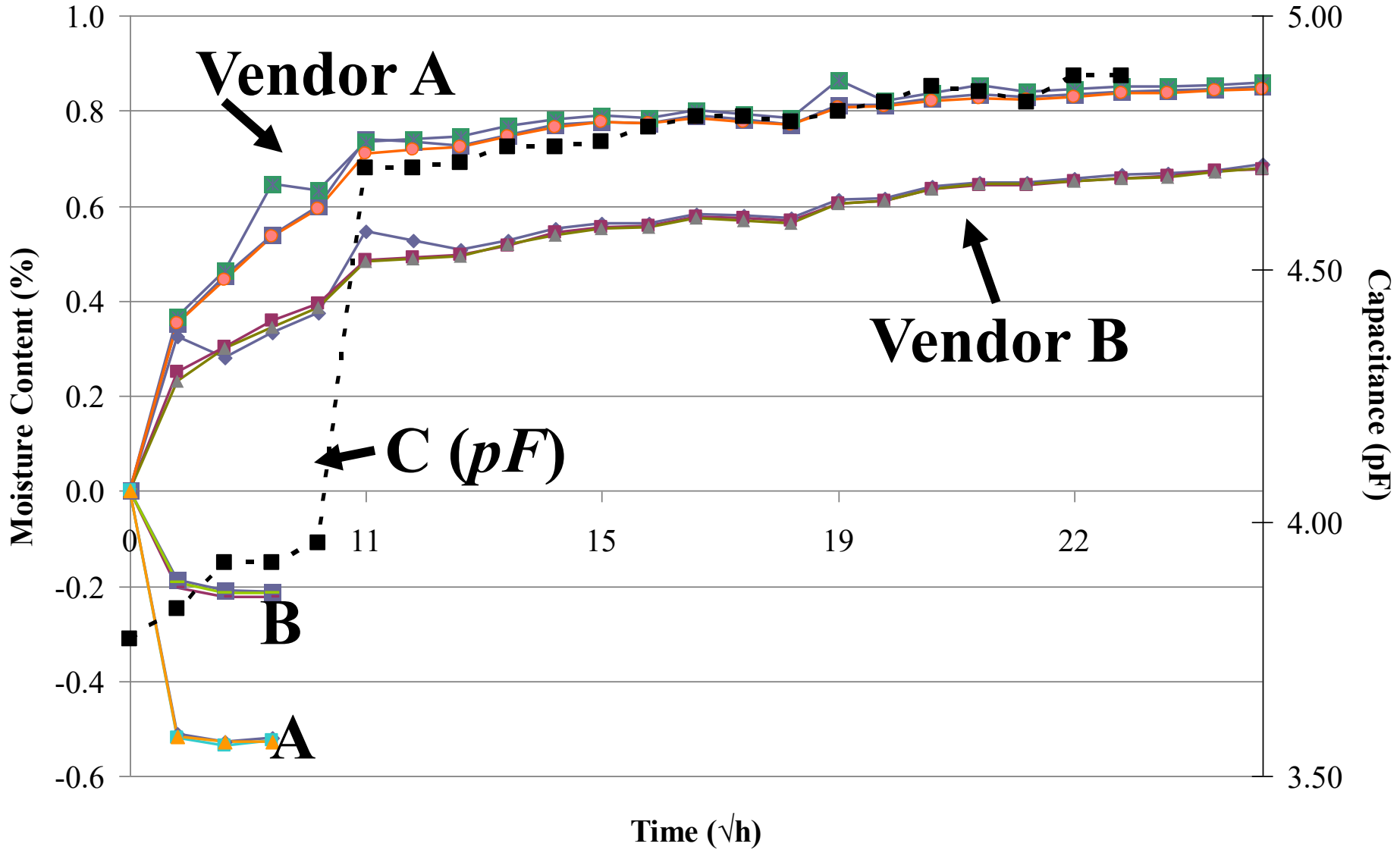
- The steam expands rapidly when the PCB is exposed to the high temperature of VPR (vapor phase reflow), IR (infrared) soldering, or, if the PCB is submerged in molten solder, wave soldering.

- Pressure from this expanding moisture can cause internal delamination, internal cracks that do not extend to the outside, bond damage...
  - In severe cases, the stress can result in external cracks.

Capacitance Measurement Nets in PCBs

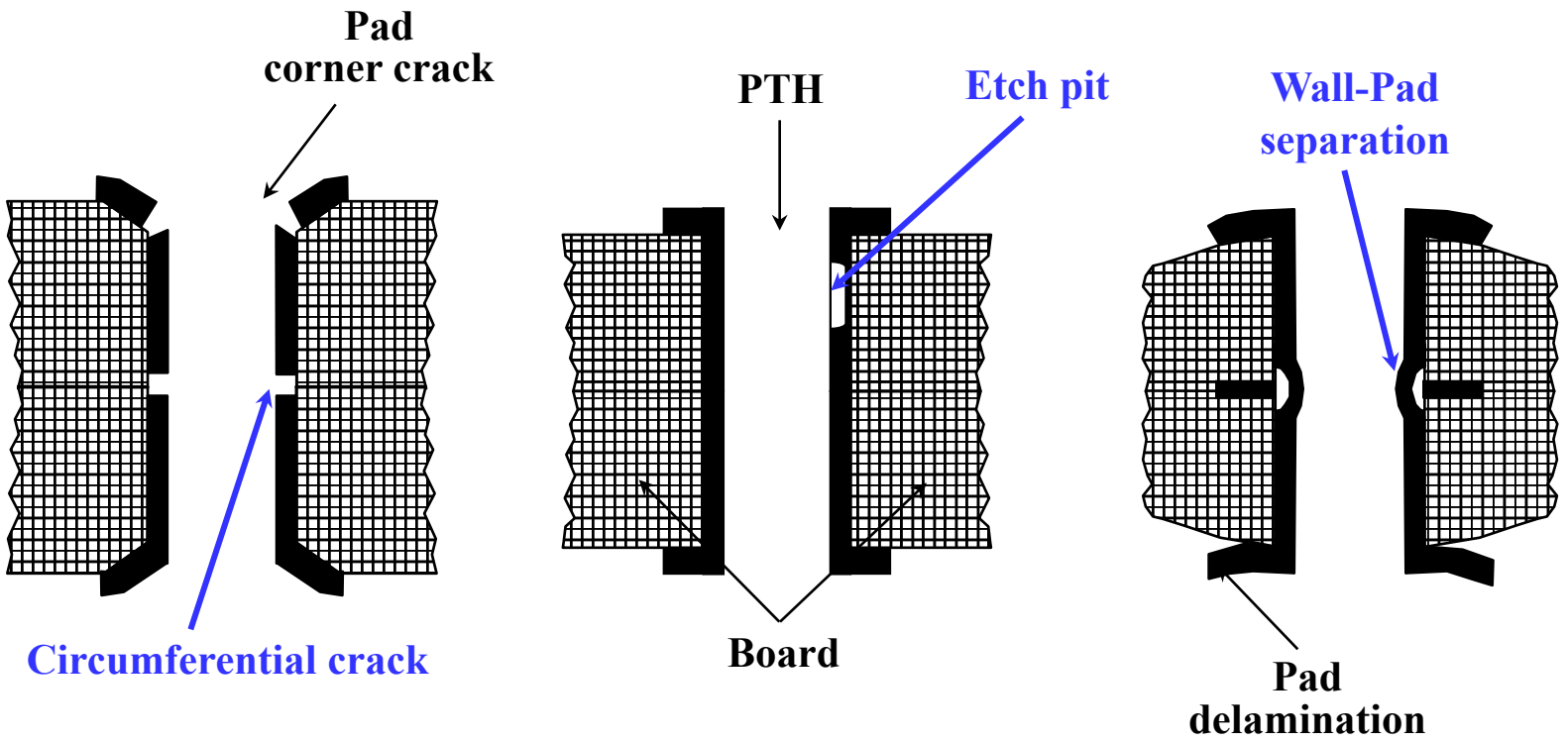
- Capacitance monitoring method is used to measure the moisture content of PCBs.
- Method allows for in situ evaluation of a laminate's moisture content.
- Inner layer copper plates simulate a parallel-plate electrical capacitor.
  - The capacitance of the laminate material increases (linearly) with moisture uptake during CFF experiment absorbed.
- Test coupons are initially calibrated by environmental exposure at 50°C/85%RH to induce moisture permeation, followed by periodic removal to measure capacitance and to weigh for moisture content.
- Results of the calibration exercise demonstrate PCB capacitance change with moisture content.

Moisture Absorption Behavior



Case Study and Discussion – PTH Fails

PTH Failures



Plated Through Hole (PTH) Failures

- Circumferential cracking
  - Single event overstress
  - Cyclic fatigue
- Openings (voids, etch pits)
  - Accelerate circumferential cracking
- Wall-Pad Separation
  - Also known as “breakout of internal lands” or “plated-barrel separation”

Moisture Control Guidelines

Introduction

- Materials used in PCB manufacturing should be protected from stresses induced during fabrication, handling or storage.
- Laminators, fabricators and end users are responsible for protection of PCB from excessive moisture.
  - Parties should ensure that effective process controls are implemented.

IPC-1601

- Guidelines on the handling, packaging and storage of printed boards (out August 2010).
  - Provides guidance on protection of PCB from contamination, physical damage, solderability degradation, electrostatic discharge and moisture uptake.
  - Covers all phases of production, from the manufacture of the bare printed board, through delivery, receiving, stocking, and soldering.
- Guidance on moisture concerns
  - Guidance on establishing recommended moisture levels
  - Baking profiles for moisture removal
  - Covers impact of baking on printed board solderability.

Should you Bake Prepregs?

- If prepregs are suspected of being stored in uncontrolled environments for extended periods.
  - Prepregs have higher moisture uptake rate

- Some fabricators may bake prepregs prior to lamination to remove moisture responsible for blisters.

- In most cases, bake is unnecessary and will not influence subsequent shrinkage or blisters.

Bake Post-lamination?

- Generally post-lamination bake is used to increase degree of epoxy cure and/or eliminate warpage.

- However, a properly run lamination cycle, in accordance with manufacturers specification, with controlled cooling, should produce warp-free panels.

- A properly run lamination cycle will attain required degree of epoxy cure.

Controls During Inner Layer Production – 1

- PCBs typically experience higher moisture absorption rates after photo imaging, etching and drilling processes (moisture may be entrapped inside PCB features).

- Minimize moisture absorption in etched cores.

Controls During Inner Layer Production – 2

- Laminates are at greater risk of moisture absorption.
  - Process flow should be designed to minimize the time between baking and lamination to prevent moisture absorption into the laminated panel.
- Etching, drilling, and plating of sub composites adds moisture absorption avenues.
  - Minimizing hold times or controlling storage conditions will help reduce moisture uptake in the sub composite.
- Once fabricated, PCBs should be placed in Moisture Barrier Bags (MBB) to ensure that no moisture is absorbed during transit.

Post Drill Bake

- Post drill bake is a known mitigation strategy against pink ring.
  - Pink ring is a localized delamination at the inner-layer oxide caused by a chemical attack on the surfaces that are exposed by cracks introduced during drilling.
- Post drill bake will provide a cosmetic fix by relaxing the epoxy enough to close the crack, but fails to reseal the crack.
  - The bake cures the epoxy smear and makes it difficult to remove.
- A solution to pink ring is to prevent drill cracking by using an innerlayer surface treatment.

Controls Implemented During Assembly – 1

- Inspect HIC at receiving.
- Verify that the HIC is authentic!!
- Always read HIC at room temperature (23 +/- 5°C).
- A pink dot indicates greater than 10% humidity
- Reseal packages promptly.

Source: Peregrine and IPC-1601

Controls Implemented During Assembly – 2

- Audit warehouse/staging/production for temperature, humidity and handling controls.
- Practice FIFO (First In/ First Out).
- Monitor reflow profiles.
- Open package just prior to assembly.

Controls Implemented During Assembly – 3

- Rework Processes – use prescribed board preheat for lead free rework.
- Baking process during assembly should also factor in presence of temp sensitive components.
  - Friction from compressed air driven drying processes may cause ESD failures.

Guidelines for Baking – Bake Parameters – 1

- Set oven below maximum operating temperature (MOT).
- Bake temperature should always be set below T_g.
- Higher temperatures (but below MOT, Tg etc) may degrade finish and solder mask.
- Always bake above 100°C (boiling point of water)
  - Consider baking in vacuum?

Selecting a Bake Temperature

- Bake temperature should always be set below T_g.
- At Tg many properties change abruptly
  - Young's modulus, shear modulus, specific heat.
  - Beyond Tg, PCB begin to lose mechanical strength due to softening of the resin.
  - Exhibit large discontinuous changes in Z axis CTE that can cause inner layer delaminations or between resin and glass fibers.

Guidelines for Baking – Bake Parameters – 2

- Establish bake time by repeated gravimetric measurements at predefined time intervals (IPC-TM-650 2.6.28).

- J-STD-033 recommends 125°C baking to a maximum of 48 hours.

- In addition to baking, cooling down in controlled environments is always necessary (desiccators may be suitable for smaller PCBs).

Moisture Absorption and Gravimetric Measurements

- IPC-TM-650 2.6.28
- The test is a process control tool
  - Determine the bulk moisture content.
  - Moisture absorption rate.
  - Determine whether the specimen conforms to the monitoring level of the user's performance specification.
- Caveats:
  - May not provide accurate analytical results on all specimens.
  - Thickness, inner construction (other moisture barrier).
  - Presence of any volatile compounds other than water.

IPC-TM-650 2.6.28

- The weight of the specimen is compared before and after a bake.
- 24 hours at 105°C +5°C/-0°C is minimum.
- Apparatus required:
  - Circulating air oven (105°C +5°C/-0°C)
  - Analytical balance (to 4 places of accuracy)
  - Tweezers to handle the test sample/coupons
  - Gloves

IPC-TM-650 2.6.28

- Nitrogen atmosphere (inert) or vacuum is not required
  - N_2 promotes drying and improve accuracy of the test.
- Place analytical balance on an isolated, grounded (ESD) surface during testing.
  - Calibrated in accordance with IPC-QL-653.
- Clean the prior to each test sample/coupon weighing session.
- Ensure that gloves are not contributing contamination material to the test samples/coupons.

IPC-TM-650 2.6.28

- Remove sample from the circulating oven and transfer within 2 minutes to the analytical balance measurement location.
  - Place each sample on the analytical balance for 15 seconds, and then record weight (to 0.0001 gram)
  - Note that the sample/coupon weight will not settle completely.
  - After 15 minutes, repeat these steps.
- The test sample/coupon weighing procedure should be conducted for a period of 4 hours

IPC-TM-650 2.6.28

- Calculate the bulk moisture content using the following equation:

$$Moisture\ Content = \frac{Initial\ weight - Conditioned\ weight}{Conditioned\ weight}$$

- Calculate the moisture absorption rate by plotting the bulk moisture content versus time using the data recorded.

Guidelines for Baking – Environment – 1

- Ensure proper calibration of the oven.
- Baking should be performed in a forced air recirculating oven, vacuum or nitrogen atmospheres are also effective.
- Ensure proper venting and cleanliness of the oven.

IPC-1601

Guidelines for Baking – Environment – 2

- Sufficient gaps between PCBs for proper circulation (do not stack PCBs).
- Fan and air flow path will dictate configuration of PCBs - vertical or horizontal orientation.
- If using trays, consider material interactions between tray and PCB/surface finishes. E.g. out-gassing or particulate contamination.

Suggestions on Baking Oven Selection

- Temperature range from +40°C to +280°C.
- Steady (+/- 1 ºC) operation
- Capability of countdown timer
- Inert inner surfaces (e.g. AISI SS304)
- Inert thermal insulation materials (natural mineral fiber)
- Adjustable shelves
- Manually controlled ventilation opening
- Safety alarm and manual reset
- Optional:
  - Programmed start-up
  - PC interface for programming and data download (GPIB or USB)

Adverse Effects of Baking

- Baking increases cost and cycle time
- Degrades solderability.
  - Affects OSP finish.
  - Causes oxidation.
  - Effects on solid diffusion between the bulk metallization and surface finish.
  - Causes excessive intermetallic growth.
  - General surface degradation.
- Stripping and refinishing may be an alternative.

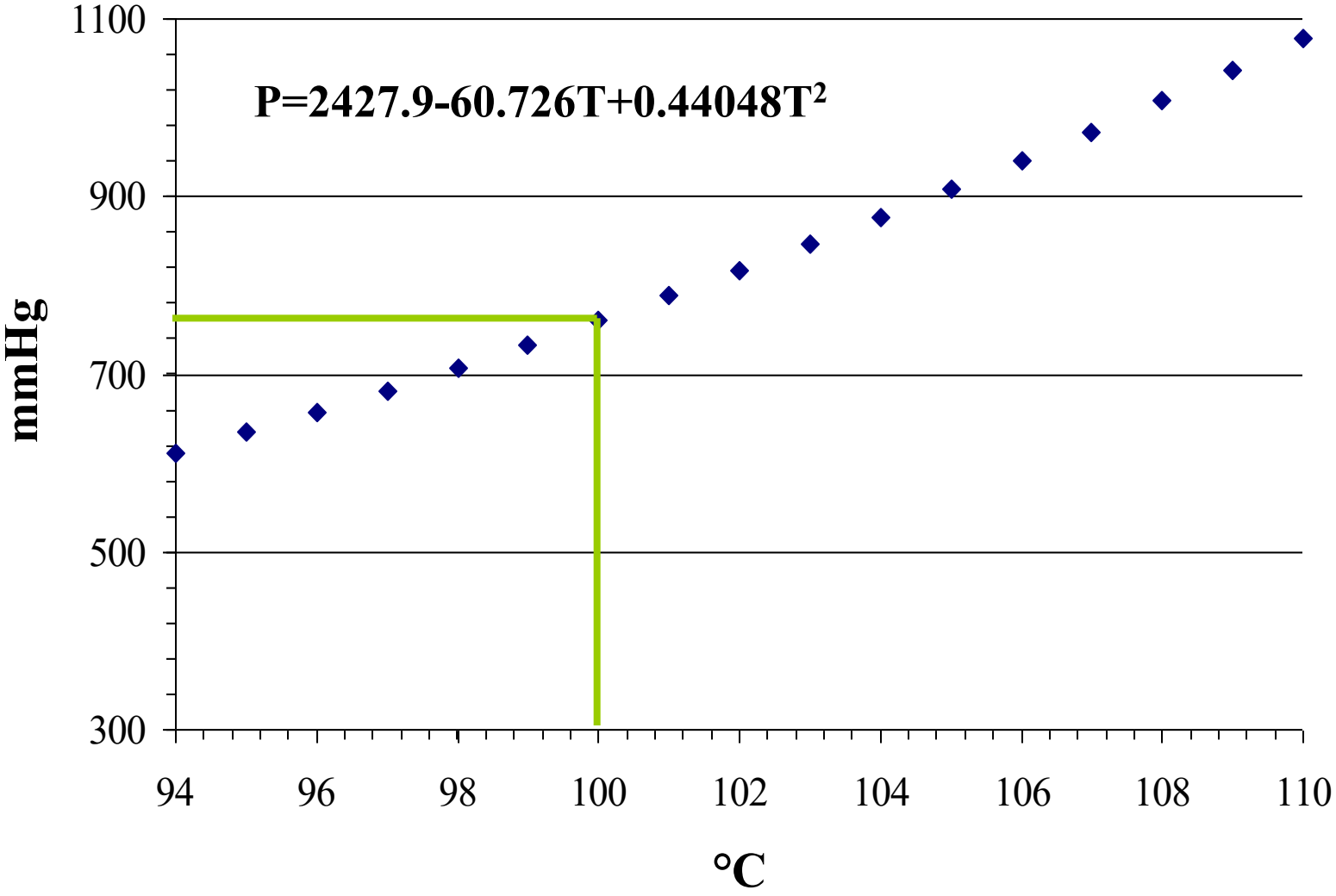
Vacuum Ovens

- Allow baking of temperature sensitive boards.
- Prevents oxidation that would normally be accelerated by high temperature treatment.
- Enables recovery of degassed products.

- Size limitations
- Higher cost
- Temperature gradients within the chamber

"Vacuum Heating and Drying Ovens" - Weiss Gallenkamp

Variations in Boiling Point of Water



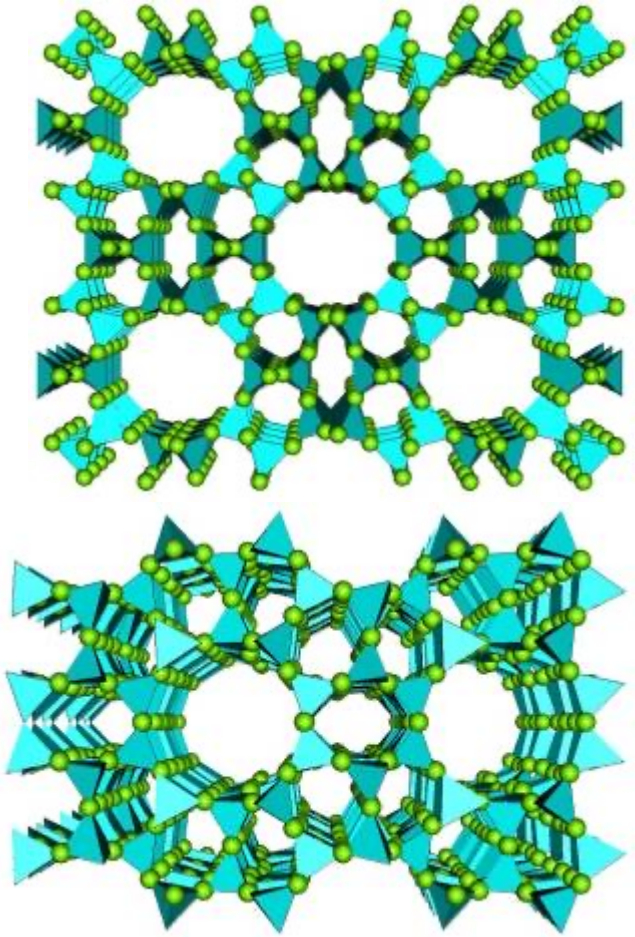
Dry Cabinets

- Dry cabinets control diffusion by maintaining low humidity atmospheres.
- Use a nitrogen-free environment and zeolite desiccant
  - Desiccant is recycled by the system by heating, which causes the release of absorbed moisture through vents to outside of the cabinet.
  - Desiccant does not require replacement.
- Digital hygrometer monitors RH levels.
- Storing PCBs before, after and between assembly (second side or selective wave).
- Can add data recorders and HEPA filtration.

Zeolite

Zeolite is a volcanic rock with three dimensional crystalline frameworks.

- High affinity for water and can adsorb and desorb without damage to the crystal structure.
- Placed in an air stream will adsorb moisture up to its saturation point, but will not adsorb moisture after that point.
- Can be regenerated by using a vacuum to pull out bulk water and baking to remove residual moisture.



Images from Tulsa University Professor Geoffrey L. Price's website

Recommendations for Flex, Rigid-Flex Circuits

- Manufacturers of flex and rigid/flex circuits recommend pre-bake prior to hand, wave, selective wave, IR or vapor phase soldering.
  - Similar recommendations for flex, rigid-flex boards prior to solder leveling.
  - Since polyimide absorb moisture quickly, it is recommended that soldering be performed within 30 minutes after baking.
- Flex-Rigid - moisture removal rate is slower
  - Thicker boards
  - High metallization density
  - Material combinations (low D v/s high D)
- Using vacuum ovens allows for lower bake temperatures.
  - Vacuum ovens also reduce the oxidation of the surface finishes.
- Baking times depend on type of base material, adhesive, board thickness, layer count, percent metallization.

Humidifiers

- ASHRAE Standard 62-2001
- Low indoor humidity levels can lead to the development of potentially damaging electrostatic discharge.

- Steam systems
  - Boiler steam, clean steam, heat exchanger steam, canister steam type.
- Cold water systems
  - Centrifugal, ultrasonic, compressed air, high pressure systems.

Moisture Barrier Bags (MBB) Introduction [1, 2] – 1

- Designed to restrict the H_2O vapor transmission.
- Used to pack moisture sensitive devices/circuit components.
- PCB should be packed with a fresh desiccant and humidity indicator card (HIC).
- The MBB should be sealed and a label (caution label or bar code) should placed on the outside.
- The amount of desiccant used shall be calculated according to the bag surface area and water vapor transmission rate (WVTR) in grams/100in^2 of barrier material per 24 hours.
  - The requirement maintains an interior relative humidity in the MBB of less than 10 % RH at 25°C.

Moisture Barrier Bags (MBB)
Introduction – 2

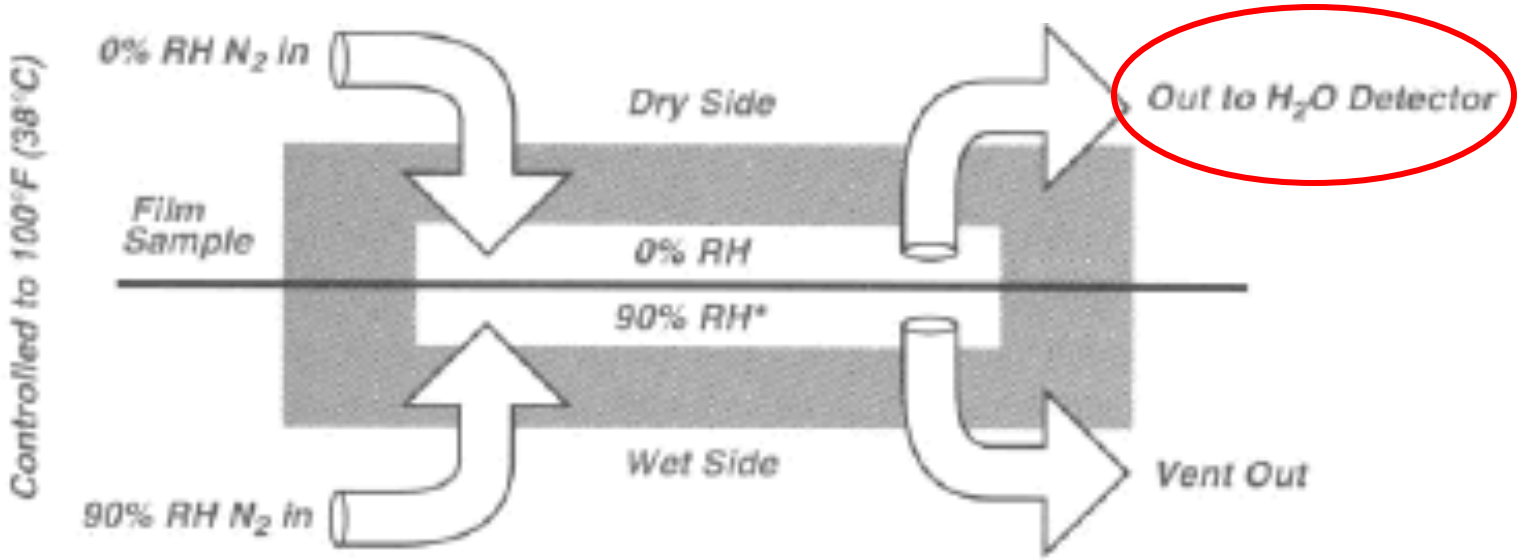
- Per J-STD-033B.1, MBBs shall meet MIL-PRF-81705, TYPE I requirements:
  - Flexibility
  - ESD protection
  - Mechanical strength
  - Puncture resistance
  - Heat sealable
- WVTR ≤0.002 gm/100 in² in 24 hours at 40°C after flex testing per condition "E" ASTM F 392.

WVTR

- WVTR – A measure of the permeability of MBB plastic film or metalized plastic film material to moisture
  - WVTR is an important rating for moisture barrier bags.
- Typical Packaging Materials:

Packaging Material	Construction	WVTR per 24 hours
Nylon/Foil/Poly	outer layer static dissipative nylon, middle layer of Al foil, inner layer of polyethylene	< 0.0005 gm/100 in^2
TyvekTM/Foil/Poly	Tyvek ™, middle layer of Al foil, inner layer of polyethylene	< 0.0005 gm/100 in^2
Aluminized Polyester/Poly	two layers of aluminized polyester laminated to sealable polyethylene	0.09mm - 0.02 gm/100 in^2
		0.18mm - 0.005 gm/100 in^2

WVTR Measurement



A WVTR test cell

WVTR is measured using ASTM F 1249 (Standard Test Method for Water Vapor Transmission Rate Through Plastic Film and Sheeting Using a Modulated Infrared Sensor).

Desiccant [1, 2] – 1

- Desiccants are absorbent materials used to maintain a low relative humidity in MBBs for dry-packing.
  - Desiccant may be a silica gel or other absorbent material
  - Desiccants should be packed in dustless pouches.
  - Desiccant must meet or exceed MIL-D-3464 Class II (non-dusting) requirements.

- One unit of desiccant is defined as the amount that will absorb a minimum of 2.85 g of water vapor at 20% RH and 25 °C.
  - Generally sold in 1/6, 1/3, 1/2, 1, 2, 4, 8, 16 units.

1. MIL-D-3464
2. J-STD-033B.1

Desiccant – 2

- Care should be taken in handling desiccants as the moisture absorption ability can diminish rapidly upon exposure to humid environment.
- It is advisable to use numerous small bags rather than fewer large ones, as this increases the available surface area of the desiccant and so improves adsorption of the water.



Various desiccant packaging units

Sample Calculation
Amount of Desiccant [1, 2]

- MIL-P-116 specifies the following formula for general dry packing to calculate the require units of desiccant:
  - Units = 0.011 × Bag Area (in²)
  - So, for a 8×10 inch bag:
    - Units = 0.011 × 160 in² = 1.76, or approximately 2 desiccant units

- Following calculation is suggested per J-STD-033:

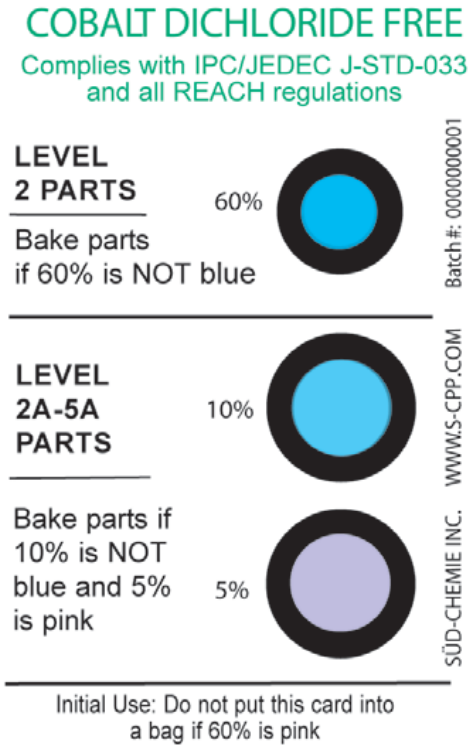
$$Units = \frac{(0.304 \times Shelf\ Life\ (months) \times WVTR \times Surface\ Area\ in^2\ )}{Amount\ of\ water\ that\ a\ unit\ of\ desiccant\ will\ absorb\ at\ 10\%RH}$$

$$Units = \frac{(0.304 \times 12 \times 0.002 \times 160\ )}{6.66} = 0.2, or\ approximately\ 1/6\ UNIT$$

1. MIL-P-116 J
2. J-STD-033B.1

Humidity Indicator Card (HIC) [1]

- HIC contains a moisture-sensitive chemical to aid in determining the level of moisture exposure.
  - Makes a significant, perceptible change in color when the indicated relative humidity is exceeded
  - HIC typically have three or five color dots with varying RH sensitivity values.
  - Typically change from blue (dry) to pink (wet)
  - HIC is packed inside MBB, along with desiccant
  - HIC comply with MIL-I-8835



1. J-STD-033B.1

A Word about HICs and $CoCl_2$

- Cobalt dichloride ($CoCl_2$) is commonly used in HIC because it changes color when exposed to changing levels of moisture.
  - European REACH requirements identified CoCl2 as a Substance of Very High Concern (SVHC) under Article 33.
- It is completely banned, but many companies have started seeking alternatives for many chemicals listed in the SVHC list.
- $CoCl_2$ free HIC materials are now available.

JEDEC HIC Color Key Code *

	Indication at 2% RH Environment	Indication at 5% RH Environment	Indication at 10% RH Environment	Indication at 60% RH Environment	Indication at 65% RH Environment
5% Spot	Blue (dry)	Lavender	Pink (wet)	Pink (wet)	Pink (wet)
10% Spot	Blue (dry)	Blue (dry)	Lavender	Pink (wet)	Pink (wet)
60% Spot	Blue (dry)	Blue (dry)	Blue (dry)	Lavender	Pink (wet)

* - Other color schemes may be used.

Recommendations – Prior to Packaging

- Use caution during PCB test and inspection steps.
- Determine requirement for bake by evaluating moisture content:
  - Pb-free process: Moisture content should not exceed 0.1% by weight (using IPC-TM-650 2.6.28).
  - Low temperature assembly: Moisture content should not exceed 0.2%.
- If bake is required, perform before the applying a final finish.
- Laminate witness coupons.
- Package immediately after final inspection.

Source : IPC-1601 PRINTED BOARD HANDLING AND STORAGE GUIDELINES

Laminate Witness Coupons

- IPC-1601 recommends laminate witness coupon (LWC) be placed in the packaging along with PCB.
- LWCs can represent the moisture level or condition of the PCBs upon receipt, after storage, and during assembly processing

LWC Design

- Guidelines on LWC selection, processing and usage are provided in section 4.2.5 of IPC-1601.
- Caveats:
  - Moisture uptake on LWC may be different than actual PCBs.
  - Can show higher % MC due to comparatively smaller x-y-z dimensions and due to absence of internal PCB features that may inhibit diffusion.

Recommendations – Packaging , Shipment and Storage – 1

- Select packaging material that will fully protect the PCB during shipment and storage.
- Ensure PCB are dry before packaging.
- Use moisture barrier bags (MBB) and desiccant material and HICs.
  - MBB should have WVTR $\leq$ 0.002/gm /100 in^2 in 24 hrs at 40°. Use adequate seal width per manufacturers recommendations.
  - Desiccant material should be non-contaminating (sulfur free) and dust-less MIL-D-3464 Class II.

Source : IPC-1601 PRINTED BOARD HANDLING AND STORAGE GUIDELINES

Recommendations – Packaging , Shipment and Storage – 2

- HIC should be non-corroding and should have an adequate number of divisions to resolve varying humidity levels.
- Place one HIC per MBB. Do not stack the HIC on top of the desiccant.
  - Provide instructions for proper interpretation of HIC cards upon opening the MBB.
  - Create guidelines for selection of other packing materials used inside the MBB. E.g. moisture content of rigid packaging or backing materials used for thin PCBs (<1.4 mm thickness).



Moisture Sensitivity Caution Label *

* - Z-Mar Technology

Other Considerations

- Effect of MBB materials on board finish
  - Consult finish manufacturer, check IPC specs, IPC-4552, IPC-4553 and IPC-4554 for ENIG, Ag and Sn finishes respectively.
- Effects of MBB and packaging materials (e.g. separator sheets) on solderability
  - Oxidation of finishes, particulate contamination.
  - Use pH neutral and sulfur free paper as separator between board finish and packaging materials.
- Place separators between the board finish and HIC/desiccant bags.

Measures for Moisture Control During Receiving & Handling – 1

- Ensure factory ambient of 30°C and 60%RH or close.
- Inspect for any damage to the MBB.
- Ensure proper seal of the MBB.
- Cut the MBB close to the seal.

Measures for Moisture Control During Receiving & Handling – 2

- Ensure that each bag contains a HIC.
- Check HIC immediately (in controlled ambient).
- Verify HIC indicates an acceptable humidity level.
  - If HIC indicates that exposure time or humidity have been exceeded: re-bake to ensure dryness prior to usage.
  - Notify supplier if HIC indicates unacceptable levels.

Measures for Moisture Control During Receiving & Handling – 3

- Verify that the HIC is authentic.
- Place PCBs in a low RH environment (<10% RH) after initial inspection **and between assembly steps**.
- Determine reuse of HIC and desiccants if returned to dry packaging with 30 minutes.
- Measure and compare state of LWC.

Section – IV
Testing and Inspection of Printed Circuit Boards and Assemblies

Electronic Testing Equipment

- Digital meters
  - Multimeters
  - Specialized parametric meters, such as LCRs, high resistance meters, etc.
- Oscilloscopes, Spectrum Analyzers
- Curve tracer/Parameter Analyzers
- Time Domain Reflectometers
- Automated Test Equipment (ATE)

Digital Multimeters

- Typically provide:
  - Voltage (DC, AC rms)
  - Resistance (2 wire)
  - Current
- Other common options:
  - Resistance (4 wire)
  - Frequency or count
  - Diode voltage
  - Capacitance
  - Temperature
  - Datalogging



Agilent 34401A

LCR Meters and Impedance Analyzers

- Variable AC voltage and frequency.
- Used to characterize
  - Capacitors
  - Inductors
  - Transformers
  - Filters
  - Dielectric materials (e.g., PCB substrates)



Agilent 4263B

High Resistance Meters

- Typically measure:
  - Leakage current
  - Insulation resistance
- Common applications:
  - Insulation resistance of dielectrics (capacitors, substrates)
  - Surface insulation resistance of PCBs



Agilent 4339B

Oscilloscopes and Spectrum Analyzers

- Digital scopes allow:
  - –Waveform storage
  - –Capture of transients
  - –Waveform measurements
  - –Math (e.g., FFT)
  - –Complex triggering
- Spectrum analyzers are used for frequency domain measurements.



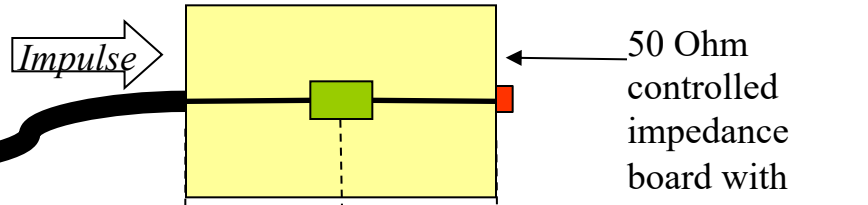
Agilent 54601

Time Domain Reflectometry (TDR)

- TDR reflection coefficient (Γ) is the ratio of the incident and reflected voltage due to impedance discontinuities in the circuit.
- In the time domain, any discontinuities due to impedance mismatches within the circuit are seen as discrete peaks.
- TDR reflection coefficient is a measure of RF impedance, and can be measured using a short pulse or high frequency sinusoidal signal (requires transformation).

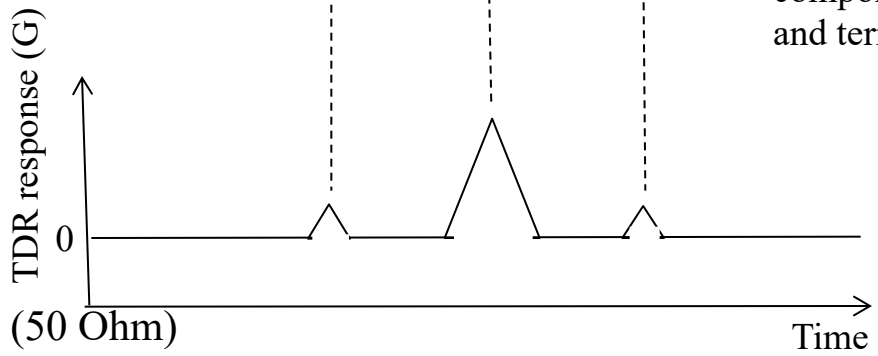


Agilent E8364A Vector network analyzer (VNA)



50 Ohm controlled impedance board with surface mount component and termination

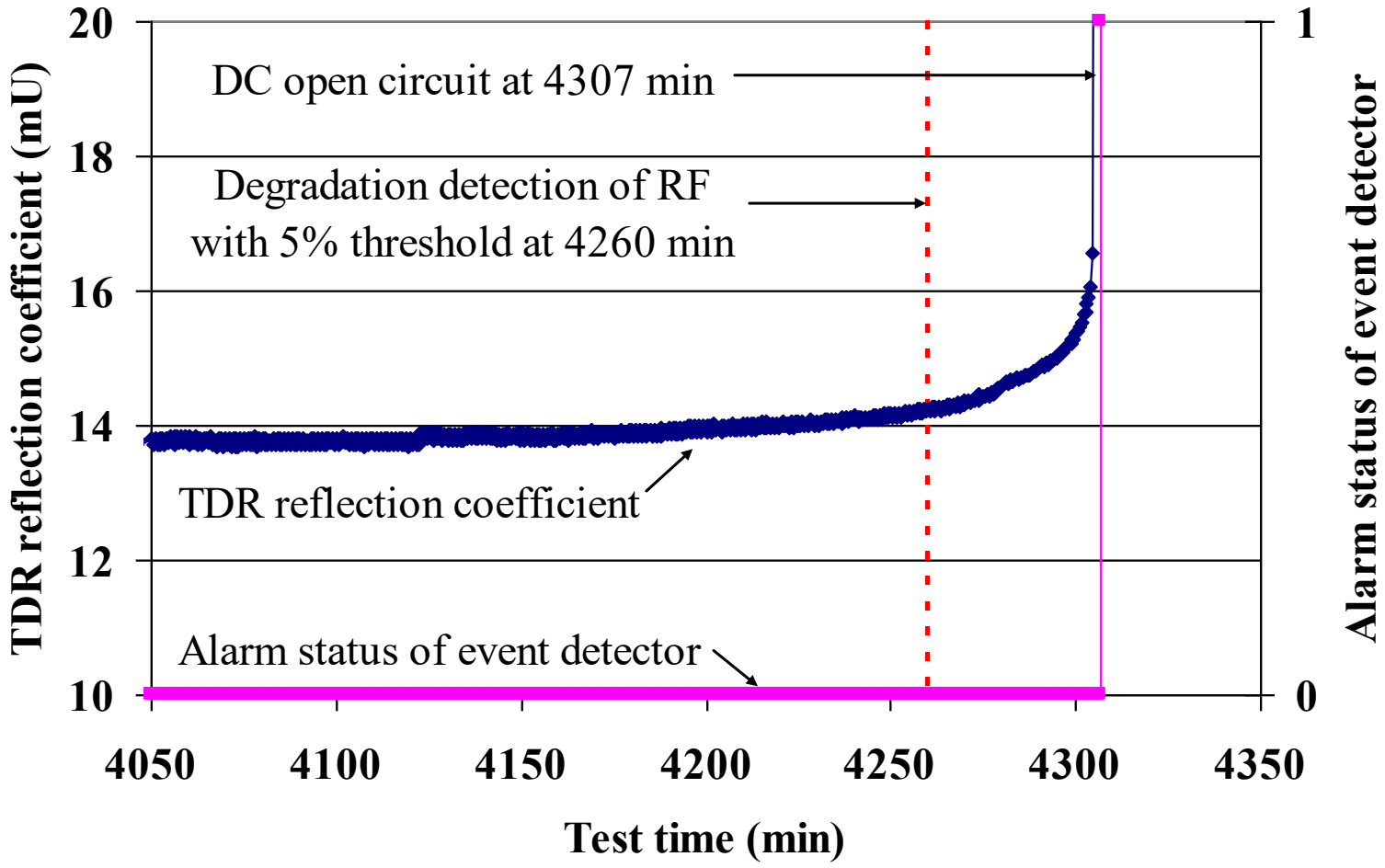
$$\Gamma = \frac{V_{reflected}}{V_{incident}} = \frac{Z_L - Z_0}{Z_L + Z_0}$$



- $-1 \leq \Gamma \leq 1$; Γ is dimensionless
- $\Gamma=1$ when $Z_L=\infty$; $\Gamma=-1$ when $Z_L=0$
  - Z_L: the impedance of device under test
  - Z_0: characteristic impedance of the circuit (50 Ohm)

TDR Sensitivity to Solder Joint Cracking

A 5% increase of the initial value occurred at 4260 minutes, which was 47 minutes earlier than the time to failure based on an event detector.



Automated PCB Test Equipment

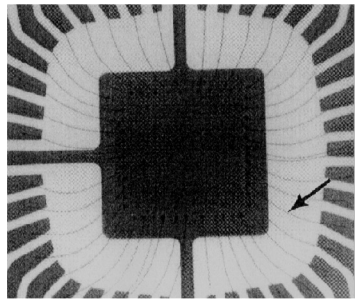
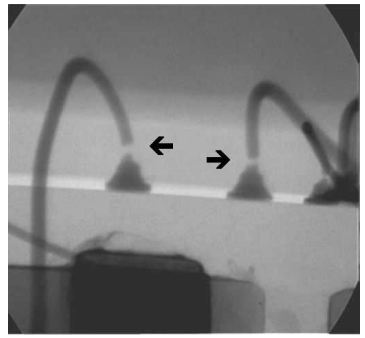
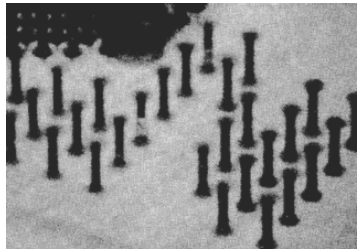
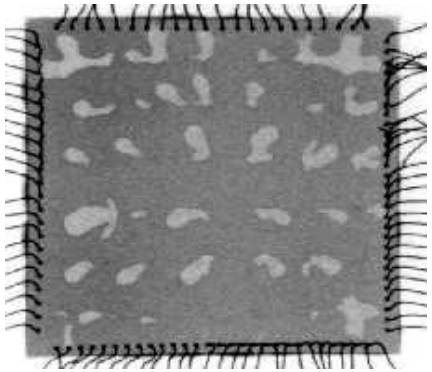
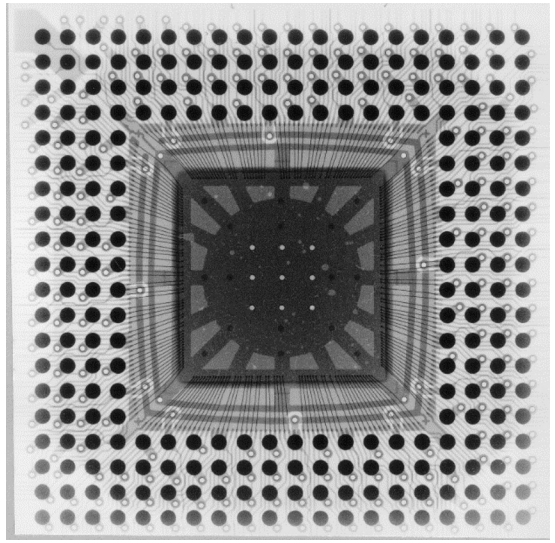
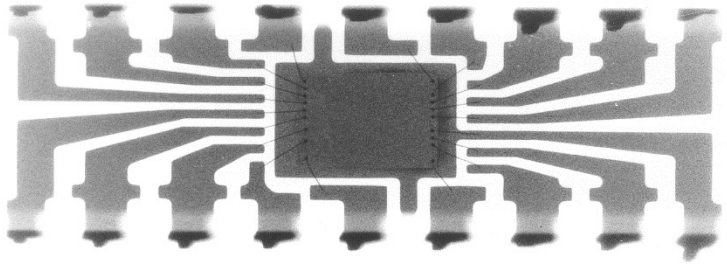
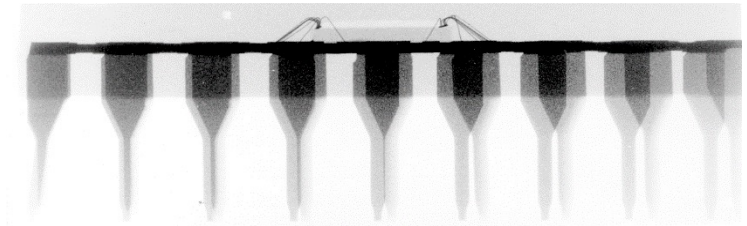
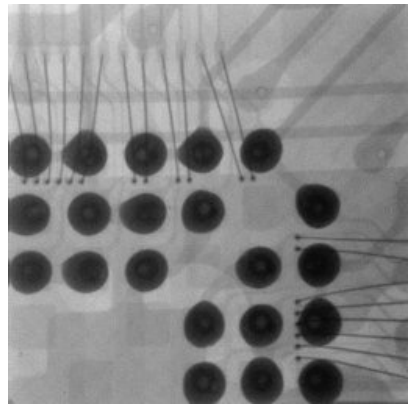
- Dedicated Wired Grid – test probes wired to the grid. High cost.
- Universal Grid ("Bed of Nails") –Low cost, reusable. Spring loaded or rigid test probes in mechanical contact to the grid.
- Flying Probe or Fixtureless System with moveable single or double probes. Expensive. Empirical techniques applied on capacitance /impedance data to determine a good board. Good for micro products. Issues with pad damage.

X-ray Radiography

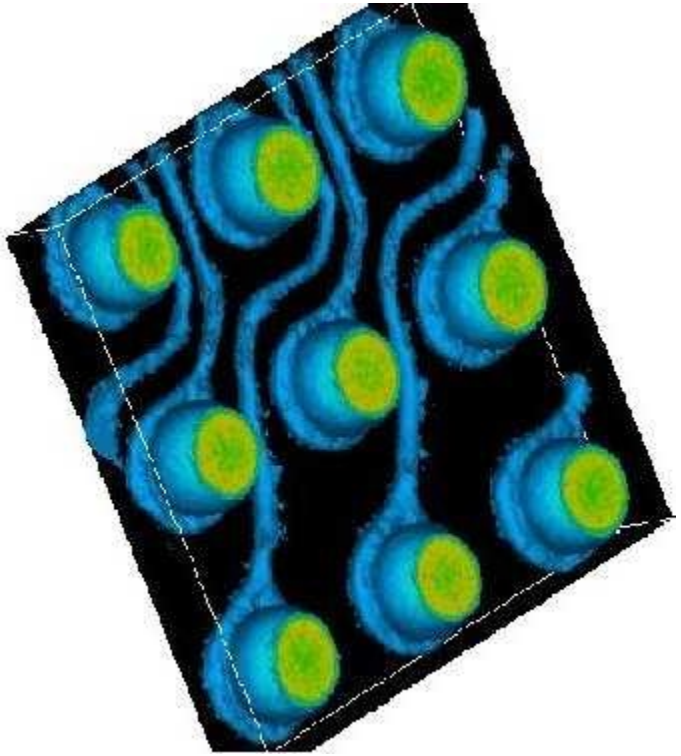
Applications and Examples

Typical applications include:

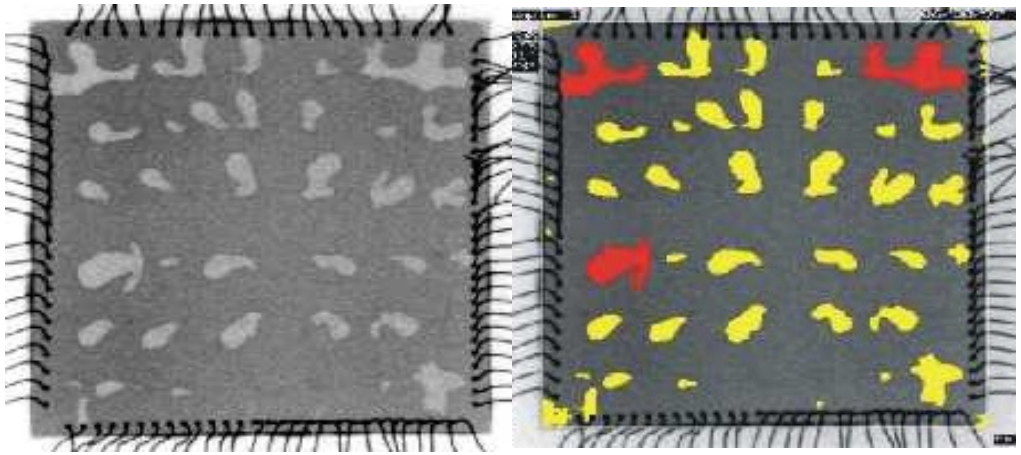
- Internal structures of electronic devices
- Connection techniques (Flip Chip, μBGA, BGA, MCM, COB)
- Inner layers of PCBs
- Popcorning *in situ* visualization

Applications: CT Visualization and Software



The computed tomography (CT) technique enables 3-dimensional inspection of planar components as seen in this BGA assembly.



Use of voiding calculation software enables the estimation of voided area observed in die attach. Given a nominal size area, voids can be color coded for easier visualization of areas larger than or smaller than these dimensions. The yellow represent normally sized voids, whereas, the red ones are larger.

Limitations of X-ray Techniques

- Although considered a non-destructive test, X-ray radiation may change the electrical properties of sensitive microelectronic packages such as EPROMS, and hence should not be used until after electrical characterization has been performed on these devices.

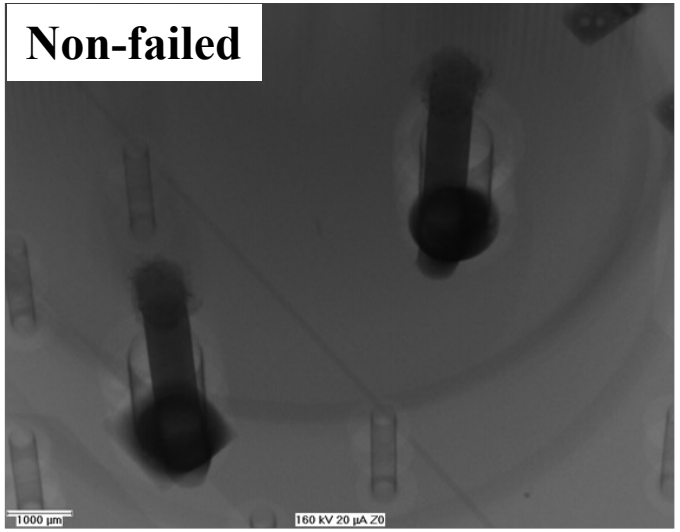
- For samples on or below thick metal layers such as large heat sinks as seen in power devices, X-ray imaging is more difficult and requires high voltages and currents.

- Magnification using contact X-ray equipment can only be done externally by a magnified view of the 1:1 photo, or from an enlarged image of the negative. Hence, resolution will decrease as the image is enlarged.

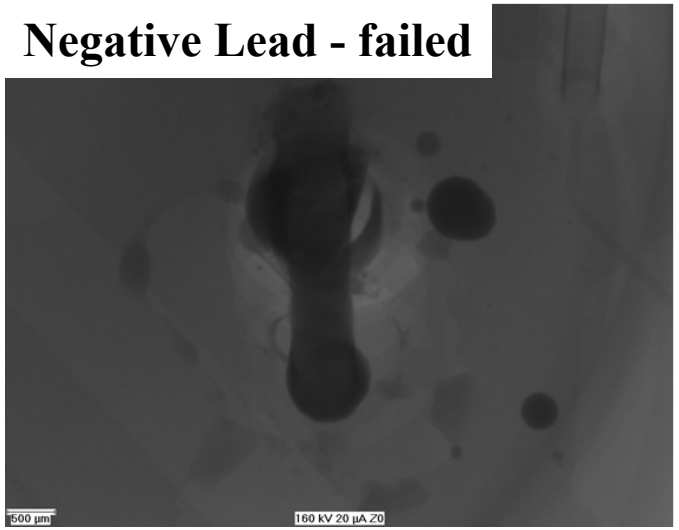
- The operator may have to experiment with voltage settings and exposure times, depending on the type of sample and film used, to obtain proper contrast and brightness in the photos.

Discussion 2 – PTH Fill on Electrolytic Cap

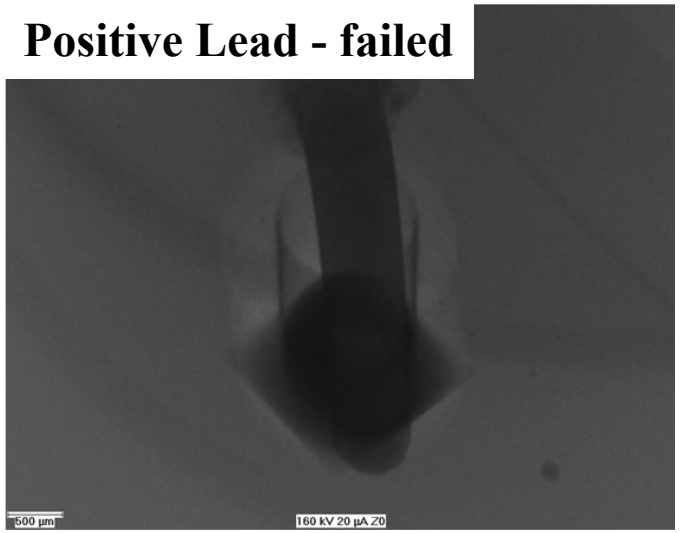
Non-failed



Negative Lead - failed



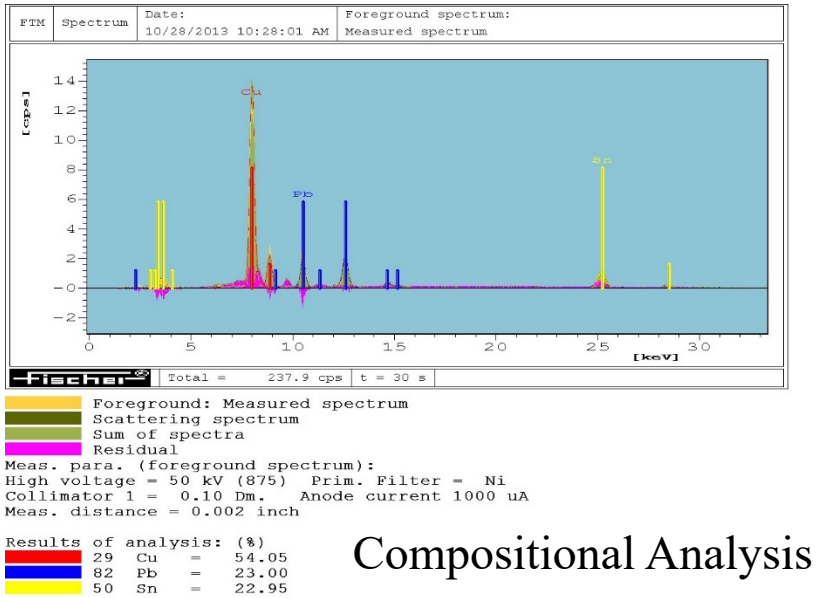
Positive Lead - failed



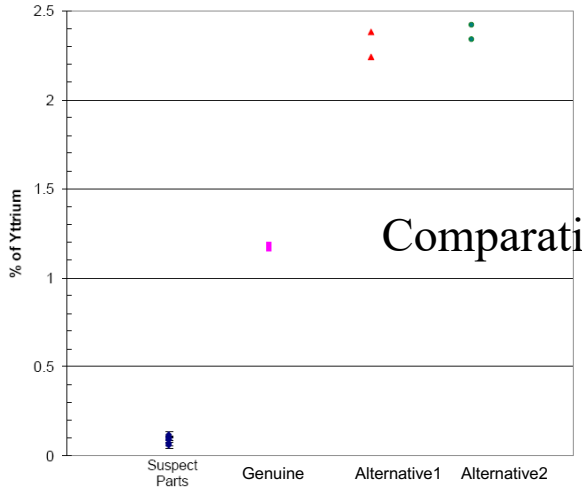
X-Ray Fluorescence (XRF)

Types of Analysis

- Spectrum analysis to determine the elements and the composition of an unknown sample.
- Material analysis for bulk samples (one layer sample)
- Thickness analysis to determine the thickness and the composition of different layers.
- Pure element and alloy standards (such as Ni, Cu, Ag, Sn, Au, Pb and SnAgCu or SnPb alloys) can be used to calibrate the spectrometer.

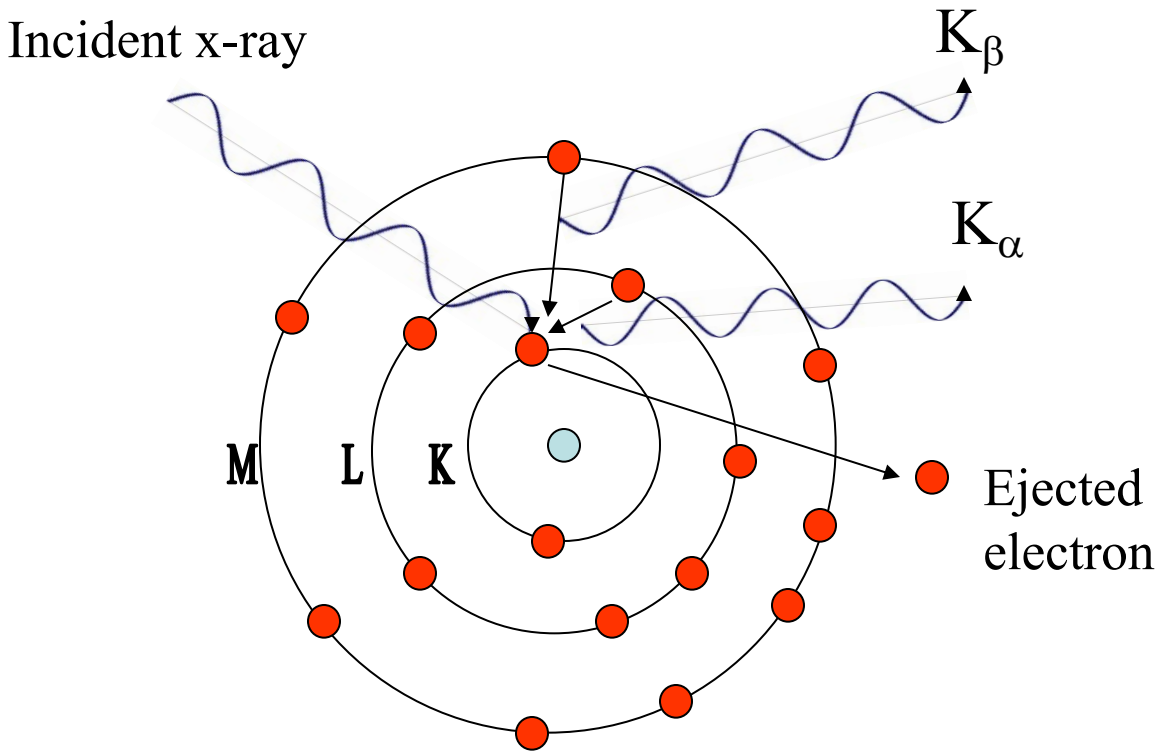


Compositional Analysis



Comparative Analysis

Background on X-Ray Fluorescence



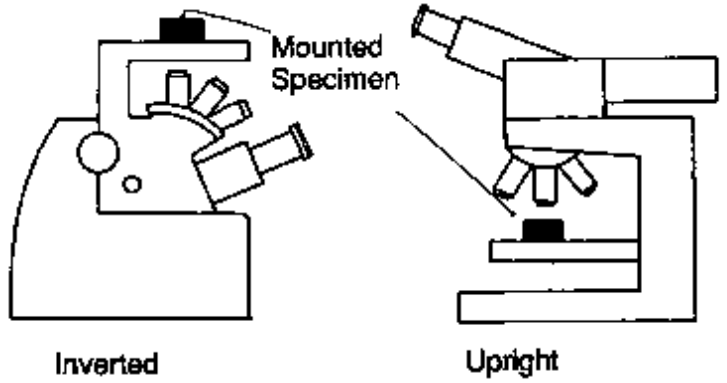
- Incident x-ray is incident on sample
- Core electron is ejected
- Electron from outer shell falls down to fill up the vacancy
- X-ray photon is emitted (energy equal to the difference between the two levels involved in the transition), which is characteristic of the element and the electronic transition

Conclusion

- XRF is a powerful tool to analyze composition and coating thickness on a variety of electronic products
- A non-destructive tool, does not require sample preparation, provides quick analysis results
- Users should be aware of the issues related to the automated analysis software

Visual Inspection

External Visual Inspection



Higher power light optical microscopes

- Inverted
- Upright

Low power stereo macroscope (up to 65x)

- Overview
- Package level
- PCB level



Typical stereo macroscope

Light Optical Microscopes

Resolution

Limit of Resolution $= \lambda / (2 \times N.A.)$

- λ , light wave length (eg 0.55 μm for green light)
- Numerical Aperture (N.A.), objective lens

For example,

Combination of a 20x objective lens (N.A. = 0.40) with a 10x eyepiece

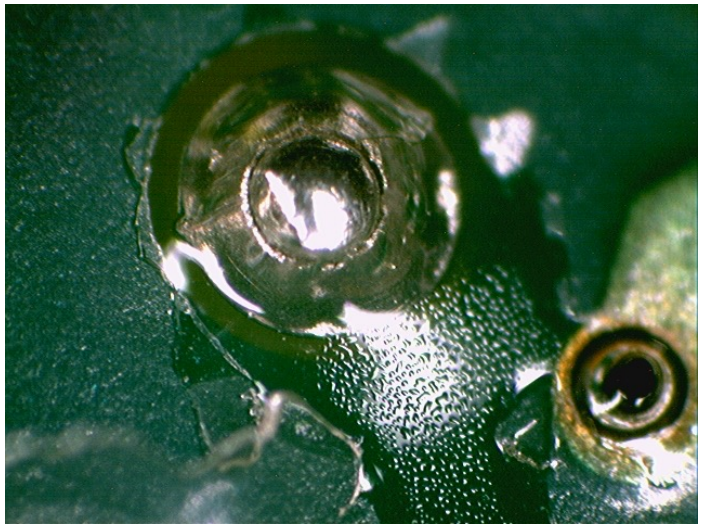
$0.55\mu m / (2 \times 0.40) = 0.69\mu m$

Analytical Techniques

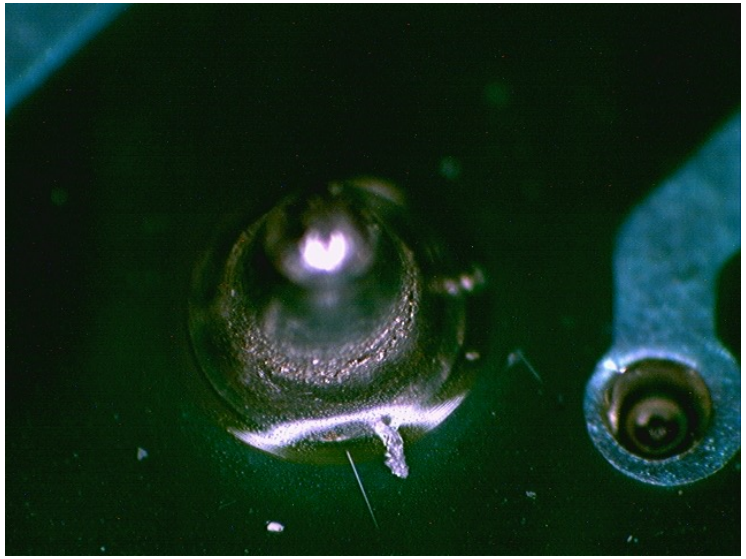
- Environmental Scanning Electron Microscopy (ESEM)
- Energy Dispersive Spectroscopy (EDS)
- Thermo-mechanical Analysis
- Microtesting (Wire Pull, Ball Bond and Solder Ball Shear, Cold Bump Pull)
- Decapsulation / Delidding
- Dye Penetrant Inspection (Dye and Pry)

Discussion - Plated Through Holes

Discussion – PTH



Through Hole Varistor



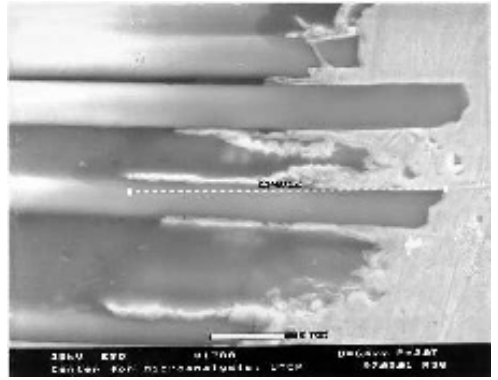
Through hole Cracking

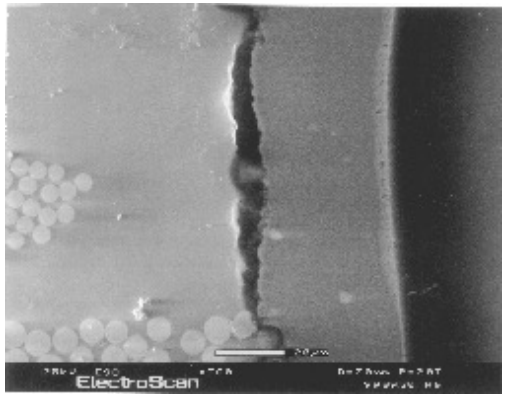
What is the mode, mechanism and root cause (s) ?

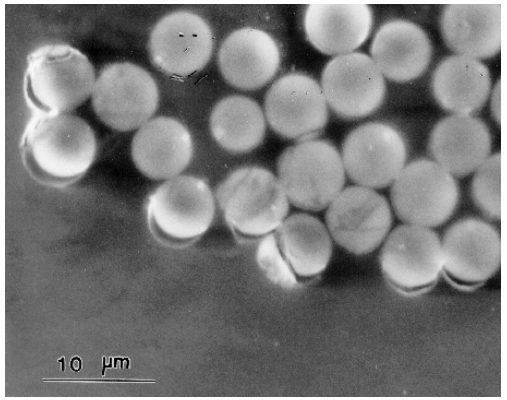
Environmental Scanning Electron Microscopy

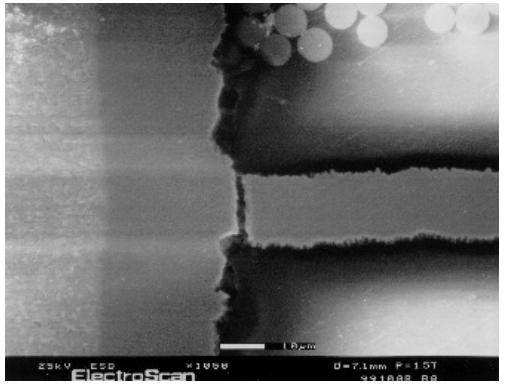
Applications and Examples

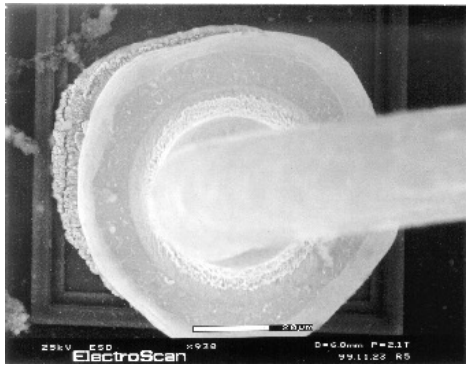
- Excessive wicking of copper in PTHs of a PWB
- Separation at the interface between the copper plating and the fiber epoxy resin board interface
- Fiber/resin interface delamination
- Corrosion and intermetallic growth at the bondpad under the gold ball bond
- Stress-driven diffusive voiding and hillock formation of Al metallization lines
- Metallization corrosion
- Wirebond fracture
- Passivation cracking
- Delamination at the die/die paddle interface
- Dendritic growth
- Electrostatic discharge/electrical overstress
- Wire fatigue
- Solder fatigue

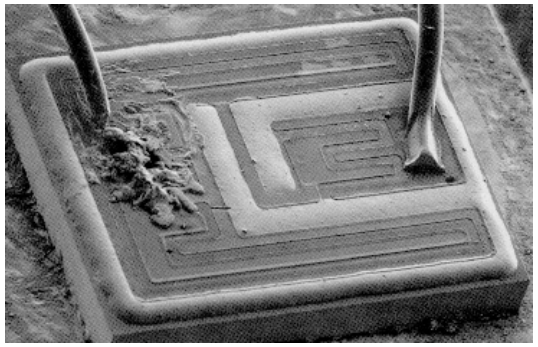












Applications

- By eliminating the need for a conductive coating, ESEM allows imaging of delicate structures and permits subsequent energy-dispersive X-ray spectroscopy (EDS) compositional analysis.

- The ESEM can image wet, dirty, and oily samples. The contaminants do not damage the system or degrade the image quality.

- The ESEM can acquire electron images from samples as hot as 1500ºC because the detector is insensitive to heat.

- ESEM can provide materials and microstructural information such as grain size distribution, surface roughness and porosity, particle size, materials homogeneity, and intermetallic distribution.

- ESEM can be used in failure analyses to examine the location of contamination and mechanical damage, provide evidence of electrostatic discharge, and detect microcracks.

Limitations

- Large samples have to be sectioned to enable viewing in a SEM or an E-SEM, due to the limited size of the sample chamber.
- Only black and white images are obtained. Images can be enhanced with artificial color. Thus, different elements in the same area, having close atomic numbers may not be readily distinguished as in optical viewing.
- Samples viewed at high magnifications for extended periods of time can be damaged by the electron beam (e.g., fiber/resin delamination can be initiated this way).
- Areas having elements with large atomic number differences are not easily viewed simultaneously; increasing the contrast to view the low atomic number element effectively makes the high atomic number element appear white, while decreasing the contrast allows a clear view of the high atomic number element, the image of the low atomic number element is drastically compromised.
- Variations in the controllable pressure and gun voltage can allow samples to appear differently. Lower pressure and voltage give for more surface detail; the same surface can look smoother by just increasing the pressure. Therefore, sample comparisons before and after experiments, especially cleaning treatments should always be examined under the same conditions.
- Image quality is determined by scan rate; the slower the scan rate, the higher the quality. However, at lower scan rates, the image takes a longer time to be fully acquired and displayed. Therefore, sample movement appears visually as jerky motions. A trade off must be made between image quality and visual mobility.

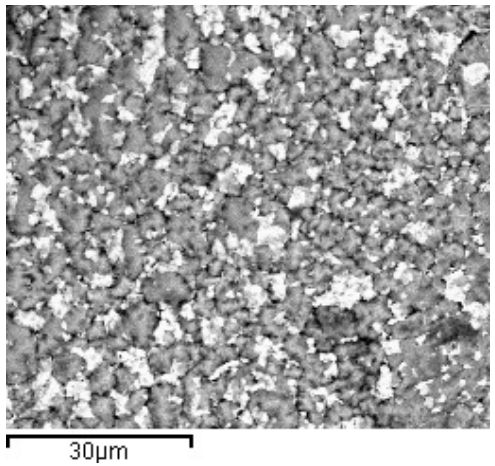
X-ray Spectroscopy

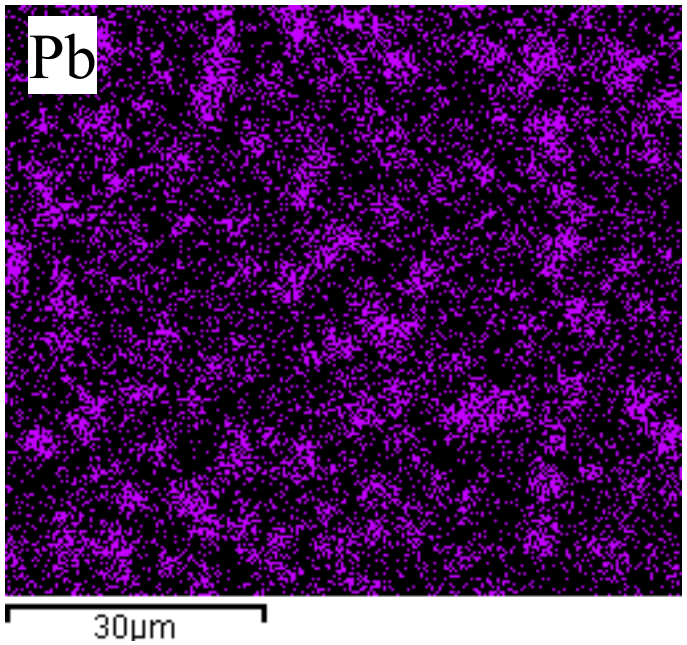
Applications

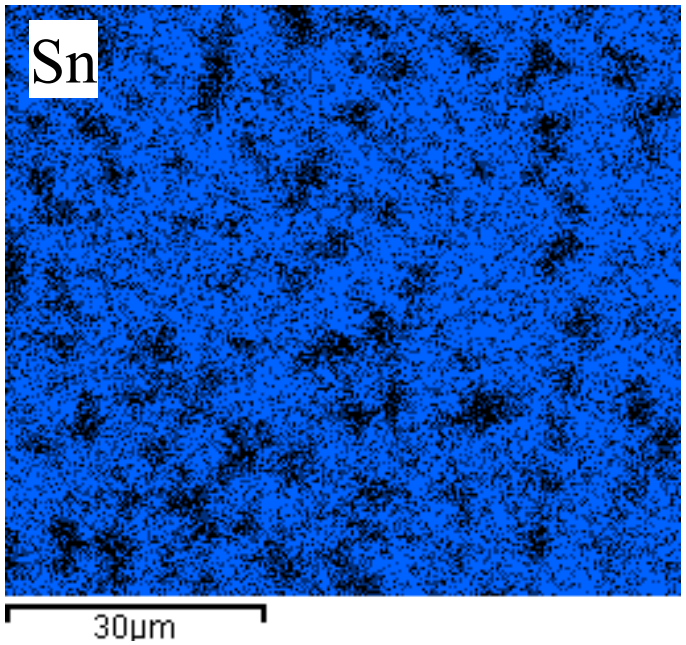
X-ray analysis can be used to detect:

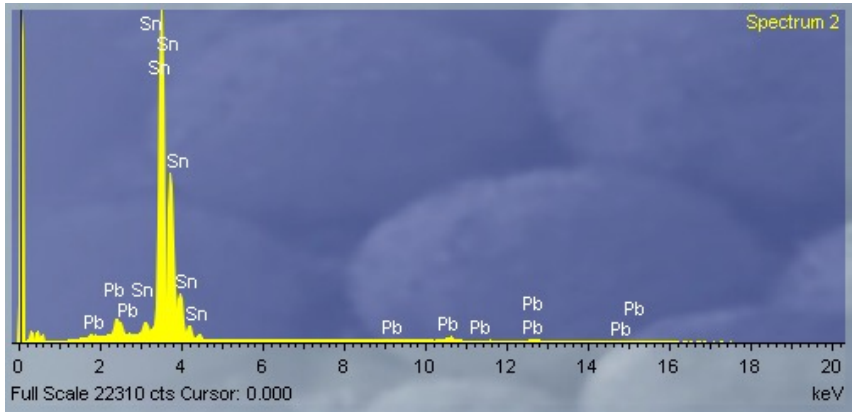
- Surface contamination (chlorine, sulfur)
- Presence of native oxides
- Corrosion
- Concentrations of phosphorus, boron, and arsenic
- Compositional analysis (i.e., Sn to Pb ratio)
- Conductive filament formation
- Intermetallic growth
- Elemental distribution using mapping techniques

X-ray Mapping



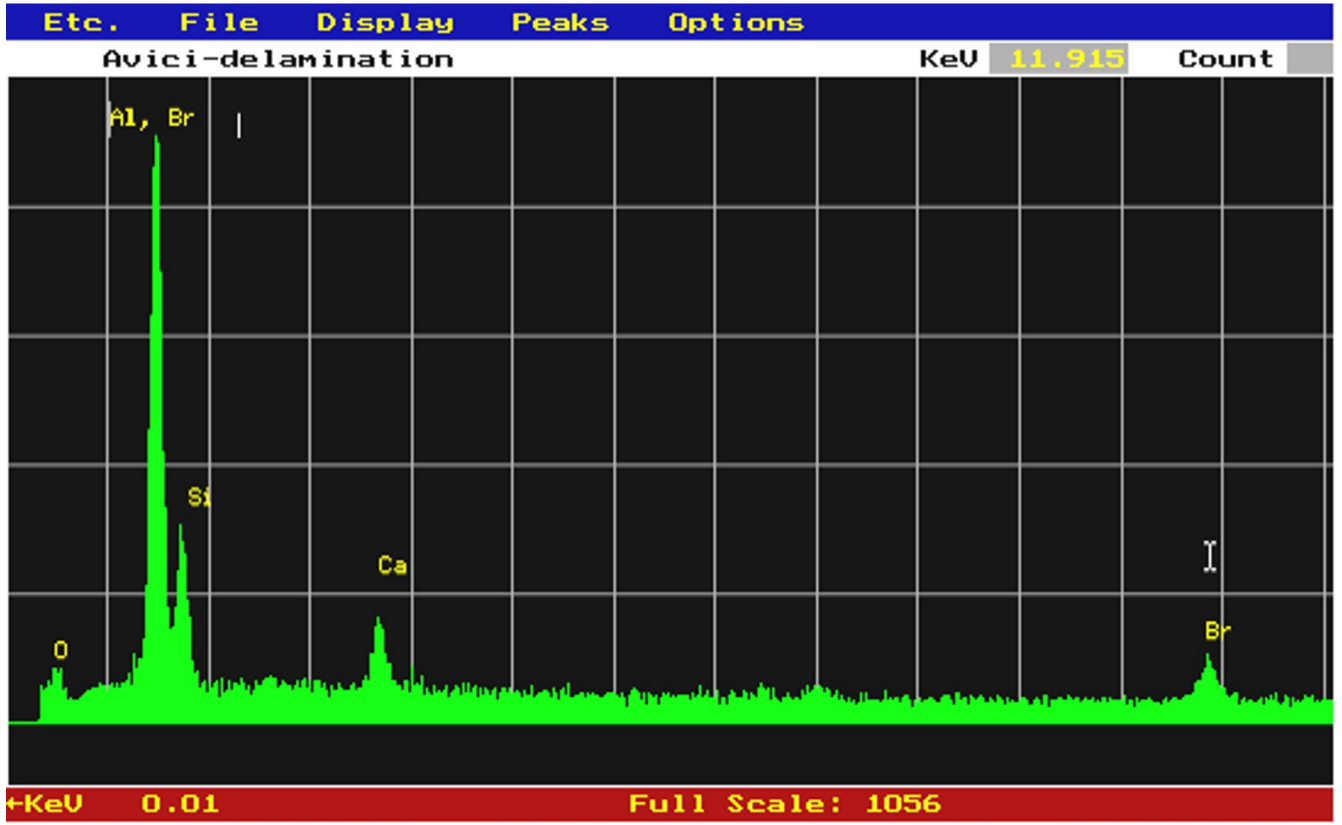






An X-ray mapping of Tin (Sn) distribution (right) and Lead (center) in a eutectic solder. The associated spectrum is shown on left bottom.

Acquired Spectrum Using EDS



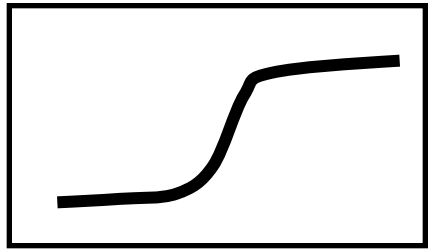
The bromine and aluminum peaks overlap, at 1.481 and 1.487 KeV respectively. It is not clear, using EDS, whether or not aluminum is in this sample. Bromine is present, as evidenced by its second identified peak at 11.91 KeV. The elemental KeV values can be found on most periodic tables.

Limitations of EDS

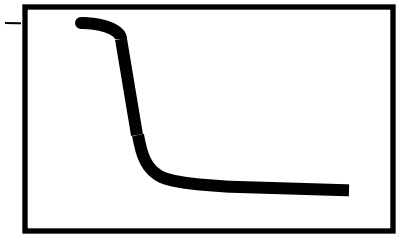
- Resolution is limited, therefore it is possible to have uncertainties for overlapping peaks (i.e., tungsten overlap with silicon and lead overlap with sulfur)
- Cannot detect trace elements
- Limited quantitative analysis
- No detection of elements with atomic number < 6
- If a Beryllium window is used, cannot detect light elements such as carbon, nitrogen and oxygen with atomic number < 9
- Specimen must be positioned in such a manner that an unobstructed path exists from the analysis site to the detector.

Thermal Analysis Techniques

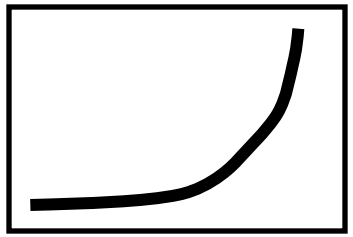
- DSC – Differential Scanning Calorimetry
  - Measures changes in heat capacity
  - Detects transitions
  - Measures Tg, Tm, % crystallinity



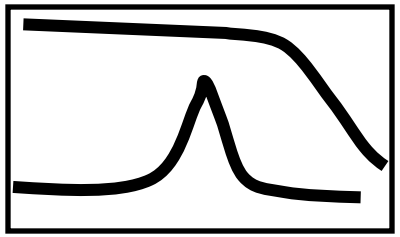
- TGA – Thermogravimetric Analysis
  - Measures changes in weight
  - Reports % weight as a function of time and temperature
  - Helps determine composition



- TMA – Thermomechanical Analysis
  - Measures changes in postion
  - Detects linear size changes
  - Calculates deflection, CTE, and transition temperature

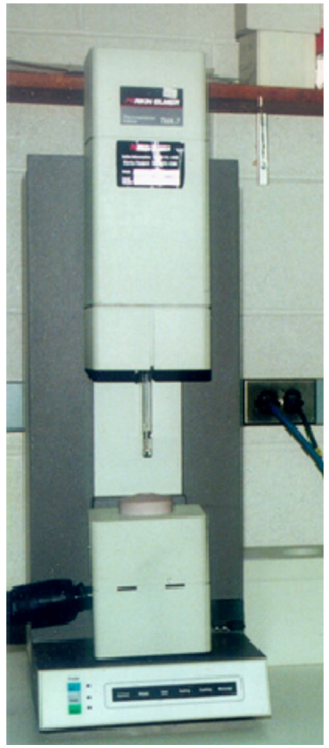


- DMA – Dynamic Mechanical Analysis
  - Measures changes in stiffness
  - Measure deformation under oscillatory load
  - Determines moduli, damping, and transition temperature



Thermal Techniques - Use

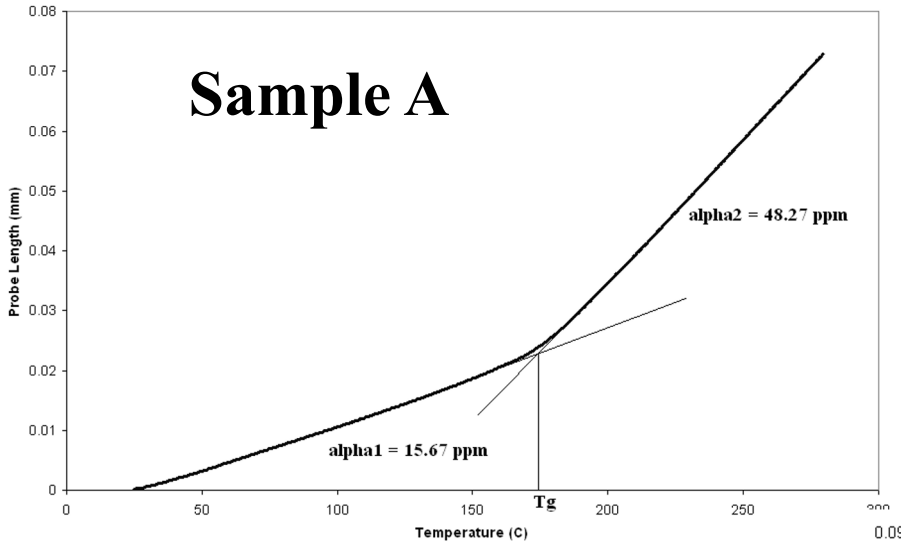
- All techniques are destructive to the sample
  - Sample will be heated above transitions
  - Will have to be cut to fit in instrument
- All techniques use small samples
  - 10 mg or so for DSC and TGA
  - Samples from 5 to 40 mm long for TMA and DMA





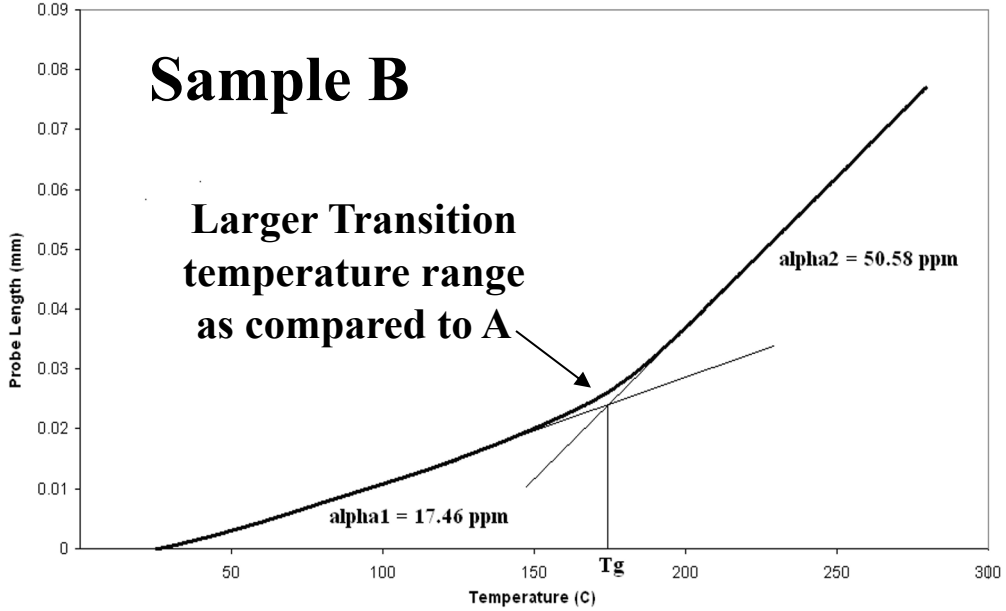


TMA (Samples A and B)



- Coefficient of thermal expansion before glass transition temperature (alpha 1) and after glass transition temperature (alpha 2) is determined.
- Glass transition temperature (Tg) is also determined.

- Constant stylus force applied on the sample: 2 mN.
- Typical scan setup:
- Hold 1 minute at 25 C.
- Heating from 25°C to 280°C at 20°C/minute.



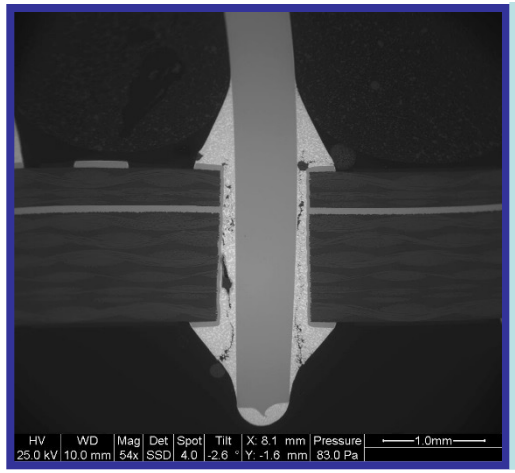
Metallographic Sample Preparation*

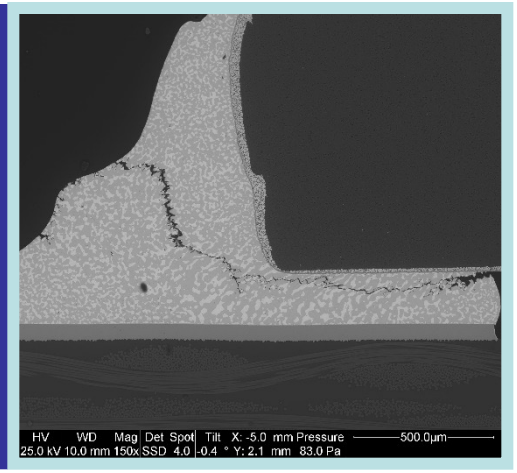
*- Material provided by Buehler Limited/ITW

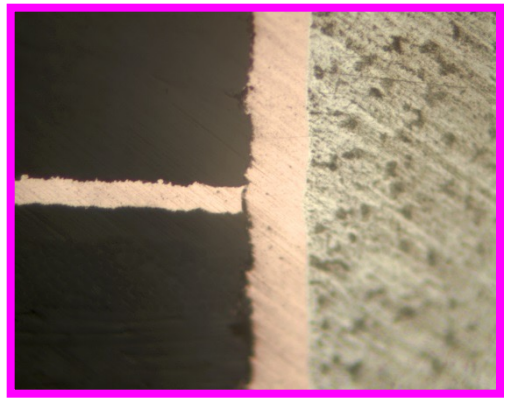
What Is Micro-sectioning of Printed Circuit Board?

Technique used to evaluate printed wiring board quality by exposing a cross-section at a selected plane such as

- **Plated through-holes**
- Plating thickness
- Via
- **Soldered connections**
- Delamination in PCB
- **Inner layer connections**







Primary Purpose of Micro-sectioning

- To monitor the processes rather than to perform final inspection because it makes no sense to add value to a product that is already rejectable!

- Therefore, the objective is to detect any deviations from normal in the manufacturing processes as early as possible to avoid adding value to a defective product. Corrections to the process should then be made as soon as possible.

Goal of Specimen Preparation

Reveal the true microstructure of all materials

- Induce no defects during specimen preparation
- Obtain reproducible results
- Use the least number of steps in the shortest time possible
- Achieve a cost effective operation

Goal of Specimen Preparation for Failure

Failure to obtain these goals can affect the microstructure as follows:

- Details in soft ductile phases may be hidden by smeared materials
- Hard constituents such as silicon may be fractured
- Fine precipitates may be removed, leaving pits that could be misinterpreted as porosity
- Critical edges may be rounded, causing a loss of visual information
- Hard constituents in highly dissimilar materials could experience relief, making an accurate analysis difficult

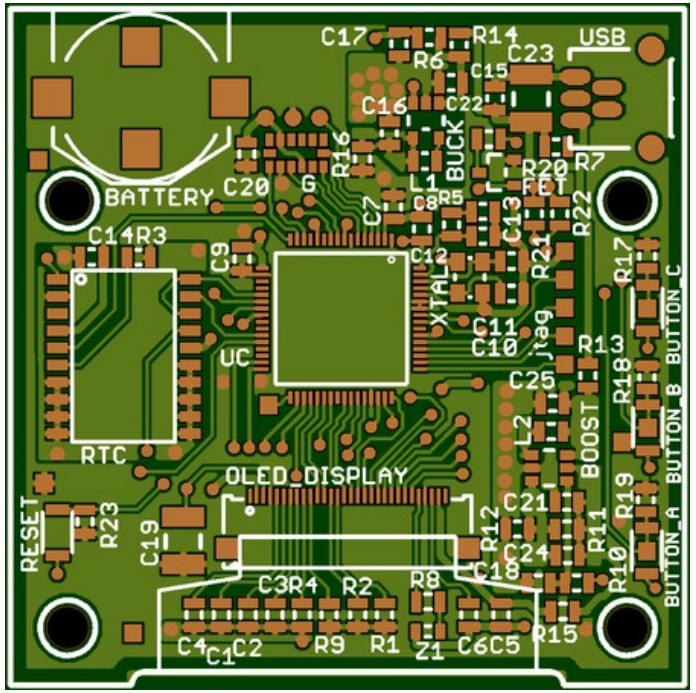
Preparation Steps

'Each step is equally important"

- Documentation
- Sectioning
- Mounting
- Grinding and Polishing
- Visual Examination
- Etching
- Analysis

Documentation

- Process data: vendor, material, batch #, part #, sampling
- Description of specimen orientation, location, cut area, Macro image
- Type of analysis and defect, area of interest
- Record mounting, polishing, etching parameters
- Record microstructure data: inclusions, porosity, grain size, etc.



Sectioning

- Equipment
- Blade, wheel (SiC, alumina, diamond)
- Load
- Blade RPM
- Feed rate
- Coolant
- Delicate materials may require encapsulation or chuck padding for holding

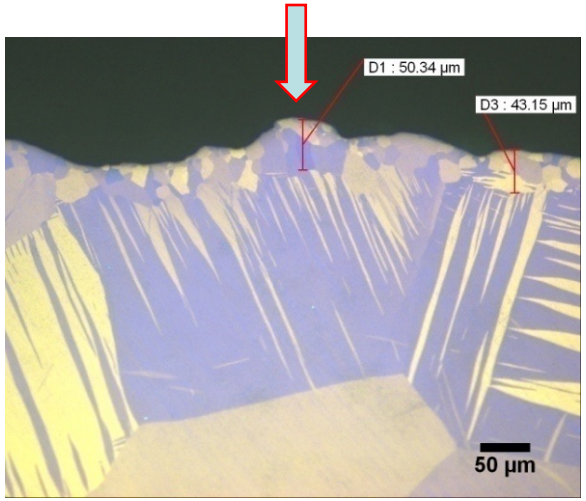
Methods

Method	Comments
Shearing	Severe torsion damage to an undetermined distance adjacent to the cutting edges
Hollow punch (Saved hole)	Convenient, and rapid but limited to boards 0.08” thick or less
Routing	Rapid and versatile with moderate damage but noisy and hard to control.
Band saw	Rapid, convenient moderate damage and easy to control when a 24-32 pitch blade is used at 3500-4500 ft./min.
Low speed saw	Least damage of any method allowing cuts to be made even into the edge of the plated through-hole barrel. However, it is too slow for high volume micro-sectioning.
Precision table saw	Least destructive method of removing specimens from component mounted boards for soldered connection analysis

Sectioning damage

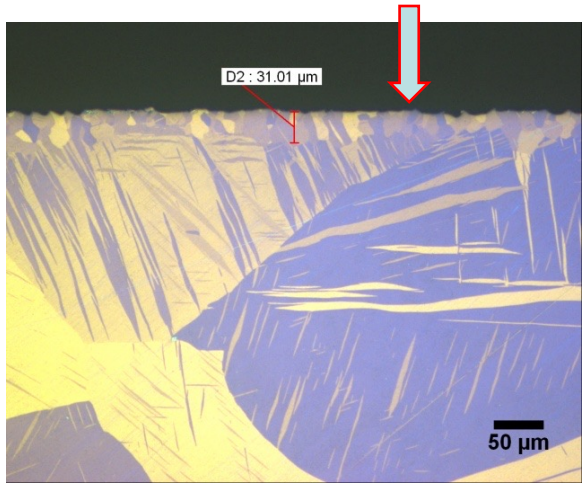
Method	Type of damage	Possible depth
Shearing	Deep mechanical damage	5 mm
Band / hack saw lubricated not cooled	Moderate thermal and mechanical damage	2.5 mm
Dry abrasive cutting	Moderate to severe thermal damage	1.5 mm
Wet abrasive cut-off saw	Minimal thermal and mechanical damage	250 μm
Diamond / precision saw	Minimal thermal and mechanical damage	50 μm

Sectioning Damage - Zinc



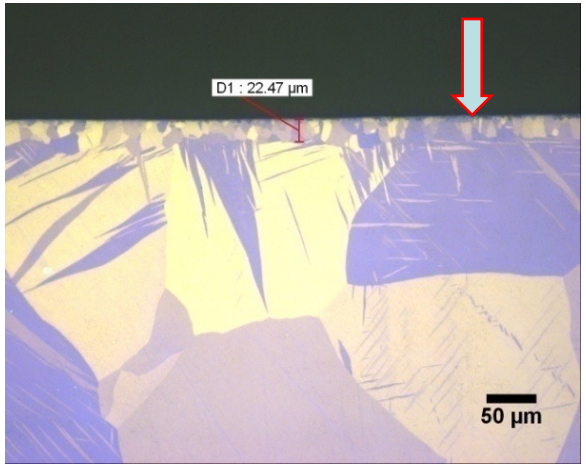
Band saw
recrystallization depth
~50 microns

Note the jagged edge and heavy mechanical twinning will prolong grinding time



Abrasive wheel
recrystallization depth ~
30 micron

Some mechanical twinning



Precision blade
recrystallization depth
~20 microns

Minimum area of twinning

Mounting Principles

- Sample encapsulated in epoxy, acrylic or other compound
- Sample edges protected during polishing process
- Delicate samples protected from breakage
- Smooth mount edges increase life of polishing surfaces
- Allows automation and ability to prepare multiple samples simultaneously
- Uniform pressure on mount maximizes surface flatness
- Safety

Mounting Method Selection

Castable (cold) mounting
- Resin/hardener selection
- Vacuum
- Additives for edges, conductivity

Compression (hot) mounting
- Compound selection
- Pressure
- Heat

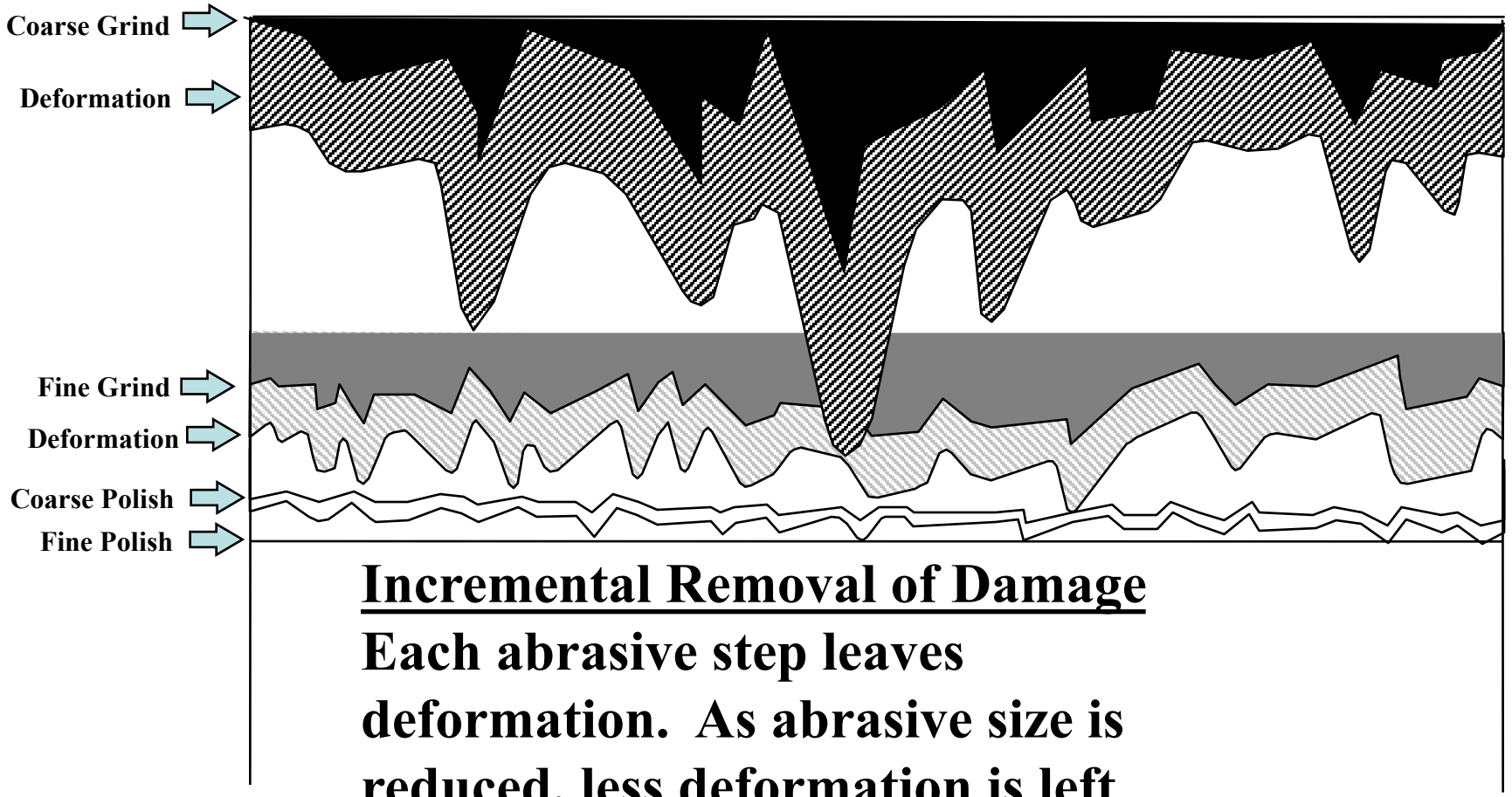
Specimen characteristics to consider:
- Softening/melting temperature
- Sample thickness, ability to withstand pressure
- Brittleness, friability
- Porosity
- Hardness & abrasion resistance relative to mounting compound
- Importance of edge retention

Potting Compounds

Resin of Choice?…EPOXY!

- **Low shrinkage and moderate hardness are important for microelectronics.**
  - **Less surface relief**
  - **Better edge protection**
- **Uncured epoxy typically has low viscosity for filling small cavities.**
- **Epoxy can be cast while under vacuum. This enhances its cavity filling ability.**

Damage



Incremental Removal of Damage

Each abrasive step leaves deformation. As abrasive size is reduced, less deformation is left behind.

Grinding Steps

- The initial grinding surface depends on the condition of the cut surface – more damaged surfaces require coarser first-step grinding
- For excessive damage, re-sectioning with an abrasive or precision saw is recommended
- A single grinding step is adequate for most materials sectioned with an abrasive or precision saw
- Softer materials require multiple grinding steps and smaller abrasive size increments
- Remove damage with progressively smaller abrasive particle sizes
- With decreasing particle size:
    1. Depth of damage decreases
    2. Removal rate decreases
    3. Finer scratch patterns emerge

Polishing Principles

- Further refinement of ground surface using resilient cloth surfaces charged with abrasive particles
- Depending on material characteristics, cloth selected may be woven, pressed or napped
- Commonly used abrasives are diamond and alumina
- The polishing process consists of one to three steps that:
  1. Remove damage from the last grinding step
  2. Produce progressively finer scratches & lesser depth of damage
  3. Maintain edges and flatness
  4. Keep artifacts to an absolute minimum

Time

- Each step must remove the surface scratches and sub-surface deformation from the previous step
- Increase time to increase material removal
- Smaller increments in abrasive size require shorter times at each step
- Increases in surface area may require longer times
- Too long times on certain cloths can produce edge rounding and relief

Additional Considerations

- Bevel mount edges to increase cloth life
- Clean specimens and holder between steps to prevent cross contamination of abrasives
- Ultrasonic cleaning may be required for cracked or porous specimens
- Dry thoroughly with an alcohol spray and a warm air flow to eliminate staining artifacts
- Remove polishing debris by rinsing cloth surface after use to increase cloth life

Final Polishing Principles

- Removes remaining scratches, artifacts and smear
- Produces a lustrous, damage-free surface
- Maintains edge retention
- Prevents relief in multiphase materials

Etching Principles

- Etching is a process of controlled corrosion
- Selective dissolution of components at different rates reveals the microstructure
- Completion of etching is determined better by close observation than timing
- Etching is best performed on a freshly polished surface before a passive layer can form
- A dry surface produces a clearer etched structure than a wet one
- An under-etched surface may be re-etched but an over-etched surface requires re-polishing

Etching Techniques

- Immersion – sample immersed directly into etchant solution
  - Most commonly used method
  - Requires gentle agitation to remove reaction products
- Swab – polished surface swabbed with cotton ball soaked with etchant
  - Preferred method for materials in which staining is a problem
- Electrolytic – chemical action supplemented with electric current
  - Attack controlled by chemical selection, time, amps

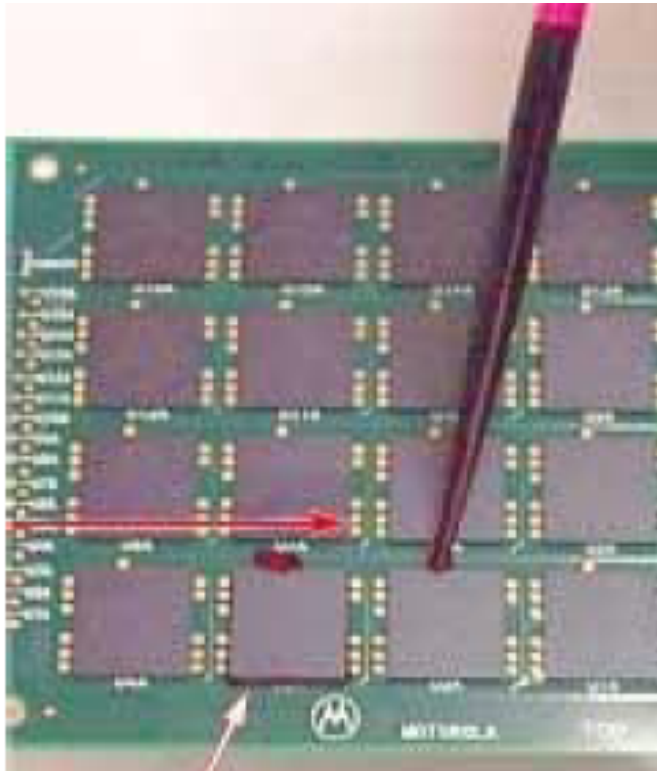
PWB Etchants
(For Copper)

- Equal parts 3% H_2O_2 and ammonium hydroxide, swab for 3 to 10 seconds, use fresh etchant to reveal grain boundaries of plating and cladding copper material.

- 5 g $Fe(NO_3)_3$, 25 mL HCl, 70 mL water, immerse 10 – 30 seconds, reveals grain boundaries very well.

Dye Penetrant (Dye and Pry)

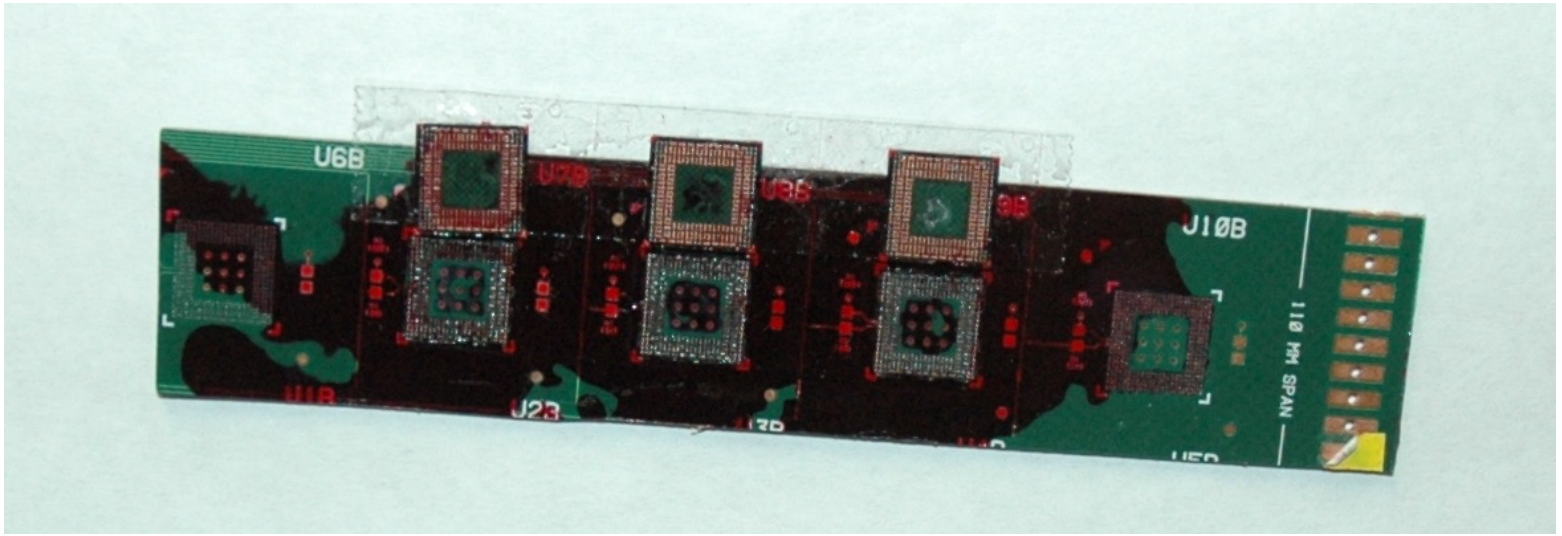
- Identify failed components (electrical measurement)
- Boards are immersed in stripping agent (Miller-Stephenson MS-111) for 25 min at room temperature to remove the solder mask. IPA can be used for a final rinse. Dry in air.
- Dye is applied to the board (DYKEM steel red layout fluid) with a pipette. Important: Flip the board, so that the dye flows into the cracks
- Place boards in vacuum for 5 minutes so that the dye penetrates into fine cracks that otherwise would be blocked by trapped air pockets. A strong vacuum pressure is not important for this process (Typical 220 mm Hg)
- Place the board on a hot plate for 30min 80°C to dry the dye (as prescribed by DYKEM).



Picture: "Solder joint failure analysis" **Dye penetrate technique**
BY TERRY BURNETTE and THOMAS KOSCHMIEDER

Dye and Pry Steps

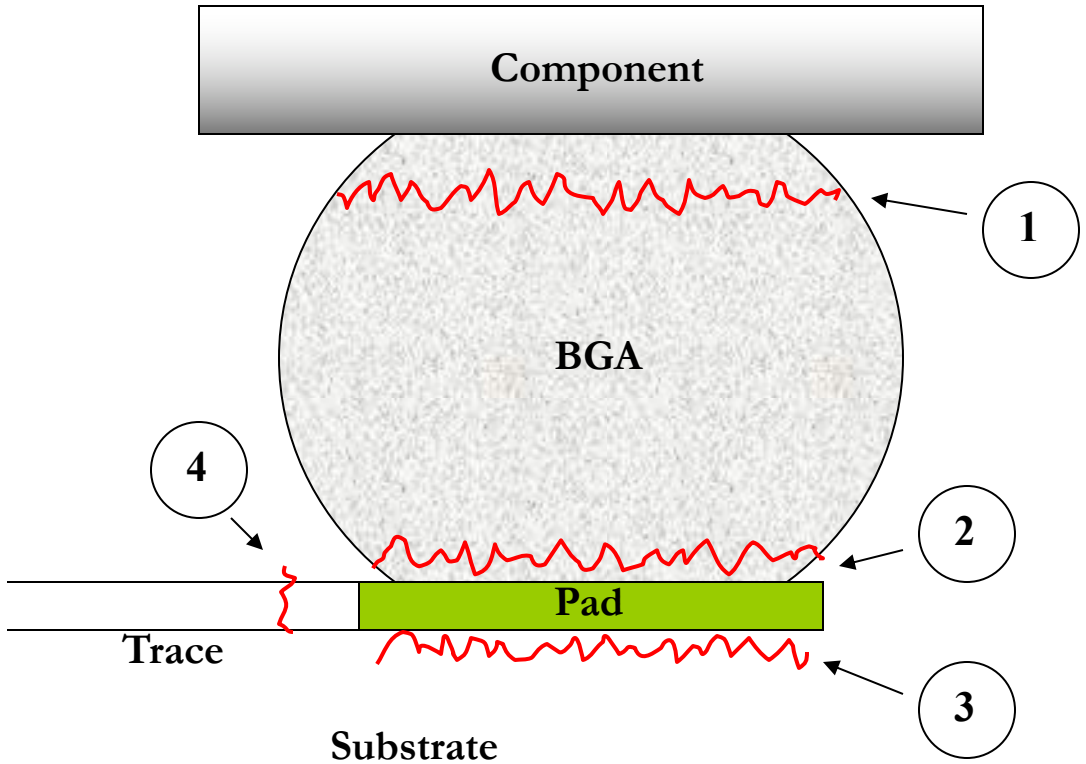
- Flex the board a pair of pliers until the components peel away.
- Remove the components with tweezers and fix with double sided tape on the board, because it is important to see the component side and the substrate side to identify the failure site.



Potential Nonconformities

(For BGAs)

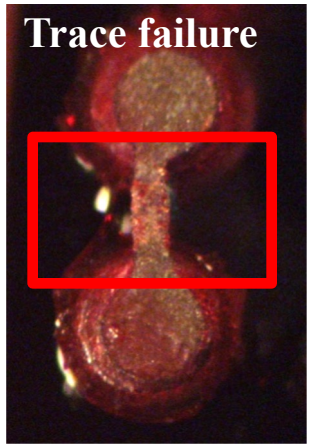
1. Solder Fail (component side)
2. Solder Fail (substrate side)
3. Pad Lift
4. Trace Fail



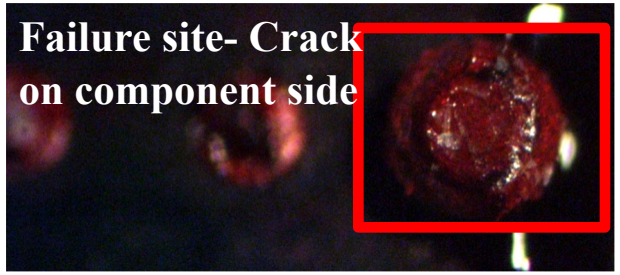
Dye and Pry:
Failure Sites Observed



(a) Failure on board side



(b) Trace failure



(b) Failure on component side



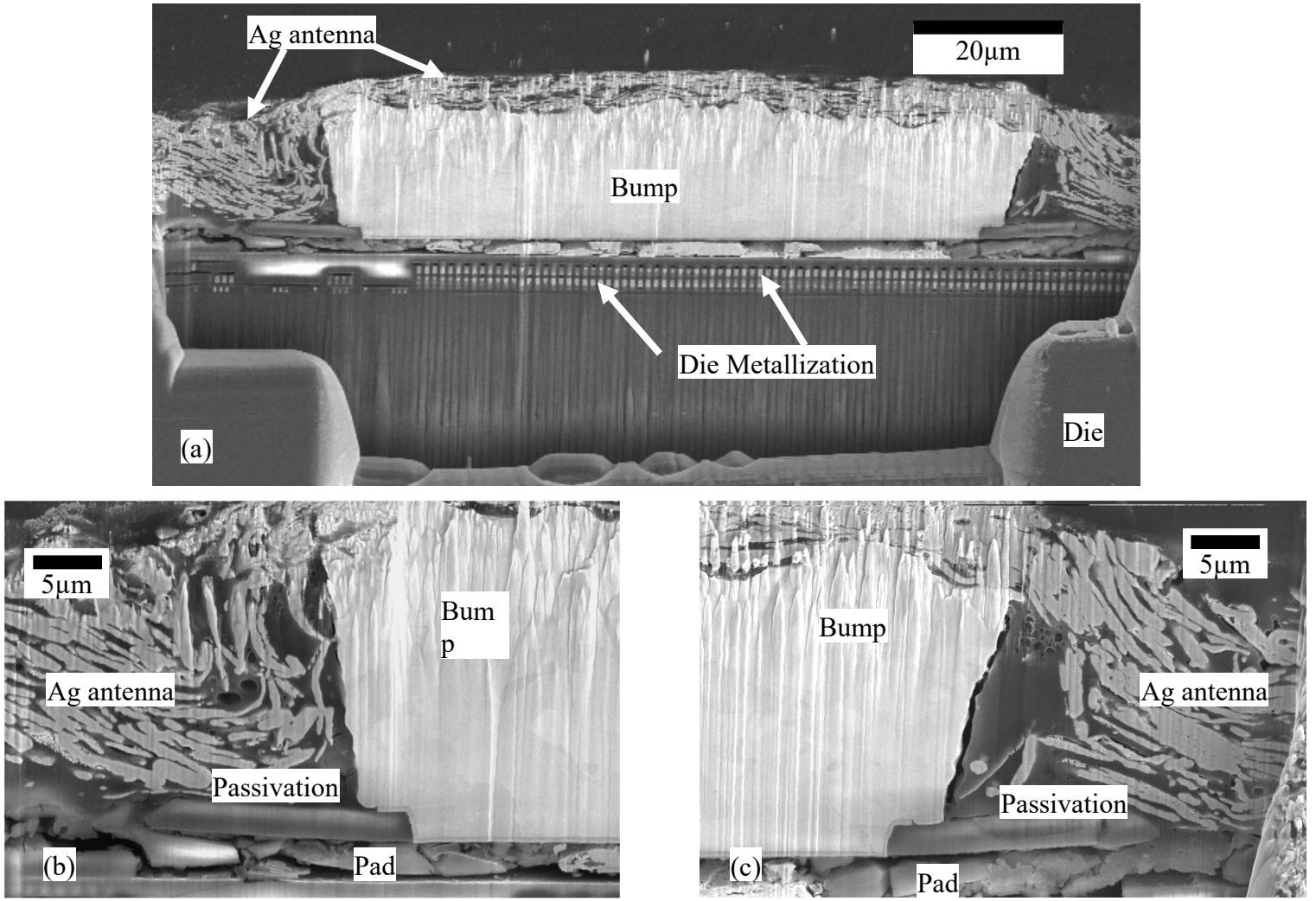
(d) Pad crater

Focused Ion Beam Etching

FIB Introduction

- Focused ion beam (FIB) processing involves directing a focused beam of gallium ions onto a sample.
- FIB etching serves as a supplement to lapping and cleaving methods for failure. The beam of ions bombarding the sample's surface dislodges atoms to produce knife-like cuts.

FIB Cross-section of Bumps



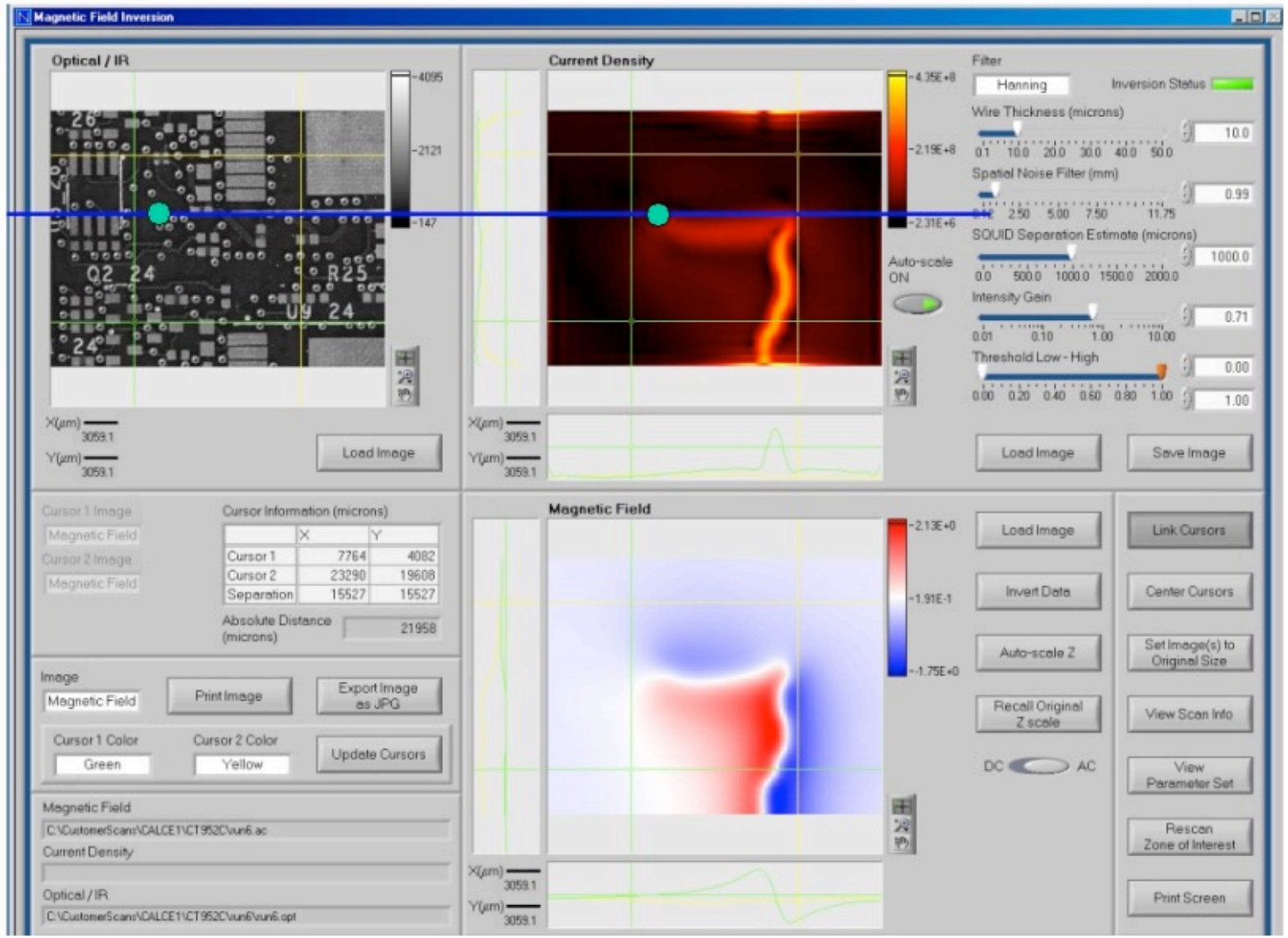
SEM image of a die-bump interface after FIB etching. Overview of the interface in (a) shows the bump, die and silver antenna, (b) and (c) show close up of the bump at two sides.

Focused Ion Beam Limitations

- Equipment is relatively expensive
- Large scale cross-sectional analysis is impractical since the milling process takes such a long time
- Operator needs to be highly trained
- Samples could be damaged or contaminated with gallium
- Different materials are etched at different rates, therefore uniform cross-sectioning using ion milling is not always possible

Superconducting Quantum Interference Device (SQUID) Microscopy

Magnetic Imaging Used to Locate Failures



Spectroscopy, including Fourier Transform Infrared Spectroscopy (FTIR)

Fourier Transform Infrared Spectroscopy – Spectrum Production

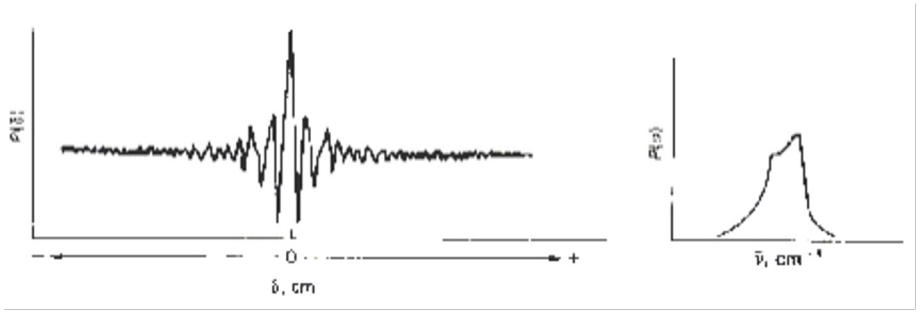
Non-absorbed Light (e.g., Reflected or Transmitted) ← Sample ← Incident Light

↓

Detector

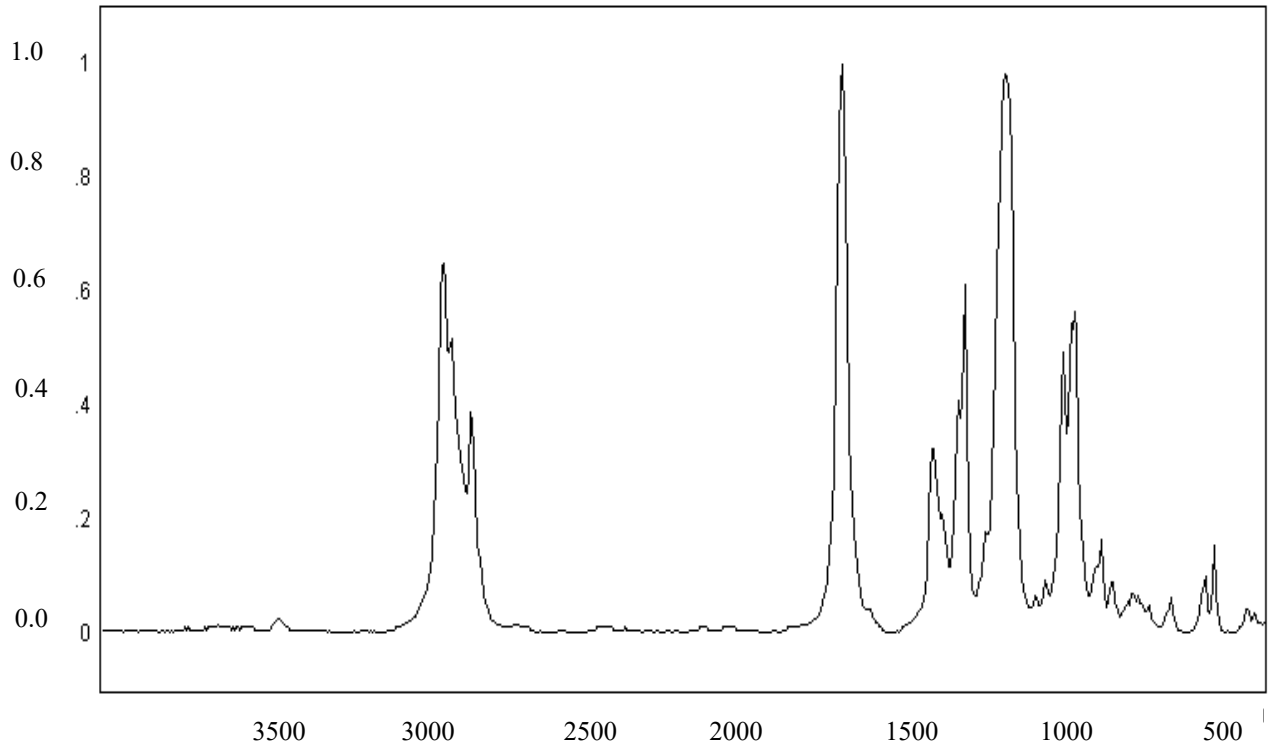
↓

Interferogram (Time Domain) → Fourier Transform → Spectrum (Frequency Domain)



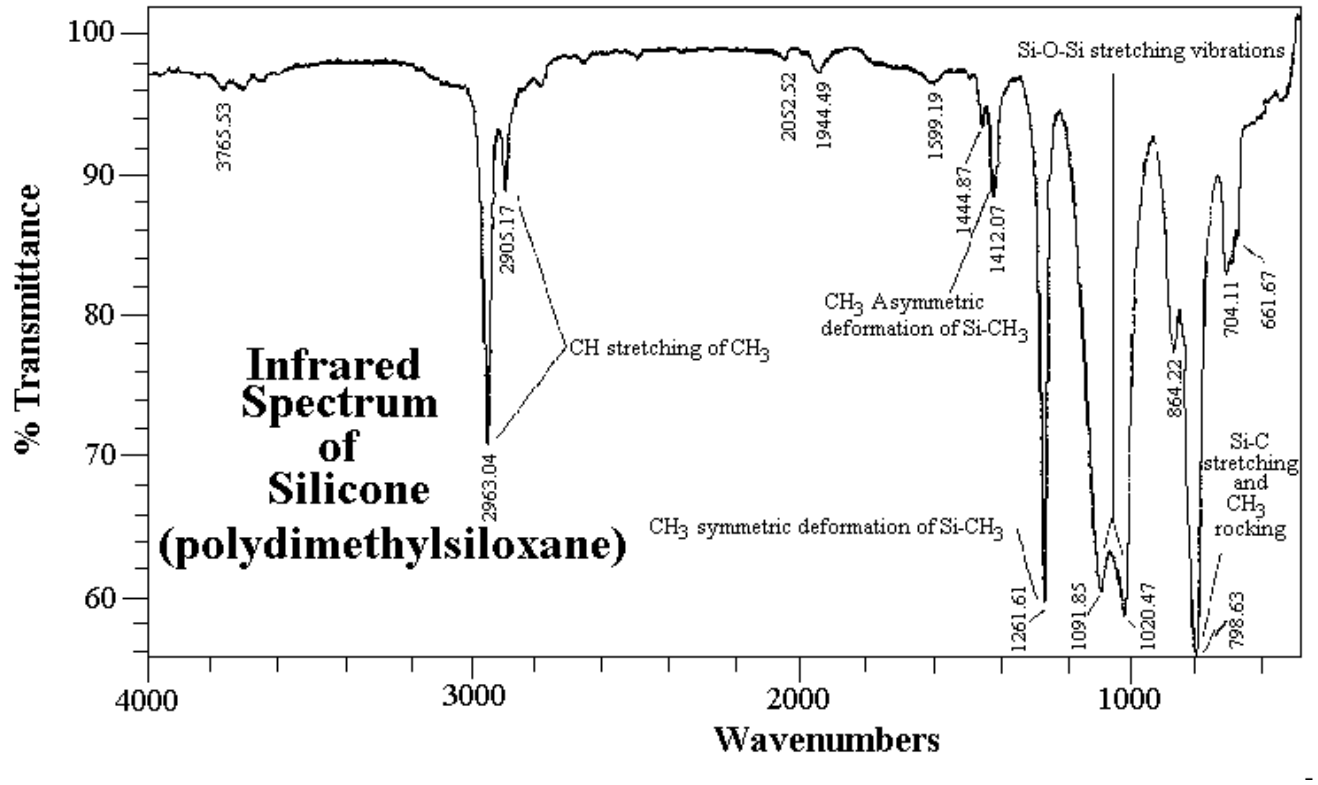
Properties of an Infrared Spectrum

- An infrared spectrum contains absorption peaks corresponding to the frequencies of vibration of the atoms of the molecules making up the sample.



Infrared Spectrum of Acetic Acid Butyl Ester

Fourier Transform Infrared Spectroscopy – Spectrum Interpretation



Correlation with charts of characteristic absorption frequencies → Identification of material

Engineering Applications of FTIR

- Materials identification and evaluation
  - Identification of unknown inorganic and organic materials by comparison to standards and by molecular structure determination
  - Determination of the locations of known and unknown materials
  - Determination of material homogeneity

- Failure analysis
  - Identification of contaminants
  - Identification of corrosion products
  - Identification of adhesive composition change

- Quality control screening
  - Comparison of samples to known good and known bad samples
  - Comparison of materials from different lots or vendors
  - Evaluation of cleaning procedure effectiveness
  - Identification of contaminants

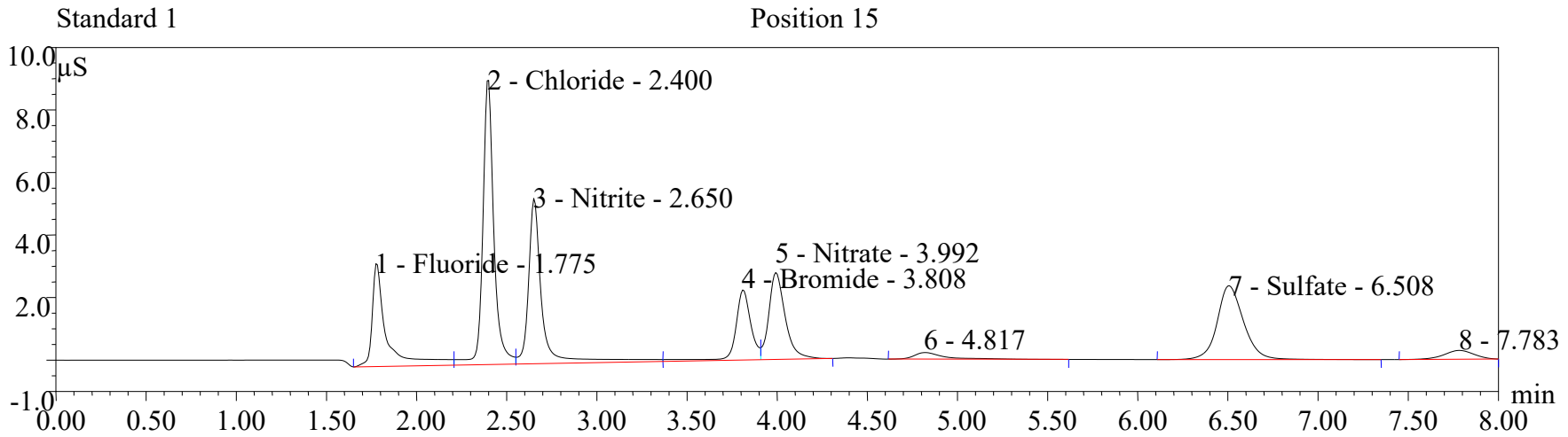
Chromatography

Ion-exchange Chromatography

- Ion exchange chromatography exploits ionic interactions and competition to realize analyte separation.
- It can be further classified into
  - cation exchange chromatography (CEC): separates positively charged ions; and
  - anion exchange chromatography (AEC): separates negatively charged ions.
- The output of a IC test is a graph of conductivity versus time.
- Calibration is with standards of known composition (elution time) and concentration (peak area).

Example of IC Results on a Mixture of Anions

- The eluent was 0.01 mol/L NaOH.
- The column used was an Dionex AS11.



- Based on the retention time, the type of ions can be determined with comparison to standard ions.
- Based on the area under the peaks, the concentration of the ions can be determined.

Applications of Ion Chromatography in Electronics Reliability

1. Tests on assembled or bare printed wiring boards (PWBs) to relate cleanliness to electrochemical migration (IPC-TM-650 Test Method No. 2.3.28).
2. Determination of amount and type of extractable ions present in encapsulation materials to relate amount and type of ionic content to corrosion failure.
3. Electroplating chemistry analysis to relate breakdown products to plating adhesion failure.

Section 6: NASA Goddard's experiences - PCB Supplier Evaluation Study

Study Objective

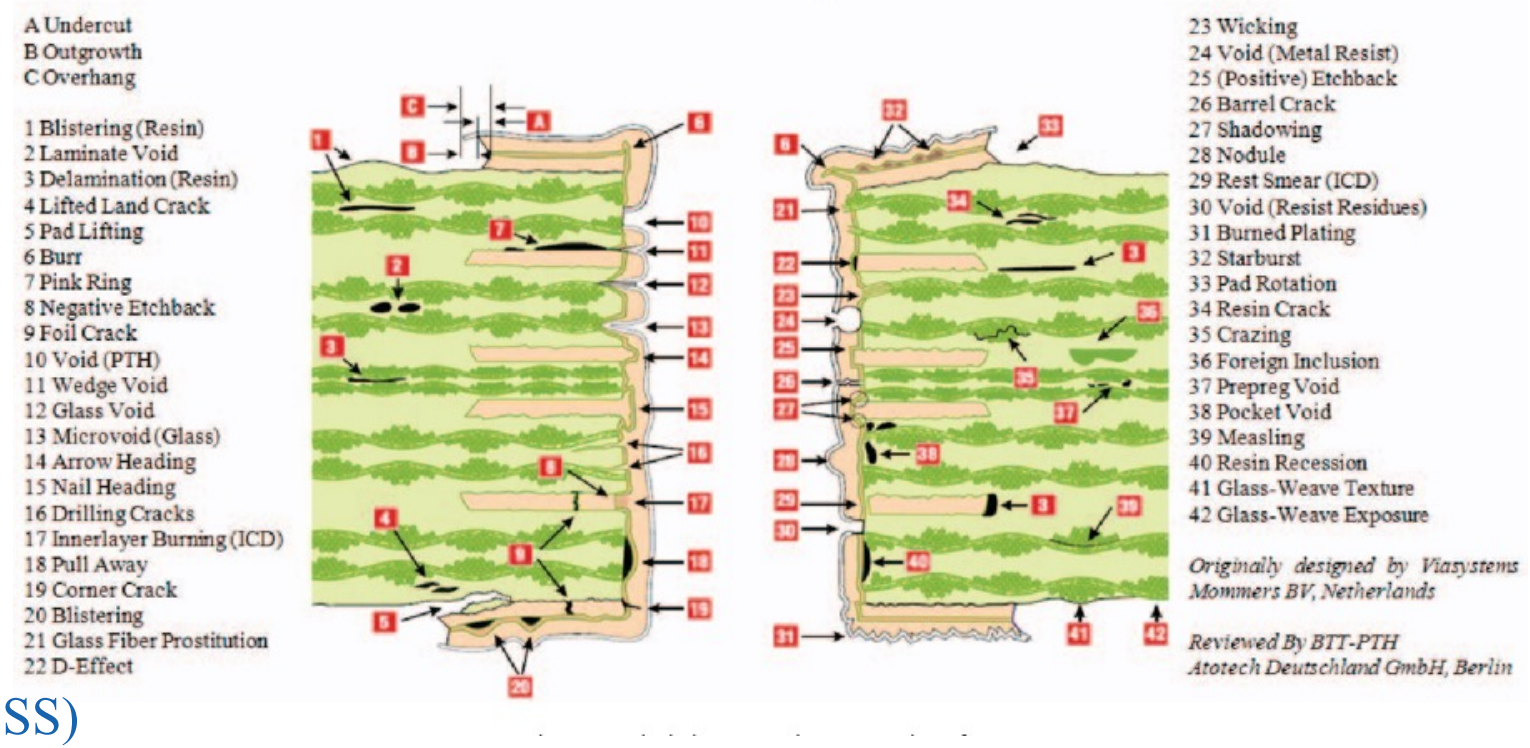
- Evaluate a subset of GSFC PCB suppliers (direct or indirect) and corresponding PCB coupon microsection testing data.
- Develop a methodology for data generation and collection to provide trend analysis
  - Identifies/predicts violation of a process limit criteria (in case of an egregious NC).
- Provide analysis for severity categories of the nonconformance.
- Provide recommendations to the suppliers (i.e. supplier quality engineering, continuous process monitoring, quality metrics definition).

Microsectioning

- Suppliers perform microsectioning and inspect per specifications.

- Secondary GSFC independent microsection analysis yielded 20-30% inspection rejects, caused by:
  - Screening escapes:
    - Test sample quality not consistent
    - Supplier microsection process, inadequate coupons
  - Requirement interpretations
  - Requirements flow-down issues
    - Alternative specifications (MIL, ECSS)
    - Buying heritage and off-the-shelf designs

IPC - PCB Multi-Issue Microsection Wall Poster*

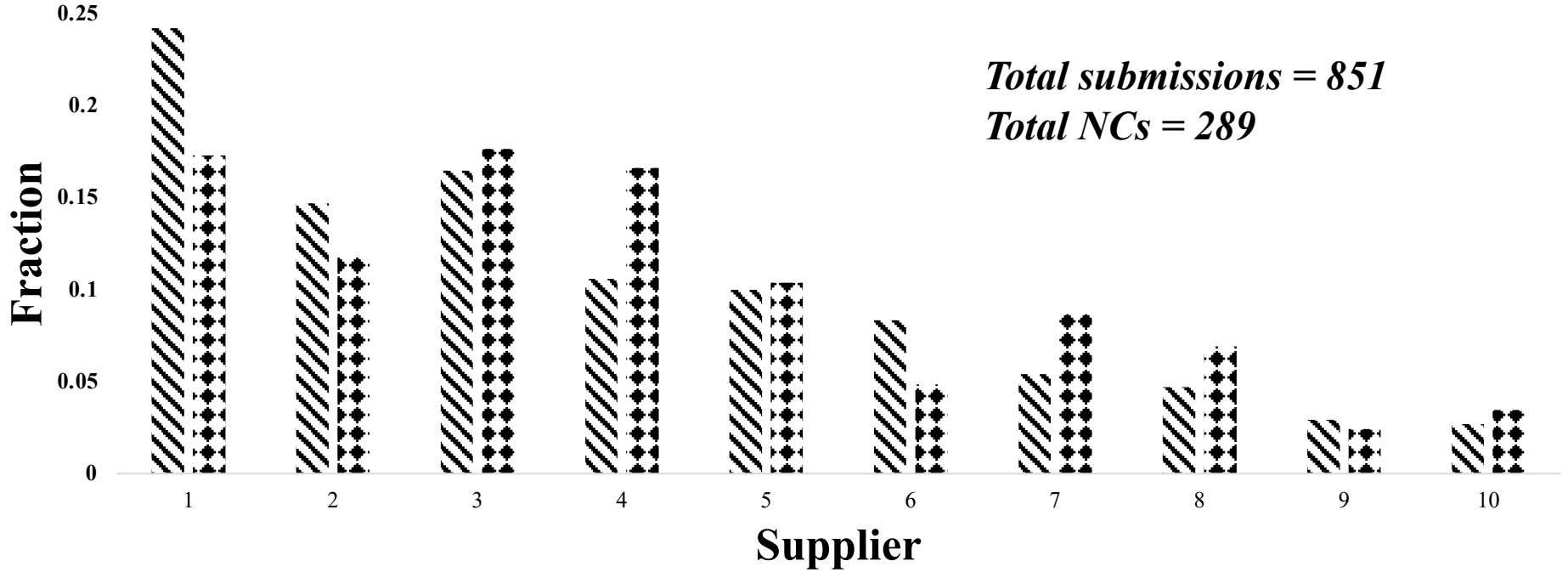


* - https://blog.ipc.org/2010/11/22/pcb-multi-issue-microsection-wall-poster/

Requirements, Nonconformance, Data Generation and Collection

- Present study evaluates jobs performed by GSFC (lately the contribution of 3rd party labs has increased).
  - PCB coupon microsection evaluation in accordance to applicable IPC standards
  - Identified NCs
- Results from all GSFC suppliers were recorded from 2015 – 2020
  - Data includes NC and acceptable conditions in accordance with IPC Standards.
  - Total number of data points: 1224
  - Each job may have a number of NC with different severity levels
- Top ten (submission rate) suppliers represent 851 submissions (~70%)
- Total nonconformance observed for these top 10 suppliers: 289
- For each supplier, analyzed nonconformance(s)
  - Identify severity trend across top 10 GSFC suppliers by analyzing submission rate and nonconformance spread.
  - Classifying and analyzing top 5 severity categories.

Data Analysis –Submission and Nonconformance for Supplier



$$Supplier\ submission\ rate = \frac{total\ submission\ by\ individual\ supplier}{total\ submission\ by\ all\ suppliers}$$

$$Nonconformance\ spread = \frac{total\ nonconformance\ by\ individual\ supplier}{total\ nonconformance\ by\ all\ suppliers}$$

Classification and Analysis - Top 5 Nonconformances

Twenty one distinct conformances observed among the ten suppliers

NC	Nonconformance	Standard
A	Inner layer separations/inclusions	IPC 6012B Class 3/A
B	Electroless Ni less than 118 microinches	IPC 6012B Class 3/A
C	Plating voids	IPC 6012DS
D	Separation/inclusions between plating layers	IPC 6012B Class 3/A
E	Copper wicking in excess of 2.0 mil	IPC 6012B Class 3/A
F	Internal annular ring less than 2.0 mil	IPC 6012B Class 3/A
G	Internal annular ring less than 5.0 mil (drwg. note)	IPC 6012B Class 3/A
H	External annular ring less than 5.0 mil	IPC 6012B Class 3/A
I	Immersion gold less than 3.0 micro inches	IPC 6012DS
J	Electroless nickel and immersion gold plating thickness < 118 micro-inches (Ni) and 2 micro-	IPC 6012B Class 3/A
K	Blind via plating thickness less than 0.8 mil	IPC 6012B Class 3/A
L	Resin recession greather than 3 mil	IPC 6012B Class 3/A
M	Solid copper micro via voids in excess of 33%	8252313C
N	Laminate delamination	IPC 6012B Class 3/A
O	laminate cracks	IPC 6012C Class 3/A
P	Etchback less than 0.2 mil	IPC 6012B Class 3/A
Q	Immersion gold plating thickness in excess of 6 mil	IPC 6012C Class 3/A
R	Copper plating thickness less than 1.0 mil	IPC 6012B Class 3/A
S	Laminate crack greater than 3.0 mil	IPC 6012B Class 3/A
T	Dielectric thickness less than 3.0 mil min	IPC 6012B Class 3/A
U	Laminate void greater than 3.0 mil	IPC 6012B Class 3/A

Common Nonconformances from suppliers

PCB Suppliers

1	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*
A	F	E	K	A	N	E	E	A	E
B	G	D	F	F	O	P	A	F	F
C	H	B	L	D	F	C	D	S	T
D	A	I	J	J	E	D	F	D	U
E	D	J	A	M	P	Q	R	P	R

Analyzing Top 5 Severities of Supplier's Nonconformance

- Observations show the nonconformances with the most occurrences (7 out of 10 Suppliers) are D and F.
- Investigated the contributors to implement techniques which may eliminate theses nonconformances from at least 7 suppliers.

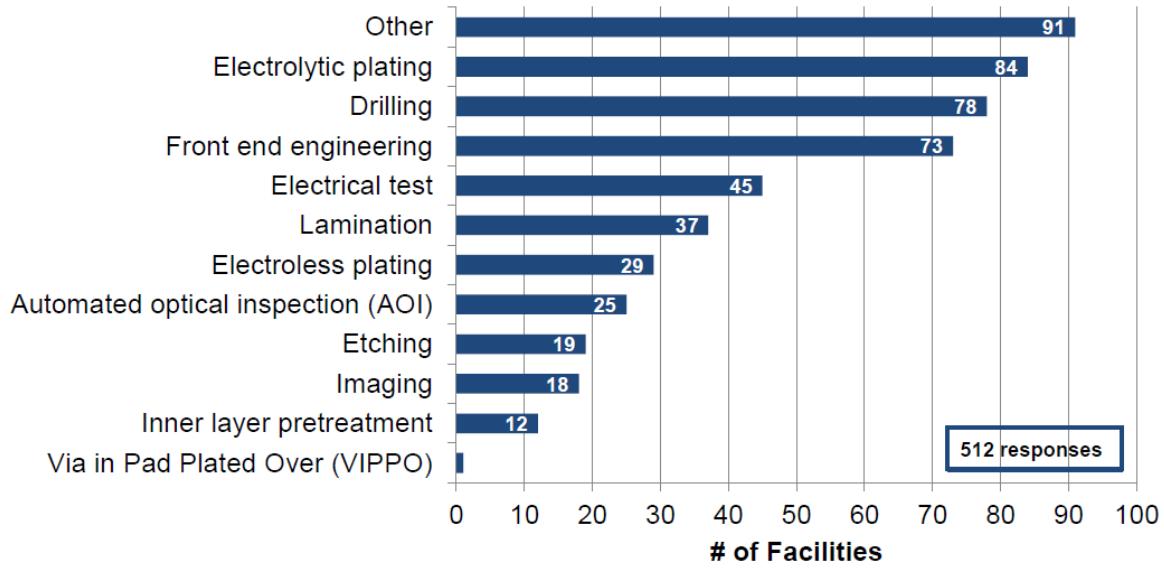
(A) Inner layer separations/inclusions

(D) Separation/inclusions between plating layers

(E) Copper wicking in excess of 2.0 mil

(F) Internal annular ring less than 2.0 mil

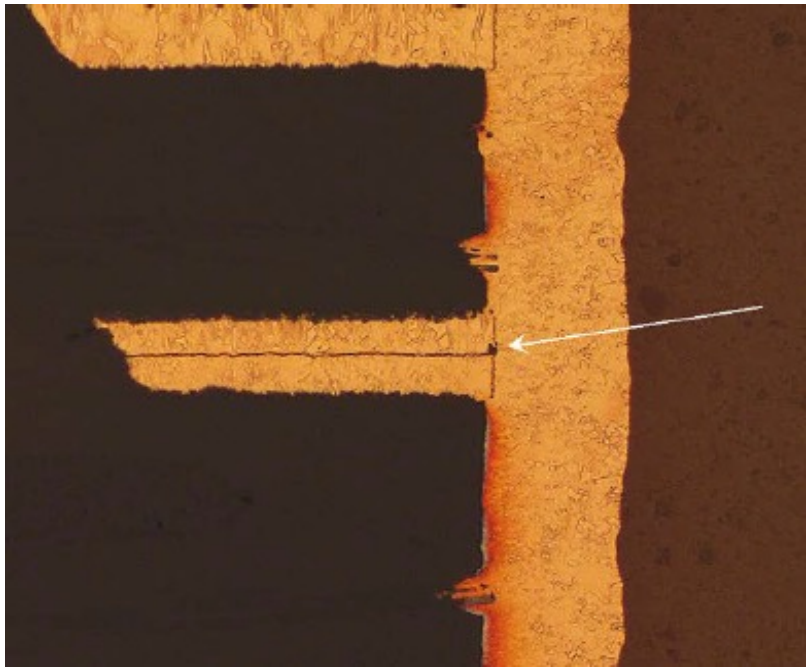
(J) ENIG is less than the minimum requirements



** - "Challenges and Opportunities: State of the U.S. Bare Printed Circuit Board Industry" Crawford M. and Botwin B., IPC APEX Expo, February 11-16, 2017, San Diego CA. Reproduced with permission.*

Inner Layer Separations or Inclusions

- Separation of inner-layer foil and the plated through hole barrel.
- Inclusion - contaminant material that is present in an area where it is not expected.



Risk: intermittent electrical open or complete open after board is subjected to thermal excursions (reflow, wave soldering or rework)

1. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.
2. Swirbel, Tom, Adolph Naujoks, and Mike Watkins. "Electrical design and simulation of high density printed circuit boards." IEEE transactions on advanced packaging 22.3 (1999): 416-423.

Inner Layer Separations or Inclusions

Contributors

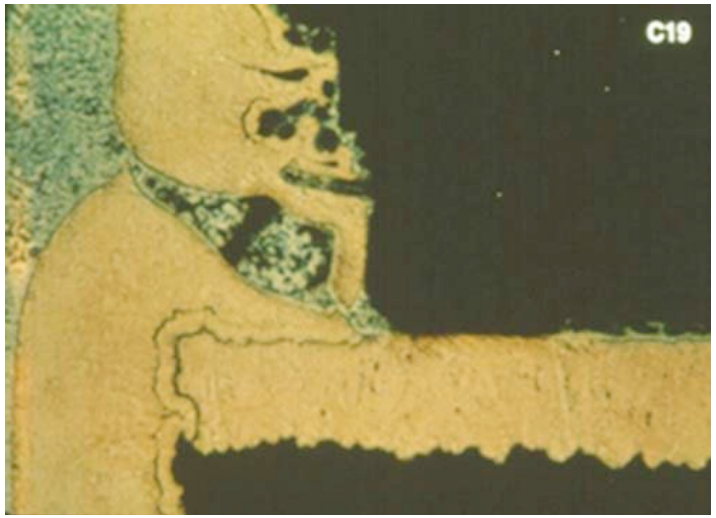
- Improper lamination press or cure cycles whether it be pressure, time, temperature.
- Others include inadequate coverage of inner layer oxide, moisture not completely removed in pre-lamination bake cycle.
- Bad batch of prepreg and or laminate.
- Post-electroless copper cleaning residues, contaminated pretreatment prior to electrolytic plating, or an out-of-control electrolytic copper process.

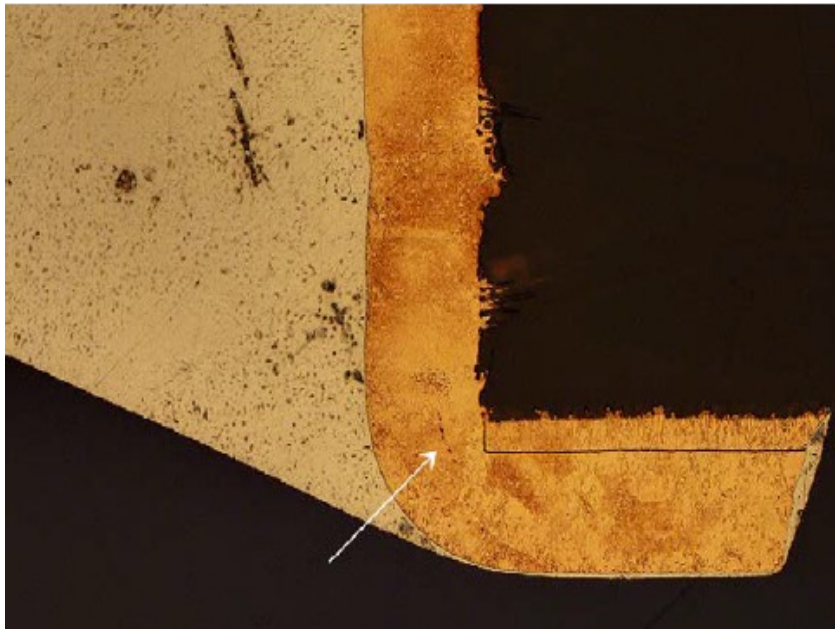
Resolution

- Consistency in drilling processes.
- Reduce the resin content in the stack up.
- Good desmear, with adequate texture.
- Provide adequate copper border for support and resin venting.

Separation or Inclusions Between Plating Layers

Plating separation -The separation between a plating layer and foil.





Risk: intermittent electrical open or complete opens due to mechanical or thermal stresses.

1. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.
2. Yung, Edward K., Lubomyr T. Romankiw, and Richard C. Alkire. "Plating of Copper into Through-Holes and Vias." Journal of the Electrochemical Society 136.1 (1989): 206-215.

Separation or Inclusions Between Plating Layers

Contributors

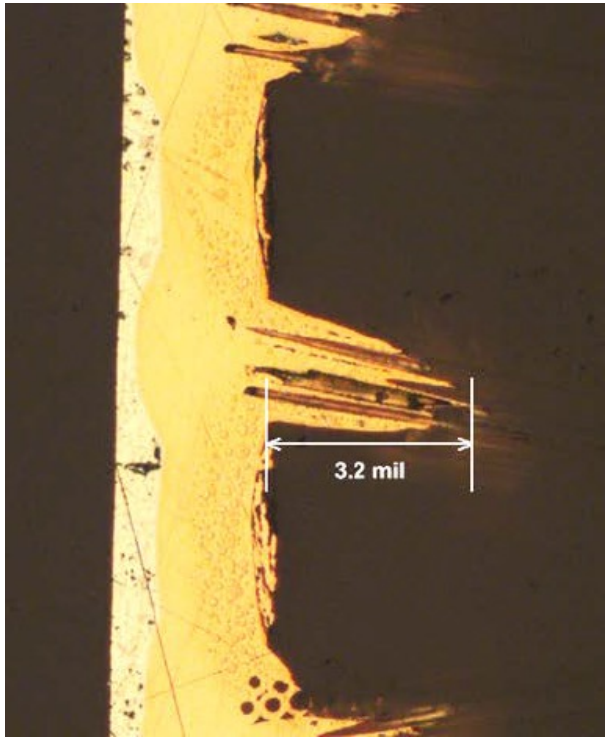
- Incomplete wrap plating
- Overly-aggressive cleaning process
- Insufficient cleaning

Resolution

- Adjust plating parameters
- Optimize cleaning processes

Copper Wicking in Excess of 2.0 mil

The extension of copper from a PTH along the glass fiber fabric.



Risk: intermittent electrical shorts or complete shorts due to bias driven migration of copper towards non-common conductors.

1. Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." Wiley Encyclopedia of Composites (2011).
2. Tummala, Rao R., Eugene J. Rymaszewski, and Y. C. Lee. "Microelectronics packaging handbook." (1989): 241-242.
3. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.

Copper Wicking in Excess of 2.0 mil

Contributors

- Dull drill bits or broken drill bits that cause a crack in the laminate.
- Incompatible laminate material.
- Insufficient glass etch.
- Poor glass to organic adhesion.

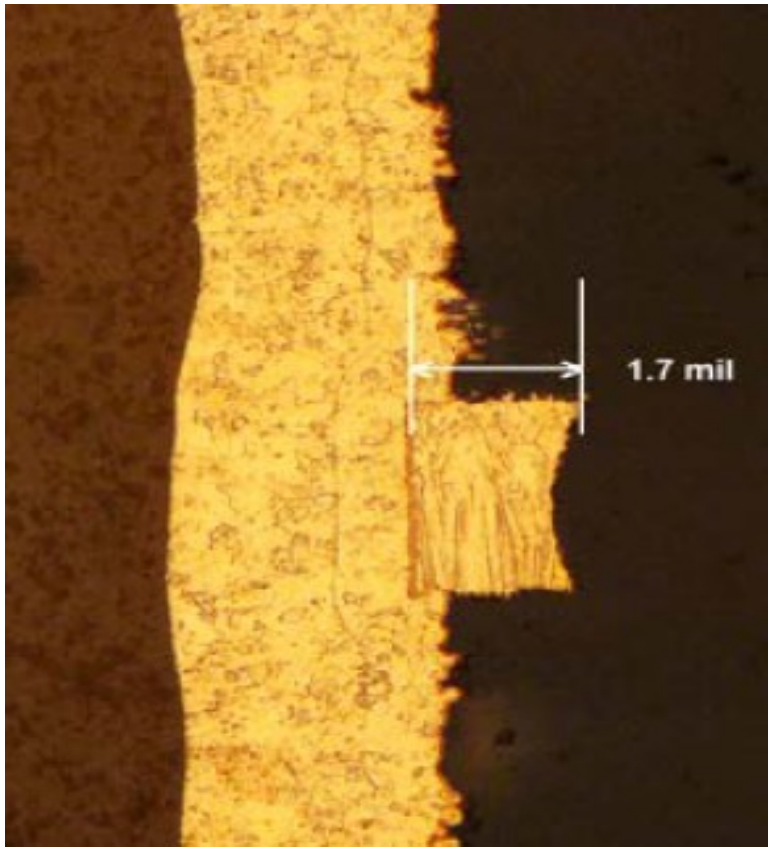
Resolution

- Optimize desmear parameters.
- Improve drilling operation (feed and speed).
- Ensure sufficient resin wet-out of glass fibers (siloxane treatment).

Internal Annular Ring (IAR) Less Than 2.0 mil

This occurs, when the inner layer copper pad (measured from the hole wall plating to its outer most length) is less than 2 mils.

Risk: inner layer breakouts after the board is subjected to thermal excursions (reflow, wave soldering or rework) leading to intermittent electrical or complete open behavior.



- **These IAR non-conformances are to an older revision of the spec. IPC 6012 transitioned to 1mil IAR in Rev C.**
- **Need more work to understand risk associated with ≤ 1mil IAR.**
- **IAR NC is a common one when working with high density design features. Most of our designs are high density.**

1. Sood, Bhanu, and Sindjui, N. "A Comparison of Registration Errors Amongst Suppliers of Printed Circuit Boards“, Proceedings, IPC APEX Expo (2018).
2. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.

Internal Annular Ring Less Than 2.0 mil

Contributors

- Drilled-hole pattern not matching the lands on the internal layers (Misregistration).
- Lamination process.
- Prelamination treatments that involve scrubbing or bending may stretch the thin laminate, which will then shrink after it is etched and baked dry.
- Application of specification or drawing notes.

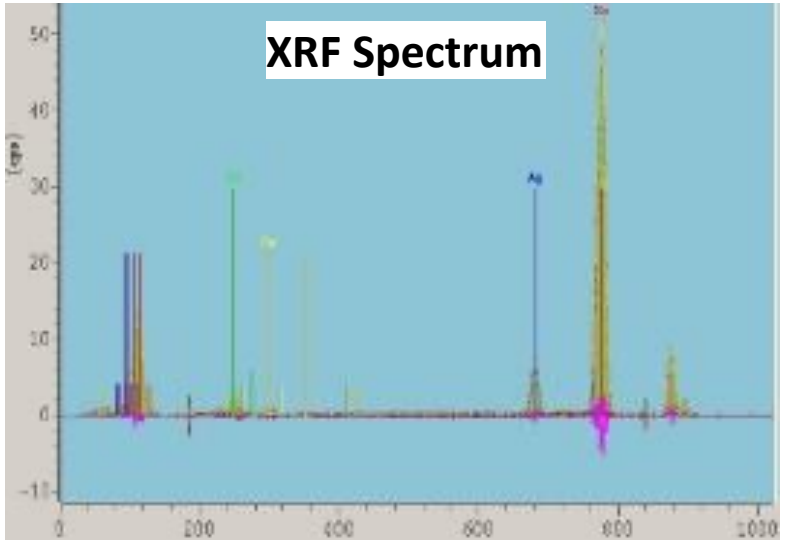
Resolution

- Better material selection of laminate, improved cleanliness, and reduction in the amount of volatiles.
- Confirm whether or not it is operator error.
- Update drawing notes to bring the notes in line with current industry maturity levels.

ENIG (Au or Ni) Less than the Minimum

Electroless nickel and/or immersion gold plating thickness (ENIG) is less than the minimum requirements (118 micro-inches for Ni and 2 micro-inches for Au).

Risk: (1) solderability and, (2) excessive dissolution of copper into the bulk solder (forming brittle intermetallic) when nickel is thin.



1. Johal, Kuldip, and Jerry Brewer. "Are you in control of your electroless nickel/immersion gold process?." Proc. Of IPC Works. No. S03-3. 2000.
2. Meng, Chong Kam, Tamil Selvy Selvamuniandy, and Charan Gurumurthy. "Discoloration related failure mechanism and its root cause in Electroless Nickel Immersion Gold (ENIG) Pad metallurgical surface finish." Physical and Failure Analysis of Integrated Circuits, 2004. IPFA 2004. Proceedings of the 11th International Symposium on the. IEEE, 2004.
3. IPC-4552 – Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards

ENIG Less than Minimum

Contributors

- Improper cleaning of surfaces.
- Improper or inadequate rinsing.
- Bath parameters not being followed (pH and chemical).
- Bath temperature too low.
- Copper surface not clean of oil or inhibiting film.

Resolution

- Re-clean copper using chemical cleaners or mechanical.
- Scrubbing Institute micro-etch step to improve cleaning.
- Improve rinsing(Check flow, agitation and water quality).
- Raise temperature per supplier specifications.
- Readjust to supplier operational parameters.

Summary - PCB Supplier Study

- The test data is analyzed using statistical method to provide trend analysis for all suppliers.
  - Root cause(s) and key contributors are identified.
  - Mitigation plan is included for the root cause of nonconformance.

- Provide recommendations to the supplier's process, identification and prediction of nonconforming process limit criterion, and improve test standards.
- New technologies (example: smaller annular rings, via-in-pads, thinner laminates or newer plating) are implemented on the basis of supplier maturity and reported NCs.

Conclusions

- Printed circuit board (PCB) quality and functionality are influenced by a variety of factors.

- The workshop provided overview of mechanisms and analysis guidelines that can be implemented at different stages of PCB production.

- This information is intended to be used by board manufacturers, assembly houses and OEMs to prevent damage and to increase the quality and reliability of PCBs.

What Does the Future Hold?

- Higher density boards (spacing is tighter)
  - Decreasing pitch, from 500μm to 100μm (or less), thicker boards
- Higher expectations of reliability
  - Rougher handling, harsher environments
- Higher circuit switching speeds
  - Makes the PCBs more susceptible to moisture ingress related reliability concerns.

Questions?



Bhanu Sood

Safety and Mission Assurance (SMA) Directorate
NASA Goddard Space Flight Center
Phone: +1 (301) 286-5584
bhanu.sood@nasa.gov