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Gateway Command and Data Handling Network Implementation and Validation

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Abstract

As initial Lunar Gateway modules approach design maturity, the Artemis Network Validation and Integration Lab (ANVIL) has begun demonstrations to validate avionics network dataflows. The flight architecture design includes utilizing Time-Triggered Ethernet (TTE) and layer-3 switching capabilities to enable greater automation and flexibility of critical and best effort traffic. Critical traffic is considered as Time-Triggered (TT), Rate Constrained (RC) and prioritized Best Effort (BE) traffic classes. End systems, such as mission computers, power control, and robotics, use three planes and all traffic classes while other devices interface via Best Effort. Typical best effort devices include video, laptops, wireless access points, and payloads. Other devices have a various hybrid approach of interfaces including alarms, telemetry/logging, and communication units.

In the paper, we will present an update of the Gateway network architecture and how the system will operate nominally and during a stack topology reconfiguration. We will also discuss the network risks, and trade-offs of performance, flexibility, and redundancy. Finally, we will show the process for validation, demonstration, and verification approaches to the vehicle network.

Keywords: Gateway, Avionics, C&DH, Time-triggered Ethernet, Network, Rate Constrained, Best Effort

Acronyms/Abbreviations

ANVIL	Artemis Network Validation and Integration Lab
BE	Best Effort
C&DH	Command &Data Handling
CMV	Gateway Co-manifested Vehicle
GDS	Gateway Data Services
EDU	Engineering Development Unit
IEEE	Institute of Electrical and Electronics Engineers
IP	Internet Protocol
ISS	International Space Station
IVR	Intra-Vehicle robotics
JSL	Joint Station LAN
LAM	Local Area Network
LPGF	Low-Profile Grapple Fixture
MSM	Module System Manager
NASA	National Aeronautics and Space Administration
PCF	Protocol Control Frame
PCI	Peripheral Component Interconnect
RC	Rate Constrained
RUC	Rectangular Umbilical Connectors
RTOS	Realtime Operating System
TT	Time-Triggered
TTE	Time-Triggered Ethernet
VL	Virtual Link
VSM	Vehicle System Manager
WAP	Wireless Access Point
XML	Extensible Markup Language

1. Introduction

As NASA, international partners, and commercial vendors approach launch of Gateway's first component to establish human presence in Lunar orbit, the Gateway Avionics team is working on creating a robust and reliable network architecture to support years of future exploration.

The Gateway Program is one of NASA's latest initiatives that extends space exploration beyond low earth orbit. The process is like the international space station with vendors and international partners building modular components.

Gateway allows for NASA to prove technologies and mature systems necessary to live and work on another celestial body before embarking on multi-year missions to Mars. The Gateway is a human-tended space station orbiting the Moon that will provide extensive capabilities to support NASA's Artemis campaign. Gateway will be a critical platform for developing technology and capabilities to support Moon and Mars exploration in the coming years.

With the increased autonomy, distance, and mixed criticality of systems on the same network, the Gateway Inter-element network provides command and data handling capabilities to all systems to support functions of Gateway. A reliable and robust network is a requirement for the Gateway program to serve for the next 15 years after first launch.

2. Architecture

Gateway module to module network architecture includes three planes of symmetrical or replicated critical traffic. The critical traffic includes classes of Time-triggered (TT), and Rate Constrained (RC). TT is based on the SAE AS6802 standard, and RC the ARINC 664-part7 standard [1].

TT and RC traffic classes use a form of time synchronization, scheduling, and path reservation to provide a deterministic link. The mechanism for time synchronization is a protocol control frame (PCF) that is sent from sync master end systems to a compression master switch. A TTE network planning tool is used for reserving traffic shaping slots to guarantee proper scheduling and delivery of frames. For path reservation, a virtual link (VL) is defined for each link and additional VLs are established for each plane to achieve fault-tolerance [2].

While TT, and RC traffic classes are symmetrical on all three planes, the best effort traffic class is not symmetrical and is only active on a single plane at a time. Since most best effort devices are uniquely single plane, cross plane switching sometimes needs to occur for certain links. The Layer 3 switches can provide the cross plane switching primarily and to bypass the layer 3 switches, TTE switches are also linked across planes for best effort traffic only. Best effort traffic class is based off the IEEE 802.3 standard and includes Internet Protocol (IP) addressing and higher layer stacks.

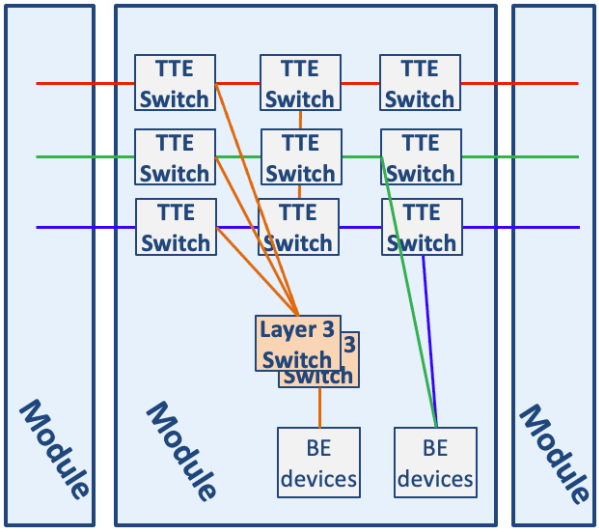

Fig. 1. Architecture Overview

Figure 1 shows the high-level network topology for the Gateway inter-element network. A matrix of TTE layer 3 switches can interface with TTE devices across 3 symmetrical planes, represented as red, green, and blue switches string. The same TTE switches can interface with best effort devices directly or via Layer-3 switches represented in the orange interfaces.

Layer 3 switches enable best effort traffic to be prioritized via quality of service or grouped in Virtual LANs (VLANs) or subnets. Best effort routing changes can be dynamic and not affect TTE switch configuration. This reduces the ground operators work hours manually configuring address tables and eliminates restarting a critical TTE switch for best effort dynamic topology changes. The layer 3 switches also meet safety and security requirements by separating routing of certain subsystem traffic [3].

Modules can choose to have other internal module networks beyond what is diagrammed. An internal module network is referred to as an intra-element network. An intra-element network would be focused on interfacing with local module specific devices and other non-network serial interfaces.

The inter-element network is aptly named because each of the three planes span beyond elements via a rectangular umbilical connector (RUC). Figure 1 shows a single set of three active planes spanning each module as logical flow, but Figure 2 shows physically how there is a pair of RUCs enabling redundancy for each set of three planes.

In the physical diagram of Figure 2, there is a RUC A and RUC B set of ethernet interfaces. If there is an issue where the connector pins on RUC A do not conduct upon initial docking, the active planes will switch to RUC B. One RUC, either RUC A or B, will be active at a time. Thus, on each TTE switch side one port per plane will also be active. The RUC is a passive cable harness though, so if nominally docked all connectors will allow for data connection.

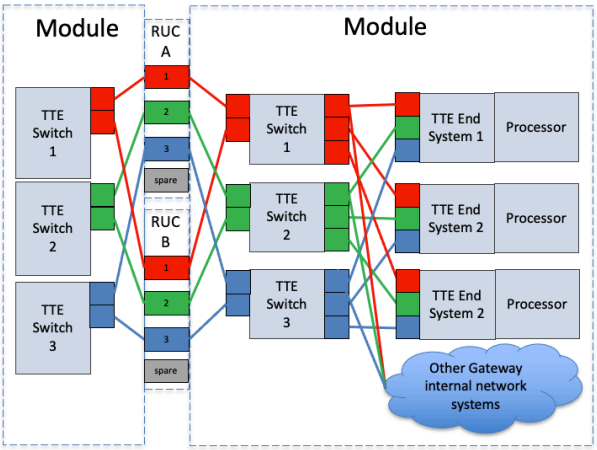

Fig. 2. Module to Module and Rectangular Umbilical Connector Interfaces

Beyond the RUC on Figure 2, each module contains TTE End Systems for critical devices such as mission computers. Each mission computer or processor is cross strapped to all three planes and symmetric in TT, and RC

traffic generation. For receiving data, a TTE end system will accept the first available frame.

Science Payloads will be stored in payload lockers as shown in Figure 3. Each payload locker space will interface to either Layer-3 switch or directly to TTE switches.

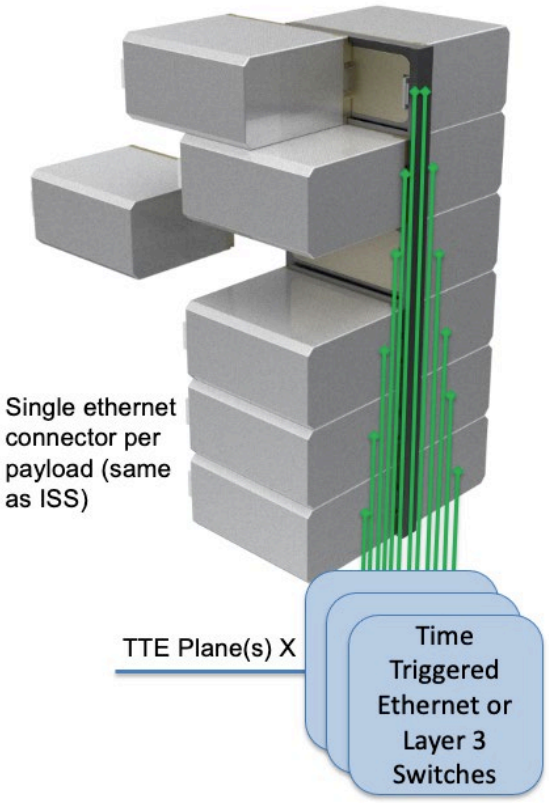

Fig. 3. Payload Interfaces

Payload health and status and bandwidth management will be coordinated by a Payload System Manager in module processors. The Payload System Manager provides the ability to autonomously monitor and control payloads in concert with the overall Gateway concept for autonomous operations [4]. The PSM connects to all three planes of the Gateway inter-element network. The PSM will typically communicate with the payloads in a module using BE traffic unless a payload is deemed to have hazardous or critical operations. If a payload is hazardous or critical the PSM will use RC or TT on all 3-planes.

3. Concept of Operations

The Gateway inter-element network provides an integrated digital communications backbone for the entire Gateway vehicle using industry-proven Time-Triggered Ethernet (TTE) technology. The network enables high-bandwidth real-time communications between devices hosting the Gateway Vehicle System Manager (VSM) software, devices hosting Module System Manager (MSM) software, payloads and payload management computers, robotics, personal computers, and other devices, and allows Gateway to communicate with visiting vehicles and lunar surface assets.

The Gateway inter-element network supports deterministic communications between devices to allow real-time operations, payloads, and safety critical operations using Time-Triggered (TT) and Rate Constrained (RC) traffic classes, while also supporting non-critical data transfers using BE traffic. It is highly reliable and scalable. The network inherently supports the phased deployment and integration of Gateway modules, the addition and removal of scientific payloads, and the periodic presence of visiting vehicles. It provides pathways for future upgrades to both the network backbone and individual devices using common, standards-compliant equipment.

4. Trade Offs and Risks

The TTE end system cards for each critical device do much to automate and provide redundancy and guaranteed determinism of frame delivery. However, each card can also add complexity. Naturally adding an end system card to each processor also adds another bus interface. In some cases, an additional bus interface adds bottlenecks in the dataflow either from the serial speed or memory access rate. In addition, the memory buffer can constrain dataflows and ultimately the number of links and frequency for each TT or RC link.

While processors with TTE end system cards can use all three planes to establish VLs, the robotics arm control unit processor will use two TTE planes. This trade was recently completed because of the number of low-profile grapple fixtures (LPGFs) the vehicle required would drive the switch ports numbers far too high. Even though the robotics system uses two TTE planes the TTE scheduling on all three planes will still be symmetrical.

Similarly for payloads to have multiple links would drive switch port count, thus most payloads utilize a single wired interface. Using one plane and BE traffic class for payloads carries the risk of potentially losing important payload owner data and will be mitigated by the payload provider using temporal redundancy on a software level if determined necessary.

As referenced in Section 2, the architecture now dictates the need for layer 3 switching. Since TTE switches are only layer 2, and many BE devices are interfacing using IP-addressing layer 3 switches were added to some modules. Layer 3 switching will ultimately automate and provide needed flexibility in network configuration. The switches will bridge VLANs for certain systems with enabled cross plane links.

Figure 4 shows a photo of the current International Space Station (ISS) Joint Station Lan (JSL) switches. JSL devices typically utilize a single port for each device as

well. The ISS physical layer currently supports fast ethernet 100Base-TX, however Gateway will utilize 1000Base-T ports [5].

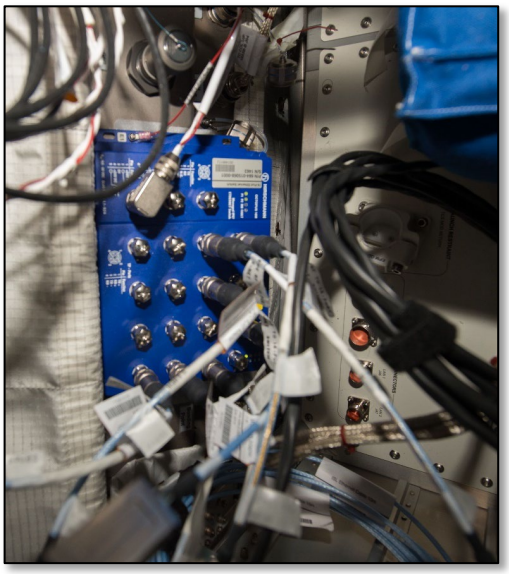

Fig. 4. International Space Station LAN Switches

ISS is fortunate to have a separate JSL network for flexibility on topology changes [6]. Before adding layer 3 switches to Gateway a change in device topology would have required power cycling backbone inter-element TTE switches. By adding separate layer 3 switches the TTE switches can remain static. Thus, from an operations perspective separate layer 3 switches allow the more critical background TTE switches to remain static for changes [7].

5. Verification

Gateway Avionics established an iterative approach to verification and validation of the network. The network data flows are being proven out through several iterative testbeds. Testbeds start with development and validation. Testbeds include partial rack based, Linux-based, and Real-time OS (RTOS) based Engineering Development Unit (EDU) hardware.

Initially single racks have been constructed to test out the initial demonstration of software applications and performance. These racks are known as Gateway in a rack and can only emulate a small portion of a module's topology.

Building upon the rack testbed is a more complex testbed of several racks of Linux hosts and TTE end systems to show a full module topology with TTE lab switches and multiple planes. This is the current approach used in the Artemis Network Validation and Integration Lab (ANVIL). Recently, commercial layer 3 switches have been added to the testbed to prove out how best effort traffic can be shaped and routed onto layer 3 with bridged VLANs.

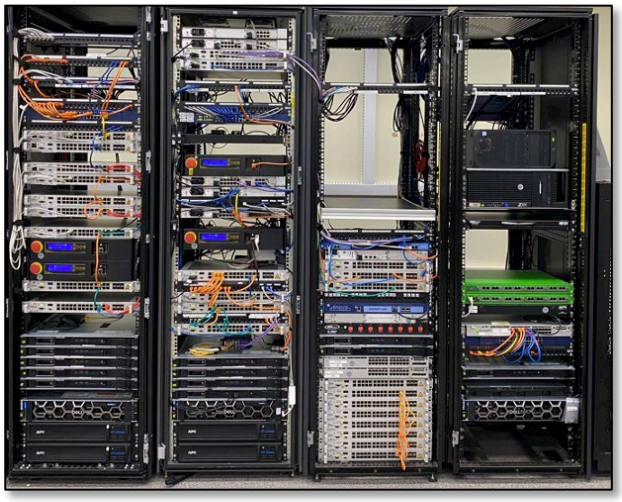

Fig. 5. Module to Module Linux Testbed

Figure 5 shows the current rack setup of the module-to-module testbed in ANVIL. Each rack is roughly generating traffic flow for a single module. Devices are hosted as virtual machines on servers with compact Peripheral Component Interconnect (PCI) end system cards. The hardware is more lab grade vs EDU flight grade but allows for a flexible and rapid development of demonstrations.

With multiple plans on this testbed, demonstrations such as network reconfiguration can take place. Reconfiguration means deploying new binaries to each TTE component in the system when network topology changes. The event for reconfiguration includes new module docking and TTE unit relocations. The binaries contain data for virtual link routing, timing, and scheduling. Synchronization, VLAN tags, and RC traffic routing is also contained in the binaries [8].

Normally TTE vehicular networks are simpler to configure, the operation can be done with a grounded aircraft or equipment not in use. However, Gateway is in a continually operating orbit with no physical access before crew arrival.

The current baseline for reconfiguration is that a central system manager can execute reconfiguration on a single plane at a time and then check each end system, then each switch on the plane for proper communication. Gateway's central system manager first receives reconfiguration data from the ground and then executes the operation.

Figure 6 shows an initial evaluation of a Wireless Access Point (WAP) for Gateway. Shown in this test setup are four wireless access points. The initial configuration for crew and devices, including inter-vehicular robotics (IVR) will need partial wireless

functionality, and additional WAPs can be added over time. Initial radiation tests of WAP candidates show physical commercial processors are not robust enough to overcome the lunar environment.

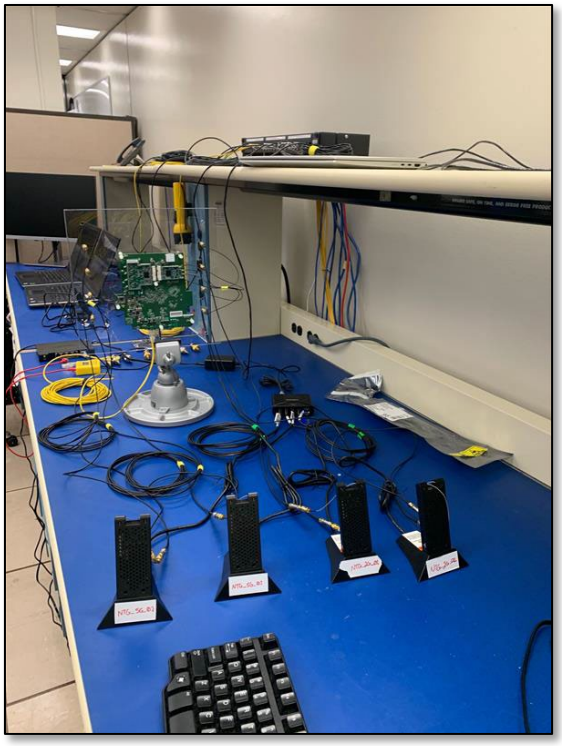

Fig. 6. Wireless Access Point Testing

Figure 7 shows initial testing of a layer 3 switch EDU. The performance for the layer 3 switch is targeting a gigabit port order of magnitude. However, this performance is dependent on many factors including memory and processing logic.

Fig. 7. Layer 3 Switch Testing

6. Network Description Build Process

Configuration for all traffic classes needs to be captured and built in a database and a tool outputs a binary file that ultimately loads into network hardware. This data provides the scheduling and slotting of frames, VLs, VLANs, and addressing needed for switches and end systems.

A network description file, a single XML file comprised of all constraints and requirements, is captured within a database Gateway Data System (GDS). The system is in place to allow specification and manipulation of network information directly from module and service providers [9].

The software tools suite is operated by the NASA Gateway avionics team. The relevant applications are Plan, Build, and Checker Tools. The Plan tool takes the network description file generated from GDS, performs the network scheduling and outputs a network configuration (XML database format) or partial schedule if scheduling fails.

The Build tool takes the network configuration and generates the network binaries. The Checker tool is not required to be run for generation of the necessary binaries but yields timing verification and analysis that is important for assessing performance and whether a schedule meets the design standards' timing requirements.

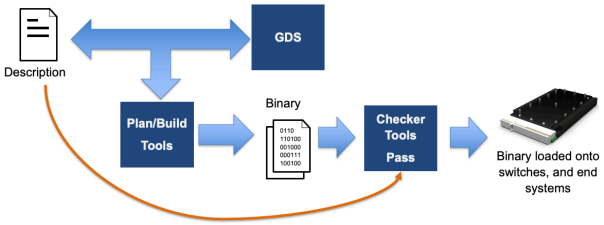

Fig. 8. Binary Generation Process

There are other tools that will be used for further analysis and testing including simulation and emulation monitoring tools. The relation between the information stored in the data model and the TTE network tools is presented pictorially in Figure 8 Binary Generation Process.

NASA owns this binary generation process, but also needs data for module network's that have VLs onto the inter-element network. Thus, the NASA team's Plan and Build applications will collect module data to input into the Gateway inter-element data model. This is shown in figure 9.

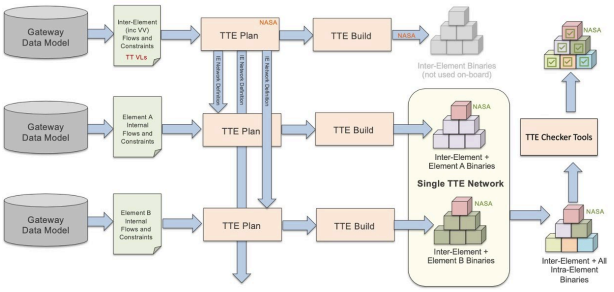

Fig. 9. Gateway Plan & Build Process with Partners

Since Gateway has a large vehicle network stack and doesn't want to reconfigure every switch and end system for every change, a function called incremental reconfiguration needs added to this tool. For example, with this function when a new module is docking and needs a virtual link scheduled the tools would only reconfigure edge switches if necessary.

7. Forward Work

For forward work, the Gateway C&DH system will finalize the design against hardware issues and bottlenecks. There are several end-to-end data flows that will go through performance testing including time distribution, translating to other legacy serial interfaces, end system memory size, and processor speed performance [10].

The software tooling functions that are unique to Gateway, for example incremental scheduling, will be going through development phases to reach the required maturity. The checker and verification tools will need certification for data flow timing verification of all critical links.

Formal verification test plans need to be written for all test labs including the modules at respective partner testbed sites and NASA's Gateway Ready Avionics Integration Lab (GRAIL). GRAIL will be comprised of flight hardware for every module provider for formal verification testing and sustaining. Other subsystem labs such as power, robotics, life support, ANVIL for C&DH and flight software development lab will initial demonstrate capability, then feed into a wholistic integrated test procedure [11].

Once forward work with hardware, and software are complete, Gateway's integration test labs will lead to improved C&DH implementation and a proper architecture to enable long-term sustainable human lunar orbit operations.

Acknowledgements

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References

[1] A. Loveless (2015). TTEthernet for Integrated Spacecraft Networks, AIAA Space and Astronautics Forum and Exposition SPACE 2015, Pasadena, CA, August 31, 2015. Retrieved from https://ntrs.nasa.gov/citations/20150002995

[2] A. Loveless (2016). Notional 1FT Voting Architecture with Time-Triggered Ethernet, AES A&S, Houston, TX, November 7, 2016. Retrieved from https://ntrs.nasa.gov/citations/20170001652

[3] C. Adamek (2019). Gateway System Requirements Document, July 10, 2019. Retrieved from https://ntrs.nasa.gov/citations/20190029153

[4] A. Loveless (2016). Overview of TTE Applications and Development at NASA/JSC, CCSDS SOIS, Rome, Italy, October 17, 2017. Retrieved from https://ntrs.nasa.gov/citations/20160012363

[5] P. Muri (2019). ISS Science Payload Command & Data Handling, ISS Research & Development Conference, Atlanta, GA, July 29, 2019. Retrieved from https://ntrs.nasa.gov/citations/20190028718

[6] P. Muri (2019). Avionics on the International Space Station: An Update, 70th International Astronautical Congress 2019, Washington, DC, October 23, 2019. Retrieved from https://iafastro.directory/iac/paper/id/49633/abstract-pdf/IAC-19,B3,4-B6.4,3,x49633.brief.pdf?2019-03-28.11:21:35

[7] A. Loveless (2017). Overview of TTE/CFS Integration, CCSDS SOIS, San Antonio, TX, May 8, 2017. Retrieved from https://ntrs.nasa.gov/citations/20170004599

[8] A. Loveless (2017). TTEthernet Development and CFS Integration, Deep Space Getaway (DSG) CFS/Open SW Multi-lateral TIM, Houston, TX, September 18, 2017. Retrieved from https://ntrs.nasa.gov/citations/20170008862

[9] D. Gwaltney (2006). Time Triggered Protocol (TTP) for Integration Modular Avionics (IMA), 2006 MAPLD International Conference, Washington, DC, August 24, 2006. Retrieved from https://ntrs.nasa.gov/citations/20070002792

[10] J. Stecklein (2019). Gateway Modeling and Simulation Plan, September 18, 2019. Retrieved from https://ntrs.nasa.gov/citations/20190032931

[11] P. Muri (2021). Gateway Avionics Concept of Operations for Command and Data Handling Architecture, IEEE Aerospace Conference February 2021. Retrieved from https://ntrs.nasa.gov/citations/20210009614