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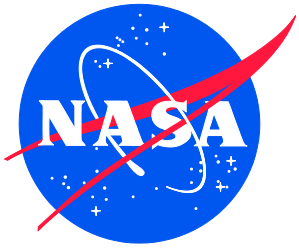

SpaceVPX Interoperability Assessment

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September 2022

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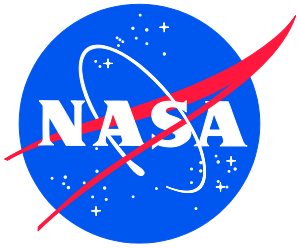

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NASA Engineering and Safety Center
Technical Assessment Report

SpaceVPX Interoperability Assessment

TI-21-01628

Dr. Robert F. Hodson, NESC Lead

Mr. Wesley A. Powell, Technical Lead

August 16, 2022

Report Approval and Revision History

NOTE: This document was approved at the August 16, 2022, NRB.

Approved: *Digital Signature on File – 9/8/22*

NESC Director

Version	Description of Revision	Office of Primary Responsibility	Effective Date
1.0	Initial Release	Dr. Robert F. Hodson, NASA Technical Fellow for Avionics, LaRC	8/16/2022
1.1	Revised wording in Sections 7.3.2 and 7.4 and deleted Figure 12.	Dr. Robert F. Hodson, NASA Technical Fellow for Avionics, LaRC	10/05/2022

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Technical Assessment Report

1.0 Notification and Authorization

As NASA exploration moves beyond low-Earth-orbit (LEO), the need for interoperable avionics systems became more important due to the cost, complexity, and the need to maintain distant systems for long periods.

The existing VMEbus (VersaModular Eurocard bus) International Trade Association (VITA)-78 industry standard, also known as SpaceVPX, addresses some of the needs of the space avionics community, but falls short of an interoperability standard that would enable reuse and common sparing on long duration missions and reduce non-recurring engineering (NRE) for missions in general.

This assessment addresses the deficiencies in the SpaceVPX standard for NASA missions enabling interoperability at the card and system level through common functionality, protocols, and physical implementations.

The key stakeholders for this assessment were:

Dr. Jeff Sheehy, Space Technology Mission Directorate (STMD) Chief Engineer
Ms. Nicole (Nicki) Rayl, Science Mission Directorate (SMD) *Former* Acting Chief Technologist

2.0 Signatures

Submitted by:

Dr. Robert F. Hodson Date

Significant Contributors:

Mr. Wesley A. Powell Date

Mr. Patrick Collier Date

Mr. Austin H. Lanham Date

Mr. Dan I. Nakamura Date

Ms. Hester J. Yim Date

Mr. Alessandro D. Geist Date

Signatories declare the findings, observations, and NESC recommendations compiled in the report are factually based from data extracted from program/project documents, contractor reports, and open literature, and/or generated from independently conducted tests, analyses, and inspections.

3.0 Team Members

The assessment team was comprised of subject matter experts (SMEs) from Goddard Space Flight Center (GSFC), the Jet Propulsion Laboratory (JPL), Johnson Space Center (JSC), and Langley Research Center (LaRC). The team included valuable external consulting support from a SME who was a key participant in the development of the original VITA-78 standard.

Name	Discipline	Organization
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Erin Moran	Technical Editor	LaRC/AMA

3.1 Acknowledgements

The STMD High Performance Spaceflight Computing (HPSC) project team provided invaluable guidance during this assessment, specifically regarding industry trends in interconnect technology. Additionally, Steve Gentz from MSFC, Mary Beth Wusk from LaRC, Tim Barth from KSC, Larry Dungan from JSC, and David Petrick from GSFC provided support to this assessment as peer reviewers.

4.0 Executive Summary

The existing VMEbus (VersaModular Eurocard bus) International Trade Association (VITA)-78 industry standard, also known as SpaceVPX, is an avionics board- and chassis-level standard derived from the OpenVPX standard as defined in VITA-65. While VITA-65 defines backplane and board-level profiles from COTS vendors to ensure interoperability of products used in developing systems and subsystems, the VITA-78 standard defines SpaceVPX to incorporate fault tolerance features that are required by many spaceflight systems. However, VITA-78 allows so much flexibility that interoperability between modules cannot be assured. This assessment provides guidelines on the use of, and extensions to, the VITA-78 standard to enable avionics interoperability for future NASA missions.

The assessment team was comprised of subject matter experts (SMEs) from Goddard Space Flight Center (GSFC), the Jet Propulsion Laboratory (JPL), Johnson Space Center (JSC), and Langley Research Center (LaRC). The team included valuable external consulting support from a SME who was a key participant in the development of the VITA-78 standard. The team had extensive collaboration with the NASA Space Technology Mission Directorate (STMD) High Performance Spaceflight Computing (HPSC) project, specifically in the development of SpaceVPX interconnect findings, observations, and NESC recommendations.

To provide an understanding of the breadth of implementations that SpaceVPX must accommodate, multiple NASA use cases were analyzed to assess the requirements for SpaceVPX implementations across a wide range of NASA missions (Appendix C). Applications included crewed missions, science missions, and orbital and surface robotic systems. Product surveys were conducted to assess the level of industry support for SpaceVPX, applications, and the variations in their implementations (Appendix D).

In-depth analysis was conducted in the areas of: (a) power management and distribution, (b) form factors and daughtercards, (c) interconnect, and (d) fault tolerance. Leveraging the use cases, product surveys, and SMEs from multiple NASA Centers, these areas were analyzed to determine the range of implementations permitted by the VITA-78 standard and potential interoperability issues. Applicable findings and NESC recommendations were provided for each area.

During this assessment, there were multiple opportunities to engage with other agencies to learn about their interest in SpaceVPX, their strategies for implementing SpaceVPX-based systems, and their internal development efforts. These engagements also generated findings and NESC recommendations.

Based on this assessment analysis, NESC recommendations were made regarding the feature set and module profiles to support NASA SpaceVPX implementations. This feature set includes restrictions on features in VITA-78, and extensions to the standard. Key recommendations in this area include the use of 10 Gigabit Ethernet and Peripheral Component Interconnect Express (PCIe) as high bandwidth interconnect on the backplane, the retention of SpaceWire interconnect for control functions, and support for 3U (unit) and 6U, form factors for NASA systems. Restrictions were proposed on the usage of user-defined signals to promote interoperability, and specific power managements and distribution schemes for 3U systems. Beyond the technical implementation of SpaceVPX, recommendations were made on areas that warrant further investigation. Primary among these is the recommendation for NASA to collaborate with other space-going agencies and industry to incorporate recommendations into a future ‘dot spec’ of

VITA-78. This would ensure wide adoption and availability of the modules that comply with the specification. The assessment includes appendices with candidate module profiles that can be considered as a starting point for this activity, and example systems based on the recommendations.

Follow-on studies are recommended for architectures beyond SpaceVPX to address potential enhancements including condensed set of interconnect, software required to implement protocol layers on the interconnect (and other features), alternative power architectures, and system-level testability.

5.0 Assessment Plan

The scope of this assessment was to define subsets and extensions to the SpaceVPX standard to ensure maximum interoperability of SpaceVPX-based avionics within NASA missions. The effort was divided into the following tasks:

1. Notional avionics use cases were defined for crewed and robotic NASA mission applications. Note that use cases addressed only spacecraft and landed systems. Launch vehicles were not addressed. Spanning the range of processing performance, input/output (I/O) bandwidth, size, weight and power (SWaP) sensitivity, and mission criticality needs, these 12 use cases provided an understanding of the SWaP of implementations that SpaceVPX must accommodate and the features, capabilities, and interfaces that are needed to implement a broad range of NASA avionics systems. A standard template and associated spreadsheet was developed that captures the salient aspects of the 12 use cases that are relevant to SpaceVPX.
2. Product surveys were conducted with industry to gain an understanding of the range of SpaceVPX modules that are available and the features, capabilities, and interfaces that they provide. In some cases, these surveys provided insight into how industry is implementing SpaceVPX systems consisting of several modules. A product survey template was developed and distributed to vendors of SpaceVPX systems. In several cases, follow up conversations were held with vendors to provide clarification on the responses provided in their completed surveys. Lastly, a spreadsheet was prepared to compare vendor responses.
3. Study Focus Area (SFA) teams were formed to analyze key aspects of SpaceVPX. These teams focused on: (a) interconnect, (b) power management and distribution, (c) form factor and daughtercards, and (d) fault tolerance. Based on the use cases, product surveys, SMEs, and other data, each SFA team provided preliminary findings, observations and recommendations relevant to their respective areas. It should be noted that the interconnect SFA was informed by a concurrent effort by the NASA STMD HPSC project to engage industry in the development of HPSC Concept Study Reports (CSRs).
4. External NASA organizations were engaged on their use and plans for SpaceVPX. To facilitate this, industry and other agency engagement was solicited at the 2021 IEEE Space Computing Conference and the 2021 Radiation Hardened Electronics Technology (RHET) Conference. The assessment team has engaged with Air Force Research Laboratory (AFRL) and other agencies to learn their plans for SpaceVPX. Lastly, a participant in this assessment has a key role within the Sensor Open Systems Architecture (SOSA™) Consortium, which is a standards organization that focuses on interoperable sensor systems with the Department of Defense (DoD). This interaction provided insight into their direction on SpaceVPX, and awareness within the SOSA™ Consortium of this assessment.
5. Based on the analysis and NESC recommendations of this assessment, candidate modules were identified and mapped to existing VITA-78 module profiles. These profiles are intended to serve as a starting point for module profile definition in follow on activities to capture the recommendations in a ‘dot spec’ to VITA-78. Example systems were defined

to illustrate the range of SpaceVPX systems that can be implemented based on the NESC recommendations.

It should be noted that flight software implications of the NESC recommendations were not considered within the scope of this assessment. It was assumed that operating system board support packages can be developed to support the identified interconnect, and that flight software modules can be developed to implement the required SpaceVPX control functions.

6.0 Problem Description and Background

6.1 Introduction to SpaceVPX

Historically, the space market has been a place where size, weight, power, and cost (SWaP-C) are key points to minimize wherever and whenever possible. Legacy space systems are often point solutions designed for its intended application. There is little to no consideration for hardware or software reuse. These legacy systems may not have the full range of redundancy options (e.g., dual-string or M-of-N reliability capabilities) as part of the overall architecture given an application system's operational requirements. The internal interfaces are often proprietary and application specific. Finally, the modules, which are defined for the purpose of this assessment as base unit slot profiles compiled to form box level systems are not designed to interoperate at either the hardware or software levels.

The forthcoming describes SpaceVPX effort and, briefly, its parent, the Next Generation Space Interconnect Standard (NGSIS). NGSIS, government-industry collaboration effort, defined a set of standards for interconnects between space system components with the goal of cost effectively removing bandwidth as a constraint for future space systems. Initial emphasis was on standardization of internal connectivity at the electronic chassis level. This included the needs for high reliability, but limited rate data needs typical for spacecraft command and data handling (C&DH) and high-rate data needs expected for next generation, high performance sensors and instruments.

The architectural approach selected several appropriate and established industry standards, such as: Ethernet, RapidIO, PCIe, and Fibre Channel as 'points of departure' and then developed a set of extensions to these standards to address space industry specific needs. The intent of this approach was to reduce cost, risk, and effort by using proven technologies, while providing a set of common extensions that can be adopted across the space industry to enable interoperability of board level components from different sources and vendors.

NGSIS selected the VITA OpenVPX standard family for the physical baseline. VPX supports 3U and 6U Plug-In Card (PIC) form factors with ruggedized and conduction cooled features suitable for use in extreme environments for chassis and their internal boards.

It is evident that this type of Modular Open System Approach (MOSA) solution is at the chassis or box level. In addition, it is apparent that the modularity carries across physical chassis boundaries in a manner befitting a distributed modular architecture. A synopsis of this effort is shown in Figure 1, where board and chassis level functions (described subsequently) are flexible building blocks for system design from bottom left moving counter clockwise are SpaceVPX Slot Profiles, which are the fundamental hardware building blocks used to build interconnected systems through a backplane (shown to the right of the SpaceVPX Slot Profiles). Moving from lower right to upper left, with these backplanes and the interconnected SpaceVPX Slot Profiles

in mind, it is understood different configurations of modules as functions for different applications for a platform. Fundamentally, the benefit lays with the SpaceVPX Slot Profiles, which are the same set of profiles that are useful for different configurations and applications. The natural consequence of this thread is at the upper right of Figure 1, the platform. So, going back to the beginning, the level of modularity is at the lower left, which is the SpaceVPX Slot Profile building blocks.

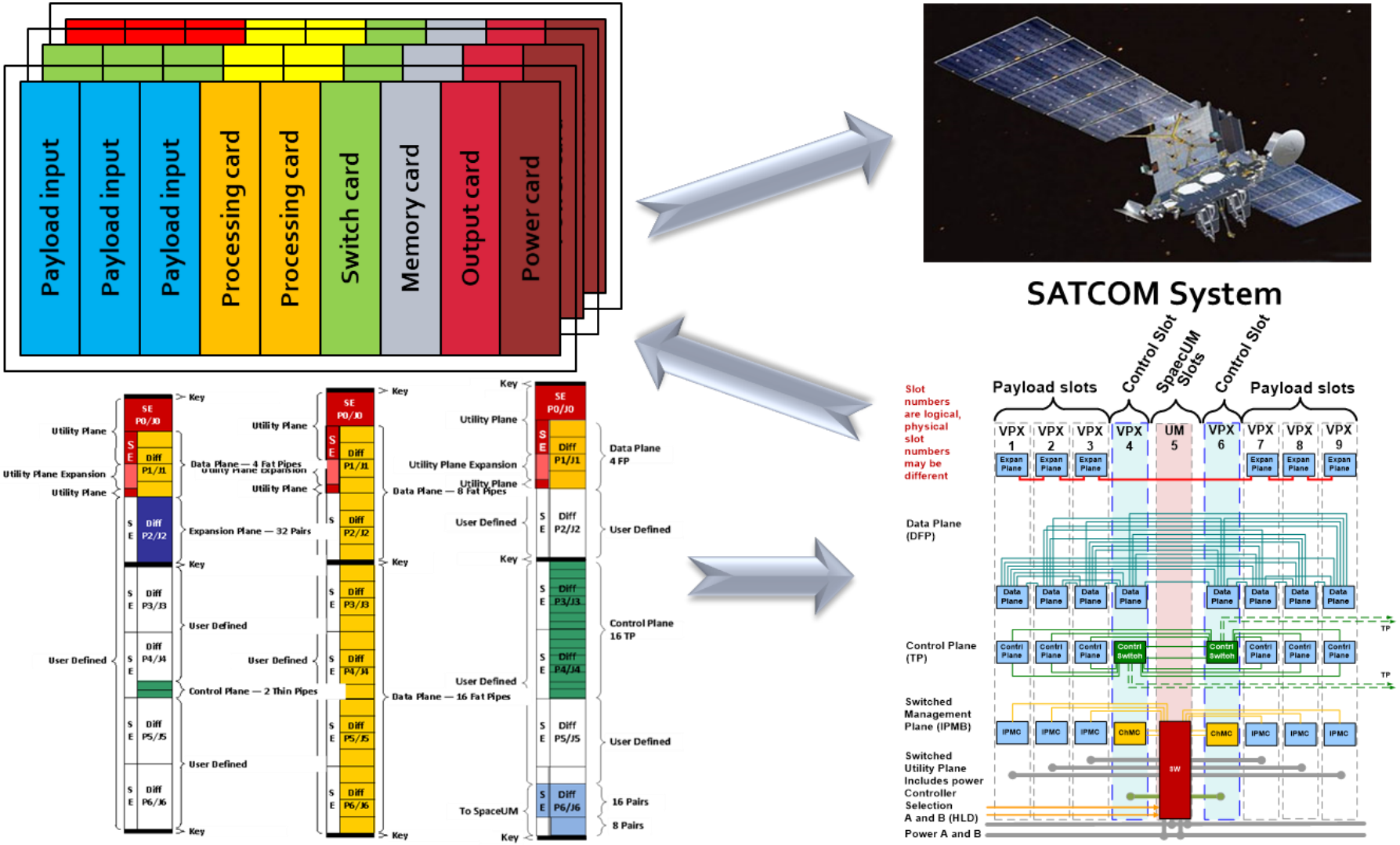


Figure 1. Modular Building Blocks for VITA-78 (SpaceVPX)

6.2 VITA-78 (SpaceVPX)

SpaceVPX builds on several standards that are part of the American National Standards Institute (ANSI)/VITA OpenVPX family. Essentially, it was created to bridge the existing VPX standards to the space market. The initial SpaceVPX working group selected existing VITA standards to incorporate into VITA-78. These include the base VITA-46 VPX standard and its ANSI/VITA-65 OpenVPX derivative. SpaceVPX allows other compatible connectors to be used, including ANSI/VITA-60 and 63. ANSI/VITA-48.2 [3] forms the base of the mechanical extensions in SpaceVPX. ANSI/VITA-62 defines a standardized power module. ANSI/VITA-66 and 67 may be applied to replace electrical connector segments with radio frequency (RF) or optical. ANSI/VITA-46.11 [4], in trial usage, provides a base of the management protocol that SpaceVPX builds on for system fault tolerant management. These aspects are illustrated in Figure 2, and Table 1 and provides a detailed description of the VITA standards that are relevant to VITA-78.

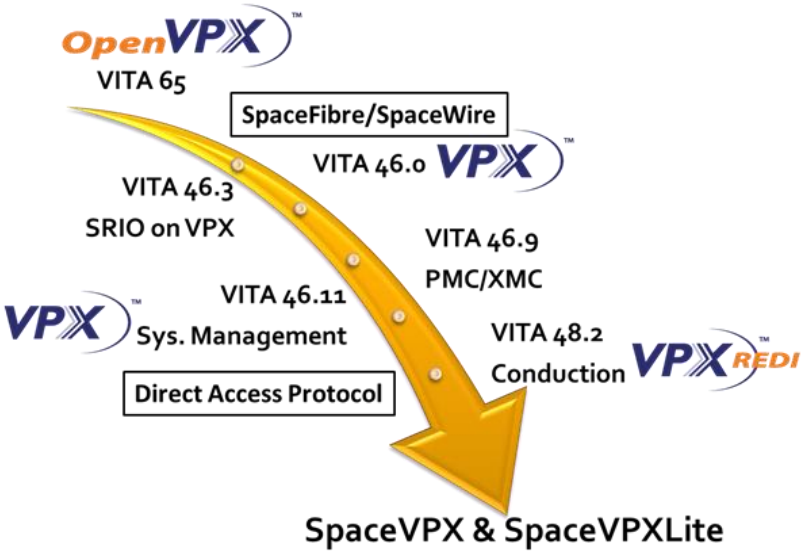


Figure 2. What is in SpaceVPX?

Table 1. Relevant VITA Standards

VITA Standard	Alternate Name	
VITA-65.0	OpenVPX	Baseline standard to VITA-78. The OpenVPX System Standard was created to bring versatile system architectural solutions to the VPX market. Based on the extremely flexible VPX family of standards, the OpenVPX standard uses module mechanical, connectors, thermal, communications protocols, utility, and power definitions provided by specific VPX standards and describes a series of standard profiles that define slots, backplanes, modules, and Standard Development Chassis.
VITA-46.0	VPX Baseline Standard	Predecessor to VITA-65.0. Baseline to VITA-78.0. This standard describes VITA-46.0 VPX Baseline Standard, which is an evolutionary step forward for the provision of high-speed interconnects in harsh mil-aero environment applications.
VITA-46.11	System Management on VPX	System Management schema offered in VITA-78.0 for modules. This document defines a framework for System Management in VPX systems. It enables interoperability within the VPX ecosystem at the Field Replaceable Unit (FRU), chassis and system levels. The framework is based on the Intelligent Platform Management Interface (IPMI) specification and leverages concepts and definitions from the AdvancedTCA® (ATCA®) specification by PICMG®.
VITA-62.0	Modular Power Supply Standard	PSC baseline standard for VITA-78.0 and VITA-65.0. This standard provides requirements for building a power supply module for use with a VPX chassis. The module will fit within the standard envelope defined for VPX modules in the VITA-48.0 standards.
VITA-48.2	Mechanical Standard for VPX REDI Conduction Cooling	Conduction Cooled standard used by VITA-78.0 and VITA-65.0. This standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules or Modules, and defines the features required to achieve Two Level Maintenance compatibility.
VITA-60.0	Alternative Connector for VPX	Alternate VITA standard connector. One of the options for VITA-78.0 and VITA-65.0. VITA-63.0 describes an open standard for Hyperboloid Alternative Connector for VPX, and provides an alternative connector to that specified in the VITA-46.0. The VITA-46.0 and VITA-63.0 connectors are not intermateable, which precludes

VITA Standard	Alternate Name	
		their use in noncompatible backplanes. However, the VITA-63.0 draft standard provides VPX users with the flexibility to choose a VPX module and backplane connector combination for their specific application requirements.
VITA-63.0	Hyperboloid Alternative Connector for VPX	VITA-63.0 provides an alternative connector to the one specified in VITA-46.0, VPX Baseline Standard.
VITA-66.0	Optical Interconnect on VPX – Base Standard	Fiber topic connector standard used in VITA-78.0. This standard defines a family of blind mate Fiber Optic interconnects for use with VPX backplanes and modules.
VITA-67.0	Coaxial Interconnect on VPX – Base Standard	Analog coaxial blind mate standard used by VITA-78.0. This standard establishes a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and modules, and to define a specific family of interconnects and configurations within that structure.

To ease the transition from bussed protocols, OpenVPX created 'bridge' profiles to enable legacy VME modules to interface with OpenVPX modules. Likewise, SpaceVPX includes bridge profiles to enable CompactPCI (cPCI) modules to interface with SpaceVPX modules. Bridge profiles enable code reuse from legacy systems targeting PCI for new SpaceVPX systems.

Four major interconnect planes organize the connections in OpenVPX. The data plane provides high-speed multi-gigabit fabric connections between modules that typically carries payload and mission data. The control plane fabric typically has less capacity and is used for configuration, setup, diagnostics, and other operational control functions within the payload has lower speed data transfers. The utility plane's function is providing setup and control of the basic modules functions that typically concern power sequencing and low-level diagnostics, and the power, clocks and other base signals needed for system operation. The expansion plane may be used as a separate connection between modules utilizing similar or bridging heritage interfaces in a more limited topology (e.g., bus or ring). Pins not defined as part of any of these planes are typically user-defined and are available for pass through from daughter or mezzanine cards, or to rear transition modules (RTM). For maximum plug-in module reuse, user-defined pins are configured to not interfere with other modules that use these pins in a different way. ANSI/VITA-65.0 provides more detail on these structures.

Figure 3 illustrates a notional redundant SpaceVPX system using a switched topology for data plane interconnect. Note that although not illustrated in this figure, SpaceVPX supports a mesh topology.

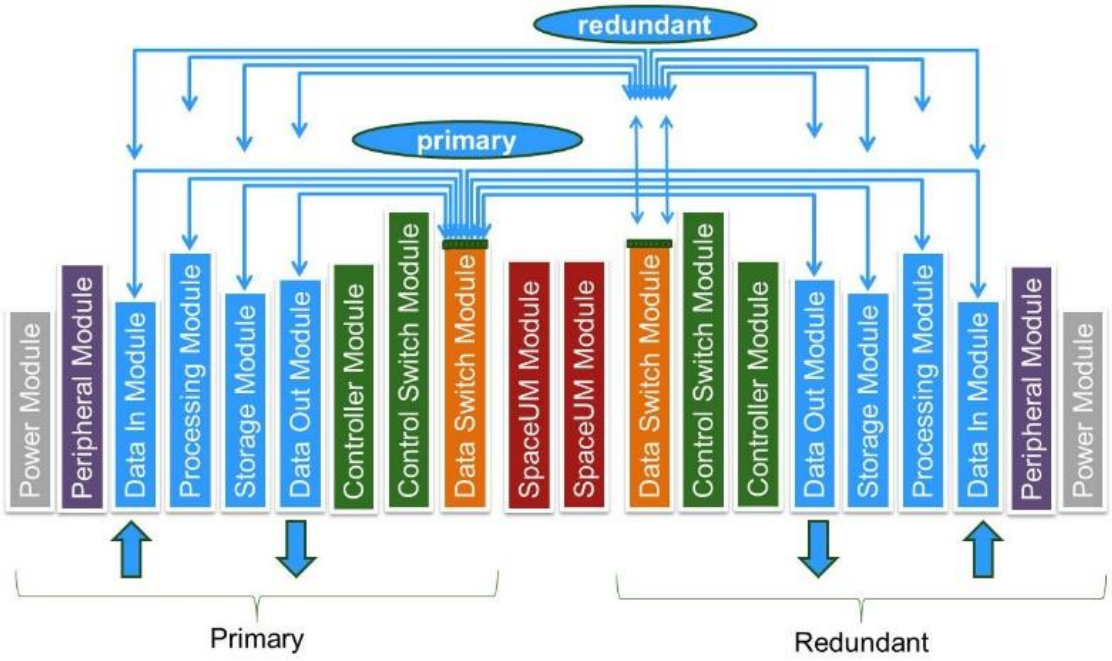


Figure 3. SpaceVPX Switched Topology Use Case

Major Changes in SpaceVPX

In evaluating the use of OpenVPX for potential space usage, several shortcomings were observed. The biggest deficiency was the lack of features that could support a full single fault tolerant and highly reliable configuration. Utility signals were bussed and, in most cases, only supported one set of signals, via signal pins to a module. Therefore, a pure OpenVPX system has opportunities for multiple failures. A full management control mechanism was not fully defined with VITA-46.11.

As the typical OpenVPX control planes are PCI Express or Ethernet, this was a concern since their usage in space applications was minimal, at the time, and SpaceWire was the dominant medium speed data and control plane interface for most spacecraft. This has evolved since the inception of SpaceVPX and the use of Ethernet and PCIe in space applications has grown. The SpaceVPX Working Group is reviewing a 2022 content proposal for the inclusion of high-rate Ethernet.

Lastly, a third area was the desire to reuse the infrastructure of OpenVPX for prototyping and SpaceVPX ground testing.

Other major changes to SpaceVPX include the absorption of SpaceVPXLite (i.e., VITA-78.1), the inclusion of SpaceFibre as part of the DRAFT revision, and an update to the 3U Space Utility Management (SpaceUM) to accommodate more Payload Modules (also known as PICs). SpaceVPXLite was a 3U SWaP constrained companion standard to SpaceVPX.

Fault Tolerance

The goal of SpaceVPX is to achieve an acceptable level of fault tolerance, while maintaining a reasonable level of compatibility with existing OpenVPX components, which includes connector pin assignments for the board and the backplane. (Note: Fault containment regions within SpaceVPX is defined at the plug-in module level.) For the purposes of fault tolerance, a plug-in

module, defined as a printed wire assembly which conforms to defined mechanical and electrical specifications is considered the minimum redundancy element. The utility plane and control plane within SpaceVPX are distributed redundantly and in star topologies to provide system fault tolerance. An example of this fault tolerance via cross-strapping is shown in Figure 4.

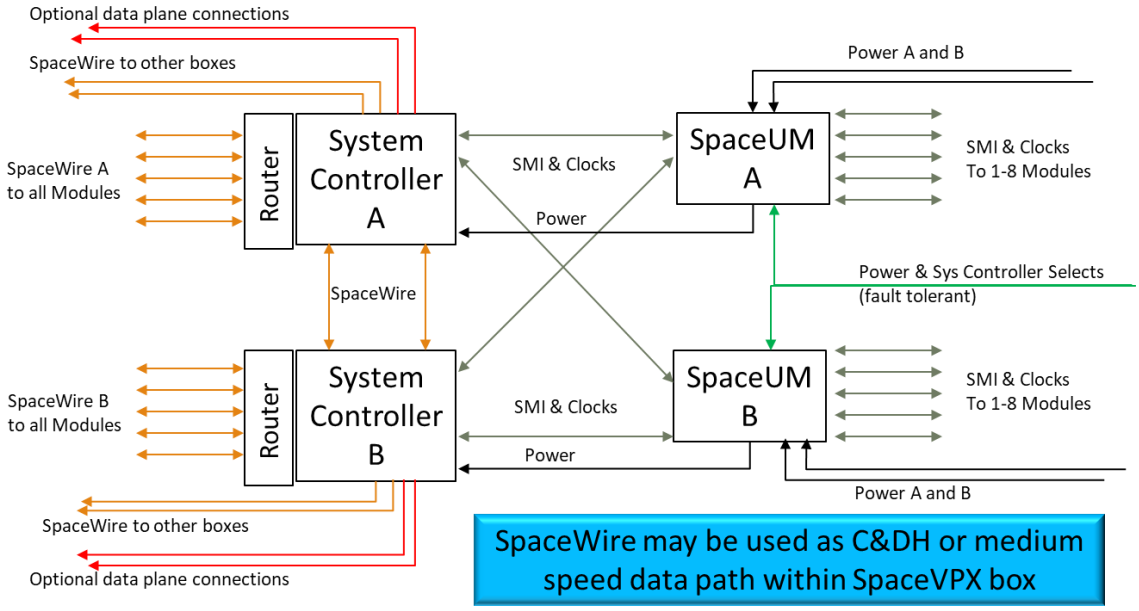


Figure 4. SpaceVPX Fault Tolerance Example through Cross-strapping

To provide the required level fault tolerance, the utility plane signals needed to be dual-redundant and switched to each SpaceVPX card. A trade study was performed to compare between various implementations including adding the switching to each card in various ways and creating a unique switching card. The latter approach was chosen so that SpaceVPX cards could each receive the same utility plane signals that an OpenVPX card receives with minor adjustments for any changes in topology. This became known as the SpaceUM module and is a major contribution of the standard.

The SpaceUM module contains up to eight sets of power and signal switches to support SpaceVPX modules. An example of this from an Utility Management perspective is shown in Figure 5. It receives one power bus from each of two power supplies, and one set of utility plane signals from each of two System Controller functions required in the SpaceVPX backplane. The various parts of the SpaceUM module are considered extensions of the Power Supply, System Controller, and other SpaceVPX modules for reliability calculation, and thus do not require their own redundancy. Two Management protocol options are provided for control of the system over the utility plane's system management interface: one is a subset of the IPMI Controller (IPMC) defined in VITA-46.11, and the other is a simpler direct access protocol developed specifically for SpaceVPX. Both use the utility plane for access to the managed modules.

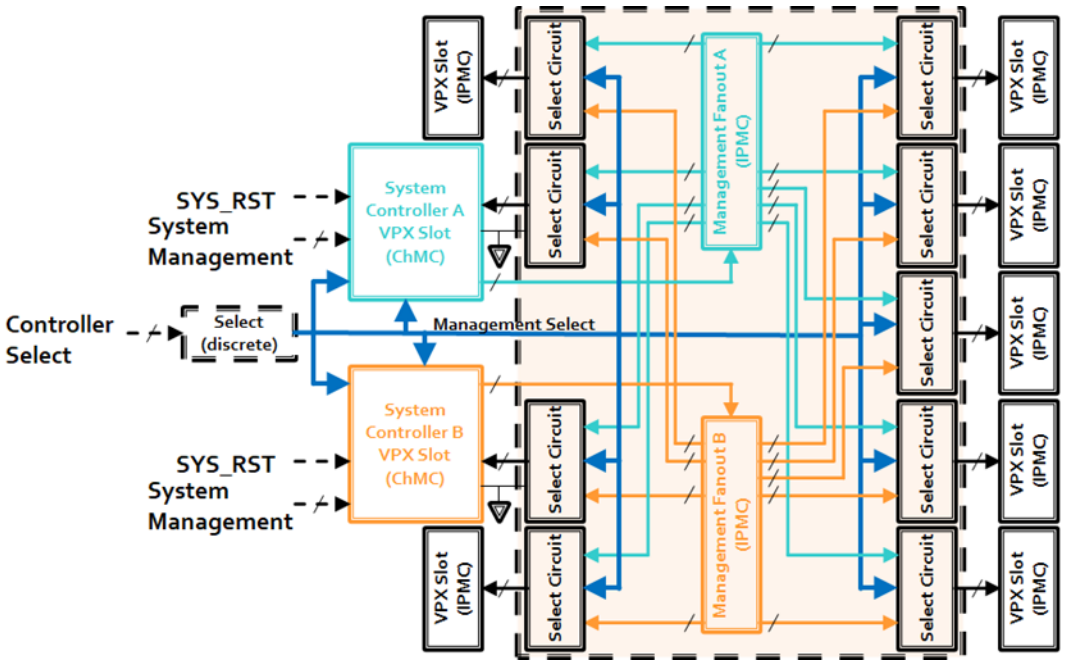


Figure 5. SpaceUM (in dashed box) Distribution of Utility Management Signals to SpaceVPX Payload Modules

Profiles

Since each slot, module, and backplane profile in OpenVPX is defined and interlinked, the changes made require a SpaceVPX version of each of these profiles to be specified. Specifically, the slot profiles provide a physical mapping of data ports onto the slot's backplane connector, which is agnostic to the type of protocol used to convey data from the slot to the backplane. The backplane profile is a physical mapping of the backplane data transfer capabilities. It is slot dependent and specifically defines a topology for channel number and buses for data interconnect. The module profiles are extensions of their accompanying slot profiles that allow for a mapping of protocols to each module port. Each module profile includes information on thermal, power, and mechanical requirements. Many are close to OpenVPX and should enable use of OpenVPX modules and backplanes for prototyping or testing, but are sufficiently different to require full specification. The section of the SpaceVPX standard that defines profiles was a significant effort and forms a majority of the completed standard given the level of modularity for the standard is the slot profile, the module profile, and the PIC.

Since cPCI has been the backplane interface of choice for many spacecraft in the past decade, special slot definitions were created for bridging SpaceVPX modules to heritage cPCI modules. The expansion plane may be used to bridge from a payload or controller module to other modules with cPCI or to a heritage cPCI module.

A slot profile for a controller for Switch topology is shown in Figure 6. P0/J0 through P6/J6 represents the segments on the SpaceVPX connector. Each segment has 8 or 16 wafers that each connects to 9 backplane pins. The only part of the connector dedicated to a specific function on the Slot Profile is P0/J0, where it is used for Utility signal (e.g., voltage and system management). The other parts of the connector (i.e., P1/J1 – P6/J6 for 6U, and P1/J1 – P2/J2 for 3U), depending on the construction of the profile, are Data Plane, Control Plane, Expansion

Plane, or the SpaceUM. Figure 6 shows how the various connections are mapped to the slot. The standard defines each pin to ensure interoperability between modules.

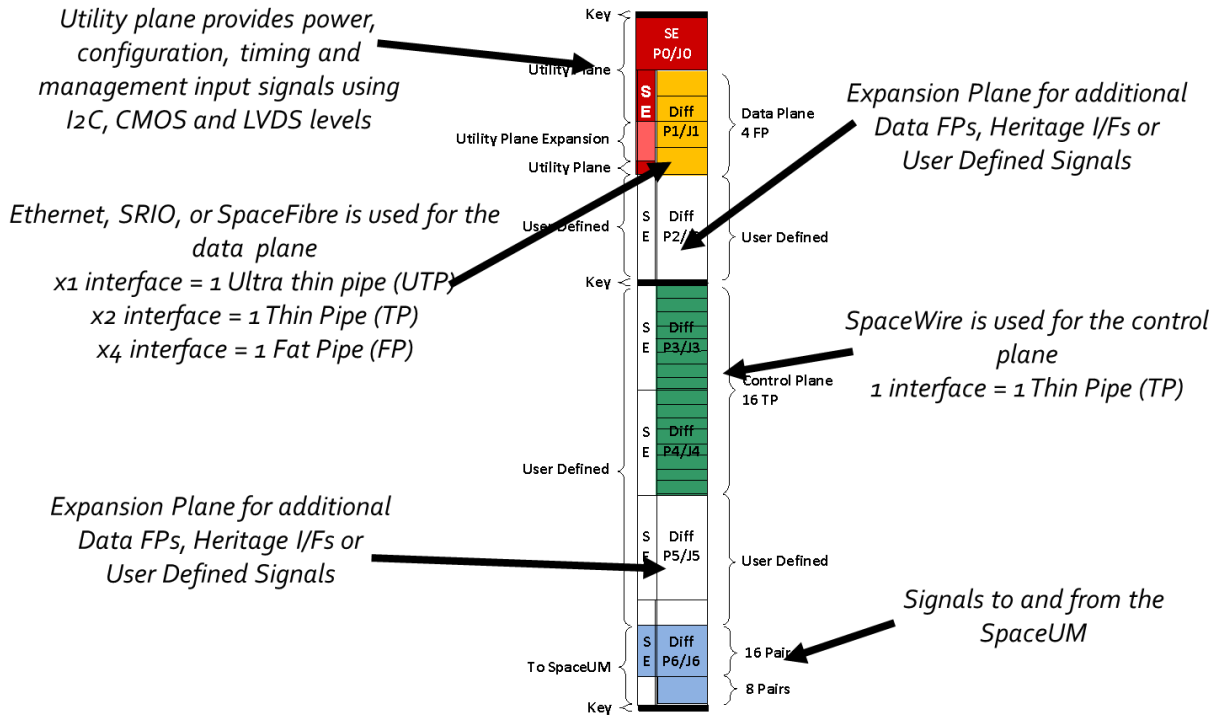


Figure 6. Example Slot Profile with Connection Notations

Mechanical

SpaceVPX builds on the OpenVPX infrastructure, but expands it for space modules, which are typically larger than commercial modules. 3U and 6U modules are defined as in OpenVPX. However, SpaceVPX defines 220mm, 280mm, and 340mm heights in addition to 160mm. Card pitches of 0.8 and 1.0 inches are kept from OpenVPX, and pitches of 1.2, 1.4, and 1.6 inches are added. To centralize dimension requirements, SpaceVPX includes dimensions on mechanical drawings within the standard. Modules are defined that use levers or extraction tools for removal from backplanes and chassis. Given the mechanical differences between VITA-78 and VITA-65.0 for 3U and 6U, it is not possible to take a VITA-65.0 PIC and set it in a VITA-78 slot. This is due to width differences between the chassis slots for VITA-78 and VITA-65.0. In the most recent version of VITA-78, the chassis slot width for 3U was changed to the same number as in VITA-65.0. However, differences in wedge lock dimensions prevent placing VITA-65.0 modules in VITA-78 chassis slots.

Interoperability with OpenVPX

Keeping interoperability with OpenVPX has been a driver in how SpaceVPX has evolved. Defining needed changes to signals so they operate with an OpenVPX board was a challenge in defining and refining the standard. Initial review of existing commercial OpenVPX boards show it should be possible to mix OpenVPX boards with SpaceVPX board profiles. It is expected this will be one of the first areas proven as SpaceVPX modules begin to be developed. The intent was to produce a specification, and a standard that allows for the use of OpenVPX boards for development work until such a time that all issues and concerns of function and capability are

addressed. With the addition of several SpaceVPX slot and module profiles that mimic OpenVPX slots and modules, it allows for an easier transition to those latter board types when migrating to an operational system.

6.3 SpaceVPXLite Introduction

SpaceVPXLite (VITA-78.1) is a companion 'dot spec' to the SpaceVPX base standard. Where SpaceVPX original focus was on larger systems that utilize 6U Eurocard modules with longer mission lifetimes and fewer constraints on power and volume. The SpaceVPXLite's focus was on small systems (i.e., "Lite"). The SpaceVPXLite notional architecture is depicted in Figure 7.

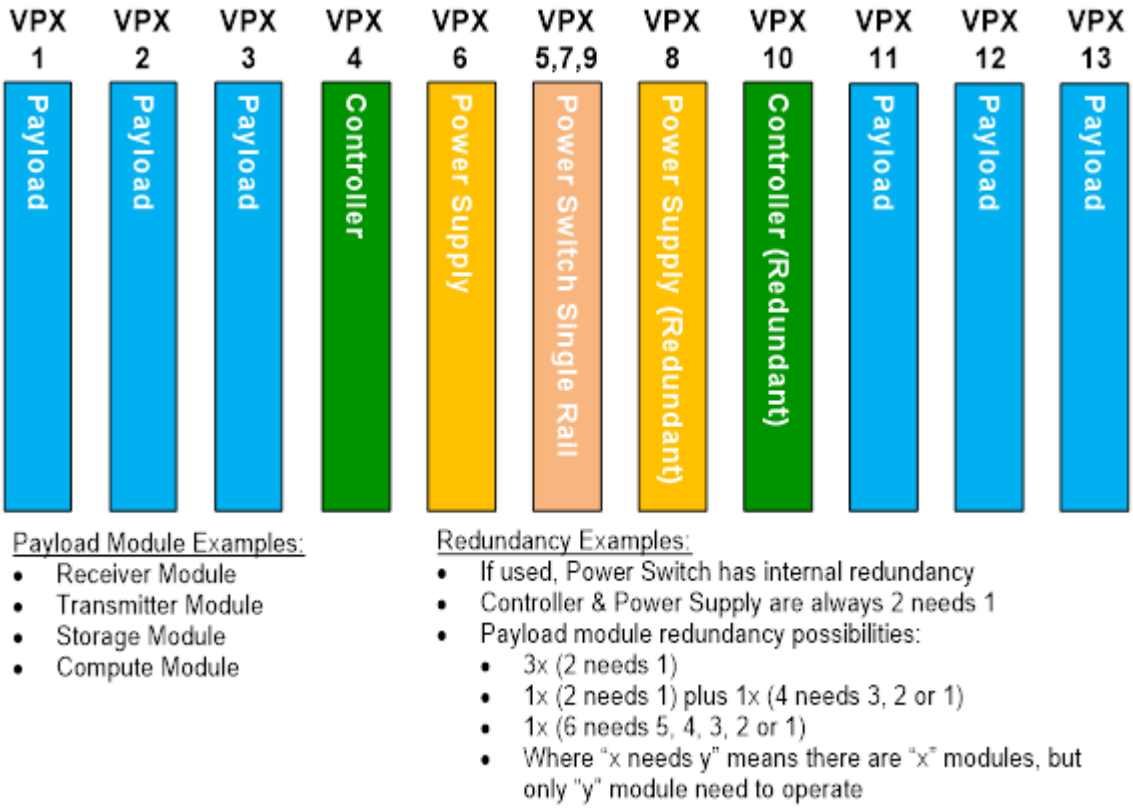


Figure 7. SpaceVPXLite Architecture

This 'dot spec' defines this type of lightweight implementation with significant advantages in SWaP-C for 3U module systems. SpaceVPXLite is 'lightweight' with respect to the reduced scope of Module and System requirements compared to the SpaceVPX base standard that results in a smaller SWaP-C footprint for deployment.

Historically, systems developers target 3U modules when confronted with driving SWaP-C constraints. However, the SpaceVPX base standard implementation for 3U results in a larger ratio of support to payload modules than for a 6U implementation. This is realized using the SpaceUM Module in a 3U system. The original incarnation of the 3U SpaceUM Module could accommodate 2 Payload Modules compared to 8 Payload Modules for the 6U SpaceUM Module.

This 'dot spec' enables a reduced support to payload module ratio by removing base standard features while retaining critical requirements necessary to deploy a single-point failure tolerant system.

SpaceVPXLite differs from SpaceVPX in several areas. SpaceVPXLite eliminates the SpaceUM module and migrates the power switching function to a new Power Supply-Switch module. There is an option for operating a SpaceVPXLite system without a Power Switch. Several of the control signals that normally are sourced to modules from the SpaceUM are redefined and are sources directly from the system controller.

The SpaceVPXLite dot standard is in DRAFT form. Main reasons for the delay in progression are available personnel and funding. The document is ready for working group review and ballot. If there is sufficient interest to revive SpaceVPXLite, then it is reasonable to assume an editor driving the development is necessary.

Given the status of SpaceVPXLite, at the time, the SpaceVPX working group agreed to incorporate targeted parts of the 'dot spec' into the base standard. The most important topics transferred from SpaceVPXLite to SpaceVPX base standard were the Power Supply-Switch Slot Profile from Section 14.8.2 and the Utility Switch Slot Profile from Section 14.9.2.

Use of SpaceVPX within NASA

Within NASA, SpaceVPX is in the early stages of adoption. The first spaceflight application of a SpaceVPX module will be on the Earth Surface Mineral Dust Source Investigation (EMIT), which is an Earth Ventures-Instrument (EVI)-4 Mission to map the mineral composition of arid dust source regions via imaging spectroscopy in the visible and short-wave infrared. EMIT was developed at JPL and launched in 2022. The instrument will observe Earth from outside the International Space Station (ISS). EMIT uses a 3U SpaceVPX solid state drive module, but it is integrated into a non-SpaceVPX avionics architecture.

The SpaceCube-V3 is a high performance processor in development at GSFC as a 3U SpaceVPX module. Central to this module is a high density Field Programmable Gate Array (FPGA) with embedded processors. This module is intended to provide onboard processing for instrument data systems, with a maximum processing bandwidth in excess of 5 giga-operations per second (GOPS).

While the identified NASA SpaceVPX uses entail the use or development of a single SpaceVPX module, the Safe and Precise Landing – Integrated Capabilities Evolution (SPLICE) Descent and Landing Computer (DLC) is implementing a full 3U SpaceVPX chassis. The DLC includes internally developed and industry provided modules, and includes the internal development of a SpaceUM module that is key to the SpaceVPX architecture.

Beyond these examples, SpaceVPX may be adopted in industry developed exploration systems.

7.0 Analysis

7.1 Use Case Activity and Results

7.1.1 Use Case Analysis

The SpaceVPX interoperability study began with an assessment of notional use cases (listed in Table 2). Note that the use cases studied do not necessarily represent active NASA projects. However, the use cases provide an understanding of the breadth of implementations that SpaceVPX must accommodate and the features, capabilities, and interfaces that are needed to implement a broad range of NASA avionics systems. Note that as these use cases were defined early in the assessment, they served as a starting point for this assessment. Hence, the notional

block diagrams provided in the use cases often will not reflect the NESC recommendations. Several use cases depart from the VITA-78 standard in their recommended power distribution schemes due to SWaP considerations. These nonetheless provided the impetus to analyze power distribution options supported by VITA-78, and desired features of future systems that could leverage SpaceVPX or future variants of the standard.

Table 2. NASA Use Cases

Use Case	Brief Description
Crewed Mission Avionics (*)	Implementation of Vehicle Control Unit (VCU) and Time Triggered Ethernet (TTE) switch
Crewed Mission Robotics and Surface Vehicle (*)	Implementation of 'Robonaut type' avionics and lunar rover avionics
SmallSat	Combined C&DH and instrument processing in single chassis for an Evolved Secondary Payload Adapter (ESPA)-class mission
On-orbit Servicing, Assembly, and Manufacturing (OSAM)	Implementation of avionics for onboard servicing, assembly, and manufacturing robotics
Science Rover	Robotic science rover avionics
Precision Landing Processor	Implementation of the SPLICE DLC
High Data Rate Missions (3)	High bandwidth Synthetic Aperture Radar (SAR)
	Spectroscopy (based on EMIT mission concept)
	Advanced Earth observing hyperspectral instrument
Low/Medium Data Rate Mission	Generic telescope mission concept with moderate data rates (less than 0.5 Gbps)
Communication Relay Spacecraft	Orbital optical communication relay payload based on Laser Communication Relay Demonstration (LCRD)
HPSC A-Team Use Cases	A hybrid of autonomous planetary mission use cases derived from a JPL HPSC A-Team study

(*) Comprised of multiple subordinate uses cases.

Use Case Criteria

Each use case addressed several criteria as listed below. A spreadsheet is provided in Appendix D, to allow comparison of each criteria across use cases.

Orbit or Destination

This topic fell into two broad categories, near-Earth orbit or deep space. Within the near-Earth orbit use cases, the specific type of orbit varied from low-Earth-orbit (LEO), geosynchronous orbit (GEO), and Cis-Lunar to Lagrange points (L1 and L2). For deep space, use case destinations were generally 'deep space' or specific to a planetary body (e.g., Mars, Saturn, or Titan). Each use case destination or orbit carries requirements specific to the case and its operational environment. Some of these requirements (e.g., radiation) are not directly applicable to this assessment. Others, including the degree of onboard processing required and fault tolerance do influence this assessment.

Mission Criticality

This topic concerns the classification and definition of mission profiles. Per NASA, these fall into four categories: Class A, Class B, Class C, and Class D. From the total number of use

cases, 2 were Class A, 3 were Class B, 3 were Class C, 1 was Class D, and 3 had potential applications in multiple mission classes.

SWaP Sensitivity

The majority of use cases were sensitive to SWaP with communication relay as the only exception. However, it should be noted that communication relays implemented in constellations of SmallSats would be SWaP sensitive.

Therefore, low SWaP was identified as a need for most use cases. Looking across the use cases, there is an apparent need to support 3U and 6U form factors, although the majority of use cases specified 3U. The number of boards specified for each use case ranged from 2 to 11 modules. Note that this number may not include power supply and SpaceUM modules from some use cases. It is interesting to note the type of cards proposed and how they were connected to others in their respective chassis. Most cards are Single Board Computers or Processing Cards, which are variants of the same general card type.

Block Diagrams – System Level, Box Level and Board Level

To assess the use case, it is important to understand the construction of the use case. Each use case document provides block diagrams from a system, box/chassis, and board/PIC perspective. For this NASA SpaceVPX Interoperability Study, the most relevant block diagrams are the box and board/PIC levels, which aligns with SpaceVPX. At this point, it can be determined the extent to which a specific use case aligns with SpaceVPX.

Required Interfaces - Data Types and Rates

The level of modularity for SpaceVPX is the board/PIC. To fully define these boards, it is important to know the type of protocol ferrying data and information and the rate at which it carries this data. Seeing similar types of data and their rates allows for common choices with respect to boards for a broad selection of missions.

Bandwidth of serial data on the backplane ranges from 10's of kilobytes per second (kbps) to >10 one billion bits per second (Gbps). However, sensor data rates do not exceed 5 Gbps, which is interesting given specified data rates inside the chassis between cards. Most use cases specified SRIO as the high-speed data plane given the use of SRIO in SpaceVPX. A clear distinction between SpaceVPX required protocols and options outside of SpaceVPX was not articulated to use case authors prior to their creation. Generally it is safe to assume the presence of SRIO as a surrogate for high-speed serial interfaces with sufficient bandwidth. SpaceWire control plane is required for the majority of use cases. The most demanding use cases require PCIe expansion plane to support coprocessing. Low-rate interfaces (i.e., below control plane bandwidth) are needed to support simple modules without FPGAs. Regarding FPGAs, there is a need for on-orbit programming over the backplane for FPGA-based modules.

Timing and Deterministic Constraints

The use case specified a requirement for timing constraints based on a latency need. This need could manifest as deterministic behavior to the point where communication between modules is tightly scheduled, or as best effort traffic with unbounded timing.

Power Architecture

The use cases specified the use of backplane voltage rails, which are converted from spacecraft bus power by a power supply module. The rails provided are 3.3, 5, or ±12 volts (V), and the majority of use cases specified use of all three voltage rails. However, most of the use cases were defined at a high level of abstraction, and some flexibility in which specific power rail(s) are used can be assumed.

Redundancy and Fault Management – Redundancy Management Approach, Fault Management Approach, and Physical Fault Containment Approaches

Level of redundancy and fault tolerance along with extent utilized across the system fell into two broad categories. These were a need for redundancy and fault tolerance or a single-string system. In some cases, only critical components were selected for redundancy, while in others redundancy boundaries were broader. Some fault tolerance schemes were very specific to the use case (e.g., hazard avoidance in the NASA HPSC A-Team). Several use cases, based on SpaceVPX, include fully dual redundant boards (i.e., spares).

7.1.2 Use Case Overview

Detailed descriptions of each use case is provided below. The full text for each of the use cases is provided in Appendix C.

Crewed Mission Avionics

This use case analyzes the Lunar Gateway Vehicle System Manager (VSM), which supervises multiple Module System Managers (MSMs) to provide overall management for Gateway and performs functions including fault management, planning, scheduling, and resource management. The use case provided an overview of a scenario where the VSM coordinates the MSM in the Power and Propulsion Element (PPE) to manage a battery fault. The existing Gateway avionics architecture maps the VSM and MSM functions to Gateway Control Unit (e.g., GCU, VCUs, and TTE Switch Units (TSUs)).

Destination	Cis-Lunar
Mission Criticality	Class A
SWaP Sensitivity	Not addressed
Number of Modules	5 for VCU/GCU 3 for TSU
Required Backplane Interfaces	PCIe or SRIO for VCU/GCU TTE for TSU
Redundancy and Fault Tolerance	Box-Level Redundancy

Crewed Mission Robotics

This use case is comprised of two subordinate use cases. First, the Robonaut, a dexterous humanoid robot built and designed at NASA JSC is analyzed. This use case focuses on dexterous robotic systems that must work in crewed environments. This system is decomposed into a Brainstem which is the main computing systems of the robot, a Joint Driver, and End Effector Driver. This use case analyzes a Lunar Terrain Vehicle, which provides crew mobility on the lunar surface.

Destination	LEO, Cis-Lunar, Lunar Surface
Mission Criticality	Class A
SWaP Sensitivity	High
Number of Modules	Robonaut – 7 LTV – 6
Required Backplane Interfaces	PCIe or SRIO
Redundancy and Fault Tolerance	Single-string, but with multiple fault containment regions for critical functions

SmallSats

In this use case, SmallSats are typically a ride-share mission opportunity for some form of technology demonstration or specific application. SmallSats are larger than CubeSats and may operate for several years beyond their design requirements. For this use case, a SmallSats based on the ASTERIA CubeSat carrying a high-definition, multi-spectral imager payload is imagined. The major functions in this use case are communications, guidance, navigation and control (GNC), power, thermal, and payload data management.

Destination	LEO, GEO, Cis-Lunar, Deep Space
Mission Criticality	Class D
SWaP Sensitivity	High
Number of Modules	6
Required Backplane Interfaces	SRIO and SpaceWire
Redundancy and Fault Tolerance	Single-string, but with hardware watchdog timers and ground monitoring

OSAM

This use case refers to autonomous or tele-robotic servicing of a satellite by a robotic spacecraft. Based on the avionics for the NASA OSAM-1 mission, this use case includes an automated rendezvous and capture operation, and an autonomous or tele-robotic servicing phase. The major functions of this are attitude control, housekeeping, robot arm control, pose estimation, and camera data ingest.

Destination	LEO (for foreseeable future)
Mission Criticality	Class B and C
SWaP Sensitivity	Low
Number of Modules	7
Required Backplane Interfaces	SRIO and SpaceWire
Redundancy and Fault Tolerance	One hot, block redundant

Robotic Science Rover

This use case was modeled on the Mars 2020/Perseverance rover. Major functions addressed in this include: cruise operations; entry, descent and landing (EDL); surface mobility and science operations; power and thermal management; and communications.

Destination	Mars
Mission Criticality	Class B
SWaP Sensitivity	High
Number of Modules	10
Required Backplane Interfaces	SRIO and SpaceWire

Redundancy and Fault Tolerance	Dual string, with hardware watchdogs and ground monitoring and continuous monitoring, diagnostics, and recovery via software

Precision Landing Processor

SPLICE is a technology demonstration project designed to build a set of hybrid technology computing and sensor hardware combined with imbedded algorithms that can be used to successfully land a spacecraft autonomously in an area with unknown surface features. The DLC is the computing element to process sensor data, to run terrain relative navigation (TRN), hazard detection (HD), EDL, and GNC.

The major functions of this use case are sensor interfaces, time tagging, time synchronizing, image processing and map comparison (i.e., TRN), safe site identification (i.e., HD), sensor modes, sequencing, EDL, and GNC.

Destination	Lunar or Mars Surface
Mission Criticality	Class A
SWaP Sensitivity	Very High
Number of Modules	7
Required Backplane Interfaces	SRIO, XAUI, PCIe, and SpaceWire
Redundancy and Fault Tolerance	Single-string for technology demonstration. Single fault tolerance with ability to operate through faults for operational system.

High Data Rate Missions

There are three distinct use cases in this category. One is based on the a EMIT high-rate spectroscopy mission, another is a high-rate Radar mission (i.e., Radar for Europa Assessment and Sounding: Ocean to Near-surface (REASON), and the third is based on the Hyperspectral Infrared Imager (HySPIRI) Intelligent Payload Module (IPM).

The spectroscopy is a hyperspectral imaging system (i.e., 'imaging spectrometer') acquiring images in a hundred or more contiguous spectral bands. The precise spectral information contained in hyperspectral images enables better characterization and identification of targets.

EMIT uses an advanced imaging spectrometer instrument that measures a spectrum from every point in the image. Sunlight reflected from minerals on the Earth's surface is imaged by a telescope and spectrometer system onto a detector area array that is sensitive from the visible to short wavelength infrared portion of the electromagnetic spectrum. The EMIT dust source minerals have distinct spectral signatures in this wavelength range. Each column of the detector array records the spectrum for a sample of 1240 cross-track EMIT instrument swath.

The major functions for this use case are high performance computing for hyperspectral data acquisition, pixel co-adding, cloud computation and screening, buffering, compression, and data storage.

The high-rate radar use case is a planetary radar astronomy use case for the study of Solar System entities by transmitting a radio signal toward the target and then receiving and analyzing the echo. This field of research has primarily involved observations with Earth-based radar telescopes, but includes certain experiments with a spaceborne transmitter and/or receiver.

REASON is a multi-frequency, multi-channel ice penetrating radar system that will be flown on the Europa Clipper mission to Jupiter's moon Europa. REASON investigation will provide the first direct measurements of Europa's ice shell surface character and subsurface structure.

The major functions for this use case are transmit chirp generation, receive signal processing and/or on-board processor/FPGA, storage of high-rate data, and downlink of radar data.

The HySPIRI IPM performs onboard hyperspectral image classification to provide real-time, high priority data products via direct broadcast to users.

Destination	EMIT – ISS REASON – Europa HySPIRI IPM - LEO
Mission Criticality	Class B - C
SWaP Sensitivity	Moderate - High
Number of Modules	EMIT – 2 REASON – 6 HySPIRI IPM - 4
Required Backplane Interfaces	SRIO, JESD204, and SpaceWire
Redundancy and Fault Tolerance	EMIT – Single-string REASON – Dual string HySPIRI – Single-string

Low/Medium Data Rate Mission

This use case focuses on Low/Medium Data Rate Missions defined as missions with on-board data rate of < 1 Gbps, which covers most NASA missions. When mapping this use case application to SpaceVPX, it is apparent that the data rates under consideration fall at the low end of the data rate spectrum. Typical functions employing these data rates include science data acquisition, time tagging, bulk data storage, data processing, and data transmission (e.g., to a downlink channel).

Destination	Mars
Mission Criticality	Class A - D
SWaP Sensitivity	Varied
Number of Modules	6
Required Backplane Interfaces	SRIO and SpaceWire
Redundancy and Fault Tolerance	Block Redundant with Cold Standby

Communication Relay Spacecraft

This use case was constructed largely from the LCRD Payload, modem box, digital slice. This card processes high-rate data frames and performs coding and decoding functions. This use case requires an array of FPGAs to achieve encoding/decoding and interleave/deinterleaving at highest data rates. Decoding demands the most resources. These FPGAs could potentially be distributed through multiple slots on a SpaceVPX backplane. Future missions must support functions (e.g., software-defined radios and data storage) and forwarding to support Delay Tolerant Networks (DTN). The major functions of this use case are framing/deframing, encoding/decoding, interleaving/deinterleaving, number of interleaved copies sent, time keeping, software defined radio (i.e., not an LCRD function), data storage and forwarding that supports DTN, and optical module (OM) pointing

Destination	GEO, Cis-Lunar
Mission Criticality	Class A - D
SWaP Sensitivity	Moderate for large relay spacecraft, high for constellations
Number of Modules	7
Required Backplane Interfaces	Aurora and SpaceWire
Redundancy and Fault Tolerance	Redundant for large relay spacecraft, single-string for constellations, onboard monitoring and fault management, ground monitoring

HPSC A-Team

The HPSC A-Team study assessed requirements for candidate mission concepts where HPSC could be used. This HPSC A-Team use case is an amalgamation of the many requirements and architectures from this assessment. This use case can be generally characterized by the need to perform complex autonomous operations in an uncertain environment. For example, in the case of the Titan Saturn System Mission (TSSM), parallel autonomous operations include Montgolfière aerial navigation using Titan atmospheric wind currents, remote image processing

and mapping of Titan's surface, feature recognition and opportunistic science data processing, drone deployment and multi-agent control, and downlink management.

These parallel operations are highly coupled (e.g., aerial navigation to high-value science targets requires imaging processing of Titan's surface and mosaic mapping to onboard Cassini data at a different image scales for relative navigation). Feature extraction and recognition will be used to determine drone targeting and navigation parameters and inform deployment operations. The Montgolfière will be delivered to ~20°N and will orbit around the equatorial region at a 10 km nominal altitude.

The major functions of this use case are:

- Cruise, Entry, Descent, and Inflation
- Power and Thermal Management
- Communications
- Multi-scale image processing
- Autonomous orbit determination and navigation
- Feature tracking and three-dimensional (3D) scene construction
- TRN, hazard avoidance and precision landing
- Surface mobility, task planning and scheduling, opportunistic science data processing
- Advanced autonomy executive for coordinating system health/fault management, GNC, situational awareness, task and resource planning, goal-based directives

Destination	Saturn Titan System
Mission Criticality	Class B
SWaP Sensitivity	High
Number of Modules	11
Required Backplane Interfaces	SRIO and SpaceWire
Redundancy and Fault Tolerance	Selective redundancy for critical functions, autonomous integrated health management system with fail operational capability

Table 3 lists the findings derived from the use case analysis.

Table 3. Use Case Analysis Findings

	Finding
F-1	While low SWaP is generally needed, 3U and 6U sizes were seen in the NASA use cases.
F-2	Module-to-module bandwidth of 10 Gbps envelopes the needs of NASA use cases.
F-3	A SpaceWire control plane is needed by the majority of NASA use cases.
F-4	Low-rate interfaces (below control plane bandwidth) are needed to support simple modules without FPGAs.
F-5	NASA use cases include both single string and redundant systems.
F-6	Due to SWaP considerations, some of the NASA use cases prefer a power management and distribution approach that differs from SpaceVPX.

7.2 NASA Product Survey Activity and Results

From a broader perspective, the use of MOSA and Open Architectures in general are becoming pervasive across government, such as the use of MOSA throughout the DoD or the development of SOSA™. The need to 'modularize' existing hardware and software and levy architectural measurements (e.g., Interoperability, Portability, and Scalability) that measure the effectiveness of an Open Architecture and its common elements are key to the success of any effort in this manner.

Since NASA studied this approach from a hardware perspective via SpaceVPX (VITA-78), the utility and overall benefit of SpaceVPX is understood with respect to common hardware building blocks which are reusable across a variety of applications. NASA focus is to study SpaceVPX against a myriad of agency Use Cases and derive a subset of hardware building blocks that maximize interoperability, portability, and scalability.

From NASA perspective, it was important to understand the SpaceVPX ecosystem and its potential growth and evolution. There are a variety of methods possible to gather useful information. A list of organizations and products were collected. This became the base list the assessment team used to create an Industry Product Survey. The survey was a method by which the team could engage with Industry in an informal manner to gain this understanding of the SpaceVPX ecosystem.

The assessment team received 12 responses from aerospace avionics/electronics companies/integrators.

The survey was divided into the following six major sections. Each section contained a specific theme with questions to elicit specific participant responses.

1. Supplier Information
2. Current Product Line
3. Future Product Line
4. Supplier Product(s) Function and Performance
5. Fault Tolerance
6. Radiation Tolerance and Parts Grade

7.2.1 Supplier Information

Important information gained from the survey was the extent to which the supplier has used SpaceVPX. This number ranged from just starting to use the standard (i.e., 0 years) to more than 7 years (i.e., since the standard was published). This speaks to the evolution of the SpaceVPX standard and the growth of its ecosystem.

Current Product Line

All participating companies using SpaceVPX produced 3U and 6U boards. Many boards produced were Single Board Computers (SBCs), Controller Modules, or Payload Modules, which is a general term encompassing reconfigurable computing boards. Similar trends followed with accompanying Module Profiles for 3U or 6U. All Module Profiles in SpaceVPX use Serial RapidIO (SRIO), SpaceFibre, or SpaceWire for the 2015 version of the standard. Interesting to note is the use of non-standard (from a SpaceVPX perspective) protocols. Example protocols used in SpaceVPX Profiles are Ethernet, PCIe, and Aurora. Lastly, given that SpaceVPX, like OpenVPX, allows for User Defined pin space in its Slot Profiles, it was prudent for the assessment team to understand if industry uses this space, how they use it, and what they put on the pins. The majority do use User Defined space.

Future Product Line

This topic naturally follows the Current Product Line. An understanding of where industry is today is gained based on their customer needs and/or the internal product line architectural plans. Where industry plans to go with their products and SpaceVPX needs to be understood. Unfortunately, the information received was less clear than that for current product lines. Some of the same questions were asked in this topic as were in the prior topic (e.g., what Slot Profiles will you support?, what Module Profiles will you support?, and do you use any protocols not represented in existing SpaceVPX Module Profiles?). A key difference between these sections was a roadmap or schedule request. When will the products become available for use?, which resulted in vague to non-existent responses. Only one respondent provided an estimate and that was in 2022. The only conclusion drawn from this information is SpaceVPX products are in development.

Supplier Products(s) function and Performance

The focus of this topic was specific in its request (i.e., what was industry doing with the SpaceVPX Slot Profiles and Module Profiles?). Responses in this topic were abundant and common. The use of the word ‘common’ is appropriate given the majority of function types listed were processing or computing in nature. Differences were observed as to whether these products were pure processing modules (e.g., central processing units (CPUs) or graphics processing units (GPUs)), or were reconfigurable FPGA modules. Other responses included Controller, SpaceUM, SSDR, and Switch function types. A complete list of applications is provided. The variety of applications is evident, which lends credence to widespread utility of SpaceVPX.

- System Computer Storage for space (e.g., LEO) and other high radiation environments (MEO, GEO, HEO, deep space)
- Sensor Processing
- Mission Computer
- Software Defined Radio

- Generic Control and Payload Processor (e.g., SBC)
- Mission Specific Payload Unit and Payload data-handling
- Sensor data processing
- Any high-performance and/or high-reliability application (e.g., bus and payload subsystems) C&DH, sensor/payload processing, network processing
- Various Electro-optical payloads
- RF payloads
- Processing & Storage Electronics
- Instrument control functions (e.g., thermal, C2, etc.)
- SpaceVPX Development Hardware for Data Plane Switching and System Control

Finally for this topic, the survey requested information on the use of Discretes. This particular request aligns with the User Defined request in the previous topic. These discretes are typically mission specific and lend themselves to creating products which are unable to port from one application to the next. Examples of discrete signals used in a typical application are single-ended or differential GPIO. It is useful to understand the type and extent a developer will leverage discretes and if it is possible to fully define them based on prevalence, or consider adopting a networked option in lieu of discretes.

Fault Tolerance

SpaceVPX was developed, initially, for applications where fault tolerance and redundancy are necessary for the system success. Within the SpaceVPX Standard, there are a number of additions above and beyond what OpenVPX provides to achieve this high level of fault tolerance. These additions were listed in the survey and respondents were asked to provide information as to how their products met these additions. The fault tolerance additions, as listed in VITA-78 Section 1.7, are provided for convenience:

- Single board shut down, sleep, or restart.
- Dual-redundant power distribution
- Dual-redundant utility signal distribution
- Card-level serial management (i.e., point-point interfaces to manage individual cards)
- Card-level power control
- Fault tolerant power supply select
- Fault tolerant system controller signal selection
- Dual-redundant data planes (point-to-point cross strapped)
- Dual-redundant control planes (point-to-point cross strapped)
- Each PIC is a managed as a FRU

Responses from industry varied. Some responded with answers to the addition list, while others discussed how they screen their products based on mission profile need. It is clear industry is working to provide their customers with products that meet mission needs. It is unclear if they are developing their products to meet the SpaceVPX requirements. Mission requirements may be the reason why some responses, and their products, do not align with the SpaceVPX fault tolerance additions list.

Radiation Tolerance and Parts Grade

The majority of responses in this section indicated that products were developed to a variety of radiation tolerance levels. This is specific in terms of what is available for use. So, while the information is not directly applicable to this assessment, it provides insight into how SpaceVPX products meet NASA mission needs. Some industry respondents stated they do not have products qualified to any radiation level. With respect to parts grade level, the majority of products were Industrial or Mil-Aero with some listed as Automotive. One company listed their parts at NASA Level 2, while another one listed theirs at EEE-INST-002 Level 1 and Level 2.

Table 4 list the findings from the analysis of the product survey.

Table 4. Product Survey Findings

	Finding
F-7	Industry lacks consensus on module interconnect and form factors, and this lack of consensus is limiting investment in product development.
F-8	Industry is developing some 'SpaceVPX modules' that are not fully compliant with VITA-78.
F-9	Industry SpaceVPX modules utilizing User Defined Space can hinder interoperability.
F-10	Majority of industry SpaceVPX modules utilize SRIO for the data plane and SpaceWire for the control plane.
F-11	There is a lack of consensus among industry 'integrators' of SpaceVPX systems on the utility of cross strapped versus single-string block redundancy systems.
F-12	Product survey suggests there is a market for SpaceVPX modules in 3U and 6U form factors.

7.3 Study Focus Areas

7.3.1 Power Management and Distribution SFA

Within the power management and distribution SFA, the SpaceVPX power management and distribution options outlined in VITA-78 were assessed and compared against how NASA specifies and builds power systems. Three power distribution options are supported in VITA-78 for 3U SpaceVPX chassis. As shown in Figure 8, a SpaceUM profile (SLT3-SUM-2S3V3A1B1R1M4C-14.7.1) is defined that can provide three main voltages (i.e., +3.3V, +5V, and +12V) to up to two modules. In addition to the main voltages of +12V_Aux, -12V_Aux, and 3.3V_Aux.

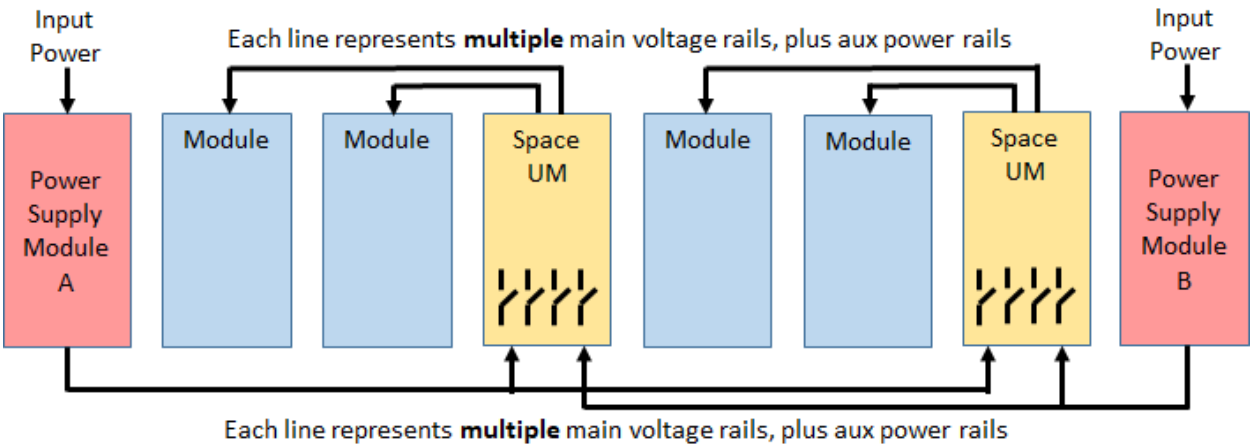


Figure 8. Two Output SpaceUM Option

Alternatively, a SpaceUM profile (SLT3-SUM-5S1V3A1R1M3C-14.7.2) can provide a single main voltage to up to five modules, as illustrated in Figure 9, in addition to the main voltages of +12V_Aux, -12V_Aux, and 3.3V_Aux.

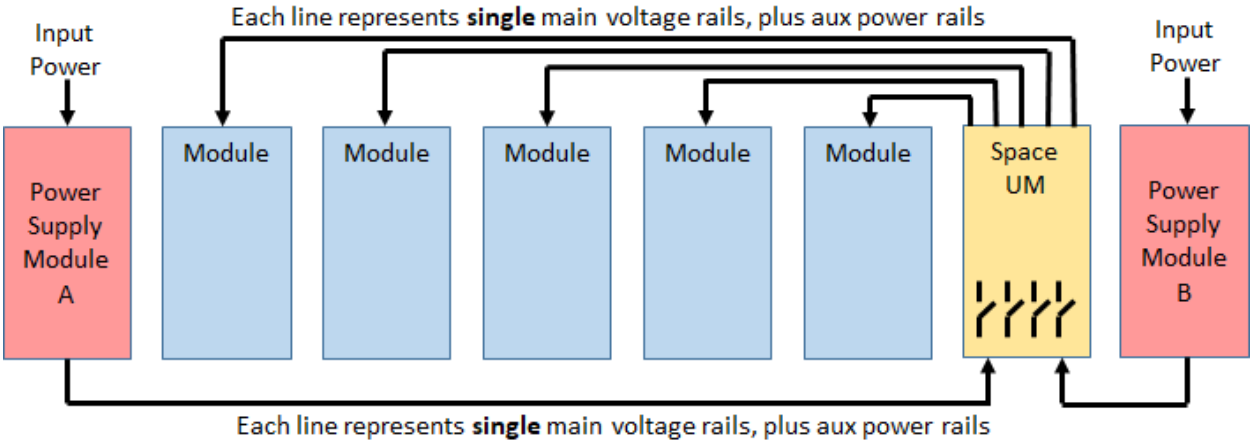


Figure 9. Five Output SpaceUM Options (showing only one side)

For each of these two options, the SpaceUM controls which power supply is used based on signals from the system controller. Note that it is not possible to interconnect the outputs of Power Supplies A and B. They use different conductors on the backplane, and the circuitry on the SpaceUM isolates the secondary power from these two modules. Note that the Power Supply modules provided isolation between the vehicle power and their secondary power services.

Lastly, there is the option to distribute power without a SpaceUM. In this configuration, two Power Supply Switch Modules (SLT3-PSS-6S3V3A1B-14.8.2) provide multiple main voltages to up to five modules. As the power inputs to each module are connected to the Power Supply Switch Modules, only one is allowed to be enabled at a given time (see Figure 10). Note that one of the modules must be a Utility Switch Module (SLT3-SUS-10S4M2C1R-14.9.2) to provide the utility plane management functions that would be performed by the SpaceUM.

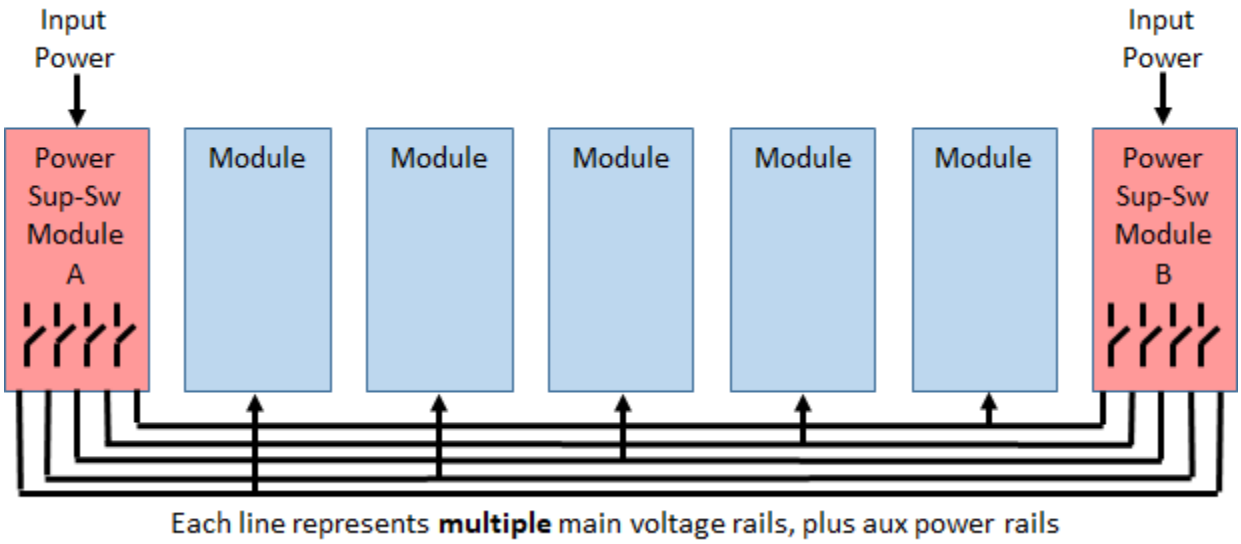


Figure 10. Power Supply Switch Option

Note that the Power Supply Switch option does interconnect the outputs from each of the power supplies. It is assumed that the spacecraft power system would ensure that the input power services to Power Supply A and B are never enabled at the same time.

To ensure interoperability between modules, only one of these three options can be supported. Table 5 lists the pros and cons for each option. Based on this assessment, Option 2 (i.e., 5 output SpaceUM) meets the needs for NASA SpaceVPX implementations.

Table 5. 3U Power Distribution Options

Option		Pros	Cons
1	SpaceUM distributes main voltages to 2 modules (SLT3-SUM-2S3V3A1B1R1M4C-14.7.1)	Compatibility with existing 3U SpaceVPX modules	Most use cases require multiple SpaceUMs, which increases the chassis SWaP
2	SpaceUM distributes one main voltage to 5 modules (SLT3-SUM-5S1V3A1R1M3C-14.7.2)	Limits the number of SpaceUM modules needed	None noted
3	Split SpaceUM function between Power Supply-Switch (SLT3-PSS-6S3V3A1B-14.8.2) and Utility Switch	The use of 2 power supply-switch modules with a utility switch module can reduce the module count for redundant 3U systems	Uncertain that power converters and switches can fit into a single 3U module

With the identification of the 5-output SpaceUM, an additional determination is needed for the main voltage to provide power to the modules. The options available are 3.3V, 5V, and 12V. Table 6 lists the pros and cons for each of these options. Based on this assessment, 5V is identified as the main voltage. This has been adopted by the SPLICE project for their power distribution architecture. With 2 processor boards, an FPGA board, and a solid state recorder board, SPLICE represents a stressing use case for a 5-output SpaceUM. The estimated SPLICE peak power, excluding the power supply, is 130W, which is 79% of the available power.

Table 6. Main Voltage Options

Option		Pros	Cons	Notes
1	3.3V	Can save voltage regulator since most NASA systems use 3.3V on a card.	Total chassis power limit may be too low for some applications.	Total primary bus power limited to 120.45W*. Per module primary power limited to 66W*.
2	5V	Adopted by SPLICE.	May be divergent from industry trends.	Total primary bus power limited to 165W. Per module primary power limited to 100W.
3	12V	Consistent with non-aerospace trends. Provides maximum power. However, thermal may be the driving issue for power.	Limited selection of radiation hardened power converters support 12V input.	Total primary bus power limited to 438W. Per module primary power limited to 240W.
* Note that the 3.3V power supply module profile in VITA-62 provides 20A, which would limit total power to 66W.				

For 6U SpaceVPX chassis, there is one power distribution option provided. The 6U SpaceUM profile (SLT6-SUM-8S3V3A1B1R1M4C-10.8.1) provides multiple main voltages to up to 8 modules. In a split 3U/6U chassis, the single main voltage for the 3U modules would be available from the 6U SpaceUM.

Within VITA-78, a separate VBAT power service shown on the pinouts of the 3U and 6U modules, but is stated as not being used in the standard. The original intent of this service was to provide power to modules from a battery internal to the chassis. This is not a credible use case for NASA applications, as batteries are typically housed in separate enclosures.

The Power Management and Distribution SFA included an assessment of the completeness of VITA-78 in addressing common power requirements that are defined for NASA applications. As shown in Table 7, VITA-78 explicitly addresses the key requirements or provides options for achieving them.

Table 7. VITA-78 and Common Power System Requirements

Common Requirements	Addressed In VITA-78	Comments
Power Capability total and per service	Yes	
Capacitive loading total and per service		Not explicit, but considered embedded in the turn-on requirement
Turn-on transient	Yes	
Turn-off time – discharge time		Can be controlled with the software control in the SpaceUM. Might need smarts in the SpaceUM (i.e., FPGA).
Sequencing	Yes	By commanding switches
Reset (Individual resets)	Yes	
Brown out protection		Can be implemented locally to the SpaceUM or the load card
Interlock side A versus side B, but not both off		Can be implemented at the SpaceUM
Primary and redundant in separate connectors		Yes, for input power from power supply. No, for output power to backplane
Distribution Voltage drop	Yes	Point to point distribution. Backplane design dependent.
Distribution Noise coupling	Yes	EMI requirements per application. One ground.
Telemetry	Yes	
Primary to Secondary Isolation	Yes	At power supply module.
Electromagnetic Interference (EMI)	Yes	EMI requirements per application
Thermal	Yes	Max power allocation established. Thermal management provisions mentioned in doc
Temperature range		None specified. Assuming analysis per application.

The voltage drop for each power service is assumed to be a mission specific backplane design issue. VITA-78 allows for remote sensing, but is assumed that this can only be implemented within the SpaceUM before the power switches. Power distribution is point-to-point from the SpaceUM to each module, with voltage drop addressed on a per module basis within the backplane design.

There are other system-level power management issues to consider. Note that SpaceVPX power distribution and management requires at least three modules (i.e., power supply module, SpaceUM, and a system controller) in the design, which can be inefficient for simple applications. While not included in the NESC recommendations, it is possible to configure SpaceVPX modules into ‘minimalist systems’ as illustrated in Appendix B. Given the number of power converters and switches required, there is uncertainty as to whether or the Power Supply Switch can be implemented in the 3U form factor. If feasibility of the Power Supply-Switch module is verified, then it provides other options for implementing minimalist systems.

In applications where the SpaceVPX system is controlling the state of the spacecraft power system, there is a need to ensure that one side of the SpaceVPX chassis is always active to manage the power system.

As defined in VITA-78, the SpaceUM depends on an external source for side A and B arbitration. On power up, power select pins provide default A/B selection. These pins are assumed to be tied to appropriate voltages on the backplane. The System Controller can provide higher level arbitration and command SpaceUMs to change power selection. However, VITA-78 does not indicate how the System Controller implements this arbitration, which can be driven by the degree of autonomy assumed at the system level.

Within VITA-78 SpaceVPX, power management can be implemented over the System Management Bus using the IPMI or the Direct Access Protocol (DAP). However, consultation with representatives of the Space Power Consortium (SPC) informed the SFA of an emerging Power Management Bus (PMBus) standard that could provide greater control and monitoring to support system-level autonomy.

Regarding redundancy, at least two options exist. A fully redundant cross strapped system can be implemented with each SpaceUM receiving power from two power supplies modules. In this architecture, power redundancy and cross strapping is maintained to the power switches in each SpaceUM. Alternatively, a block redundant architecture can be implemented, with each block comprised of a single-string system. In each single-string, one power supply and one SpaceUM feeding all modules. Input power from two power sources can be cross strapped at the power supply. Regardless of the architecture adopted, it should be noted that backplane distribution is single-string and each module only accepts one set of power inputs.

Table 8 lists six findings were derived from the Power SFA.

Table 8. Power SFA Findings

	Finding
F-13	The needs of most 3U use cases cannot be met with the 2-output SpaceUM (SLT3-SUM-2S3V3A1B1R1M4C-14.7.1) but can be met with the 5-output SpaceUM (SLT3-SUM-5S1V3A1R1M3C -14.7.2).
F-14	The SpaceVPX standard power management and distribution approach supports interoperability, but constraints are needed on main bus voltage for the 5-output 3U SpaceUM.
F-15	The needs of 6U use cases can be met with the standard 8-output SpaceUM (SLT6-SUM-8S3V3A1B1R1M4C-10.8.1).
F-16	While IPMI and DAP are specified in the SpaceVPX standard, a development SPC PMBus specification may offer system level features (i.e., controlled from within or outside of the SpaceVPX chassis) that can enable higher autonomy levels.
F-17	VBAT is included within VITA-78 for systems with batteries within the chassis, but is not applicable to NASA systems.
F-18	The feasibility of implementing a 3U Power Supply-Switch module that can be achieved with the required number of power converters, switches, and control circuitry is uncertain.

7.3.2 Interconnect Study Focus Area

Within the Interconnect SFA, the SpaceVPX interconnect options outlined in VITA-8 were assessed for the various planes defined in the standard. These options were compared the needs of NASA use cases, technology trends within industry, and guidance from SMEs. This analysis led to the development of a notional block diagram, shown in Figure 11, that illustrates an instrument data system to show the potential interconnect between modules.

It should be noted that while SpaceVPX separate different types of traffic into separate planes, there are trends within industry to control and data flow traffic on a single high-bandwidth onboard network. One example of this is Time Triggered Ethernet (TTE) which offers 3 levels of Quality of Service (QoS) for different traffic classes. Another example is SpaceFibre, which combines support for both control and data functions within a single protocol. One product survey respondent did recommend combining control and data plane functions on SpaceFibre links.

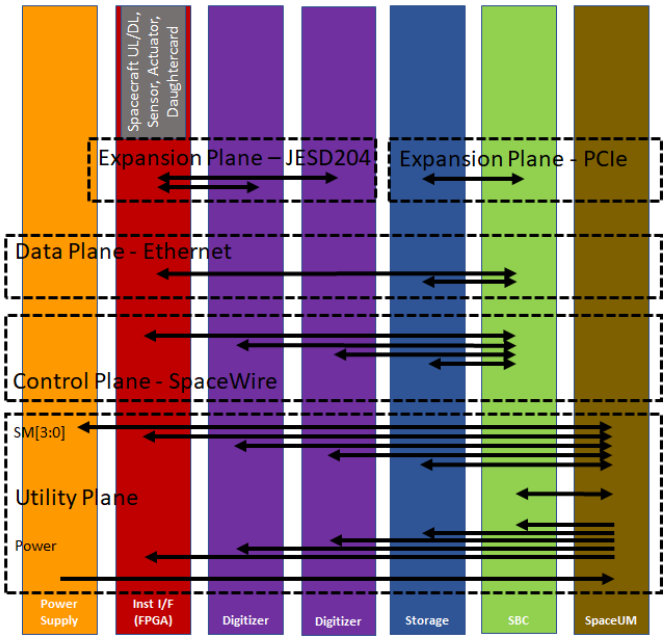


Figure 11. Notional Instrument Data System

Based on the use cases, product surveys, and SME guidance, this SFA defined recommendations for the interconnect to be used for NASA systems and which VITA-78 options to avoid. Note that in determining proposed interconnect standards, the SFA was not bound by the options listed in VITA-78.

This SpaceVPX Interoperability Study was concurrent with the concept study phase of the NASA STMD HPSC project. In this phase, the HPSC project awarded contracts to three vendors to develop CSRs for a general-purpose, multi-core processor that will be widely applicable to missions across NASA and the broader spaceflight community.

The overlap of this assessment with the HPSC concept phase allowed requirements choices made by the HPSC team, and industry surveys and the rationale for design choices from the CSRs, to inform interconnect findings and recommendations. Use case analysis performed by this assessment influenced processor requirements choices made by the HPSC team. Furthermore, as inferred, this assessment has informed the development of HPSC SBC.

Data Plane

SRIO and SpaceFibre are defined within VITA-78 as options for the data plane. Based on the product survey analysis, several SpaceVPX products are on the market that utilize SRIO. One respondent to the product survey lists plans for SpaceVPX products based on SpaceFibre. However, neither of these interfaces have strong industry support moving forward. Industry engagement in the SRIO standards organization has waned in recent years, leaving a void of

stakeholders that can maintain the standard in the future. SpaceFibre is a standard that has been developed specifically for aerospace applications, and while it has stakeholders within the European Space Agency (ESA), the intellectual property (IP) core for this standard is only available from one source. The HPSC CSR vendors found limited interest within their anticipated customer base for SRIO or SpaceFibre, and as a result neither is planned to be supported as native on the HPSC chiplet.

Based on guidance from the HPSC CSRs, the HPSC project, and other SMEs, Ethernet was determined to be the ideal option for the data plane. Specifically, Ethernet 10GBASE-KR, as defined in IEEE 802.3ap, with support for Time Sensitive Networking (TSN) is proposed. The 10GBase-KR standard provides point-to-point 10 Gbps links and is targeted for backplane applications.

TSN is a set of standards that provides bounded latency interconnect for applications requiring determinism, allowing time sensitive messages to be transferred over Ethernet networks. These standards define mechanism for time synchronization across network nodes, traffic shaping to prevent bottlenecks that can increase latency, and fault tolerance.

TSN Industry surveys conducted by HPSC CSR vendors have indicated strong interest in Ethernet/TSN as the future onboard network standard. Other government agencies have expressed support for Ethernet for future onboard networks and have expressed some interest in TSN. This standard supports autonegotiation to 10 and 1 Gbps data rates, which support the broad range of NASA use cases.

TSN 'profiles' are defined that adopt a subset of the TSN standards to meet the needs of specific application domains. Driven by the HPSC requirements, the TSN standards that are proposed for use within SpaceVPX are listed in Table 9.

Table 9. TSN Standards

Standard	Description
IEEE 802.1AX	Link Aggregation
IEEE 802.1CB	Frame Replication and Elimination for Reliability
IEEE 802.1AS	Timing and Synchronization for Time-Sensitive Applications
IEEE 802.1Qbv	Enhancements for Scheduled Traffic
IEEE 802.1Qav	Forwarding and Queuing Enhancements for Time-Sensitive Streams
IEEE 802.1Qci	Per-Stream Filtering and Policing
IEEE 802.1Qcc	Stream Reservation Protocol (SRP) Enhancements and Performance Improvements
IEEE 802.1Q (Clauses 8.6.5.1 and 8.6.8.2)	Bridges and Bridged Networks

While TTE is a necessary interface for many NASA avionics systems, it is not planned as a native interface within HPSC and is not suited for use on the SpaceVPX backplane. However, it can be implemented as a front panel interface on SpaceVPX modules.

Control Plane

VITA-78 defines SpaceWire as the interconnect standard for the control plane. In addition to this standard, the Interconnect SFA assessed controller area network (CAN bus) as a potential alternative. CAN is a fault tolerant serial bus that has broad adoption within the automotive industry. Within the space community, ESA can define extensions to the CAN standard for

spaceflight applications. The product survey showed that two companies have interest in CAN. However, one of those companies indicated that their interest was only in a front panel connector. Interest has been expressed in CAN by other government agencies, due to the broad availability of low-cost test equipment. While there are many differences between the two standards, a key difference between SpaceWire and CAN is data rate, with CAN providing a maximum data rate of 5 Mbps and SpaceWire providing up to 400 Mbps.

Based on the needs identified in the NASA use cases, the Interconnect SFA found that SpaceWire is suited to meet control plane needs. SpaceWire, as defined in ECSS-E-ST-50-12C, continues to have broad support as a control bus and medium rate onboard network for future avionics systems. This was affirmed by the HPSC CSR vendors. Within SpaceVPX, SpaceWire can serve as the primary interconnect to medium data rate modules, in addition to providing control traffic to higher data rate modules. While the Remote Memory Access Protocol (RMAP) Standard, as specified in ECSS-E-ST-50-52C, can be implemented on SpaceWire, its use is not mandatory.

Expansion Plane

VITA-78 defines the expansion plane to provide additional connections between modules. For NASA applications, the expansion plane fulfils two roles.

In addition to the links provided by Ethernet on the data plane, there is a need for dedicated high bandwidth links to coprocessor devices and data storage modules. Due to its broad industry adoption for these applications, PCIe Gen 3.1 was determined an ideal standard to provide as an optional expansion plane interface. Many commercial-off-the-shelf (COTS)-based coprocessing devices have native support for this interface. PCIe Gen 3.1 will have native support on the HPSC chiplet, and it is anticipated that this interface can provide interconnect to GPUs, AI accelerator devices, and additional HPSC chiplets.

SME guidance, with one of the high bandwidth instrument use cases, highlighted a need to provide industry standard interfaces to high bandwidth analog-to-digital-converters (ADCs) and digital-to-analog-converters (DACs). JESD204C is the standard interface for these devices, providing backwards compatibility to existing JESD204B-based devices. As an additional option for the expansion plane, JESD204C enables communication between high bandwidth digitizer modules and FPGA modules. It is assumed that FPGA modules could perform processing and formatting of digitizer data and provide prior to communicating it to/from other modules via the Ethernet data plane interface. Note that while JESD204C supports data rates up to 32 Gbps, it should be limited to 12.5 Gbps, which is consistent with JESD204B for NASA applications due to signal integrity limitations of the SpaceVPX backplane.

Utility Plane

VITA-78 provides IMPI and DAP options for protocols on the utility plane System Management Bus. IPMI implements a command response protocol to allow the System Controller to control and monitor, via the SpaceUM, modules within the chassis. As defined in the VITA-78 standard, DAP provides a register mapped control and status interface between the System Controller to the modules. Both are viable options for NASA applications, and System Controllers should have the capability to support IPMI and DAP within a single chassis. Note that developments of PMBus should be tracked for potential future adoption within SpaceVPX.

Other Interfaces

Analysis of NASA use cases and existing NASA avionics architectures raised the need for a low-rate interface (i.e., below SpaceWire bandwidth) to provide connectivity to simple modules that can be implemented without an FPGA. Examples of such module functions include:

- Temperature monitoring
- Power control and monitoring
- Motor control
- Actuator control

To meet these needs, I2C is included on the backplane. Note that this is not the same bus that is used within the System Management Bus in the utility plane.

JTAG

The JTAG interface is specified in VITA-78 to support debug and test. It provides an industry standard interface to program FPGAs with the SpaceVPX chassis. The capabilities of JTAG can raise security concerns, as a malicious actor can in theory use the interface to extract sensitive data or alter FPGA configuration files or flight software. However, the relevance of these potential vulnerabilities to NASA missions is unclear, and any needed mitigations are undefined. Until there is more clarity regarding JTAG security concerns, it is advisable to include JTAG on the backplane with the ability to disable the interface for flight via a pin on a front panel connector on the System Controller. It should be noted that while JTAG (and potentially the IMPI or DAP interface of the utility plane) can provide a means for test and debug, SpaceVPX does not define a system-level test and debug scheme.

User Defined Signals

While the VITA-78 standard allows for user-defined signals to provide flexibility, their use can hinder interoperability. To strike a balance between flexibility and interoperability, the Interconnect SFA defines two types of user-defined signals and restricts implementation.

To allow implementation of mission unique SERDES interfaces or interfaces to modules that only support legacy interconnect standards (e.g., SRIO, Aurora, or SpaceFibre), user-defined SERDES interconnect are provided. These logic signals must be connected to FPGA SERDES I/O. The flexible logic behind the I/O allows individual modules the flexibility to implement a variety of standards and can allow their usage to be tailored on a per mission basis. However, to ensure interoperability between modules, these I/O must be standardized. The Interconnect SFA evaluated existing spaceflight FPGA specifications and derived the following standards:

- 1600mV peak-to-peak AC-coupled differential signaling
- 8b/10b encoding
- Data rates of 1.25, 2.5, 3.125, 5, 6.25, and 10 Gbps. Note that some modules may not support all of these rates.

A minimal number of single-ended user-defined signals are provided, with the requirement that they be connected to configurable pins, typically FPGA I/O. This allows their usage to be tailored on a per mission basis. To ensure interoperability, 2.5V low voltage complementary metal oxide semiconductor (LVCMOS) signaling is proposed.

FPGA Programming

Several of the use cases require the use of FPGA-based modules to accelerate onboard processing, which typically use high density reprogrammable FPGAs for these applications. These FPGAs require scrubbing to correct radiation induced upsets to configuration, but provides the capability for reprogramming during flight. To support in flight FPGA reprogramming, the Interconnect SFA considered the programming options of JTAG, SelectMAP, and SpaceWire.

JTAG programming has the advantage of being an industry standard that is ubiquitous in modern microelectronics, and is being broadly supported in FPGAs. However, this interface is relatively slow and interactions with other agencies have raised potential security concerns. The 2016 IEEE paper "A Brief Review on JTAG Security" describes several of the general concerns regarding JTAG security.

SelectMAP is the fastest programming method available for Xilinx FPGAs, with programming up to 40x faster than JTAG. However, this is a parallel interface which increases the number of pins required on the backplane connector. While SelectMAP may be a viable option for 6U modules, there is insufficient space to accommodate this interface on 3U modules, specifically the SBC module that would drive the interface.

An alternative to these methods is to use an existing SpaceWire link to FPGA modules to communicate configuration files. This requires a separate 'manager' device on the FPGA modules to receive and internally store the files. This 'manager' device would locally manage the FPGA configuration from that memory. It should be noted that many spaceflight reprogrammable FPGA boards use manager devices for scrubbing and configuration. Consultation with SMEs familiar with these designs indicated that loading configuration files via these manager devices is feasible in current designs. However, NASA-wide best practices for FPGA programming and management have not been defined. A better understanding of the current and emerging FPGA configuration options is needed to define these best practices, which may influence future implementations of SpaceVPX.

Utilization of 3U and 6U interconnect

Focusing on the 3U SBC module, analysis showed that the limited pin count of the 3U connector would not support the full interconnect provided on the HPSC processor chiplet. However, it should be noted that the SBC needs of the NASA use cases in this assessment can be met within the 3U connector space by limiting the number of ports per plane. A control plane switch is needed for some use cases. The larger pin count of 6U connectors provides for 192 differential pairs, which can allow an HPSC-based SBC to accommodate the full number of ports per plane supported by the HPSC processor chiplet.

Backplanes

As discussed, this assessment does not advocate specific backplane profiles. While the SpaceVPX standard includes them, backplanes are likely to be mission specific. This can be seen by the variety of SpaceVPX implementations in the use cases. Furthermore, standardizing backplanes does not significantly promote interchangeability since it will be mounted in a chassis. It should be noted that, as specified in VITA-78, only passive backplanes are proposed.

SpaceVPX Interconnect Not Proposed for Use

Based on the analysis completed in this assessment, Table 10 lists interconnect standards that are allowed within VITA-78, but are not proposed for use in NASA applications.

Table 10. VITA-78 Interconnect Not Proposed for Use

Standard	Rationale
SRIO(*)	Product surveys and discussion with industry indicated that support for SRIO is dwindling. Some companies express interest in supporting it as a legacy interface, but they are moving on from this standard.
SpaceFibre(*)	This standard is seeing use in NASA missions, but the IP is single sourced from a vendor in Europe. The product surveys and industry surveys conducted by HPSC CSR vendors do not show broad interest.
cPCI(**)	The SpaceVPX standard allows use of cPCI heritage modules in a SpaceVPX backplane, with one or more heritage cPCI cards attached to a SpaceVPX Payload Module with cPCI bridging. However, to ensure interoperability use of cPCI is not proposed. Note that this interface may be used in 'interim systems' until the full complement of SpaceVPX module types is developed.
Unconstrained User Defined Signals	While accommodated in the VITA-78 standard, use of these signals can hinder interoperability. Analysis showed that control and status between modules and the System Controller module, typically a SBC, can be communicated via the SMBus. However, this does require modules to include a microcontroller that can communicate via SMBus while other circuitry on the module is inoperable. However, a limited number of user-defined signals are supported with the requirement that they be user configurable on a per mission basis.
(*) Note that SRIO and SpaceFibre can be implemented with User Defined SERDES signals. (**) Note that some missions may choose to implement cPCI to allow use of heritage boards.	

Signal Integrity

With the proposed Ethernet interconnect operating at up to 10 Gbps, the Interconnect SFA consulted with signal integrity SMEs to ensure that expected printed wiring board traces on the modules and the backplanes, and the SpaceVPX connectors, can support that bit rate. Leveraging analysis performed in the development of the SpaceCube-Mini, it was determined that 12.5 Gbps SERDES signals can be supported with a trace length of 13.5 inches, two SpaceVPX connectors, and a 22-layer printed wiring board (PWB) using Arlon material.

Connectors

The Interconnect SFA received support for spaceflight connector SMEs to analyze SpaceVPX connectors. There are currently four vendors of SpaceVPX, but only two offer connectors that can intermate. These intermating connectors are each compliant to the VITA-46 standard. To ensure interoperability, connectors for SpaceVPX modules and backplanes should be selected that are compliant to the VITA-46 standard.

During the SpaceVPX connector analysis, potential reliability issues were raised regarding the attachment of SpaceVPX connectors to PWBs, including the ability to tolerate shock and vibration environments. While these issues are beyond the scope of this assessment, they are critical to ensuring the reliable use of SpaceVPX modules for NASA missions.

Table 11 lists findings that were derived from the Interconnect SFA.

Table 11. Interconnect SFA Findings

Finding	
F-19	In assessing the current VITA-78 data plane standards, SpaceFibre is a sole source solution with limited spaceflight usage, and the SRIO standard lacks industry support.
F-20	TSN, which leverages Ethernet and is defined in multiple IEEE 802.1 standards, has broad industry engagement and support.
F-21	The HPSC project does not require native support for SRIO, SpaceFibre, or TTE, although these and other non-native I/O protocols can be provided at the board level using external circuitry.
F-22	The I2C bus provided within the utility plane is capable of handling PMBus functions within the SpaceVPX chassis.
F-23	12.5 Gbps SERDES signals can be supported with a trace length of 13.5 inches, two SpaceVPX connectors, and a 22-layer printed wiring board (PWB) using Arlon material.
F-24	The VITA-78 standard allows for user-defined signals to provide flexibility, but their use can hinder interoperability.
F-25	There is need to provide industry standard JESD204 interfaces to high bandwidth ADCs and DACs in excess of 1 gigasample per second (GSPS).
F-26	There is need for a low-rate I2C interface (i.e., below SpaceWire bandwidth) to provide connectivity to simple modules that can be implemented without an FPGA.
F-27	While system management is provided via IPMI or DAP on the System Management Bus, and JTAG is included to support testing, SpaceVPX does not define a system-level test and debug scheme.
F-28	Industry trends are to combine control and data flow traffic on a single high-bandwidth onboard network, and one product survey respondent recommended combining control and data plane functions on SpaceFibre links.
F-29	There are four vendors of SpaceVPX connectors, but only two offer connectors that can intermate.

7.3.3 Form Factor and Daughtercards

The SpaceVPX standard specifies two form factors, four module lengths, and five module pitches (see Table 12). There are multiple daughtercard (mezzanine card) standards. The objective of the Form Factor and Daughtercard study focus area is to enhance interoperability and interchangeability across multiple missions by limiting the configurations adopted by NASA.

Table 12. SpaceVPX Card Physical Parameter Options

Parameter	Options
Form Factor	3U 6U
Module Length (mm)	160 220 280 340
Module Pitch (in)	0.8 1.0 1.2 1.4 1.6

When designing systems for space-based applications, typically the envelope of the electronics box is negotiated. This envelope will determine the board dimensions and the number of boards that can be accommodated. The board dimension (e.g., 3U, 6U) constrains it a standard width allowing integration of COTS when available. Typically, the card's pitch or thickness is 0.8 in. The board length varies, but is sized to fit the components supporting all card features.

The advantage of longer/wider boards is higher space efficiency. The board border is dedicated to wedge locks on the sides and connectors on the top and bottom, which is the same regardless the width or length. The remaining space is available for integrated circuits (ICs), passives, and wiring. However, size has to be balanced against the thermal disadvantage of removing heat from the board's center, and mechanical disadvantage in terms of flex and vibration.

NASA Legacy cPCI Form Factors Products

The SpaceVPX standard is relatively new and adoption for NASA flight systems is low. To predict future SpaceVPX form factors used by NASA, it is best to look at the history of cPCI designs (e.g., 3U versus 6U, Figure 12). A majority of NASA's cPCI designs are 6U (6U: 64%; 3U: 36%). It is expected that this ratio will hold true for SpaceVPX form factors.

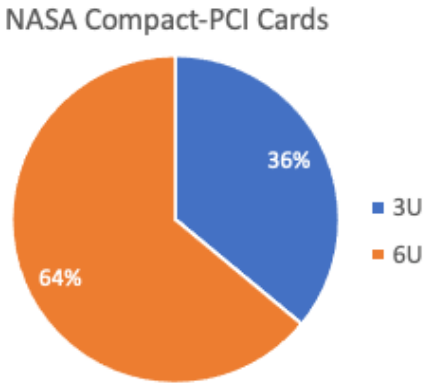
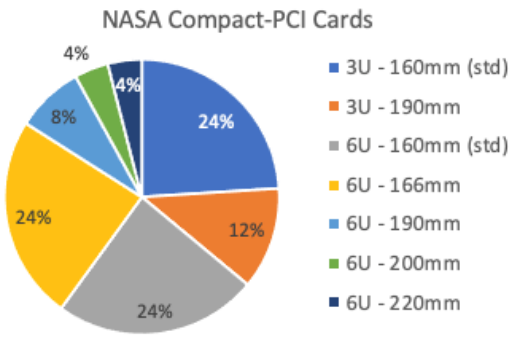


Figure 12. NASA 3U versus 6U cPCI Designs

The cPCI specification only identifies the 160mm length. NASA's cPCI cards have conformed to this standard length about half of the time (i.e., 48%). See Figure 13. To fit the larger radiation hardened components, NASA designers have customized the board lengths from 160mm to 166 through 220mm with the largest percentage for the 166mm length at 24%. Designers followed the design principal where a subsystem will integrate cards with the same length to simplify the chassis design. Thus, a custom subsystem design can choose any card length as long as all cards are designed to that length.

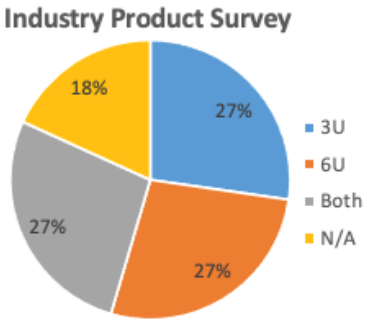


Card Dimension	% of Designs	Number of Designs
3U - 160mm (std)	24%	6
3U - 190mm	12%	3
6U - 160mm (std)	24%	6
6U - 166mm	24%	6
6U - 190mm	8%	2
6U - 200mm	4%	1
6U - 220mm	4%	1

Figure 13. NASA cPCI Card Lengths

Product Survey Data

The Product Survey engaged 11 companies from BAE Systems to STAR-Dundee. A detailed account is given in Section 7.2. Analyzing the form factor for each company's SpaceVPX offerings and cards in development shows the companies split between 3U (27%), 6U (27%), Both (27%), and No-Response (18%) as shown in Figure 14. This shows that industry sees the need to support 3U and 6U form factors. This industry result would almost mirror NASA's cPCI result if all the no responses (N/A) became 6U resulting in 3U (40.5%) and 6U (59.5%).

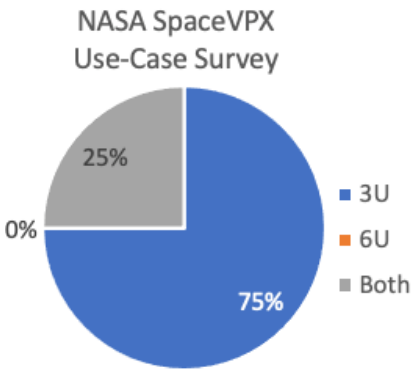


Form Factor	Percentage	Count
3U	27%	3
6U	27%	3
Both	27%	3
N/A	18%	2

Figure 14. NASA Product Survey, Supported Form Factors

Use Case Survey Data

The Use Case Survey studied 10 areas of interest for NASA from SmallSat to High Data-Rate Missions. A detailed account is given in Section 7.1.2. Analyzing the anticipated form factors for these use case areas showed 3U (75%), 6U (0%), and Both (25%) as seen in Figure 15. This confirms that NASA needs to continue to support 3U and 6U form factors.



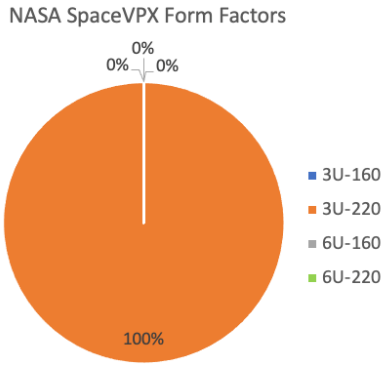
Form Factor	Percentage	Count
3U	75%	9
6U	0%	0
Both	25%	3

Figure 15. NASA Use Case Driven Form Factors

NASA SpaceVPX Form Factors Products

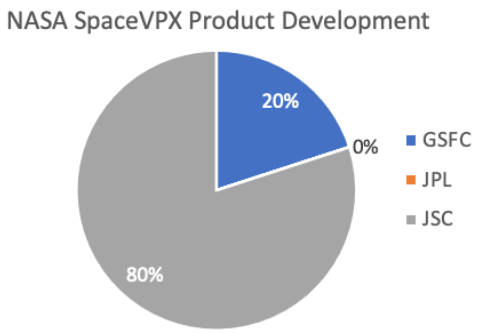
Historically, 3U or 6U cards are designed to match a mission's needs and all functionality is fixed at the onset. If a follow-on mission requires alternate features, then the card would be re-designed. If one looks at the progression of NASA's product lines that support missions, subsystem core functionality remains fairly constant, but interfaces to other subsystems can change. So rather than continuing the approach of redesigning cards, it may be prudent to split the design and place core functionality on the base card and mission specific functionality (i.e., personality) on the daughtercards. Future missions could purchase COTS daughtercards and reuse existing NASA daughtercards for rapid prototyping to improve schedule and cost.

As mentioned, NASA's migration to deploy SpaceVPX subsystems has started. JSC is leading the way developing a SpaceVPX lunar landing system under the SPLICE. GSFC has designed a SpaceVPX processor card for SpaceCube v3.0. JPL is in the product planning stage. All of the SpaceVPX cards developed are a 3U – 220mm form factor. This implies that a standard 220mm length for 6U modules is needed to enable hybrid 3U/6U subsystems. See Figures 16 through 18.



NASA SpaceVPX Form Factors	Percentage	Cards
3U-160	0%	0
3U-220	100%	5
6U-160	0%	0
6U-220	0%	0

Figure 16. NASA SpaceVPX Supported Form Factor and Lengths



NASA SpaceVPX by Center	Percentage	Cards
GSFC	20%	1
JPL	0%	0
JSC	80%	4

Figure 17. NASA SpaceVPX Development by Institutions

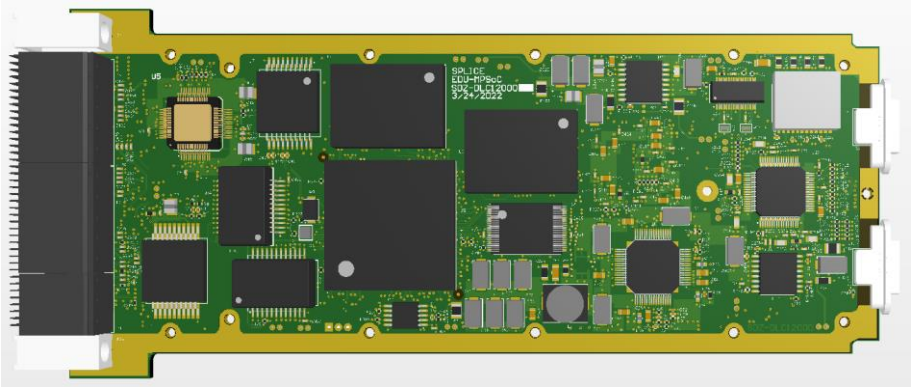


Figure 18. SPLICE 3U-220 SpaceVPX MPSoC Card

Daughtercard (Mezzanine Card) Survey

There are two predominant daughtercard (mezzanine card) standards: FPGA Mezzanine Card (FMC) [VITA-57.1] and Switched Mezzanine Card (XMC) [VITA-43 and 61]. Extended standards FMC+ (VITA-57.4) and XMC+ (VITA-88) provide enhanced electromechanical capability, but are not part of this survey. A packaging expert at JPL reviewed the manufacture's qualification testing (EIA 364) results and as a first step did not see any issues which would prevent their use. Neither FMC nor XMC connectors have gone through flight qualification testing. So qualification testing should be performed capturing at least 80% of mission environments before designing with them.

FMC Background

FMC is an electromechanical standard that creates a low/no overhead protocol bridge between the front panel IO and an FPGA. FPGAs offer a large number of configurable IOs that can support complex IO standard. Once implemented in the FPGA, all that remains are the physical IO components and connectors.

The standards goals are to:

- Maximize data throughput
- Minimize latency
- Reduce FPGA design complexity
- Minimize system costs
- Reduce system overheads

Maximum data rate for FMC IO are:.

- Supporting up to 10 Gbps transmission with adaptively equalized I/O
- Supporting single-ended and differential signaling up to 2 Gbps

Size (Conduction cooled):

- Single width: 69mm x 78.8mm
- Double width: 139mm x 78.8mm

Pin Count:

- High Pin Count (HPC): 400
    - 160 user-defined single-ended signals; or 80 user-defined differential pairs
    - 10x gigabit serial transceiver pair
    - 6 Clocks
    - JTAG
    - I2C for optional IPMI
- Low Pin Count (LPC): 160
    - 68 user-defined single-ended signals; or 34 user-defined differential pairs
    - 1 x gigabit serial transceiver pairs
    - 6 Clocks
    - JTAG
    - I2C for optional IPMI

Switched Mezzanine Card (XMC) Background

The XMC is an electromechanical standard for supporting high-speed switched interconnect protocols (e.g., RapidIO and PCI Express). The standards goal is to support:

- A high-speed switched interconnect that provides multiple points of contact
- Open standardized technologies for switched fabrics
- Standard PMC form factors
- Compatibility with existing PMC standards
- Standard PMC stacking heights
- Air and/or Conduction Cooling

Maximum data rate for XMC is listed below. Moving forward, VITA-61.0 and VITA-88.0 connectors are listed as 'alternative' solutions to the VITA-42 connector. The latest 2021 specification was updated to provide compatibility with PCI Express Gen 4 and Gen 5.

- PCIe Gen4 x1 link, 16 Gbps
- PCIe Gen5 x1 link, 32 Gbps

Size (Conduction cooled):

- Single width: 74mm x 143.75mm
- Double width: N/A (Double width specified for air cooled only)

Pin Count: 114 (min), 228 (max)

- Primary: 114
    - 20 user defined differential pairs
    - JTAG
    - I2C with IPMI
- Secondary: 114 (Usage: Fabric mode versus User I/O mode)
    - Fabric Mode

- 20 user-defined differential pairs
- 38 user-defined single-ended signals
- 36 grounds

- User I/O mode
  - Only recommended to include the same ground pins defined in Fabric Mode

Daughtercard Comparison

Companies producing FMC and XMC connectors are providing product exceeding the standards, as shown in Table 13. The following are Samtec's connector characterization speed reports from their FMC and XMC families. Note that FMC and XMC connectors have a similar speed rating of 25 versus 40 Gbps, respectively.

Table 13. FMC versus XMC Specification Comparison

Description	FMC	XMC
VITA Standard	VITA 57.1	VITA 42 [VITA 61, Ruggedized]
Technology Driver	FMC is driven by FPGA requirements that have growing bandwidth needs (i.e. higher pin-count)	XMC is driven by serial communication protocols such as Ethernet and PCIe (i.e. higher connecter performance)
Pin Count	160 (LPC), 400 (HPC)	114 (min), 228 (max)
Max Data I/O Rate	30 GB/sec	32 GB/sec
Full Duplex I/O	10 lanes	16 lanes
Interface Standard	Custom	PCIe, SRIO
Max frequency per pin		5 GHz
Board Size	53 cm^2	110 cm^2
Power Dissipation (Relative)	Low	High
Max Power	10W	70W
SOSA slot profiles	None	3U and 6U

Samtec FMC Characterization Reports

Connector System Speed Rating

SEAM/SEAF Series, 1.27mm x 1.27mm (.050" x .050") pitch interconnect, 7 mm Stack Height.

Signaling	Speed Rating
Single-Ended: 1:1 S/G	**12.5 GHz/ 25Gbps**
Single-Ended: 2:1 S/G	**12.5 GHz/ 25Gbps**
Differential: Optimal Horizontal	**13 GHz/ 26Gbps**
Differential: Optimal Vertical	**13 GHz/ 26Gbps**
Differential: High Density Vertical	**12.5 GHz/ 25Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

Connector System Speed Rating

SEAM/SEAF Series, 1.27mm x 1.27mm (.050" x .050") pitch interconnect, 10mm Stack Height.

Signaling	Speed Rating
Single-Ended: 1:1 S/G	**18.0 GHz/ 36Gbps**
Single-Ended: 2:1 S/G	**17.0 GHz/ 34Gbps**
Differential: Optimal Horizontal	**18.0 GHz/ 36Gbps**
Differential: Optimal Vertical	**17.5 GHz/ 35Gbps**
Differential: High Density Vertical	**17.0 GHz/ 34Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

Samtec XMC Characterization Report

Connector System Speed Rating

YFT/YFS Series, 1.27mm x 1.27mm pitch interconnect, 5mm Stack Height.

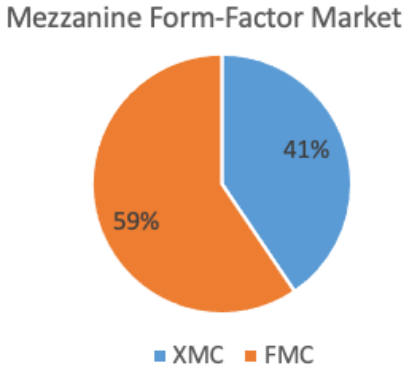
Signaling	Speed Rating
Single-Ended: 1:1 S/G	**20 GHz/ 40Gbps**
Single-Ended: 2:1 S/G	**14 GHz/ 28Gbps**
Differential: Optimal Horizontal	**13GHz/ 26Gbps**
Differential: Optimal Vertical	**20GHz/ 40Gbps**
Differential: High Density Vertical	**13 GHz/ 26Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

Daughtercard Survey Results

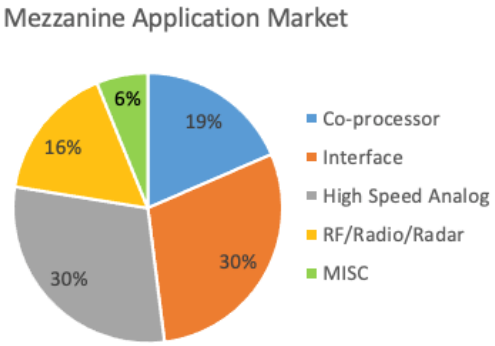
A survey of the daughtercard market was performed. The starting point for the survey was the list of FMC community members on the VITA website. An internet search was performed afterwards to find additional daughtercard manufacturers. Based on daughtercard product offerings (i.e., part numbers), FMC holds a larger share of the market at 59% as opposed to XMC at 41%. Organizing the data by application markets (coprocessor, interface, high-speed analog, RF/radio/radar, and other miscellaneous functions), FMC dominates in the interface (32%) and high-speed analog space (49%), while XMC dominates in the coprocessor (42%) and RF/Radio/Radar (27%) space. This is because FMC targets applications needing high pin count with direct connection to an FPGA while XMC targets low pin count high bandwidth

applications supporting a complex serial protocol for communication transport (Figures 19 through 22).



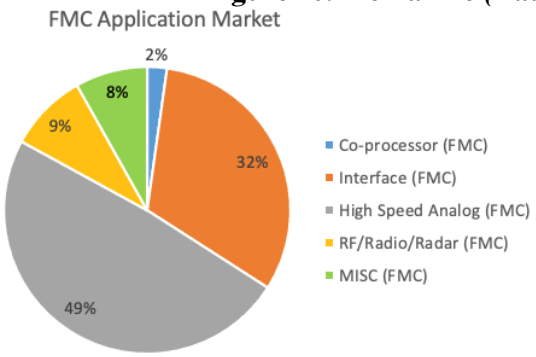
Mezzanine Standard	Percentage	Number
XMC	41%	92
FMC	59%	135

Figure 19. FMC versus XMC Market



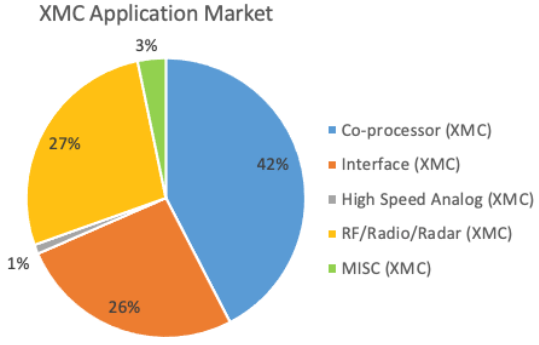
Application Market	Percentage	Number
Co-processor	19%	42
Interface	30%	67
High Speed Analog	30%	67
RF/Radio/Radar	16%	37
MISC	6%	14

Figure 20. Mezzanine (Daughtercard) Application Market



FMC Application Market	Percentage	Number
Co-processor (FMC)	2%	3
Interface (FMC)	32%	43
High Speed Analog (FMC)	49%	66
RF/Radio/Radar (FMC)	9%	12
MISC (FMC)	8%	11

Figure 21. FMC Daughtercard Application Market



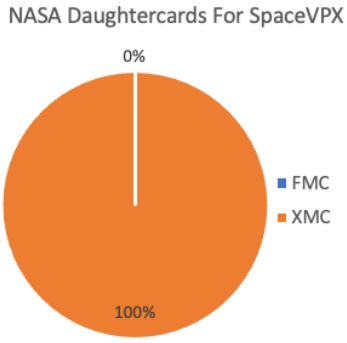
XMC Application Market	Percentage	Number
Co-processor (XMC)	42%	39
Interface (XMC)	26%	24
High Speed Analog (XMC)	1%	1
RF/Radio/Radar (XMC)	27%	25
MISC (XMC)	3%	3

Figure 22. XMC Daughtercard Application Market

NASA FMC/XMC Daughtercard Products (Figures 23 through 25)

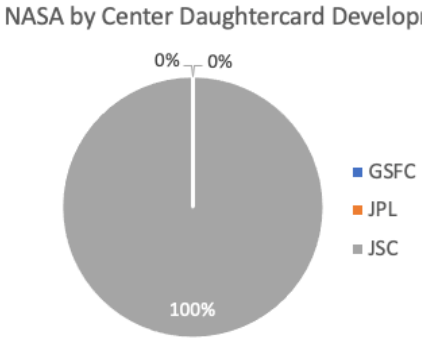
To date, the only XMC daughtercards have been developed by JSC for SPLICE.

- One 32-channel ADC daughtercard
- One I/O expander (Gigabit Ethernet, SpaceWire, RS-422) daughtercard



NASA Daughtercard	Percentage	Number
FMC	0%	0
XMC	100%	2

Figure 23. NASA Daughtercard Design by Standard (FMC versus XMC)



NASA Center	Percentage	Daughtercards
GSFC	0%	0
JPL	0%	0
JSC	100%	2

Figure 24. NASA Daughtercard Designs by Institutions

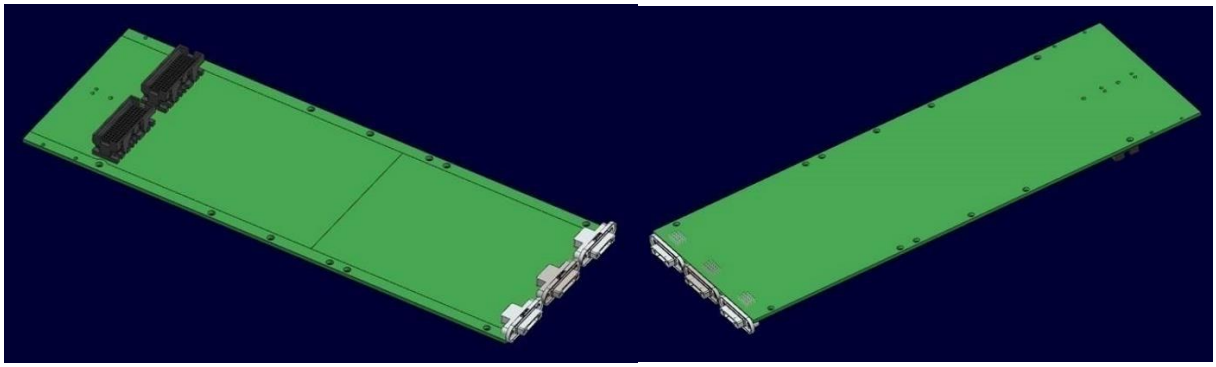


Figure 25. PCB Model of Extended XMC Daughtercard for SPLICE

SpaceVPX + Daughtercard Configurations

A 3U base card is capable of supporting 1 x FMC, or 1 x XMC daughtercard. A 6U base card is capable of supporting 3 x FMC, or 2 x XMC daughtercards (Figures 26 through 29).

3U + FMC

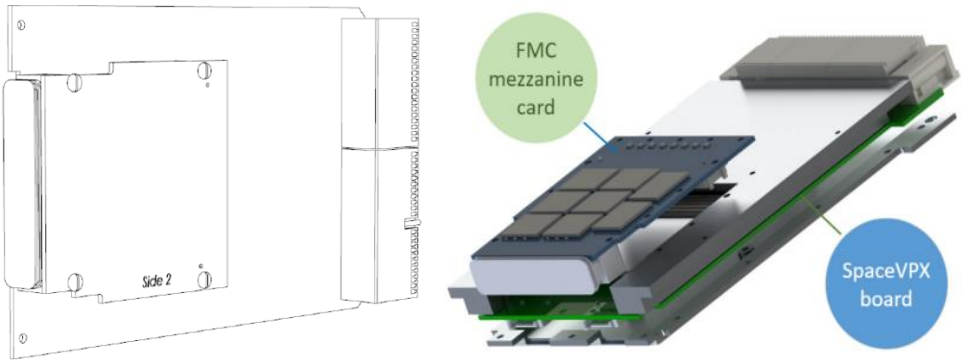


Figure 26. 3U SpaceVPX with FMC (Novo Space)

3U + XMC

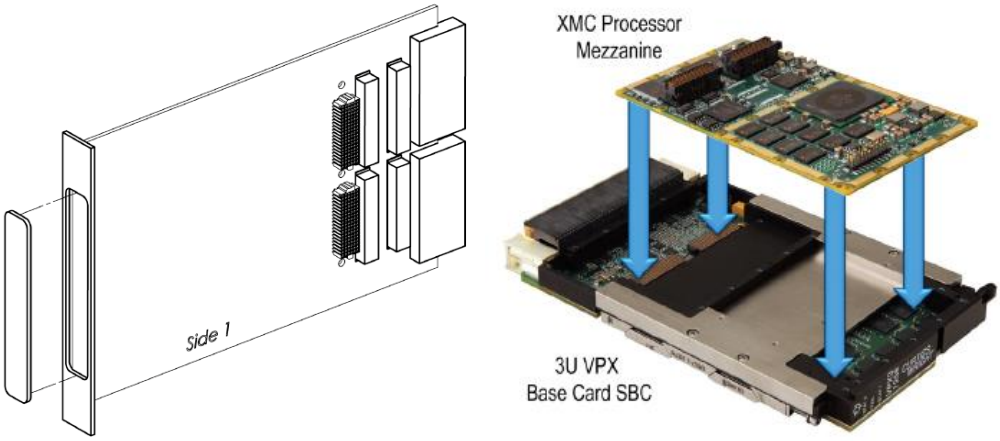


Figure 27. 3U VPX with XMC (Curtiss-Wright)

6U + 3 x FMC

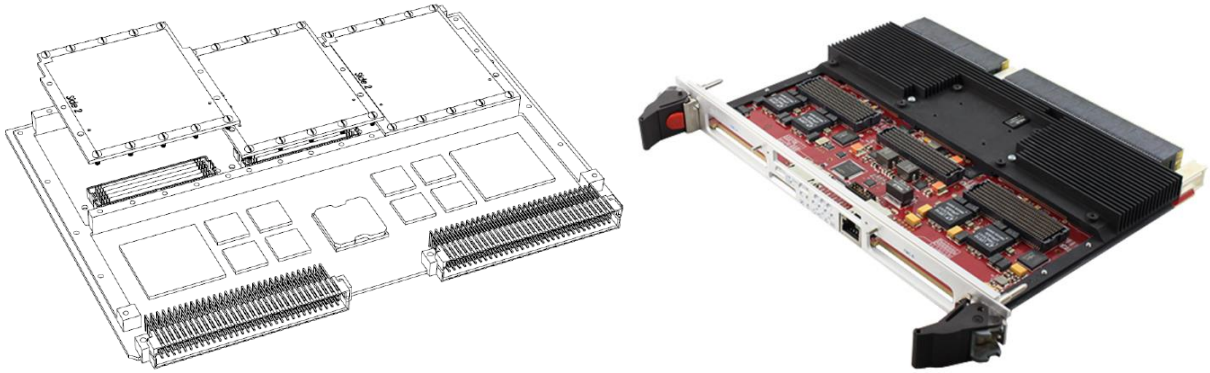


Figure 28. 6U VPX with Dual FMC+ and Single FMC (Abaco)

6U + 2 x XMC

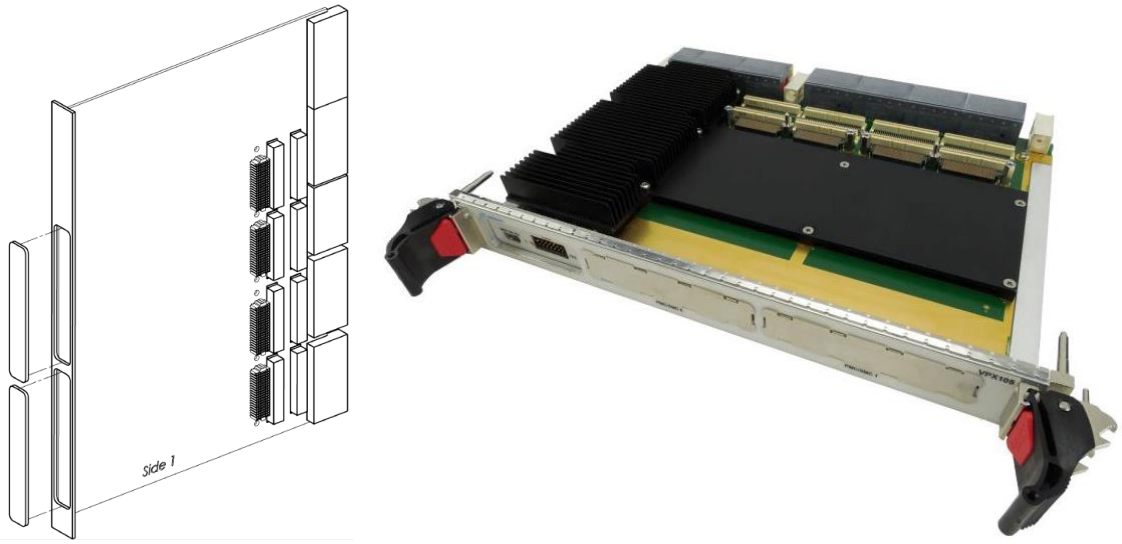


Figure 29. 6U VPX with Dual XMC (VadaTech)

NASA Form Factor Roadmap

SpaceVPX development within NASA is targeting 3U form factors cards with XMC daughtercards to minimize SWaP. As NASA transitions from cPCI to SpaceVPX systems, expectation is that mixed 3U/6U hybrid systems will become prevalent with cPCI systems (Figures 30 and 31).

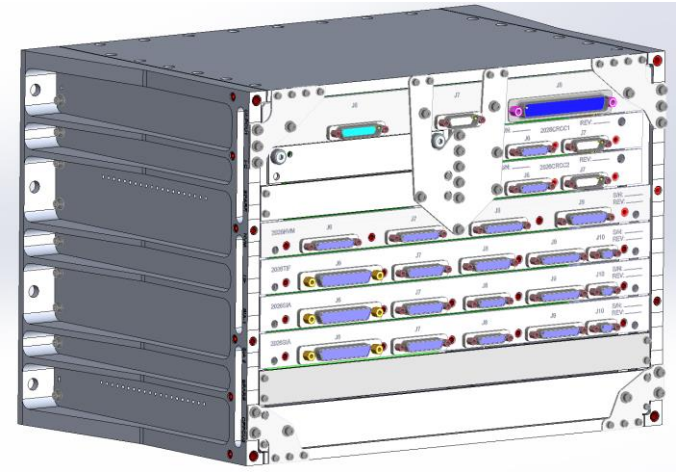


Figure 30. Hybrid 3U/6U cPCI Subsystem

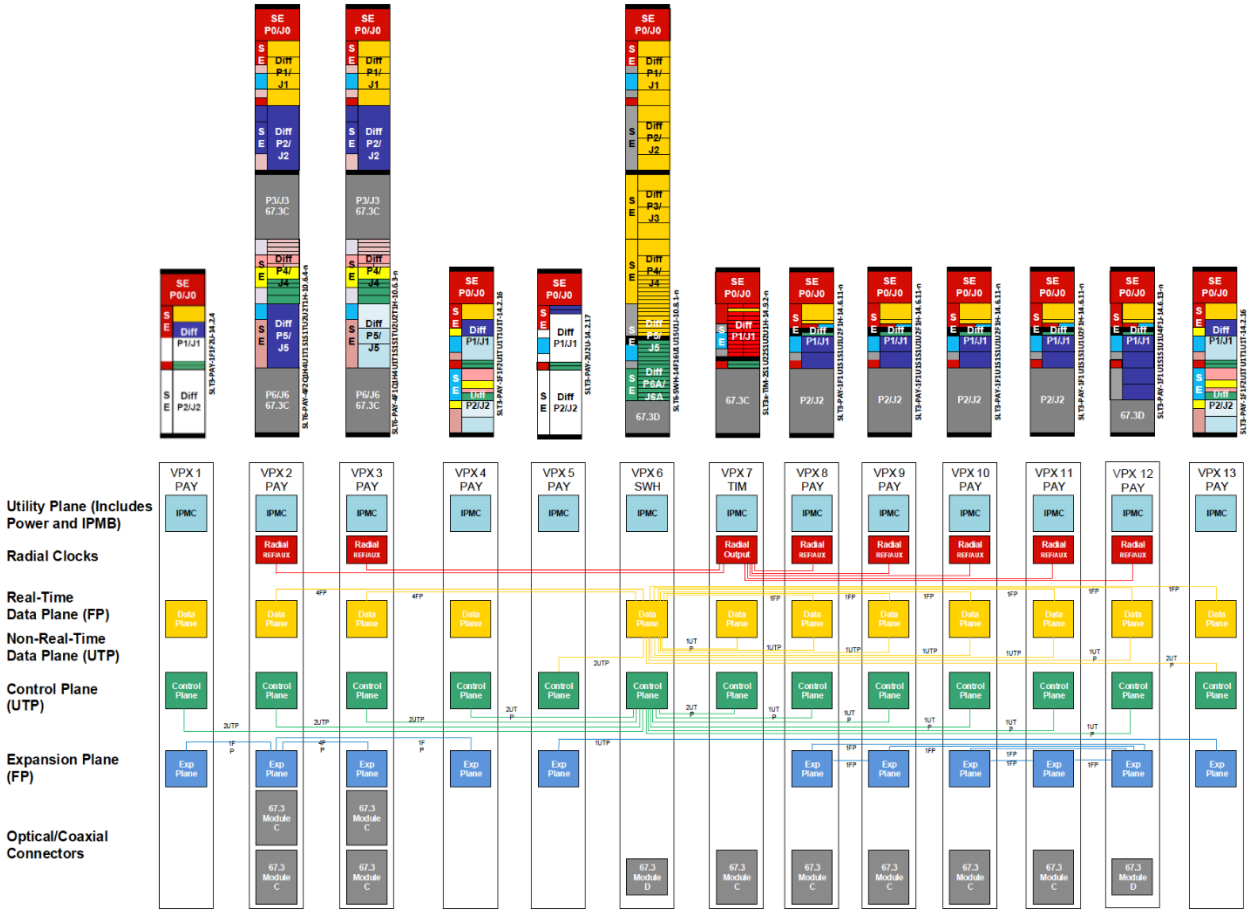
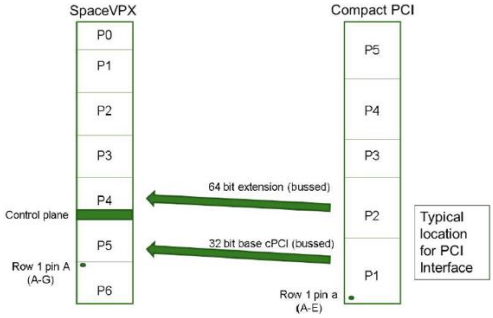


Figure 31. 3U/6U Hybrid Example (SOSA, Figure 67)

While cPCI support is not proposed in this assessment, it is recognized that systems comprised of SpaceVPX and cPCI cards may be implemented as NASA transitions to SpaceVPX. This will allow heritage cPCI cards to be leveraged on an as needed basis until the full spectrum of SpaceVPX modules are available.

SpaceVPX provides for bridge and peripheral SpaceVPX cards that can communicate with cPCI cards. This would be accomplished over SpaceVPX's expansion bus. A SpaceVPX to cPCI mapping is available in the DRAFT VITA-78.00-2015 rev 1.16 standard shown in Figure 32.



P5	G	F	E	D	C	B	A
1	PCI_REQ6_N	PCI_GNT6_N	GND	PCI_GNT1_N	GND	PCI_AD: 00	PCI_AD: 01
2	PCI_REQ1_N	PCI_AD: 02	GND	PCI_GNT2_N	GND	PCI_AD: 03	PCI_AD: 04
3	PCI_REQ2_N	PCI_AD: 05	GND	PCI_GNT3_N	GND	PCI_AD: 06	PCI_AD: 07
4	PCI_REQ3_N	M66EN	GND	PCI_CBE 0	GND	PCI_AD: 08	PCI_AD: 09
5	GND	PCI_CLK4	GND	PCI_REQ4_N	GND	PCI_CLK1	GND
6	PCI_AD: 10	PCI_AD: 11	GND	PCI_AD: 12	GND	PCI_AD: 13	PCI_AD: 14
7	PCI_PAR	PCI_CBE 1	GND	PCI_SERR_N	GND	PCI_PERR_N	PCI_AD: 15
8	PCI_TRDY_N	PCI_IRDY_N	GND	PCI_LOCK_N	GND	PCI_DEVSEL_N	PCI_STOP_N
9	PCI_FRAME_N	PCI_AD: 16	GND	PCI_CBE 2	GND	PCI_AD: 17	PCI_AD: 18
10	GND	PCI_CLK5	GND	PCI_REQ5_N	GND	PCI_CLK2	GND
11	PCI_AD: 19	PCI_AD: 20	GND	PCI_AD: 21	GND	PCI_AD: 22	PCI_AD: 23
12	GND	PCI_CLK6	GND	PCI_GNT4_N	GND	PCI_CLK3	PCI_UDB
13	IDSEL	PCI_AD: 24	GND	PCI_CBE 3	GND	PCI_AD: 25	PCI_AD: 26
14	PCI_AD: 27	PCI_AD: 28	GND	GND	GND	PCI_AD: 29	PCI_AD: 30
15	PCI_GNT_N	PCI_REQ_N	GND	PCI_CLK0	GND	PCI_RST_N	PCI_AD: 31
16	PCI_INTA	PCI_INTB	GND	PCI_GNT5_N	GND	PCI_INTC	PCI_INTD

cPCI line	
24	1, 17
23	1, 2
22	1, 3
21	
	1, 2, 3
19, 20	
17, 18, 19	
15, 16	
11, 15	
	2, 3, 15
9, 10	
	3, 20, 21
8, 9	
7	
5,6	
3	

Figure 32. cPCI to SpaceVPX mapping

Table 14 lists the findings derived from the form factor and daughtercard analysis.

Table 14. Form Factor and Daughtercard Findings

	Finding
F-30	Commercial industry (COTS) has more FMC than XMC offerings, with the application market for mezzanine/daughtercards being interface and high-speed analog.
F-31	NASA subsystems utilizing a backplane standard (i.e., VME, cPCI, SpaceVPX) will typically select a width (e.g., 3U, 6U, 9U) and customize the card length in a chassis to minimize SWAP-C.
F-32	The 3U 160mm module size is limiting for implementing processor boards with large processor packages and multiple memory banks. Project use cases at NASA (e.g., SpaceCube-V3 and SPLICE DLC) use the 3U 220mm SpaceVPX form factor.

7.3.4 Fault Tolerance

The assessment team explored the following questions related to SpaceVPX fault tolerance:

1. Are the mechanisms sufficient for use cases described in Appendix C?
2. Are they sufficient for mission critical systems (i.e., systems within Class A, human-rated, or high-profile missions)?
3. Are they sufficient for low SWaP constraints?

In fault tolerant systems, the two dominant considerations are availability and integrity. Loosely speaking, availability is the capacity to perform a function on demand, and integrity is the freedom from undetected malfunction. A fault tolerant system that simultaneously guarantees availability and integrity will perform its functions on demand in the presence of a specified number of faults. However, there are many systems that do not require simultaneous guarantees of availability and integrity.

Prior to developing a fault tolerance strategy, it is helpful to perform a preliminary analysis to determine potential adverse effects of: 1) a detected loss of function, and 2) a malfunction, including active misbehavior. This analysis should consider worst-case severity of potential adverse effects, with consideration of other relevant factors (e.g., time-to-criticality). Different mission requirements will give rise to different fault tolerance strategies. For some avionics functions, a loss of function or a malfunction could result in a catastrophic loss event. This generally leads to stringent real-time fault tolerance requirements, including demonstration that there are no single-point failures. For others, the fault tolerance requirements are not as stringent. It is often possible to tolerate a temporarily loss of function or malfunction. Of the Appendix C use cases with fault tolerance requirements, only the EDL (e.g., SPLICE) functions have a possibility of a catastrophic failure resulting from an integrity violation. With this exception, all that remains for question 1 is to determine if the SpaceVPX fault tolerance mechanisms are sufficient for applications that can withstand temporary integrity and availability violations. The scenario for EDL will be addressed in the context of question 2.

As listed in VITA-78 Section 1.7, SpaceVPX includes the following features to support fault tolerant systems design:

- Single-board shut down, sleep, or restart.
- Dual-redundant power distribution
- Dual-redundant utility signal distribution

- Card-level serial management (i.e., point-point interfaces to manage individual cards)
- Card-level power control
- Fault tolerant power supply select
- Fault tolerant system controller signal selection
- Dual-redundant data and control planes (i.e., point-to-point cross strapped)
- Each module (PIC) is a managed FRU

The notional fault tolerance strategy for SpaceVPX is dual redundancy in an active/standby configuration. For this strategy to be appropriate, there needs to be sufficient time to detect and isolate fault effects and to successfully reconfigure before a loss event occurs (i.e., strategy is suitable when temporary availability and integrity violations are tolerable). Generally, it is easier to recover from an availability than an integrity violation. Thus, it is common to use additional strategies (e.g., algebraic encoding, in-line integrity checks) to decrease the probability of integrity violations within this architecture.

Within SpaceVPX, the module is the defined unit of failure. Modules are assumed to fail independently. However, the standard does not explicitly require engineering analysis to support this assumption. The degree of analysis that is sufficient will be based on the mission safety requirements.

The SpaceUM modules provide the capability to manage the redundancy within a SpaceVPX chassis. The standard supports power cycling and resetting modules based on Fault-Detection, Isolation and Recovery (FDIR) results. The mechanisms within SpaceVPX that support FDIR and redundancy management are effective building blocks to support all NASA use cases defined in Appendix C.

For question 2, whether SpaceVPX is suitable for mission critical systems, there are key differences between fault tolerance for human-rated systems versus unmanned or robotic missions. Fault tolerance for human-safety-critical systems includes increased scrutiny for potential common cause or single-point failures. This involves analysis of a range of implementation characteristics for common failures due to spatial proximity, logic errors in redundancy management, and greater focus on physical isolation between independent fault containment regions. In general, this is a detailed focus and analysis to substantiate failure independence requirements. Human-safety-critical systems trigger scrutiny of rare failure modes that are not applicable for robotic or uncrewed missions.

Mission-critical system requirements generally include stricter constraints on availability and integrity. To guarantee integrity with potential temporary loss of availability, it is common to use a self-checking pair as a fault tolerance building block. This is possible in SpaceVPX with the addition of specific systems software to manage the data exchange and comparisons needed to realize a self-checking pair. If the system requires integrity and availability for defined intervals (e.g., EDL), then it may be possible to achieve this within a single SpaceVPX chassis. This could be achieved by configuring a self-checking pair in each side of a SpaceVPX chassis and establishing a dual self-checking pair configuration. However, additional analysis will be required to ensure that there is sufficient isolation and independence of failure between the

redundant modules[1]. Furthermore, analysis will be required to ensure that a single power supply module has sufficient capacity to simultaneously power both sides of the chassis.

The dual redundant approach of SpaceVPX makes implementation of voting systems for masking fault tolerance challenging. For this reason, the assessment team believe the dual-dual pattern discussed to be more appropriate for higher criticality applications within SpaceVPX.

Another alternative is to engineer additional high integrity mechanisms within a single module. The implementation of a self-checking pair within a module is one example. If the fault coverage within a module is sufficiently high, then it may be feasible to meet mission reliability targets. In summary, it may be possible to use SpaceVPX for safety-critical systems with a requirement for single fault tolerance. However, such applications will require additional engineering analysis that is outside the scope of the SpaceVPX standard.

Given that the SpaceVPX chassis is built around dual redundancy, there will be certain combinations of two faults that cannot be tolerated within a single SpaceVPX chassis. As a result, systems requiring tolerance to multiple faults would necessarily involve multiple SpaceVPX chassis augmented with appropriate system level analysis to substantiate fault tolerance claims.

VITA-78 Section 1.7 includes the typical SpaceVPX reliability model diagram, included as Figure 33. Since the SpaceUM controls individual power and management signal distribution to the modules, SpaceUM failures can dominate the cut sets for fault tree analysis. As shown in Figure B.1 in Appendix B, a SpaceUM failure results in loss of redundancy.

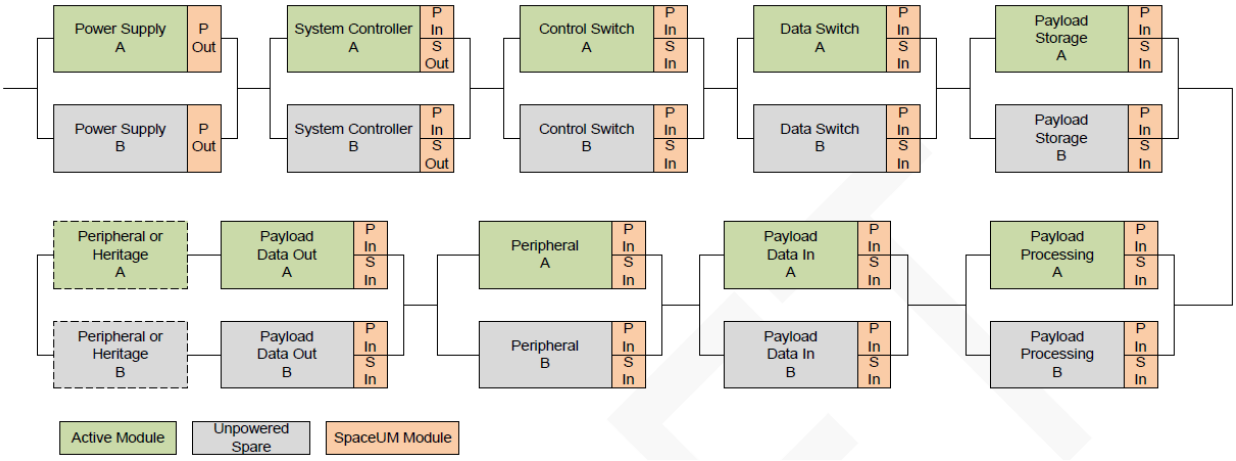


Figure 33. Typical SpaceVPX Reliability Model Diagram

For question 3, suitability for missions with extremely tight constraints on SWaP, with the current trends in semiconductor devices toward systems on chips (SoC), it is common to have several redundancy strategies available within a single device. These strategies serve to enhance the integrity of these devices such that for almost all applications there are no externally visible malfunctions caused by random failures (i.e., the only mechanism for malfunction would be due to errors in requirements or software implementation). It is worth noting that on-chip redundancy mechanisms are not in the scope of the SpaceVPX standard. It is possible that for

[1] B. Hall and K. Driscoll, Distributed System Design Checklist, NASA/CR–2014-218504

some missions, the desired reliability can be met without invoking the explicit fault tolerance mechanisms defined in SpaceVPX.

Table 15 lists the findings derived from the fault tolerance analysis.

Table 15. Fault Tolerance Finding

	Finding
F-33	Since the SpaceUM controls individual power and management signal distribution to the modules, SpaceUM failures can dominate the cut sets for fault tree analysis.
F-34	The mechanisms within SpaceVPX that support FDIR and redundancy management are effective building blocks to support all NASA use cases.

7.4 Engagement with Outside Organizations

Throughout this assessment, there have been engagements with outside organizations for a variety of purposes. First, other government agencies were engaged to determine their interest in SpaceVPX and gain insight into how they plan to implement the standard. The assessment team considered other standards organizations to assess the suitability of those standards to include in the NASA SpaceVPX recommendations, or to incorporate the NASA recommendations into their standards. Lastly, as discussed, industry was surveyed to assess their support for SpaceVPX within their product portfolios.

The AFRL briefed the assessment team on their Heterogeneous On-Orbit Processing Engine (HOPE) development. HOPE is hybrid SpaceVPX/OpenVPX architecture that will be flown as an experimental payload in LEO. The objective of the HOPE experiment is to leverage the high performance of COTS OpenVPX boards for spaceflight applications. Central to the HOPE architecture is a radiation hardened SpaceVPX SBC, a radiation hardened FPGA router, and a 'smart backplane' that provides power monitoring and watchdog functions for the OpenVPX boards. Collectively, these provide a degree of radiation mitigation for the COTS boards.

The objectives and plans for the NESC SpaceVPX interoperability assessment were presented at the RHET conference. This conference was held in November 2021 where this presentation garnered interest from other government agencies and government-sponsored organizations.

Following up on an initial contact at the RHET conference, Sandia National Laboratories (SNL) briefed the assessment team on the development of their Delphi Heterogeneous Cognitive Computing Platform. Delphi is a computing platform leveraging the Xilinx Versal device, which has resources to accelerate machine learning applications. SNL is planning to implement Delphi as a 6U module, based on internal analysis concluding that 6U systems are optimal for SWaP. SNL is in the early development stages, and are seeking input and guidance on how to implement Delphi as a SpaceVPX module.

The RHET presentation spawned interest in SMEs from other agencies, which has led to an ongoing engagement with the avionics community within these agencies. In general, these agencies have expressed interest in advancing SpaceVPX use within their systems and, and shared NASA's concerns regarding SpaceVPX interoperability issues. However, further discussions are needed to assess their interest in adopting the NESC recommendations of this assessment.

The assessment team met with the SPC and was briefed on their standards development efforts. The consortium is developing a variant of the PMBus standards that could be incorporated into

SpaceVPX for fine grained control and monitoring of power circuitry throughout the SpaceVPX chassis. This increased control can help enable greater system-level autonomy. Once the PMBus standard is complete, further work is needed to determine how it can be implemented on the I2C bus within the utility plane.

There has been indirect engagement with the SOSA™ Consortium, which was founded to promote MOSA within government sensor systems. This Consortium is a voluntary, consensus-based member of The Open Group, which is a vendor-neutral technology standards organization. The SOSA™ Consortium is a government, industry, and academic alliance developing an open technical standard for sensors and Command, Control, Communication, Computers, Cyber, Intelligence, Surveillance and Reconnaissance (C5ISR) systems. The consortium provides a vendor-neutral forum for members to work together to harmonize, align, and create open standards to facilitate the development of agile, interoperable, and affordable sensors. The indirect engagement with the consortium has been facilitated by the ongoing participation by a member of the assessment team in the SOSA™ Consortium as part of a separately funded effort. It should be noted this Consortium does not focus on spaceflight systems. There has been some historical interest to extend the Consortium into this domain, but this would require active participation by NASA and other spacefaring agencies.

While interactions with outside organizations have been informative to this assessment and the resulting NESC recommendations, further engagement and workshops are needed with other government agencies, the SOSA™ Consortium, and VITA to standardize the recommendations of this assessment and incorporate them in a subversion of VITA-78 as a ‘dot spec’.

Table 16 lists the finding derived from engagement with other organizations.

Table 16. External Engagement Finding

	Finding
F-35	There is a recognition within other government agencies that SpaceVPX as specified in VITA-78 presents interoperability challenges, and interest in collaborating to refine the specification to address those challenges.

8.0 Findings, Observations and NESC Recommendations

The findings, observations, and NESC recommendations are a product of the analysis conducted in this assessment.

8.1 Findings

Table 17 provides a compiled list of the findings generated during this assessment. Where appropriate, the findings include traceability to the recommendations that they support. The 'R' prefix corresponds to the general recommendations listed in this section.

Table 17. Findings

	Finding	Traceability
F-1	While low SWaP is generally needed, 3U and 6U sizes were seen in the NASA use cases.	RT-4
F-2	Module-to-module bandwidth of 10 Gbps envelopes the needs of NASA use cases.	RT-3
F-3	A SpaceWire control plane is needed by the majority of NASA use cases.	RT-3
F-4	Low-rate interfaces (below control plane bandwidth) are needed to support simple modules without FPGAs.	RT-3
F-5	NASA use cases include both single string and redundant systems.	RT-1
F-6	Due to SWaP considerations, some of the NASA use cases prefer a power management and distribution approach that differs from SpaceVPX.	R-4
F-7	Industry lacks consensus on module interconnect and form factors, and this lack of consensus is limiting investment in product development.	R-3
F-8	Industry is developing some 'SpaceVPX modules' that are not fully compliant with VITA-78.	R-3
F-9	Many industry SpaceVPX modules utilize User Defined Space, which can hinder interoperability.	R-4
F-10	The majority of current industry SpaceVPX modules utilize SRIO for the data plane and SpaceWire for the control plane.	RT-3
F-11	There is a lack of consensus among industry 'integrators' of SpaceVPX systems on the utility of cross strapped SpaceVPX implementations versus block redundancy of single-string SpaceVPX systems.	RT-1
F-12	Product survey suggests there is a market for SpaceVPX modules in 3U and 6U form factors.	RT-4
F-13	The needs of most 3U use cases cannot be met with the 2-output SpaceUM (SLT3-SUM-2S3V3A1B1R1M4C-14.7.1) but can be met with the 5-output SpaceUM (SLT3-SUM-5S1V3A1R1M3C -14.7.2).	RT-2
F-14	The SpaceVPX standard power management and distribution approach supports interoperability, but constraints are needed on main bus voltage for the 5-output 3U SpaceUM.	RT-2
F-15	The needs of 6U use cases can be met with the standard 8-output SpaceUM (SLT6-SUM-8S3V3A1B1R1M4C-10.8.1).	RT-2
F-16	While IPMI and DAP are specified in the SpaceVPX standard, a development SPC PMBus specification may offer system level features (i.e., controlled from within or outside of the SpaceVPX chassis) that can enable higher autonomy levels.	R-4

F-17	VBAT is included within VITA-78 for systems with batteries within the chassis, but is not applicable to NASA systems.	RT-8
F-18	The feasibility of implementing a 3U Power Supply-Switch module that can be achieved with the required number of power converters, switches, and control circuitry is uncertain.	
F-19	In assessing the current VITA-78 data plane standards, SpaceFibre is a sole source solution with limited spaceflight usage, and the SRIO standard lacks industry support.	RT-3
F-20	The TSN standard, which leverages Ethernet, has broad industry engagement and support.	RT-3
F-21	The HPSC Project currently does not require native support for SRIO, SpaceFibre, or TTE, although these can be provided at the board level using external circuitry.	RT-3
F-22	The I2C bus provided within the utility plane is capable of handling PMBus functions within the SpaceVPX chassis.	R-4
F-23	12.5 Gbps SERDES signals can be supported with a trace length of 13.5 inches, two SpaceVPX connectors, and a 22-layer printed wiring board (PWB) using Arlon material.	
F-24	While the VITA-78 standard allows for user defined signals to provide flexibility, the use of these signals can hinder interoperability.	RT-3
F-25	There is need to provide industry standard JESD204 interfaces to high bandwidth ADCs and DACs in excess of 1 gigasample per second (GSPS).	
F-26	There is need for a low-rate I2C interface (below SpaceWire bandwidth) to provide connectivity to simple modules that can be implemented without an FPGA.	
F-27	While system management is provided via IPMI or DAP on the System Management Bus, and JTAG is included to support testing, SpaceVPX does not define a system-level test and debug scheme.	RT-3
F-28	Industry trends are to combine control and data flow traffic on a single high-bandwidth onboard network. Within the aerospace community, Star Dundee (the current supplier of SpaceWire and SpaceFibre IP) recommends combining control and data plane functions on SpaceFibre links.	R-4
F-29	There are four vendors of SpaceVPX connectors, but only two offer connectors that can intermate.	RT-7
F-30	Commercial industry (COTS) has more FMC than XMC offerings, with the application market for mezzanine/daughtercards being interface and high-speed analog.	
F-31	NASA subsystems utilizing a backplane standard (VME, cPCI, SpaceVPX) will typically select a width (3U, 6U, 9U) and customize the length of all cards in a chassis to minimize SWAP-C. The chassis for these subsystems are a custom design.	RT-4
F-32	The 3U 160mm module size is very limiting for implementing processor boards with large processor packages and multiple banks of memory. Current project use cases at NASA (SpaceCube-V3 and SPLICE DLC) are using the 3U 220mm SpaceVPX form factor.	RT-4
F-33	Since the SpaceUM controls individual power and management signal distribution to the modules, SpaceUM failures can dominate the cut sets for fault tree analysis.	R-2
F-34	The mechanisms within SpaceVPX that support FDIR and redundancy management are effective building blocks to support all NASA use cases.	

F-35	There is a recognition within other government agencies that SpaceVPX as specified in VITA-78 presents interoperability challenges, and interest in collaborating to refine the specification to address those challenges.	R-3

8.2 Observations

Table 18 provides the observations from this assessment.

Table 18. Observations

	Observation
O-1	There is no standardized approach or best practice for FPGA programming and management based on a firm understanding of the current and emerging FPGA configuration options.
O-2	There are potential JTAG security vulnerabilities to NASA missions that have not been fully assessed.
O-3	During the SpaceVPX connector analysis, potential issues were raised regarding the attachment of SpaceVPX connectors to printed wiring boards.

8.3 NESC Recommendations

The recommendations of this assessment are listed in Table 19 with a cross-reference to the supporting findings and are directed to SMD, STMD and the space avionics community.

Table 19. NESC Recommendations

	Recommendation	Traceability
R-1	NASA projects and programs should standardize the use of SpaceVPX for NASA avionics systems as defined in Table 20.	
R-2	NESC and STMD should develop a NASA standard SpaceUM module architecture and reliability model.	F-33
R-3	NESC and STMD should engage with industry, other government agencies, and the SOSA™ Consortium on revision to VITA-78, and refine the module definition and interoperability (see Appendix B) and daughtercard use.	F-7, F-8, F-9, F-35
R-4	NESC and STMD should conduct a follow-on study, in collaboration with other government agencies, for a next generation avionics architecture (i.e., beyond SpaceVPX), addressing: (a) simplified interconnect with data streams combined into fewer planes, (b) alternative power management and distribution options, (c) possible adoption of PMBus, (d) support for a broader set of fault tolerance methodologies, (e) hierarchical system-level self-test and debug architectures, and (f) module-level interchangeability and reuse across NASA systems.	F-6, F-16, F-27, F-28

Table 20 provides NESC recommendations detailing the application of the SpaceVPX standard (VITA-78) for NASA applications. These recommendations include subtractions from the VITA-78 standard for options and features are disallowed, and extensions to VITA-78 for new features.

Table 20. Proposed NASA SpaceVPX Specification

	Proposed NASA SpaceVPX Specification	Traceability
	General	
RT-1	Support dual redundant and single-string SpaceVPX systems.	F-5, F-12
	Power distribution and management	
RT-2	Consider preference to the 5-output SpaceUM (SLT3-SUM-5S1V3A1R1M3C-14.7.2) for 3U implementations with a 5V main power voltage. Consider preference to the 8-output SpaceUM (SLT6-SUM-8S3V3A1B1R1M4C-10.8.1) for 6U implementations with +12, +5, and +3.3 main supply voltages.	F-13, F-14, F-15
	Interconnect	

RT-3	• Data Plane – Support for Ethernet 10GBASE-KR as specified in IEEE 802.3ap with support for TSN as specified in IEEE 802.1AX, CB, AS, Qbv, Qav, Qci, Qcc, and 802.1Q clauses 8.6.5.1 and 8.6.8.2
	• Control Plane - SpaceWire as defined in ECSS-E-ST-50-12C
	• Expansion Plane – JESD204C
	• Expansion Plane – Support for PCIe Gen 3.1
	• Utility Plane – IPMI and DAP as specified in VITA-78
	• User Defined signals with the requirement that they are user programmable
	  • SERDES.- 1600mV peak-to-peak AC-coupled differential signaling; 8b/10b encoding; data rates of 1.25 Gbps, 2.5 Gbps, 3.125 Gbps, 5 Gbps, 6.25 Gbps, and 10 Gbps (note that some modules may not support all of these rates)
	  • Single ended - 2.5V LVCMOS signaling
	• Low-Rate Interconnect – I2C
	• JTAG
	  • Provide pin on a front panel to disable JTAG for flight.
		F-2, F-3, F-4, F-11, F-19, F-20, F-21, F-22, F-24, F-25, F-26, F-27

	Form Factors and Daughtercards	
RT-4	Support 3U and 6U – 220mm form factors. Support for XMC and/or FMC daughtercards on SpaceVPX FPGA-based modules. Combined 3U/6U chassis as needed.	F-1, F-13, F-31, F-32
	Fault tolerance	
RT-5	Adopt fault tolerance methodologies as defined in VITA-78.	F-33
	Backplanes and Chassis	
RT-6	Use VITA-78 identified passive backplanes.	F-31
	Connectors	
RT-7	Utilize SpaceVPX module and backplane that comply with VITA-46.	F-29
	VITA-78 features not be used to ensure future interoperability	
RT-8	• Specified chassis and backplane profiles. • SRIO on data plane (can be implemented with User Defined SERDES). • SpaceFibre on data plane (can be implemented with User Defined SERDES). • System Controller interfacing to 4 SpaceUM modules (recommendation is 2). • Support for heritage cPCI modules. • Support for 2-output 3U SpaceUM (SLT3-SUM-2S3V3A1B1R1M4C-14.7.1). • Support for VBAT voltage. • System management discrete input and output interfaces. • Full latitude on user defined signal usage.	F-17

The following features are proposed that are not in VITA-78.

- Explicit support for single-string systems
- Using Ethernet/TSN for data plane
- Use of PCIe 3.1 for expansion plane
- JESD-204C support for high bandwidth digitizers
- Constraints on user defined signals
- Explicit daughtercard support

9.0 Alternate Technical Opinion(s)

No alternate technical opinions were identified during the course of this assessment by the NESC assessment team or the NESC Review Board (NRB).

10.0 Other Deliverables

No unique hardware, software, or data packages, other than those contained in this report, were disseminated to other parties outside this assessment.

11.0 Recommendations for the NASA Lessons Learned Database

There are no specific lessons learned for the NASA database.

12.0 Recommendations for NASA Standards, Specifications, Handbooks, and Procedures

A future dot-spec for the VITA-78 SpaceVPX standard may be appropriate but, at this time, further study is required.

13.0 Definition of Terms

Finding	A relevant factual conclusion and/or issue that is within the assessment scope and that the team has rigorously based on data from their independent analyses, tests, inspections, and/or reviews of technical documentation.
Lesson Learned	Knowledge, understanding, or conclusive insight gained by experience that may benefit other current or future NASA programs and projects. The experience may be positive, such as a successful test or mission, or negative, as in a mishap or failure.
Observation	A noteworthy fact, issue, and/or risk, which is not directly within the assessment scope, but could generate a separate issue or concern if not addressed. Alternatively, an observation can be a positive acknowledgement of a Center/Program/Project/Organization's operational structure, tools, and/or support.
Problem	The subject of the independent technical assessment.
Recommendation	A proposed measurable stakeholder action directly supported by specific Finding(s) and/or Observation(s) that will correct or mitigate an identified issue or risk.

14.0 Acronyms and Nomenclature List

ADC	Analog-to-Digital-Converter
AFRL	Air Force Research Laboratory
ANSI	American National Standards Institute
ATCA®	AdvancedTCA®
C&DH	Command and Data Handling
C5ISR	Command, Control, Communication, Computers, Cyber, Intelligence, Surveillance and Reconnaissance
CAN	Controller Area Network
CE	Compute Element
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial-Off-The-Shelf
cPCI	Compact PCI
CPU	Central Processing Unit
CSR	Concept Study Report
DAC	Digital-to-Analog-Converter
DAP	Direct Access Protocol
DLC	Descent and Landing Computer
DoD	Department of Defense
DTN	Delay Tolerant Network
EDL	Entry Descent and Landing
EMI	Electromagnetic Interference
EMIT	Earth Surface Mineral Dust Source Investigation
ESA	European Space Agency
ESPA	Evolved Secondary Payload Adapter
ETU	Engineering Test Unit
EVI-4	Earth Ventures-Instrument
FDIR	Fault-Detection, Fault-Isolation and Recovery
FMC	FPGA Mezzanine Card
FP	Fat Pipe
FPGA	Field-Programmable Gate Array
FRU	Field Replaceable Unit
gbps	One Billion Bits Per Second
GCU	Gateway Control Unit
GEO	Geosynchronous Orbit
GNC	Guidance, Navigation, and Control
GOPS	Giga-Operations Per Second
GPU	Graphics Processing Unit
GSPS	Gigasamples Per Second
GSFC	Goddard Space Flight Center
GTU	Ground Test Unit
HALO	Habitation and Logistics Outpost
HD	Hazard Detection
HEO	Highly Elliptical Orbit
HOPE	Heterogeneous On-Orbit Processing Engine
HPC	High Pin Count

HPSC	High Performance Spaceflight Computing
HySPIRI	Hyperspectral Infrared Imager
I/F	Interface
I/O	Input/Output
IC	Integrated Circuit
IP	Internet Protocol
IPM	Intelligent Payload Module
IPMC	IPMI Controller
IPMI	Intelligent Platform Management Interface
ISS	International Space Station
JPL	Jet Propulsion Laboratory
JSC	Johnson Space Center
kbps	Kilobytes Per Second
LaRC	Langley Research Center
LCRD	Laser Communication Relay Demonstration
LEO	low-Earth-orbit
LPC	Low Pin Count
LTV	Lunar Terrain Vehicle
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
MEB	Main Electronics Box
MEDA	Mars Environmental Dynamics Analyzer
MEO	Medium Earth Orbit
MOSA	Modular Open Systems Approach
MOXIE	Mars Oxygen In-Situ Resource Utilization Experiment
MSM	Module System Manager
NESC	NASA Engineering and Safety Center
NGSIS	Next Generation Space Interconnect Standard
NRB	NESC Review Board
NRE	Non Recurring Engineering
OM	Optical Module
OSAM	On-orbit Servicing, Assembly, and Manufacturing
PIC	Plug-In Card
PIXL	Planetary Instrument for X-ray Lithochemistry
PMBus	Power Management Bus
PPE	Power and Propulsion Element
PWB	Printed Wiring Board
QoS	Quality of Service
REASON	Radar for Europa Assessment and Sounding: Ocean to Near-surface
RF	Radio Frequency
RHET	2021 Radiation Hardened Electronics Technology
RIMFAX	Radar Imager for Mars' Subsurface Experiment
RMAP	Remote Memory Access Protocol
RTM	Rear Transition Module
SAR	Synthetic Aperture Radar
SBC	Single Board Computer

SDR	Software Defined Radio
SFA	Study Focus Area
SHERLOC	Scanning Habitable Environments with Raman & Luminescence for Organics and Chemicals
SMD	Science Mission Directorate
SME	Subject Matter Expert
SNL	Sandia National Laboratories
SoC	Systems on Chip
SOSA™	Sensor Open Systems Architecture
SpaceUM	Space Utility Management
SPC	Space Power Consortium
SPLICE	Safe and Precise Landing – Integrated Capabilities Evolution
SRIO	Serial Rapid IO
SRP	Stream Reservation Protocol
SSDR	Solid State Data Recorder
SSR	Solid State Recorder
SSRI	Spacecraft Solid-State Recorder
STALO	Stable Local Oscillator
STMD	Space Technology Mission Directorate
SWaP	Size, Weight and Power
SWaP-C	Size, Weight, Power and Cost
TIR	Thermal Infrared
TP	Thin Pipe
TRN	Terrain Relative Navigation
TSN	Time Sensitive Networking
TSSM	Titan Saturn System Mission
TSU	TTE Switch Unit
TTE	Time Triggered Ethernet
U	Unit
UTP	Ultra Thin Pipe
UV	Ultraviolet
V	Volt
VCU	Vehicle Control Unit
VITA	VMEbus International Trade Association
VMEbus	VersaModular Eurocard bus
VSM	Vehicle System Manager
VSWIR	Visible-To-Short-Wave Infrared
VV	Visiting Vehicle

15.0 References

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Appendices

Appendix A. Candidate Module Definitions
Appendix B. Example Systems
Appendix C. Use Cases
Appendix D. Product Survey Spreadsheet

Appendix A. Candidate Module Definitions

While common module standardization is not required for interoperability, they are a necessary step toward achieving interchangeability (which is beyond the scope of this assessment). This appendix identifies modules types and suggests candidate profiles to provide starting points for further studies to standardize module profiles. Table A-1 provides a mapping of these module types to the use cases.

Table A-1. Module Type to Use Case Mapping

	SBC	Switch	Low Density FPGA	High Density FPGA	Storage	Digitizer
A-Team	A Team – HPSC, SBC A, and SBC B	A Team – Network Switch		A Team – Imaging PIC A & PIC B		
Comm Relay		Comm Relay – Network Switch		Comm Relay – Digital Modem	Comm Relay – Data Storage	
VSM Fault	VSM Fault– HPSC A & HPSC B					
HyspIRI	HyspIRI – Adv Proc PIC A and Adv Proc PIC B			HyspIRI – I/O PIC	HyspIRI - SSDR	
REASON				REASON – Payload and Proc/FPGA	REASON - SSDR	Digital-to-Analog Converter
Low/ Med	Low/Med Rate – Processor Card		Low/Med Rate – Analog Input, Mechanism Control, and Power Output	Low/Med Rate – Detector Readout	Low/Med Rate – Data Storage	
OSAM	OSAM - SBC			OSAM – HW Accel 1, HW Accel 2, and HW Accel 3.	OSAM – Bulk Memory (2)	
Robonaut	Robonaut – HPSC 1, HPSC 2, HPSC 3, SBC A, and SBC B	Robonaut – Network Switch		Robonaut– TLM/CMD A & B NAV A & B	Robonaut - SSDR	
Robotic Rover						
LTV						
Small Sat	Small Sat - SBC		Smallsat Actuator	Small Satellite – TLM/CMD		
SPLICE	SPLICE – MPSoC SBC Primary and MPSoC SBC Backup			SPLICE – FPGA PIC	SPLICE -SSDR	

Within this assessment, module definitions are approached differently between 3U and 6U modules. With the limited area and pin resources of 3U modules, there is advantage to defining an increased number of modules mapped to specific functions. As 6U modules relax the resource constraints of 3U modules, it is possible to combine functions onto modules. This leads to a fewer needed module types.

3U Modules

For each of these module types, a set of proposed interconnect for 3U modules is provided in Table A-2. The recommendations reflect the needs identified in the use cases. It should be noted that the SBC is the most stressing case for accommodating the needed interconnect onto the available 3U connector space.

Table A-2. Interconnect Allocations for 3U Modules

Slot Profile Category	Ethernet (Data Plane)	PCIe (Expansion Plane)	JESD204B (Expansion Plane)	SpaceWire (Control Plane)	I2C (Other)	Custom SERDES (Other)	SpaceUM Control (Other)
Low Density FPGA				2 Ports – 8 Differential Pairs	1 Port – 2 Single Ended		
SBC (HPSC)	4, 2 Lane, Ports (TSN/Ethernet) – 16 Differential Pairs	2 x4 Ports - 16 Differential Pairs		4 Ports – 16 Differential Pairs	2 Port – 4 Single Ended	8 Differential Pairs	8 Differential Pairs
Switch	6, 4 Lane Ports TSN/Ethernet – 48 Differential Pairs			4 Ports – 16 Differential Pairs			
High Density FPGA	4, 2 Lane, Ports (TSN/Ethernet) – 16 Differential Pairs		32 Differential Pairs	2 Ports – 8 Differential Pairs			8 Differential Pairs
Storage	4, 2 Lane Ports (TSN/Ethernet) – 16 Differential Pairs	4, x4 Ports - 32 Differential Pairs		2 Ports – 8 Differential Pairs			
Digitizer			32 Differential Pairs	2 Ports – 8 Differential Pairs	1 Port – 2 Single Ended		

SBC Module – The primary SpaceVPX interconnect analysis focused on the 3U SBC module (specifically an HPSC-based SBC) that can assume the role of System Controller. This was the stressing case for implementing the necessary interconnect on a 3U connector. It is assumed that an HPSC-based SBC would include a companion FPGA that can provide User Defined SERDES signals. It should be noted that while the definition of the SBC interconnect allocations are based on HPSC, other SBC module profiles could be defined with different interconnect allocations. Figure A-1 depicts an existing VITA-78 profile that provides a potential starting point for an SBC module profile, and a notional new profile that accommodates the proposed interconnect. Note that a portion of the existing planes would be repurposed as a PCIe expansion plane.

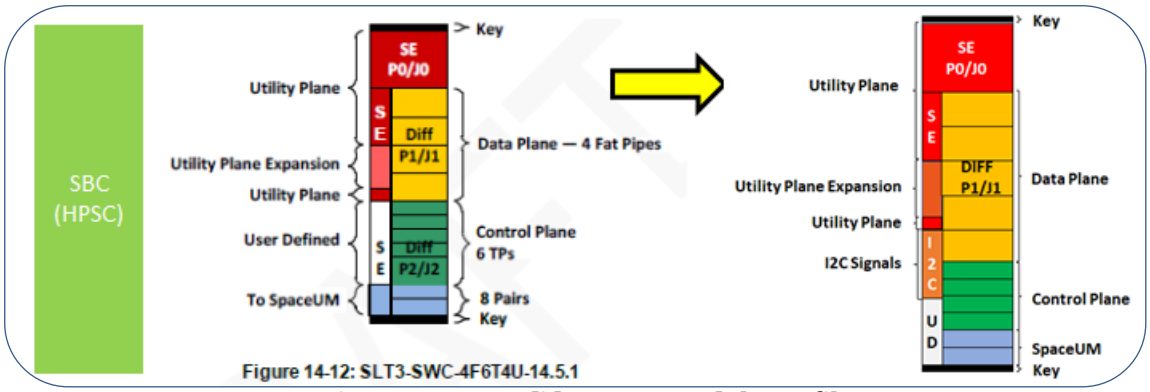

Figure A-1. Candidate SBC Module Profile

FPGA Module – An FPGA module is common to most SpaceVPX implementations. Front panel interfaces can be provided on these modules via daughtercards. With the flexibility of the FPGA, combined with the ability to add application specific daughtercards, an FPGA module has the flexibility to implement several common avionics functions, including uplink/downlink formatting, motor/actuator control, sensor data ingest and processing, and network switches. It should be noted that an FPGA module with a processor implemented within the FPGA can be

used in the SBC and system controller functions. Figure A-2 provides two examples of FPGA modules tailored for specific functions.

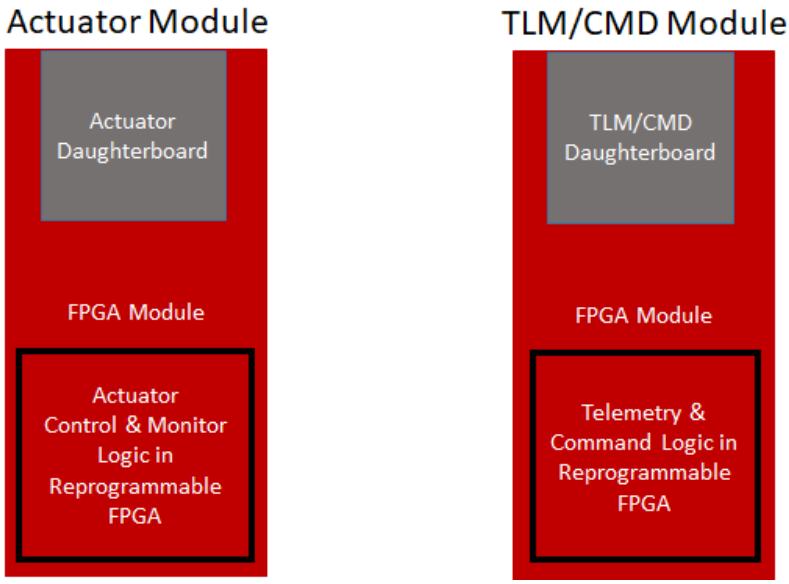

Figure A-2. Functions Implemented with FPGA Modules

FPGA modules can be further classified into high density and low density modules. For the purpose of this assessment, high density modules are those that include FPGAs that support SERDES interfaces (e.g., Ethernet and PCIe). These modules are assumed to perform functions including onboard processing acceleration and high bandwidth sensor interfacing. These modules may serve as SBCs, with processors implemented as IP cores within the FPGA. To allow their use in this role, the high density FPGA modules include SpaceUM control signals on their backplane connectors. Low density modules are assumed to have FPGAs that do not provide SERDES interfaces and rely on SpaceWire for interconnect. These modules are assumed to perform functions including low bandwidth sensor interconnect and management of motors and actuators. Figure A-3 and Figure A-4 provides candidate VITA-78 profiles that can be used as starting points for high density and low density FPGA module profiles.

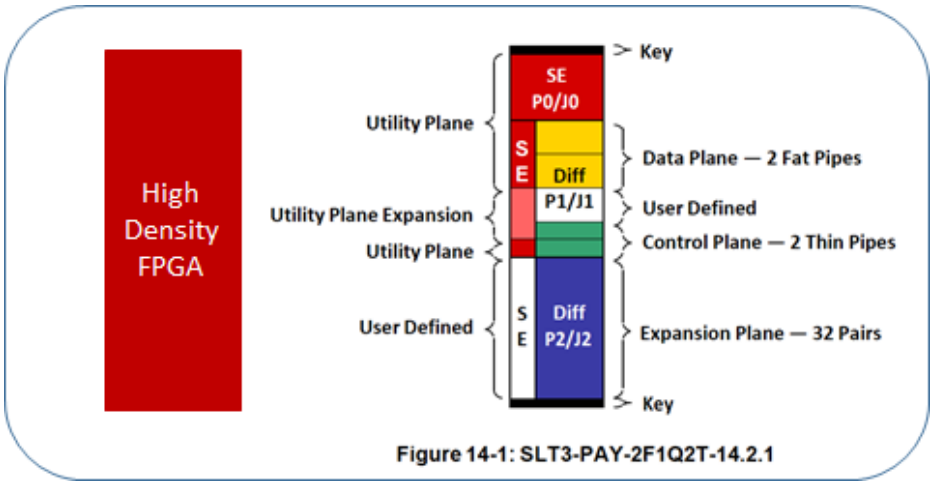

Figure A-3. Candidate High Density FPGA Module Profile

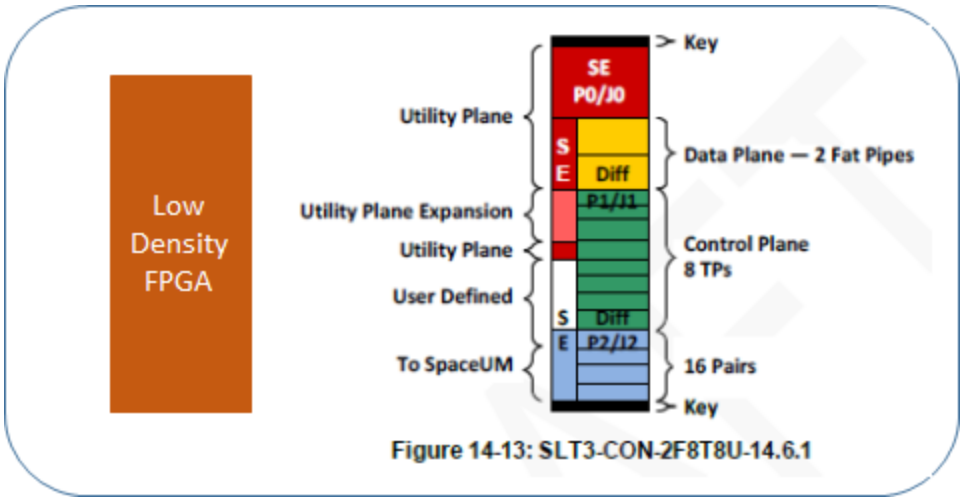

Figure A-4. Candidate Low Density FPGA Module Profile

Switch Module – Switch modules are needed for use cases where the number of control plane or data plane ports on modules exceeds the number provided by the SBC. These modules can provide external network interfaces via the front panel. Figure A-5 depicts candidate VITA-78 profiles that can be used as a starting point for a switch module profile.

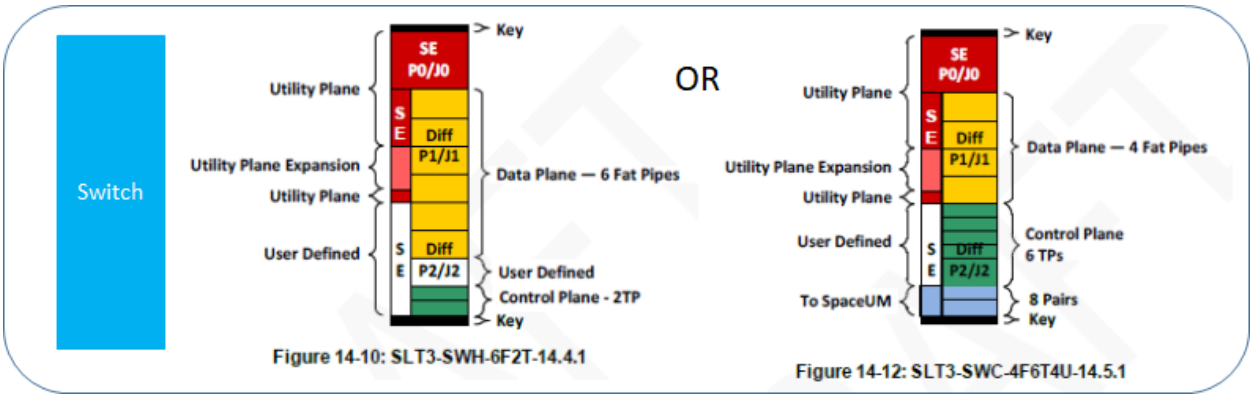

Figure A-5. Candidate Switch Profiles

Storage Module – Several use cases require data storage beyond the capacity provided on the SBC. Storage modules, implemented with solid state nonvolatile memory, provide this mass storage. Figure A-6 illustrates a candidate VITA-78 profile for this module type.

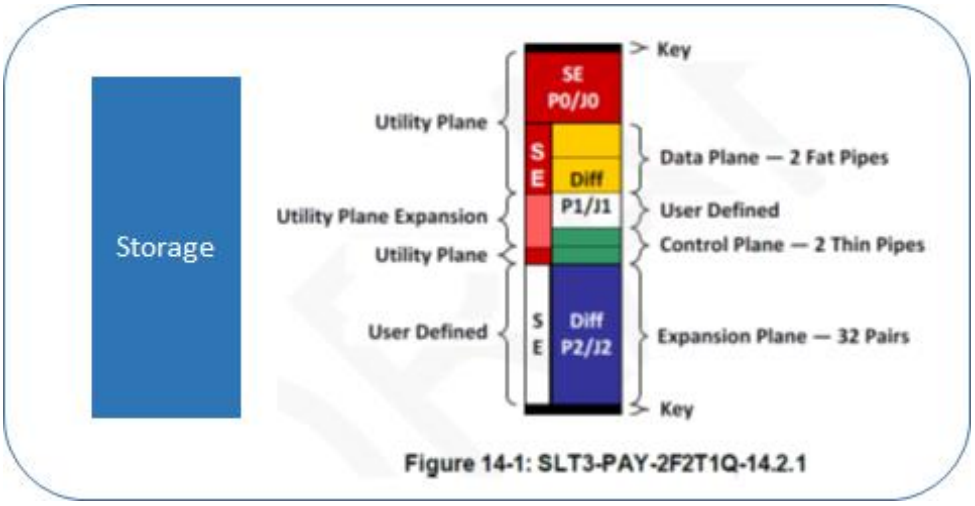

Figure A-6. Candidate Storage Module Profile

Digitizer Module – While not explicitly included in the use cases studies, SME guidance indicated that digitizer modules with high bandwidth analog-to-digital converters and/or digital-to-analog converters with JESD204B interfaces could be needed for some future SpaceVPX systems. Applications include Software Defined Radios (SDRs) and microwave instruments. Figure A-7 provides a candidate VITA-78 profile for this module type.

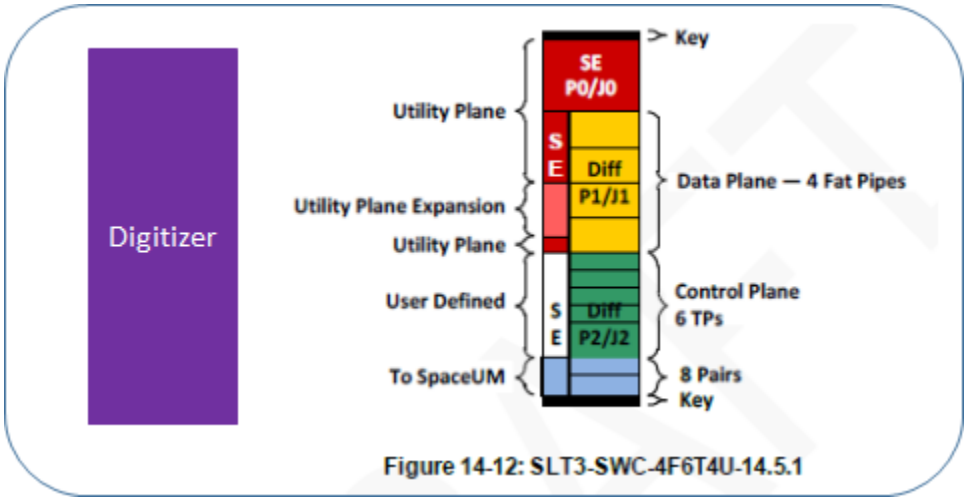

Figure A-7. Candidate Digitizer Module Profile

6U Modules

6U modules provide increased area and significantly increased pin resources as compared to 3U modules. Table A-3 lists the three general options for how these additional resources can be used.

Table A-3. Uses for Additional 6U Resources

Option	Examples
Combine multiple functions onto a single module	• Combined SBC and FPGA module • Combined SBC and switch module
Expand capacity for a given module function	• Increase storage module capacity with more memory devices • Increase mission specific functions and implemented on FPGA modules • Increase number and variety of port on switch module
Increase fault tolerance	• Redundant interfaces on backplane • Redundant circuitry internal to module

Considering the examples listed in the first two options, a set of standard 6U modules can be defined. Table A-4 lists these modules and provides the proposed interconnect.

Table A-4. Proposed Interconnect for 6U Modules

Slot Profile Category	Ethernet (Data Plane)	PCIe (Expansion Plane)	JESD204B (Expansion Plane)	SpaceWire (Control Plane)	I2C (Other)	SPI	Custom SERDES (Other)	SpaceUM Control (Other)
SBC/FPGA	4, 4 Lane, Ports (TSN/Ethernet) –32 Differential Pairs	2 x8 Ports - 32 Differential Pairs	32 Differential Pairs	8 Ports – 32 Differential Pairs	8 Port – 16 Single Ended	4 Ports – 16 Single Ended	40 Differential Pairs	16 Differential Pairs
FPGA	4, 4 Lane, Ports (TSN/Ethernet) –32 Differential Pairs		32 Differential Pairs	8 Ports – 32 Differential Pairs	8 Port – 16 Single Ended	4 Ports – 16 Single Ended		
Switch	10, 4 Lane Ports TSN/Ethernet – 80 Differential Pairs	5 x8 Ports - 80 Differential Pairs		8 Ports – 32 Differential Pairs				
Storage	4, 4 Lane, Ports (TSN/Ethernet) –32 Differential Pairs	2 x8 Ports - 32 Differential Pairs		4 Ports – 16 Differential Pairs				

SBC/FPGA Module – This module pairs a processor with a high density FPGA to provide general purpose processing and FPGA-based acceleration. This module could perform other functions including command and telemetry processing and bridging to different networks on front panel connectors. Figure A-8 depicts a candidate VITA-78 profile that could be starting points to define a module for this profile.

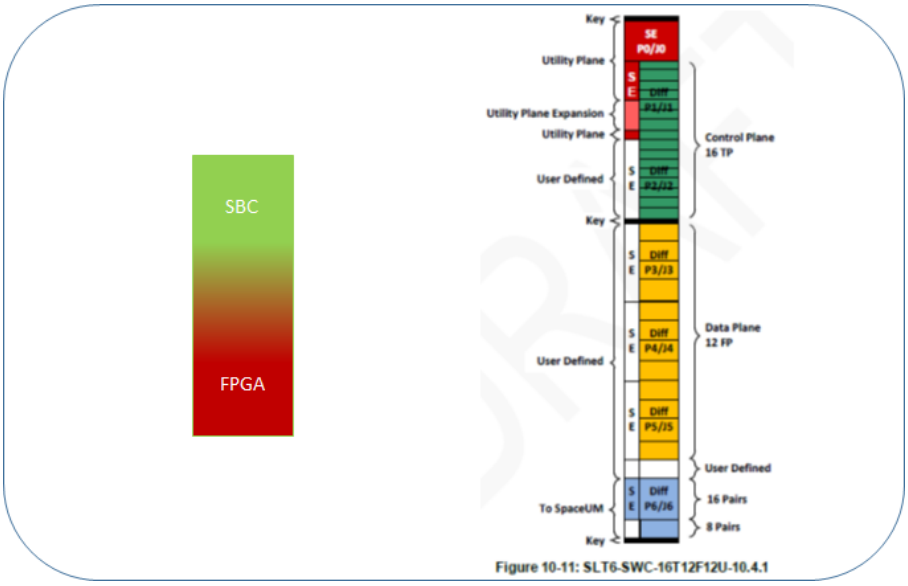

Figure A-8. Candidate Profile for 6U Hybrid SBC/FPGA Module

FPGA Module – Options for using the 6U FPGA module include multiple FPGA devices, increased memory capacity, and accommodating additional daughtercards and front panel interfaces. Given its flexibility, it is envisioned that this module would serve as the basis for mission unique modules, including instrument readout and control, and motor and actuator control for robotic systems. The 6U module increased the number of Ethernet ports for increased aggregate bandwidth. To allow interfacing to 3U digitizer modules in hybrid 3U/6U systems, the 6U FPGA module retains the JESD204 interface. As with 3U FPGA modules, 6U modules can be classified into high density and low density modules. However, the increased pin resources of the 6U connector allow a single profile to accommodate both types. Figure A-9 provides a candidate VITA-78 profile that can provide a starting point to define this profile.

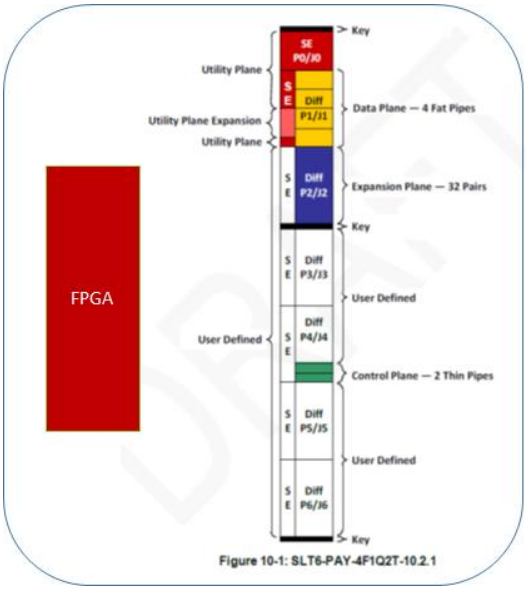

Figure A-9. Candidate Profile for 6U FPGA Module

Switch Module – The 6U module increases the number of Ethernet and SpaceWire ports. The 6U module provides interfaces to allow implementation of a PCIe switch. Figure A-10 provides a candidate VITA-78 profile that can provide a starting point to define this profile.

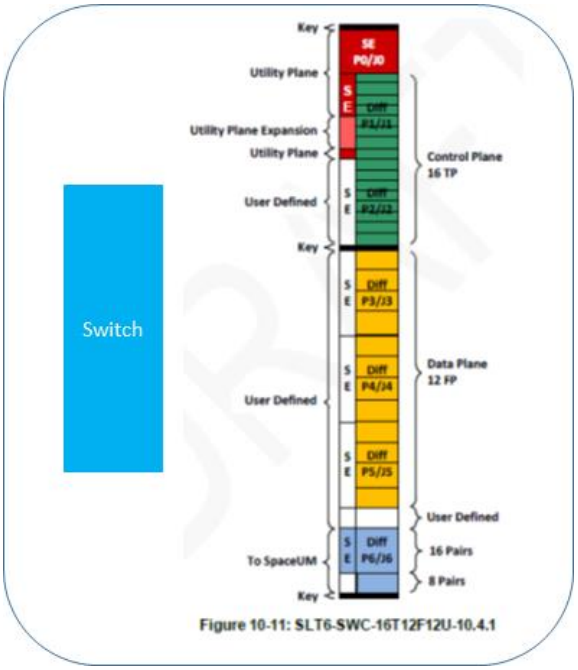

Figure A-10. Candidate Profile for 6U Switch Module

Storage Module – The 6U module increases the number of Ethernet and SpaceWire ports, while retaining the PCIe port. Figure A-11 provides a candidate VITA-78 profile that can provide a starting point to define this profile.

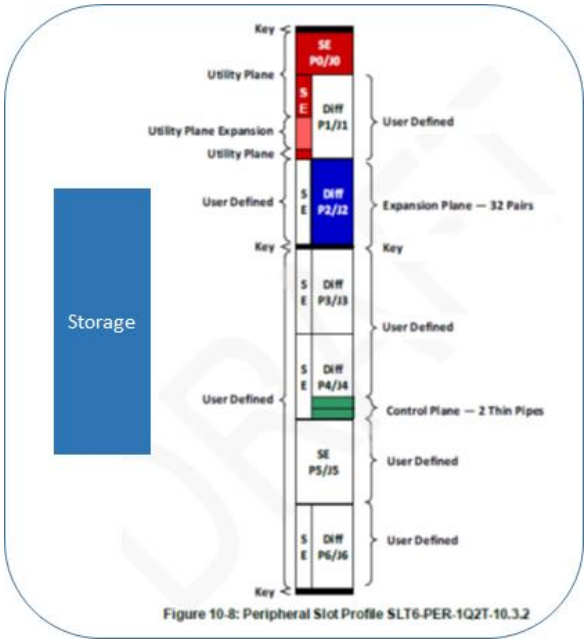

Figure A-11. Candidate Profile for 6U Storage Module

Appendix B. Example Systems

This appendix provides the module definitions provided in Appendix A. The example systems included are intended to illustrate single-string and redundant implementations. A minimalist system is illustrated that does not require the use of a SpaceUM. Lastly, an interim system combining SpaceVPX and cPCI modules is shown.

Redundant 3U System

The redundant 3U example in Figure B-1 illustrates the largest possible 3U system (14 modules). Each redundant side is comprised of seven modules that are cross strapped between primary and redundant sides. In this configuration, the system can operate if at least one of each module type (i.e., primary or redundant) is operational. The exception to this is the SpaceUM. Failure of a SpaceUM will render all modules it controls nonoperational. This example assumes that the SBC is based on HPSC, and interfaces to a storage module via PCIe on the expansion plane. Two FPGA modules are included on each side, with the Tlm/Cmd module assumed to have a low density FPGA without an Ethernet interface, and an Imager module assumed to have a high density FPGA with an Ethernet interface.

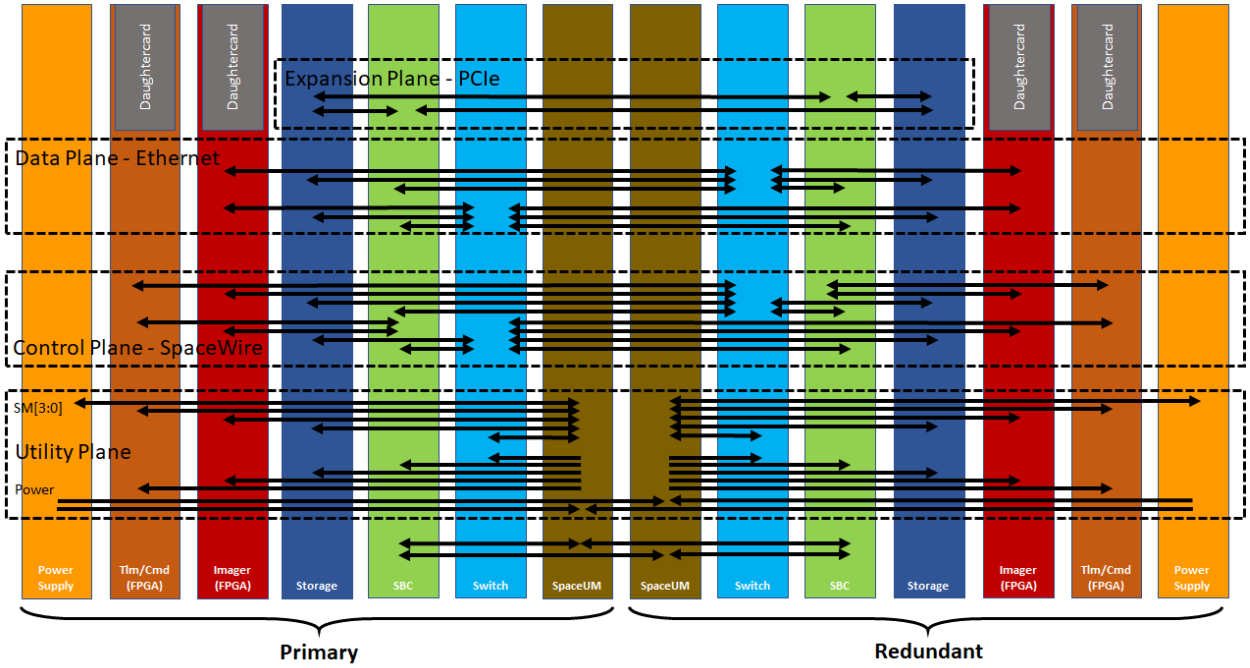

Figure B-1. Redundant 3U Example System

Single-String 3U Systems

Two examples of single-string 3U systems are provided. Figure B-2 illustrates a SmallSat application. With seven modules, this represents the largest possible single-string system. This example assumes that the SBC is based on HPSC, and interfaces to a storage module via PCIe on the expansion plane and three FPGA modules via Ethernet on the data plane. Two of the FPGA modules perform instrument control functions, while the third FPGA module performs spacecraft control functions. In single-string configurations, the SpaceUM provides the ability to reset and power cycle modules in the event of transient faults. In the event of permanently failures, the SpaceUM can power down the failed modules to allow degraded modes of operation.

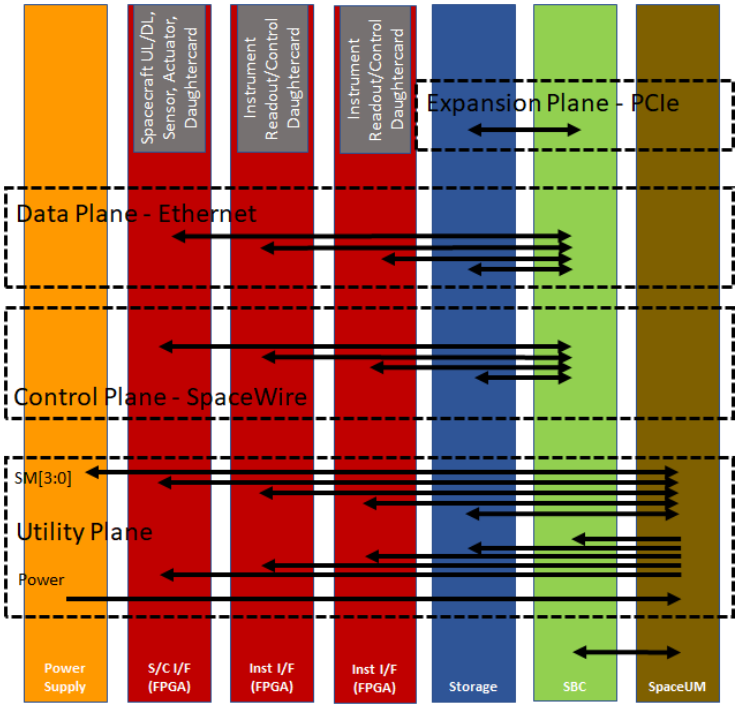

Figure B-2. Example Single-String SmallSat Avionics

Figure B-3 illustrates a single-string instrument controller. This example assumes the use of two separate expansion planes in different regions of the chassis. The SBC interfaces to a storage module via PCIe on one expansion plane, and digitizer modules interface to an FPGA module using JESD204C on a separate three expansion plane.

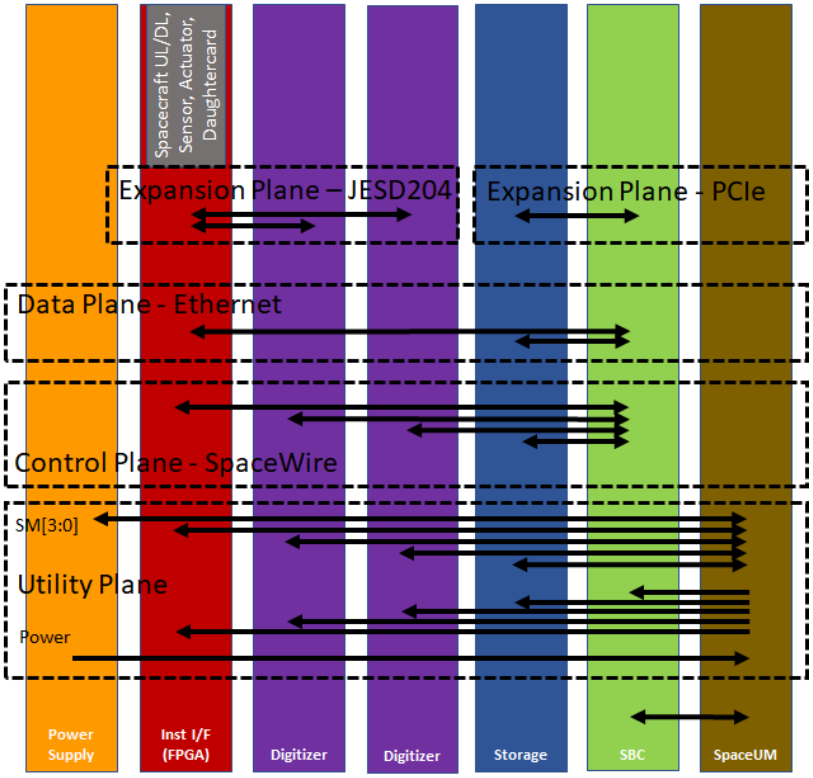

Figure B-3. Example Single-String Instrument Controller

Minimalist Systems

For small single-string systems, the resources required for a SpaceUM may outweigh its benefits. For these applications, it is possible to implement 'minimalist' systems consisting of a small number of SpaceVPX modules without a SpaceUM. Figure B-4 illustrates one option for implementing a minimalist system. However, other options exist.

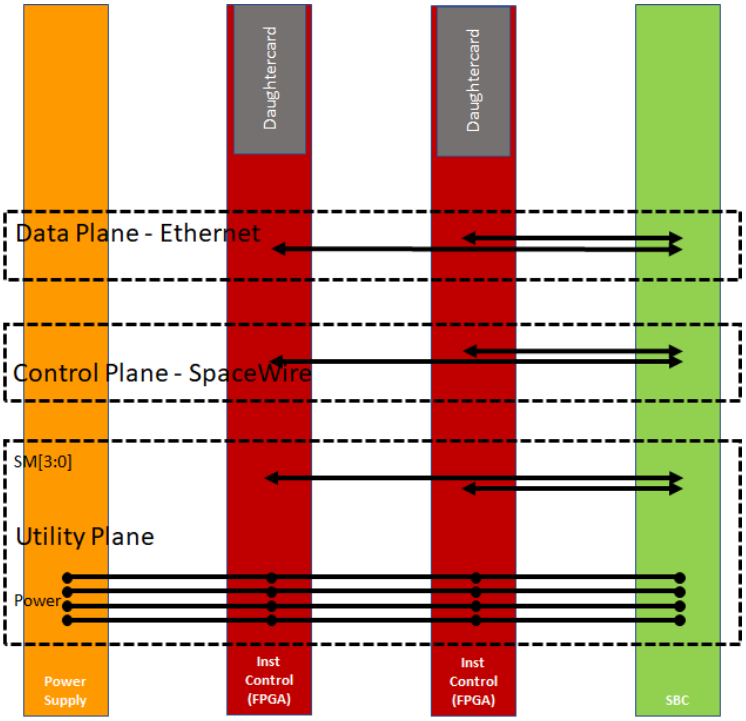

Figure B-4. Minimalist System

In this configuration, the SM[3:0] signals sources by the SBC that would typically be used by SpaceUMs are routed directly to two modules. Without the power switching provided by the SpaceUM, the backplane provides bussed power to all modules. Furthermore, without control from the SBC, the power supply will enable all supplies once input power is stable.

Interim Systems

It is understood that all of the proposed module types listed in Appendix A are currently available. Until the full complement of SpaceVPX modules are available, missions may opt to implement 'interim systems' that include SpaceVPX modules and heritage cPCI modules. Figure B-5 illustrates an example of a redundant interim system.

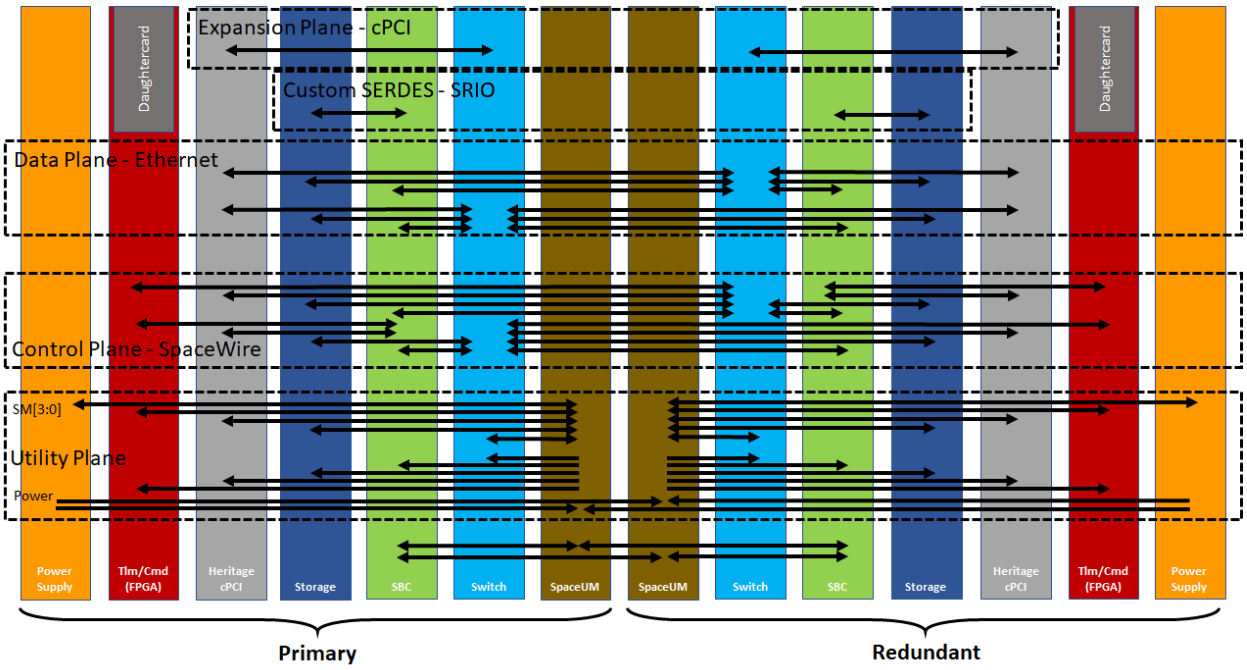

Figure B-5. Interim System

The 3U switch modules as defined in Appendix A do not have a sufficient number of pins to support a cPCI interface. Hence, interim systems with cPCI support must include 6U switch modules. This will likely lead interim systems to use hybrid 3U/6U backplanes and chassis. As shown above, each switch module serves as a cPCI bridge to a heritage board. However, interim systems can be configured with multiple cPCI modules per switch module. The interim system shown above leverages the custom SERDES I/O to implement a legacy SRIO interface to a storage module.

Appendix C. Use Cases

If the reader would like to review the 12 Use Cases, please contact the NESC at the following link: https://www.nasa.gov/nesc.

C.1 Gateway Vehicle System Manager (VSM) Safing Action
C.2 On-orbit Servicing, Assembly, and Manufacturing
C.3 Rover - Robotic
C.4 SmallSat (ESPA Class)
C.5 A-Team Use Case
C.6 SPLICE (Safe & Precise Landing Integrated Capabilities Evolution) DLC
C.7 High Data Rate - RADAR
C.8 High Data Rate - Spectroscopy
C.9 Low/Medium Data Rate Missions
C.10 Robonaut2, LTV GTU
C.11 Advanced, Earth Observing Hyperspectral Instruments
C.12 Communications Relay

Appendix D. Product Survey Spreadsheet

The team surveyed avionics manufacturers. Some responses are considered proprietary. If the reader would like to review the SpaceVPX Product Survey, please contact the NESC at the following link: https://www.nasa.gov/nesc.

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14. ABSTRACT
As NASA exploration moves beyond low-Earth-orbit (LEO), the need for interoperable avionics systems became more important due to the cost, complexity, and the need to maintain distant systems for long periods. This assessment addresses the deficiencies in the SpaceVPX standard for NASA missions enabling interoperability at the card and system level through common functionality, protocols, and physical implementations.

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