European Conference on Radiation and its Effects on Components and Systems
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H-6: Ionizing Radiation Effects on Hole Collection Backside-Illuminated P-Type Deep-Trench Pinned Photo-MOS Pixels under Image Acquisition

Session H: Photonics, Optoelectronics & Sensors

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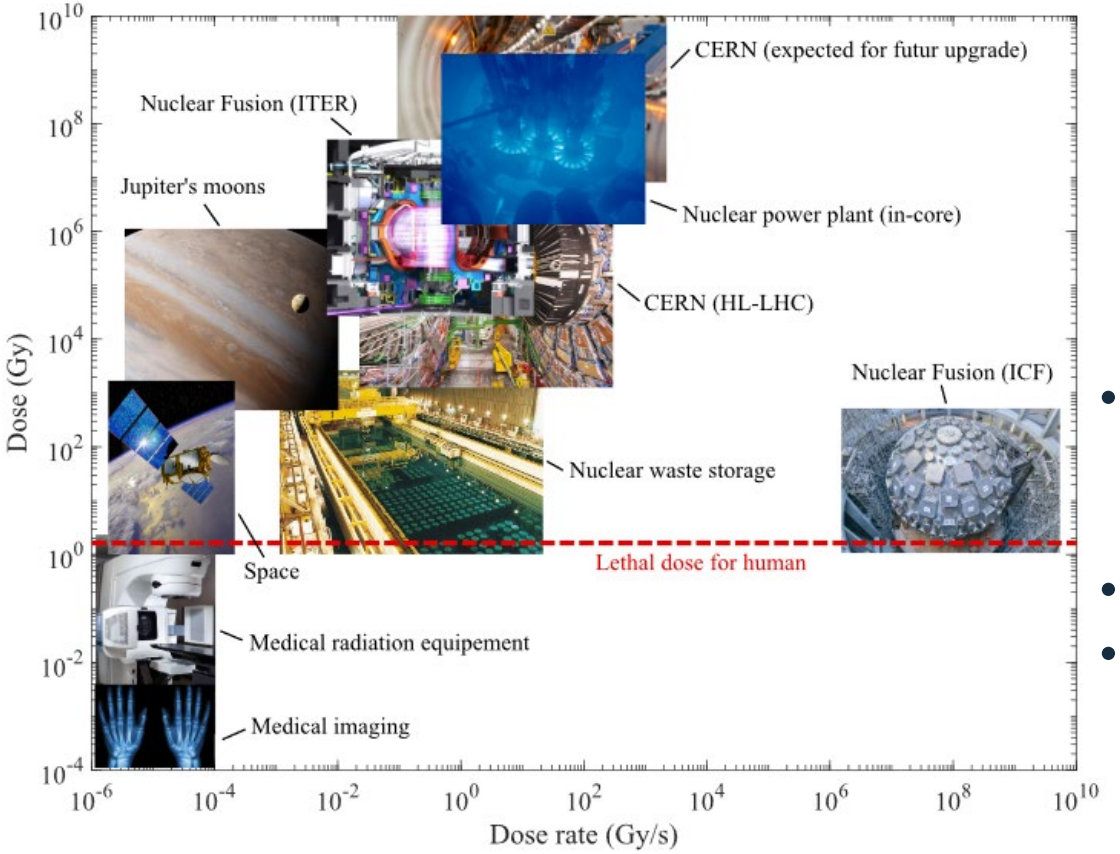
Acronyms & Abbreviations

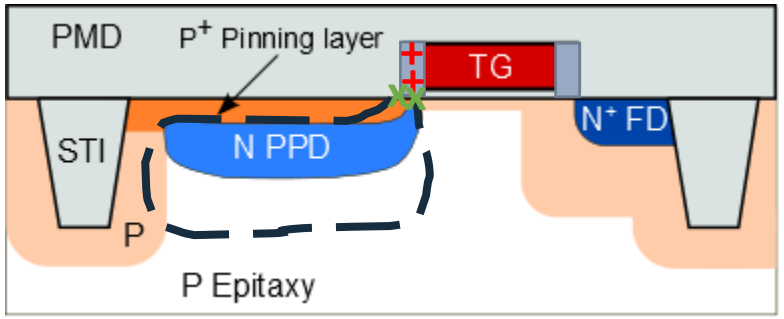
3T	Three Transistor
CCD	Charge Coupled Device
CDTI	Capacitive Deep-Trench Isolation
CERN	European Organization for Nuclear Research
CIS	CMOS Image Sensor
CMOS	Complementary Metal-Oxide Semiconductor
DDD	Displacement Damage Dose
DTI	Deep Trench Isolation
FD	Floating Diffusion
FWC	Full Well Capacity
ICF	Inertial Confinement Fusion
ITER	International Thermonuclear Experimental Reactor
ONO	Oxide-Nitride-Oxide
PMD	Pre-Metal Dielectric
PPD	Pinned Photodiode
ROIC	Read-Out Integrated Circuit
RS	Row Select
SF	Source Follower
SN	Sense Node
STI	Shallow Trench Isolation
TG	Transfer Gate
TID	Total Ionizing Dose

CIS in radiation environment

Electronics in radiation environment Dose rate vs Dose (1)



Planar Pinned PhotoDiode (PPD) 4T cross section



x Interface states

+ Positive trapped charges

- **Ionizing radiation induces positive charge buildup in SiO_2 and interface states that act as generation/recombination centers at Si/SiO_2 interfaces**
- PPD use is restricted to applications under ≈ 1Mrad
- 3-transistor pixels can be use at higher doses at the expense of lower performance

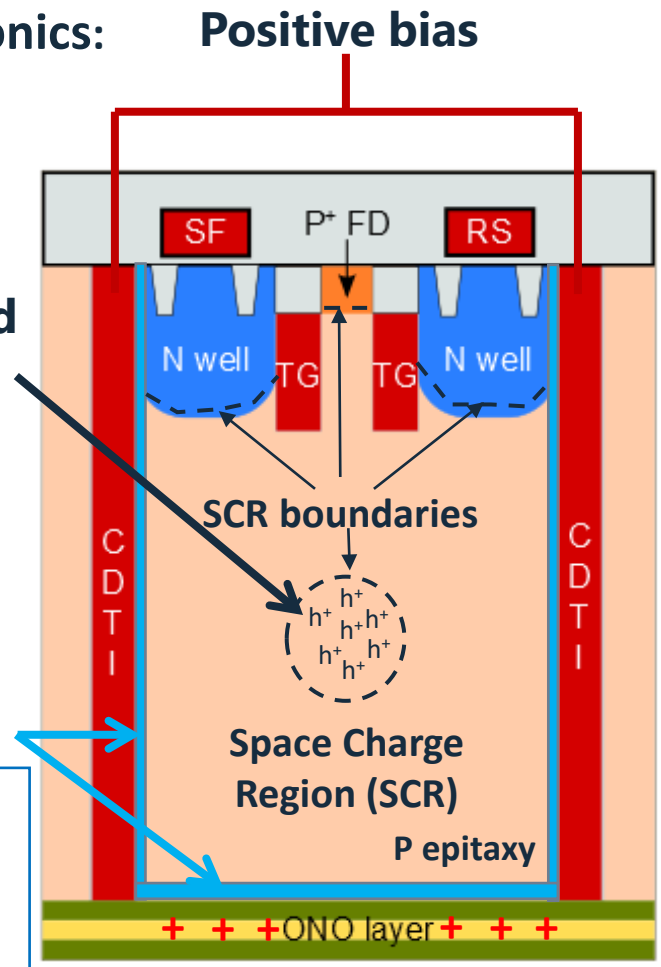
PhotoGate: A new device to bring 4T pixel CIS performance above 1Mrad ?

(1) Dewitte, H., "*Ultra-high dose effects and junction leakage current in CMOS technologies for analog applications*", Doctoral dissertation, Toulouse, ISAE-SUPAERO, 2022.

Photogate working principles

A novel pixel architecture/process under development at STMicroelectronics:

- P epitaxy: hole collecting device
- **4-Side Isolated using Capacitive Deep-Trench Isolation (CDTI)**
- Vertical Transfer Gate (TG)
- Charge collecting and storage volume isolated from all interfaces using purely electrostatic means:
  - Positive voltage applied to the CDTI, creating an electron sheet along the sidewalls
  - Backside interface passivated by positive trapped charges in the ONO layer



- No Si/SiO_2 depleted interface
- Fully isolated on the sides using CDTI
- TID induced positive charge buildup expected to enhance the interface passivation

Promising design from a radiation hardness standpoint!

Motivations and irradiation details

First radiation tolerance study:

- Dark current increase with total dose on grounded samples
- Gamma rays and fusion neutron
- Reverse annealing observed

Clarifying the physical mechanisms at the origin of the degradation by:

- Studying the effect of bias under irradiation
- Clarifying the role of the CDTI
- Clarifying the role of the transfer gate
- Studying the influence of high temperature annealing on the device behavior

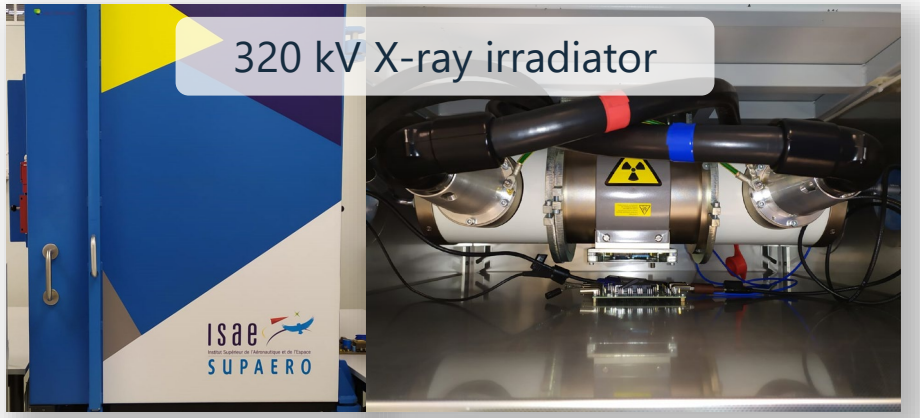
Device under test

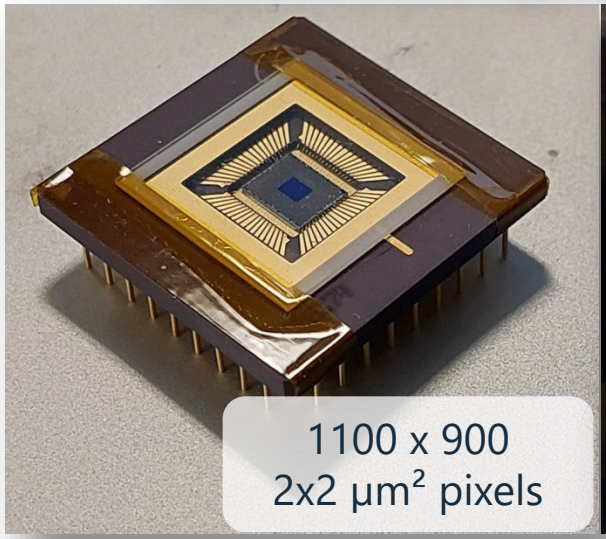
- 1100x900 2x2µm² pixel matrix with custom proximity board in charge of power supply, sequencing and readout.

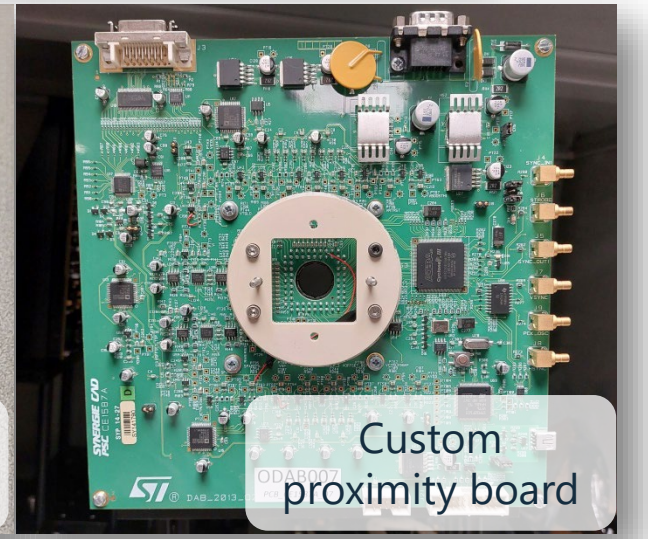
Irradiation using a 320 kV X-ray irradiator at 100 kV

- 10 krad to 5 Mrad at 3krad/min
- 10 Mrad to 60 Mrad at 5 Mrad/h, **results under investigation**

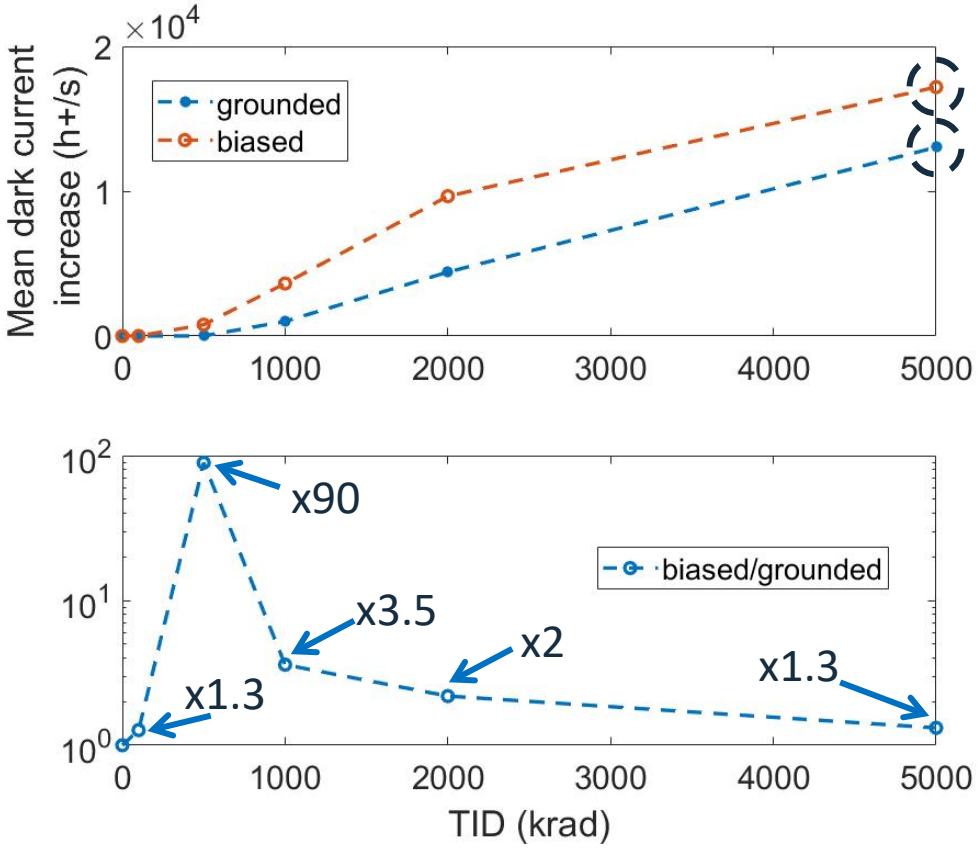
rad = rad(SiO_2)



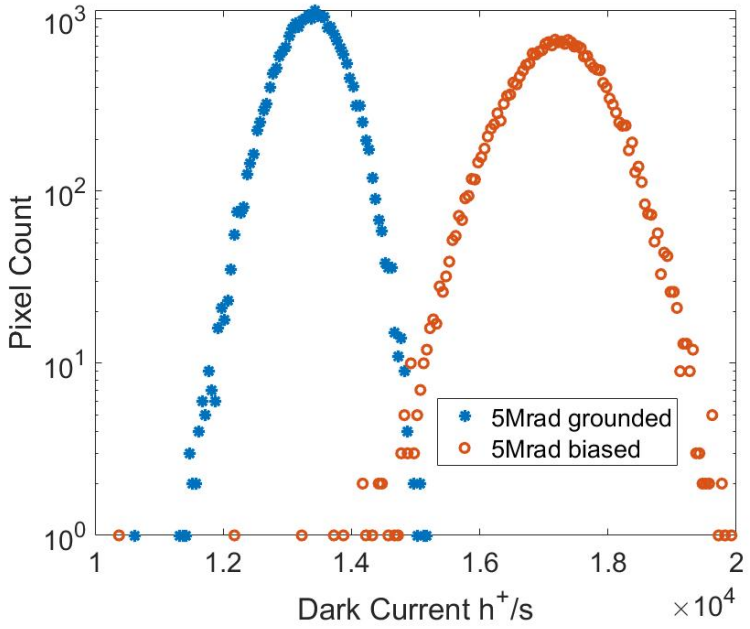




Dark current increase – Role of the bias



Significant difference at 1 Mrad

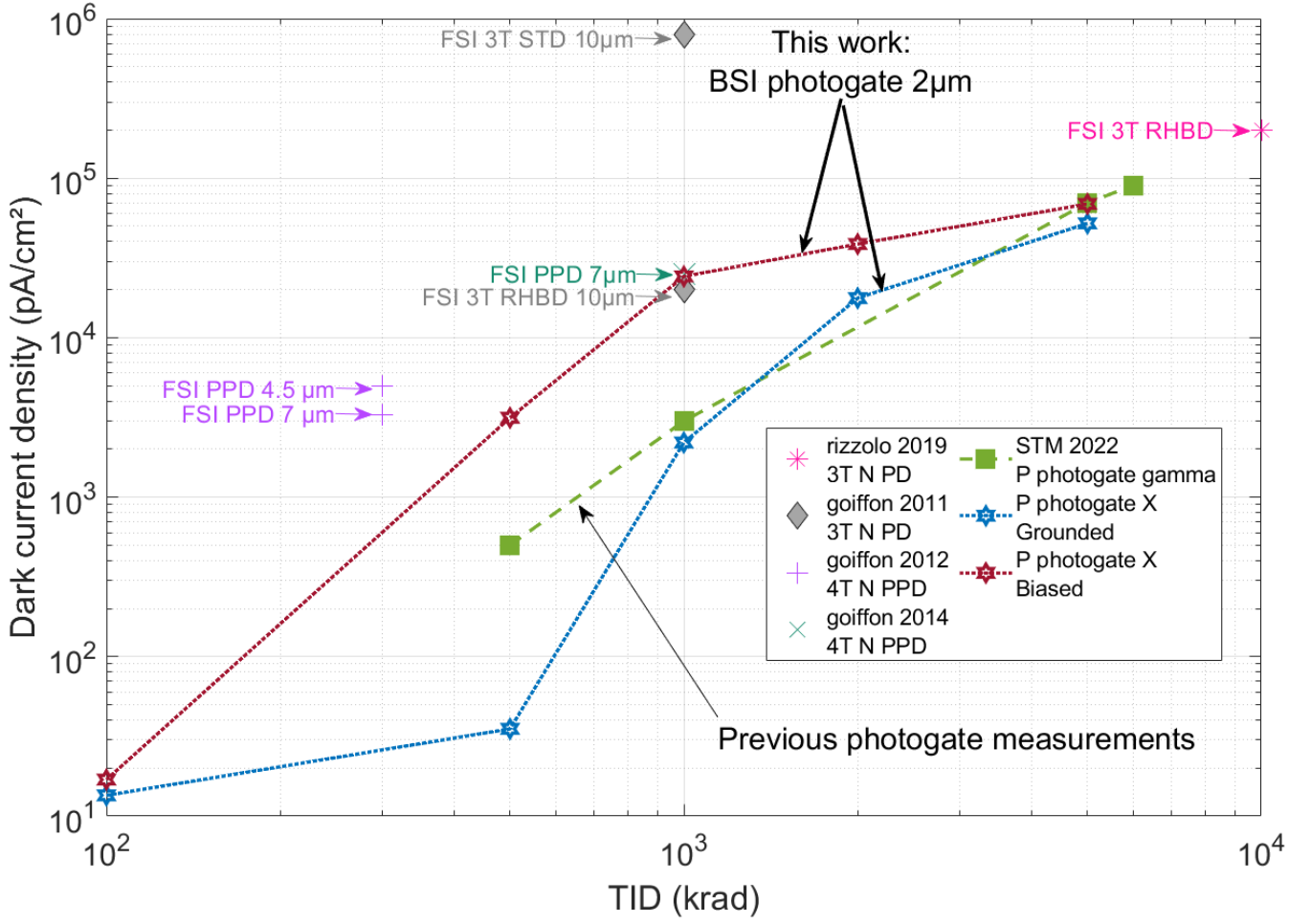


- Sharp dark current increase after 100 krad when biased and 500 krad when grounded
- Gaussian shaped: uniform degradation and no obvious field effect

Typical radiation induced dark current increase as reported in CCDs and CIS

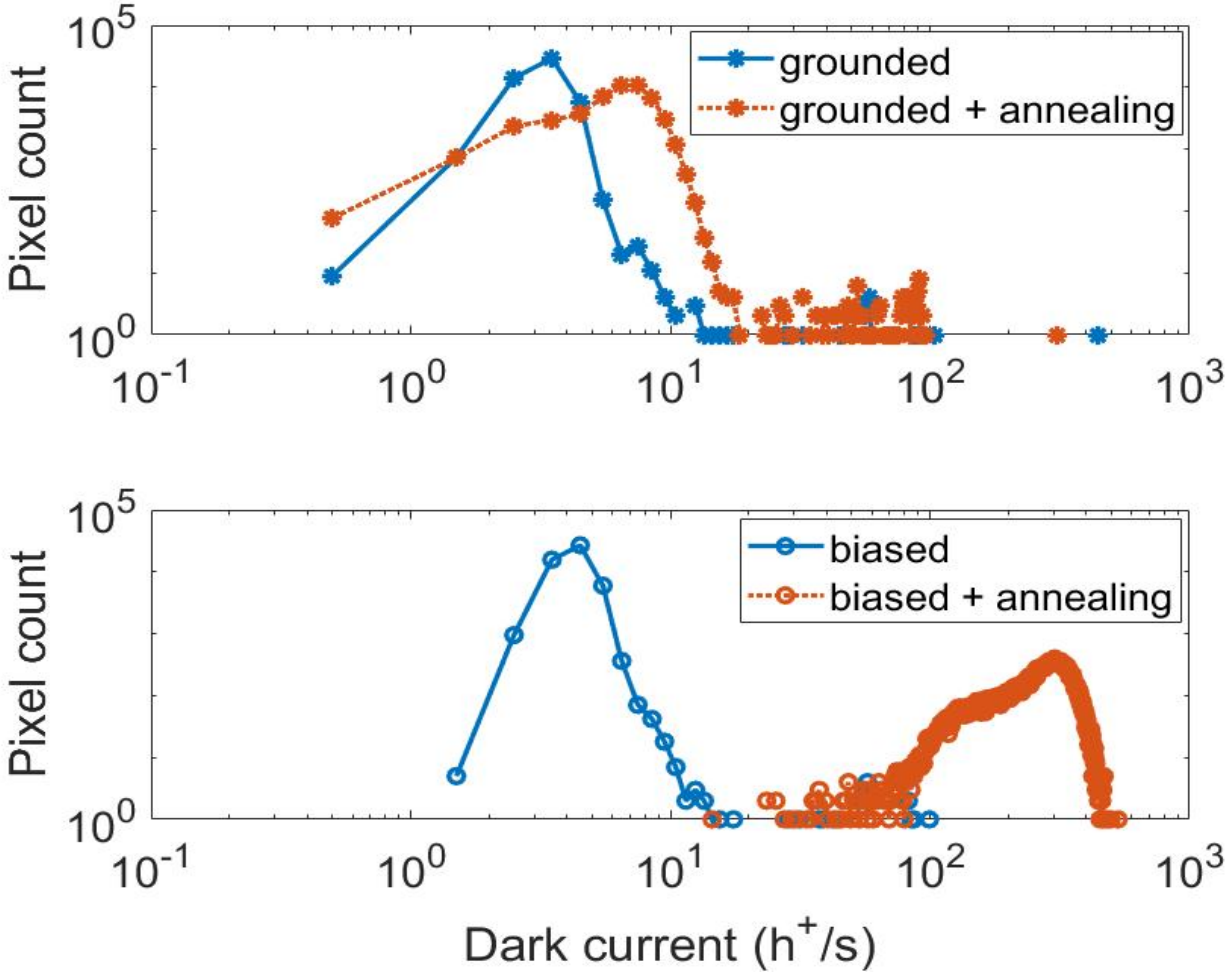
Biasing the device accelerates the degradation under irradiation

Comparison with other pixel architectures



- The dark current increase is very low up to 100 krad (≈4 h^+/s at 100 krad before annealing)
- The dark current increase is comparable to a PPD in the 500 krad – 1 MRad range
- Very small conversion gain factor (µV/h^+) variations (< 5% at 5 Mrad)
- **No lag detected: big concern in PPDs over 500 krad**
- **Taken up to 5 Mrad without failure**
- **Backside-Illuminated: favorable for the Fill-Factor and the Quantum Efficiency**
- **2 µm pitch unlocks high resolution applications: advantage over larger 3T pixels**

Annealing behavior at 100 krad



Annealing at 100°C for 1 week

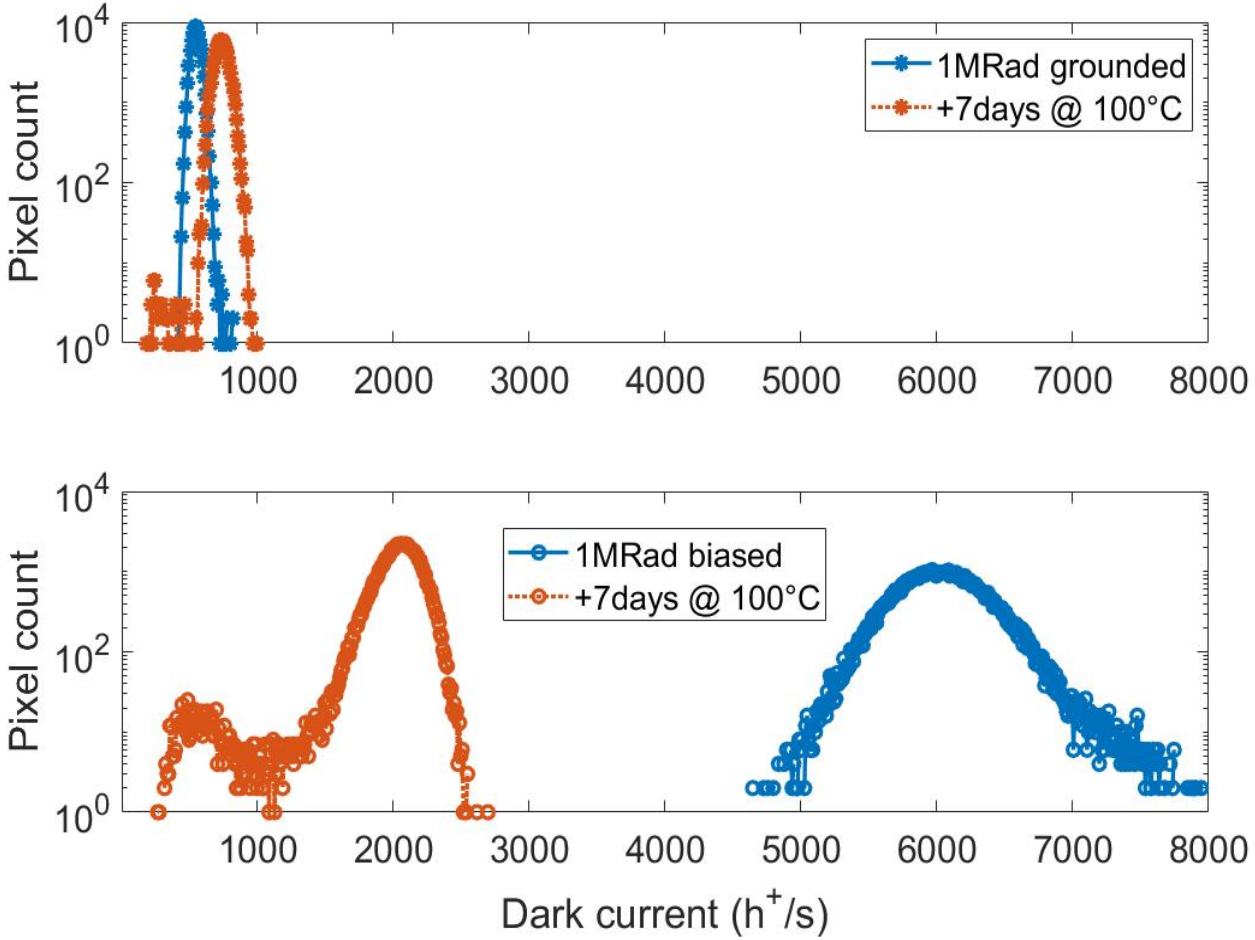
The dark current increases from 3.3 to 6.8 h^+/s after annealing when grounded

The dark current increases from 4.3 to 285 h^+/s after annealing when biased

Reverse annealing effect confirmed

Biasing conditions have an impact on the annealing behavior

Annealing behavior at 1 Mrad



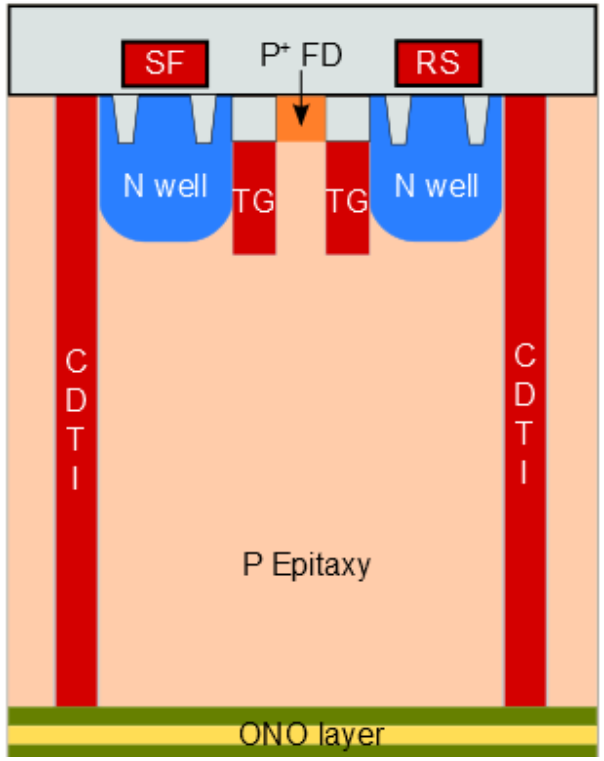
Annealing at 100°C for 1 week

The dark current **increases** from 550 to 735 h^+/s after annealing when **grounded**

The dark current **decreases** from 6000 to 2000 h^+/s after annealing when **biased**

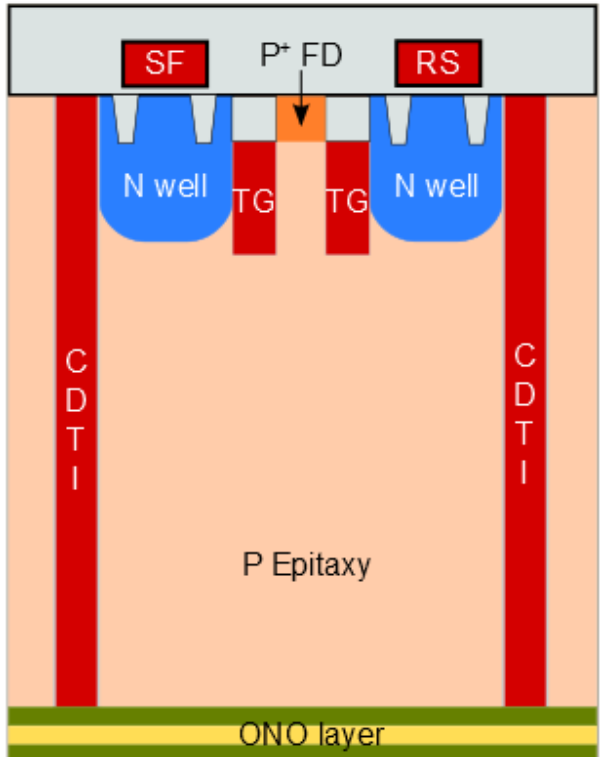
Reverse annealing effect confirmed on the grounded sample but "classical" annealing on the biased sensor

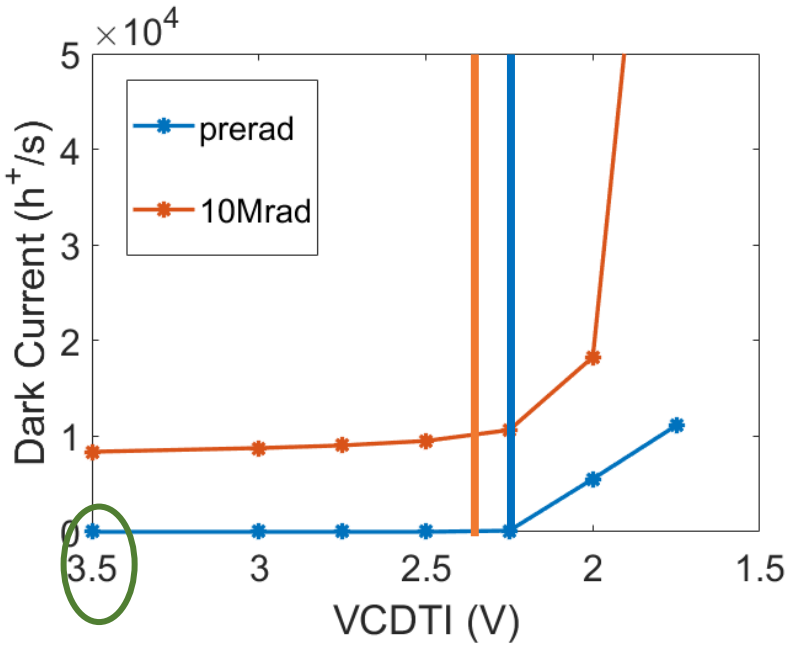
Dark current origin – 4 suspects



- CDTI sidewalls
- TG oxide contribution
- Top STI and PMD
- Backside interface: ONO stack

Dark current origin – 4 suspects

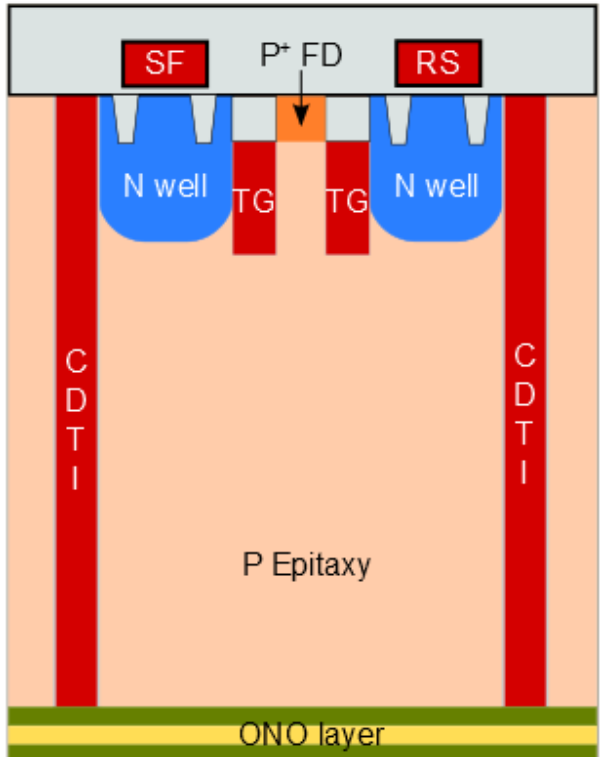


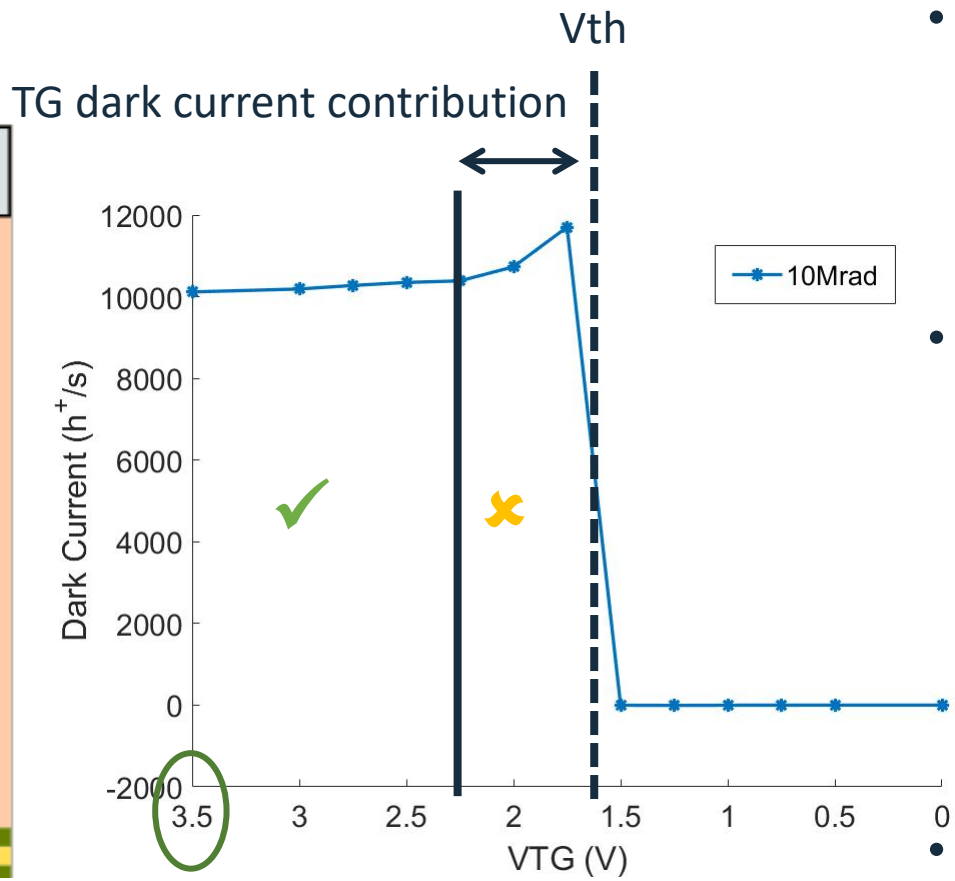


Operating voltage

- CDTI sidewalls
  - Small inversion voltage shift at 10 Mrad
  - **Operating voltage guarantees proper passivation**
- TG oxide contribution
- Top STI and PMD
- Backside interface: ONO stack

Dark current origin – 4 suspects



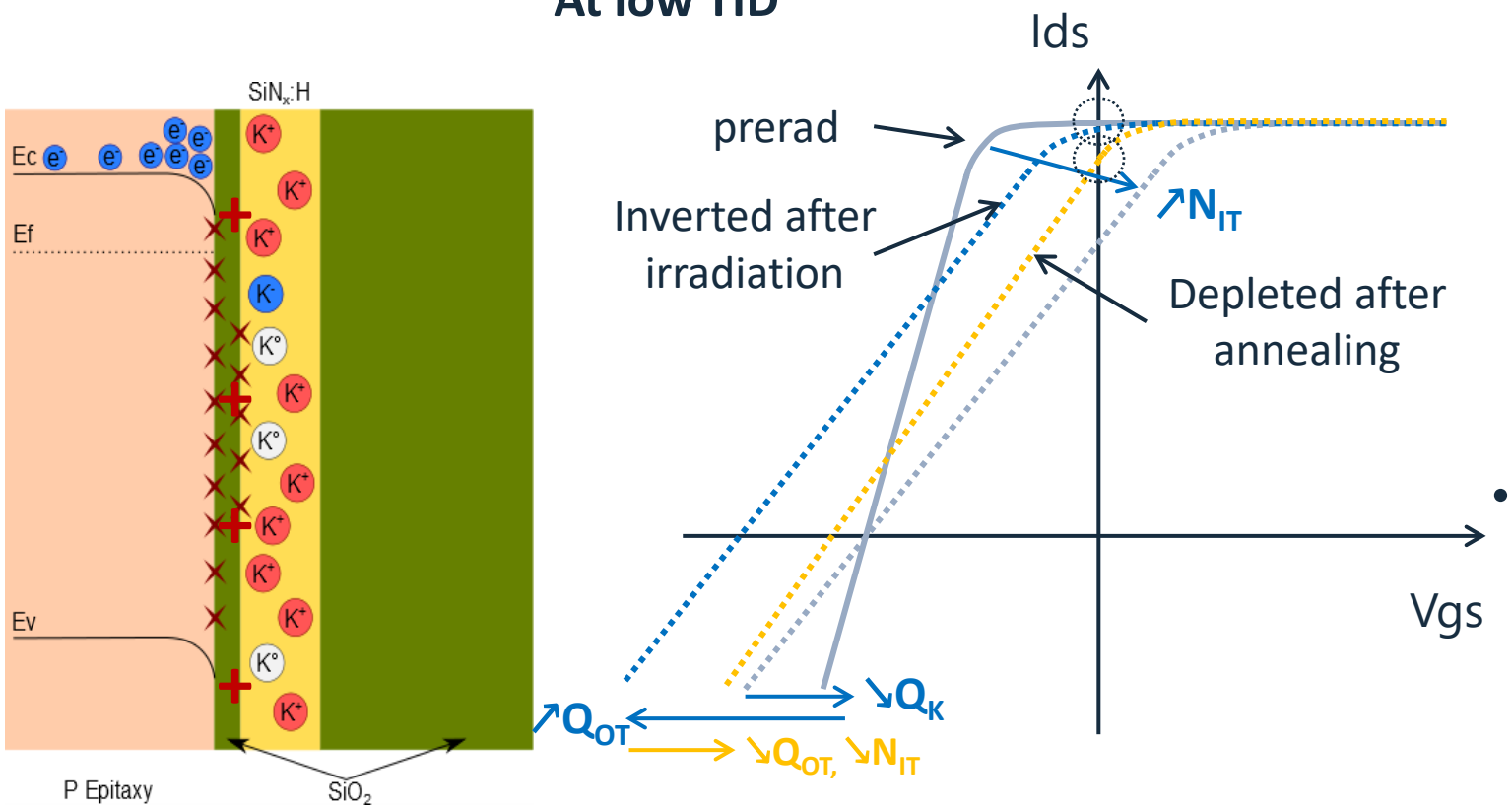


Operating voltage

- CDTI sidewalls
  - Small inversion voltage shift at 10 Mrad
  - **Operating voltage guarantees proper passivation**
- TG oxide contribution
  - Visible contribution when the TG isn't properly inverted
  - **Operating voltage guarantees proper passivation during integration**
  - **Charge transfer discussed in the paper**
- Top STI and PMD: little to no impact on dark-current, under investigation
- Backside interface: ONO stack

ONO backside interface – working hypothesis

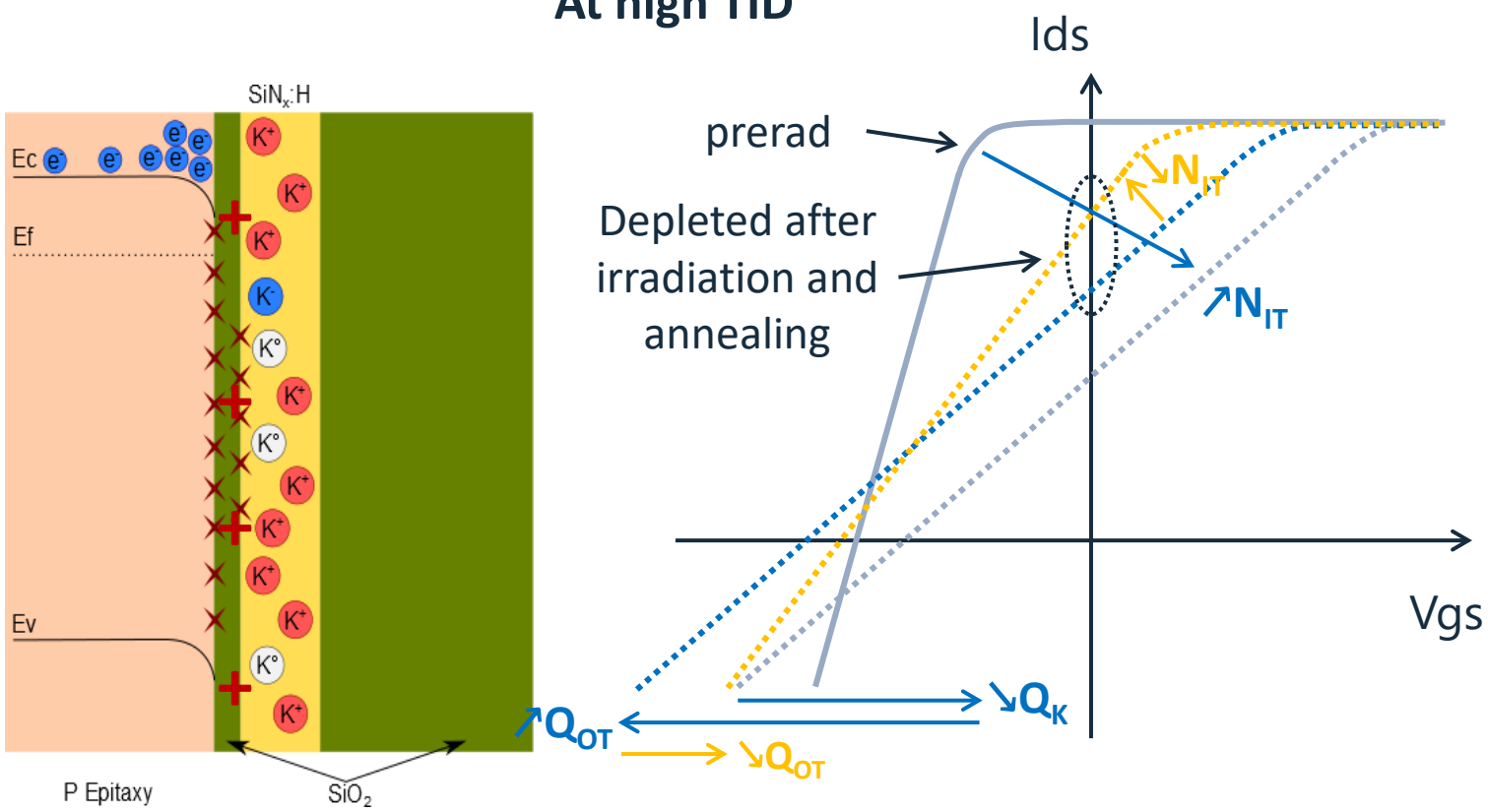
At low TID



Depleted interface after annealing leads to dark current increase

- Charged during process using K centers' ability to be positively, negatively charged, or neutral
  - **K centers are known for losing their charge state under UV**
  - **Similar behavior under X rays expected**
- Complex behavior under investigation involving:
  - K center concentration (Q_K)
    - **↘ irradiation, = annealing**
  - Oxide trap concentration (Q_{OT})
    - **↗ irradiation, ↘ annealing**
  - Interface trap concentration (N_{IT})
    - **↗ irradiation, ↘ annealing**

ONO backside interface – working hypothesis



Depleted interface after irradiation and annealing but N_{IT} decrease during annealing so the dark current decreases during annealing

- Charged during process using K centers' ability to be positively, negatively charged, or neutral
  - **K centers are known for losing their charge state under UV**
  - **Similar behavior under X rays expected**
- Complex behavior under investigation involving:
  - K center concentration (Q_K)
    - **↘ irradiation, = annealing**
  - Oxide trap concentration (Q_{OT})
    - **↗ irradiation, ↘ annealing**
  - Interface trap concentration (N_{IT})
    - **↗ irradiation, ↘ annealing**

Conclusion

- Dark current increase consistent with results previously observed (V. Malherbe et. al., 2022)
- The dark current increase is ≈2 times faster when the device is biased and sequenced during irradiation
- Reverse annealing confirmed but new behavior also observed
- The ONO stack at the backside interface is probably driving both the dark-current increase and the annealing behavior
- Biasing the device is important to characterize the device
- Very high TID effects (>10 Mrad) under investigation

The novel pixel architecture based on 4T pixel P type Photogate, **backside illuminated, 2 µm pixel pitch** offers **promising results up to 5 Mrad** and could be a better candidate than PPDs to create **high-performance, high-resolution,** and **radiation-tolerant** image sensors.

Thank you for your attention!

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