National Aeronautics and Space Administration

SpaceVPX Interoperability Study Briefing

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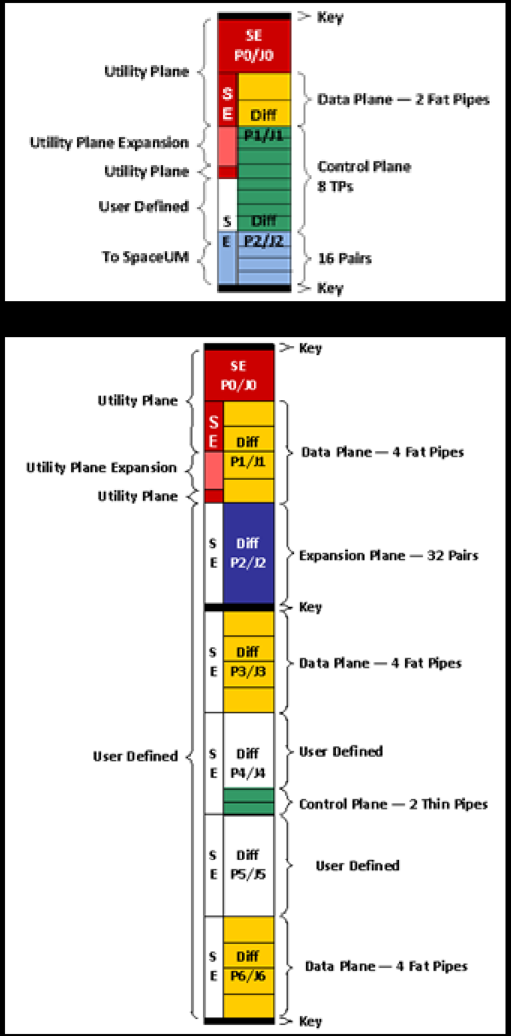
NASA and SpaceVPX

As NASA exploration moves beyond low-Earth-orbit (LEO), the need for interoperable avionics systems becomes more important due to the cost, complexity, and the need to maintain distant systems for long periods

The existing SpaceVPX industry standard addresses some of the needs of the space avionics community, but falls short of an interoperability standard that would enable reuse and common sparing on long duration missions and reduce NRE for missions in general

A NASA Engineering & Safety Center (NESC) study was conducted to address the deficiencies in the SpaceVPX standard for NASA missions and define the recommended use of the SpaceVPX standard within NASA

The future infusion of HPSC into SpaceVPX systems was a consideration in this study



3U and 6U Slot Profiles [VITA-78]

Scope of Assessment

- As NASA's crewed exploration missions move beyond low-Earth-orbit (LEO), the need for interoperable avionics systems becomes more important due to the cost, complexity, and the need to maintain distant systems for long periods.

- The previous NASA-developed and widely adopted standard for backplane-based chassis interconnect, cPCI is over 20 years old and no longer supports modern architectures. cPCI has fallen by the wayside and no other standard has risen to replace it. Stacked-card avionics, including MUSTANG, have arisen that address applications that require limited bandwidth communication between modules. However, no standard architecture supporting high-bandwidth, tightly coupled modules, has emerged are, resulting in ad hoc, non-optimal box level avionics, with attendant impact on cost, risk, schedule.

- An existing industry standard (SpaceVPX) addresses some of the needs of the space avionics community, but it falls short of an interoperability standard that would enable reuse and common sparing on long duration missions and reduce NRE for missions in general.

- **This assessment is to address the deficiencies in the SpaceVPX standard for NASA missions enabling interoperability at the card and system level through common functionality, protocols, and physical implementations.**

The report can be found at: https://ntrs.nasa.gov/citations/20220013983.

NESC Assessment Team

Name	Discipline	Organization
Core Team		
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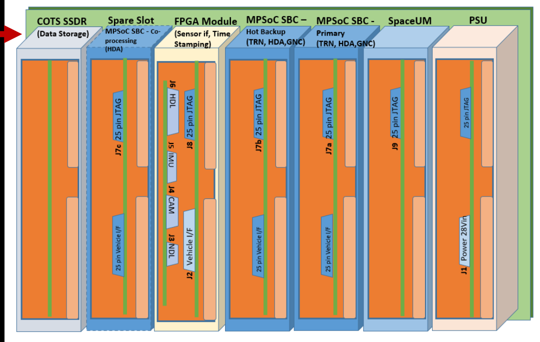
SpaceVPX Overview

SpaceVPX is an architecture standard that defines modules, backplanes, and chassis for spaceflight avionics boxes (the SpaceVPX standard is managed by VMEbus International Trade Association (VITA) as VITA-78)

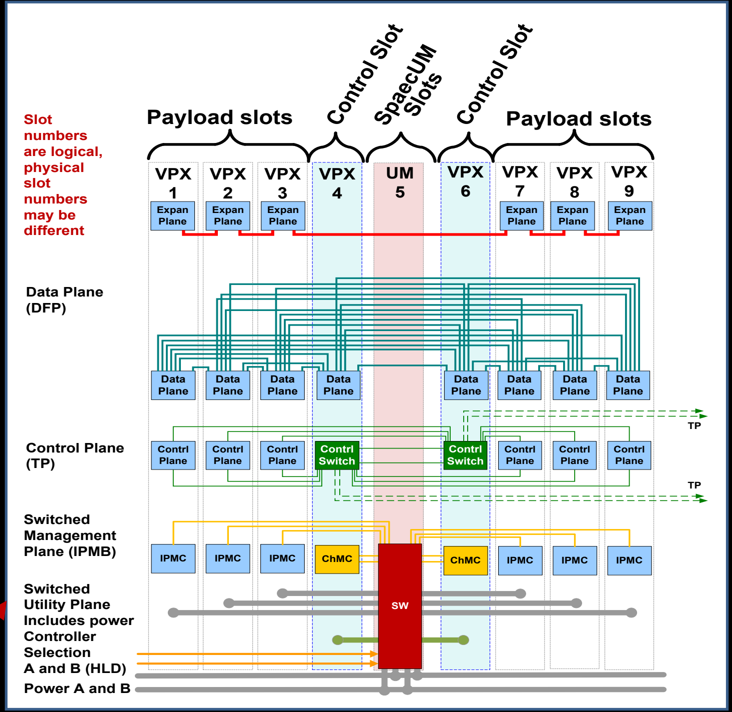
SpaceVPX adapts a Modular Open System Approach (MOSA), derived from VPX and OpenVPX (VITA-65), for space

SpaceVPX defines several general module types and how they can be interconnected, using the concept of "profiles"

- Slot Profile – A physical mapping of ports onto a slot's backplane connectors
- Module Profile - Extends a slot profile by mapping protocols to a module's ports and defines physical dimensions
- Backplane Profile - Defines number and types of modules supported and their interconnection topology



Profile Name	Data Plane 4 FP	Expansion Plane P2/J2	Control Plane 2 TP	User Defined
	DP01 to DP04		CPtp01 to CPtp02	P3/J3, P5/J5
MOD6-PAY-4F1Q2T-12.2.1-1-cc	sRIO 2.2 at 3.125 Gbaud per Section 5.2	sRIO 2.1 at 3.125 Gbaud per Section 5.2	SpaceWire per Section 5.2.1	User Defined DIFF pins



[VITA-78]

Over 40 specific slot "profiles" define the backplane signal interconnection for different variants of these module types

SpaceVPX Challenges

It is possible to implement two different modules that are fully compliant with SpaceVPX yet cannot interoperate

- Modules with different form factor and depth complicate chassis implementation
- Even modules with identical slot profiles will not talk to each other if one uses SpaceWire and the other SRIO for datal plane network protocols

The immense flexibility of SpaceVPX can limit interoperability

- The standard defines modules with widely varying physical dimensions
  - Form factor (3U and 6U)
  - 4 options for module length
- **There are 48 separate slot profiles defined (not including variations in length and pitch)**
- SpaceVPX does not specify a single network protocols for the control and data planes
  - Possible options include SpaceWire, SpaceFibre, Serial RapidIO (SRIO), Ethernet
- User defined signals

Interoperability guidelines are needed to constrain the configuration, design choices and usage of SpaceVPX, enabling systems that can be composed of modules from different developers

- Ensure that NASA developed modules can be used across multiple missions and applications
- Allow industry to develop SpaceVPX modules that meet NASA mission needs

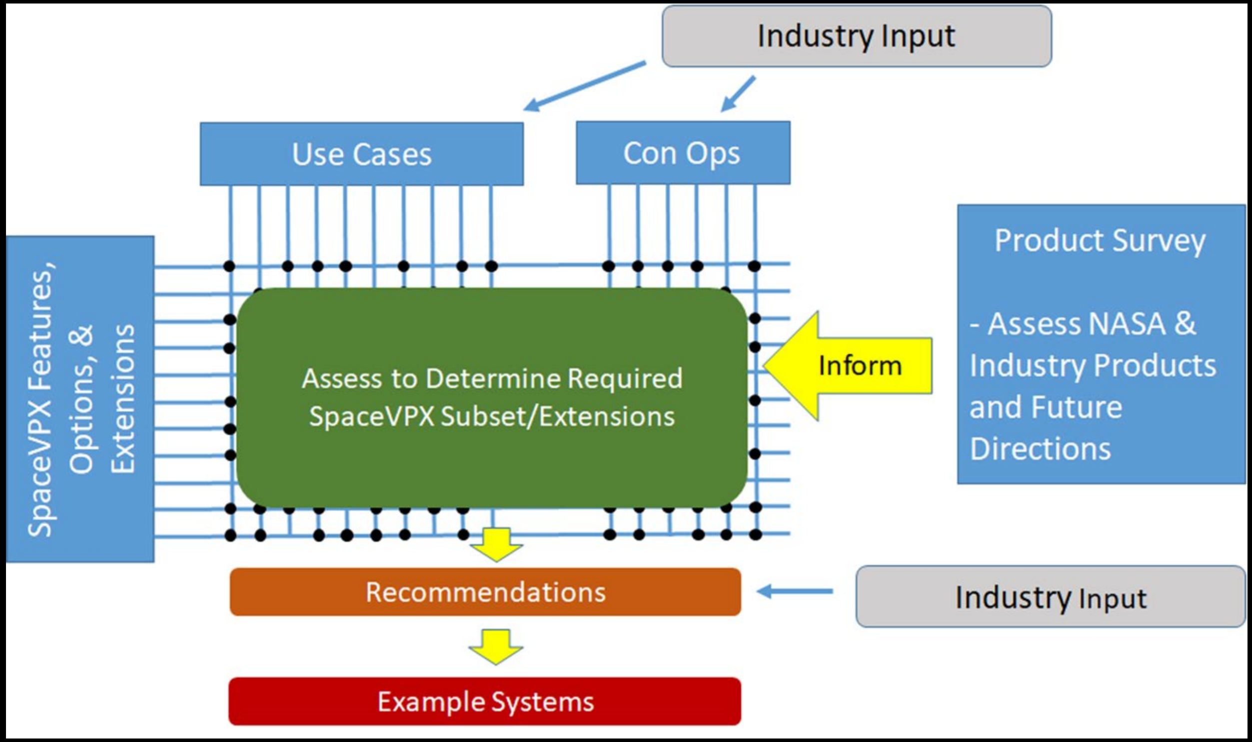
Other aspects of the SpaceVPX standard present challenges for NASA

- Required redundancy in several areas limits the development of single string systems
- Limits types of fault tolerance architectures and implementations (natively only supports dual redundancy, and does not map directly to other system level fault tolerance patterns)

NASA SpaceVPX Study Approach

The effort was divided into the following tasks:

- Notional use case analysis
- Product surveys
- Study focus area analysis
  - Interconnect
  - Power management and distribution
  - Form factor and daughtercards
  - Fault tolerance
- Engagement with other organizations
- Definition of proposed NASA SpaceVPX specification
- Identification of candidate modules
- Definition of example SpaceVPX systems



Study Approach

Use Case Analysis

Notional use case analysis provided an understanding of the breadth of implementations that SpaceVPX must accommodate and the features, capabilities, and interfaces that are needed to implement a broad range of NASA avionics systems

The following was assessed for each of the12 use cases

- Orbit / Destination
- Mission Criticality
- SWaP Sensitivity
- Block Diagrams
- Required Interfaces
- Timing and Deterministic Constraints
- Power Architecture
- Redundancy and Fault Management

Notional Use Case	Brief Description
Crewed Mission Avionics (*)	Implementation of Vehicle Control Unit (VCU) and Time Triggered Ethernet (TTE) switch
Crewed Mission Robotics and Surface Vehicle	Implementation of 'Robonaut type' avionics and lunar rover avionics
SmallSat	Combined C&DH and instrument processing in single chassis for an Evolved Secondary Payload Adapter (ESPA) -class mission
On-orbit Servicing, Assembly, and Manufacturing (OSAM)	Implementation of avionics for onboard servicing, assembly, and manufacturing robotics
Science Rover	Robotic science rover avionics
Precision Landing Processor	Implementation of the SPLICE DLC
High Data Rate Missions (3)	High bandwidth Synthetic Aperture Radar (SAR)
	Spectroscopy (based on EMIT mission concept)
	Advanced Earth observing hyperspectral instrument
Low/Medium Data Rate Mission	Generic telescope mission concept with moderate data rates (less than 0.5 Gbps)
Communication Relay Spacecraft	Orbital optical communication relay payload based on Laser Communication Relay Demonstration (LCRD)
HPSC A-Team Use Cases	A hybrid of autonomous planetary mission use cases derived from a JPL HPSC A-Team study

Use Case Analysis - Findings

	Finding
F-1	**While low SWaP is generally needed, 3U and 6U sizes were seen in the NASA use cases.**
F-2	**Module-to-module bandwidth of 10 Gbps envelopes the needs of NASA use cases.**
F-3	A SpaceWire control plane is needed by the majority of NASA use cases.
F-4	Low-rate interfaces (below control plane bandwidth) are needed to support simple modules without FPGAs.
F-5	**NASA use cases include both single string and redundant systems.**
F-6	**Due to SWaP considerations, some of the NASA use cases prefer a power management and distribution approach that differs from SpaceVPX.**

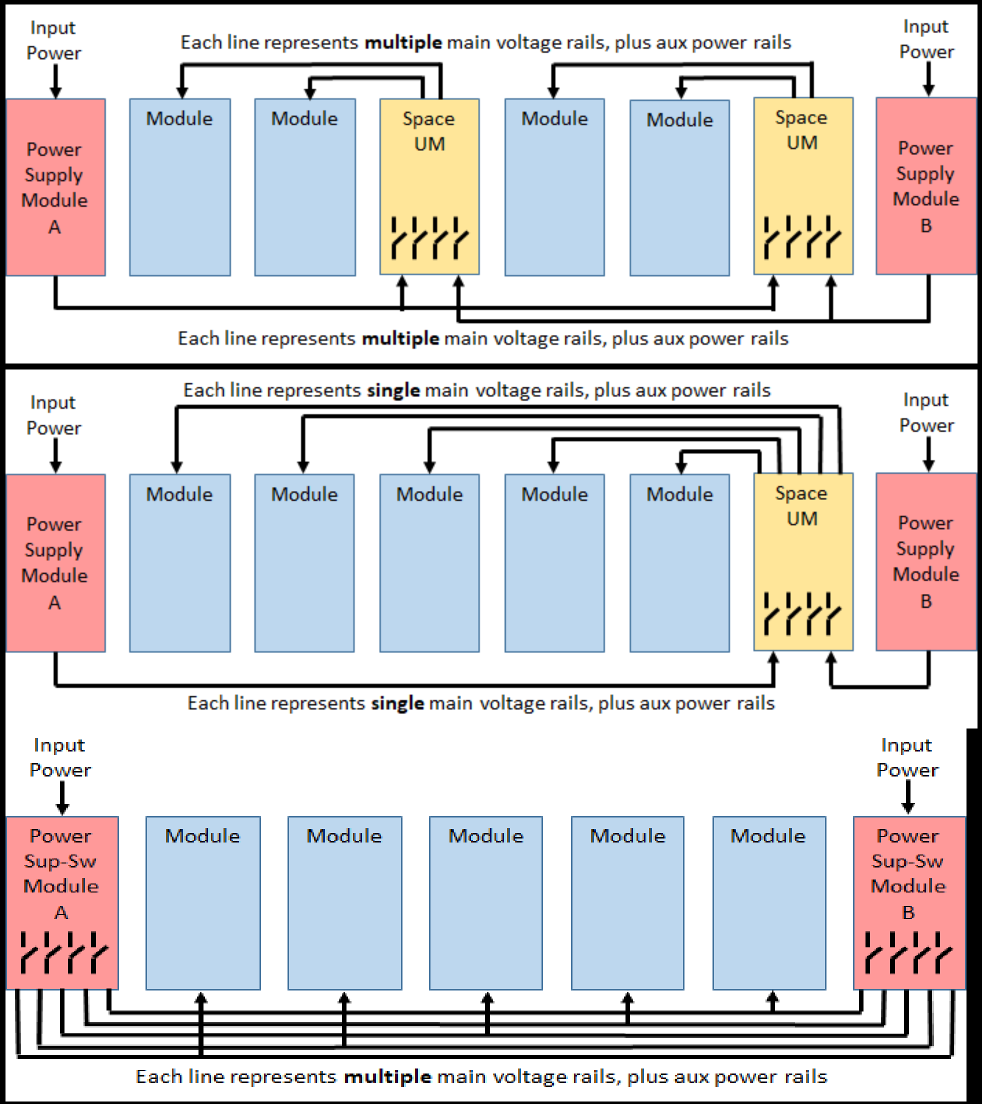
Product Survey - Findings

	Finding
F-7	**Industry lacks consensus on module interconnect and form factors, and this lack of consensus is limiting investment in product development.**
F-8	Industry is developing some 'SpaceVPX modules' that are not fully compliant with VITA-78.
F-9	**Industry SpaceVPX modules utilizing User Defined Space can hinder interoperability.**
F-10	Majority of industry SpaceVPX modules utilize SRIO for the data plane and SpaceWire for the control plane.
F-11	There is a lack of consensus among industry 'integrators' of SpaceVPX systems on the utility of cross strapped versus single string block redundancy systems.
F-12	Product survey suggests there is a market for SpaceVPX modules in 3U and 6U form factors.

Power Management and Distribution Analysis

- Three power architectures are supported in VITA-78 for 3U systems

Option		Pros	Cons
1	SpaceUM distributes main voltages to two modules (SLT3-SUM-2S3V3A1B1R1M4C-14.7.1)	Compatibility with existing 3U SpaceVPX modules	Most use cases require multiple SpaceUMs, which increases the chassis SWaP
2	SpaceUM distributes one main voltage to 5 modules (SLT3-SUM-5S1V3A1R1M3C-14.7.2)	Limits the number of SpaceUM modules needed	None noted
3	Split SpaceUM function between Power Supply-Switch (SLT3-PSS-6S3V3A1B-14.8.2) and Utility Switch	The use of 2 power supply-switch modules with a utility switch module can reduce the module count for redundant 3U systems	Uncertain that power converters and switches can fit into a single 3U module



Power Management and Distribution Analysis

- If the 5-output 3U SpaceUM is used, the main power bus voltage must be defined to ensure interoperability.

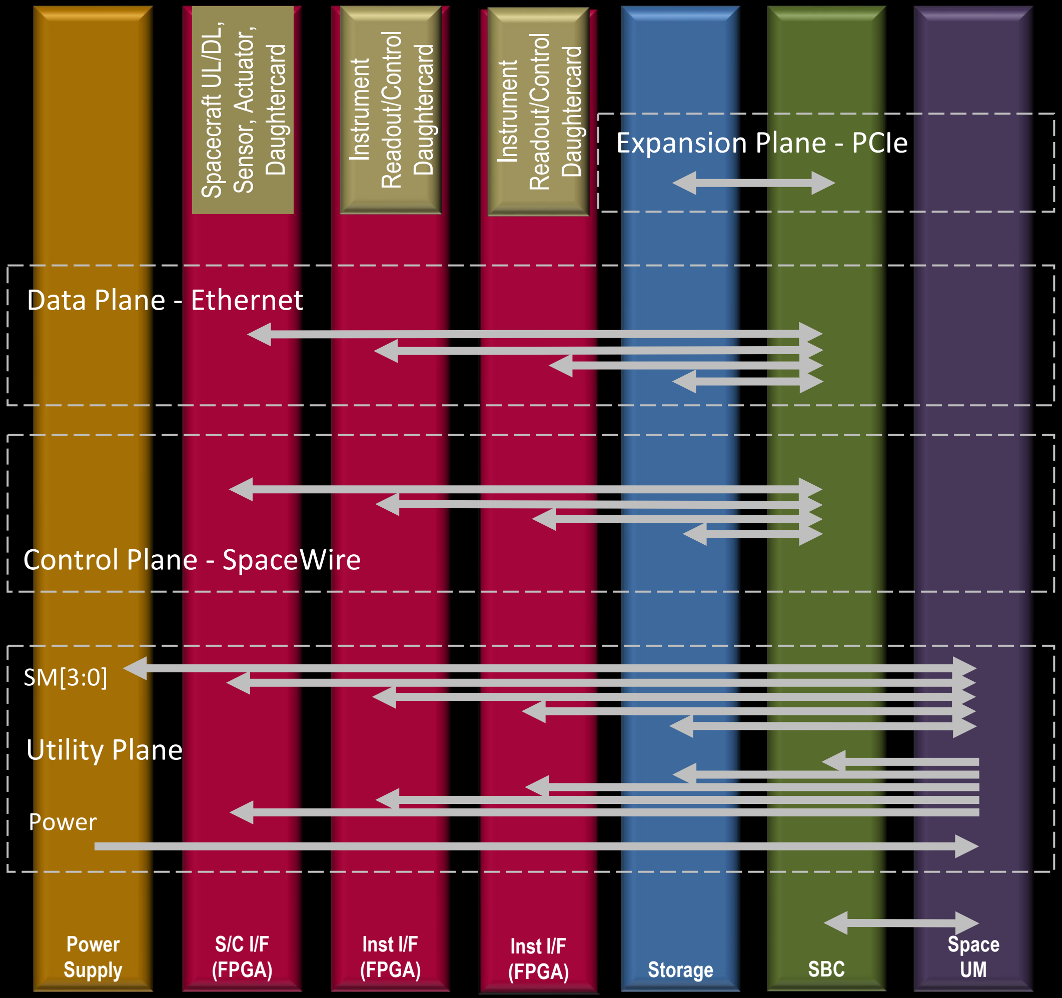
Option		Pros	Cons	Notes
1	3.3V	Can save voltage regulator, since most NASA systems use 3.3V on a card.	Total chassis power limit may be too low for some applications.	Total primary bus power limited to 120.45W*. Per module primary power limited to 66W*.
2	5V	Adopted by SPLICE.	May be divergent from industry trends.	Total primary bus power limited to 165W. Per module primary power limited to 100W.
3	12V	Consistent with non-aerospace trends. Provides maximum power. However, thermal may be the driving issue for power.	Limited selection of radiation hardened power converters support 12V input.	Total primary bus power limited to 438W. Per module primary power limited to 240W.
* Note that the 3.3V power supply module profile in VITA-62 provides 20A, which would limit total power to 66W.				

Power Management and Distribution Analysis - Findings

	Finding
F-13	**The needs of most 3U use cases cannot be met with the 2-output SpaceUM (SLT3-SUM-2S3V3A1B1R1M4C-14.7.1) but can be met with the 5-output SpaceUM (SLT3-SUM-5S1V3A1R1M3C -14.7.2).**
F-14	**The SpaceVPX standard power management and distribution approach supports interoperability, but constraints are needed on main bus voltage for the 5-output 3U SpaceUM.**
F-15	**The needs of 6U use cases can be met with the standard 8-output SpaceUM (SLT6-SUM-8S3V3A1B1R1M4C-10.8.1).**
F-16	While IPMI and DAP are specified in the SpaceVPX standard, a development SPC PMBus specification may offer system level features (i.e., controlled from within or outside of the SpaceVPX chassis) that can enable higher autonomy levels.
F-17	VBAT is included within VITA-78 for systems with batteries within the chassis but is not applicable to NASA systems.
F-18	The feasibility of implementing a 3U Power Supply-Switch module that can be achieved with the required number of power converters, switches, and control circuitry is uncertain.

Interconnect Analysis

- The SpaceVPX interconnect options outlined in VITA-78 were assessed for the various planes defined in the standard.
- These options were compared the needs of NASA use cases, technology trends within industry, and guidance from SMEs.
- This analysis led to the development of a notional block diagram that illustrates an instrument data system to show the interconnect between modules.
- Note that in determining recommended interconnect standards, the analysis was not bound by the options listed in VITA-78.
- Key interfaces include:
  - Ethernet with support for Time Sensitive Networking (TSN) - TSN is a set of standards that provides bounded latency interconnect for applications requiring determinism, allowing time sensitive messages to be transferred over Ethernet networks
  - PCIe
  - SpaceWire



Single String 3U Smallsat Avionics

Interconnect Analysis

- The High Performance Spaceflight Computing (HPSC) concept study phase significantly influenced the recommendations for SpaceVPX interconnect, and their evaluation of required processor features and interfaces also guided the recommended interconnect standards for the SpaceVPX backplane.
  - The SpaceVPX study also influenced some HPSC requirements.

- Key interfaces include:
  - Ethernet with support for Time Sensitive Networking (TSN) - *TSN is a set of standards that provides bounded latency interconnect for applications requiring determinism, allowing time sensitive messages to be transferred over Ethernet networks*
  - PCIe
  - SpaceWire

Interconnect Analysis

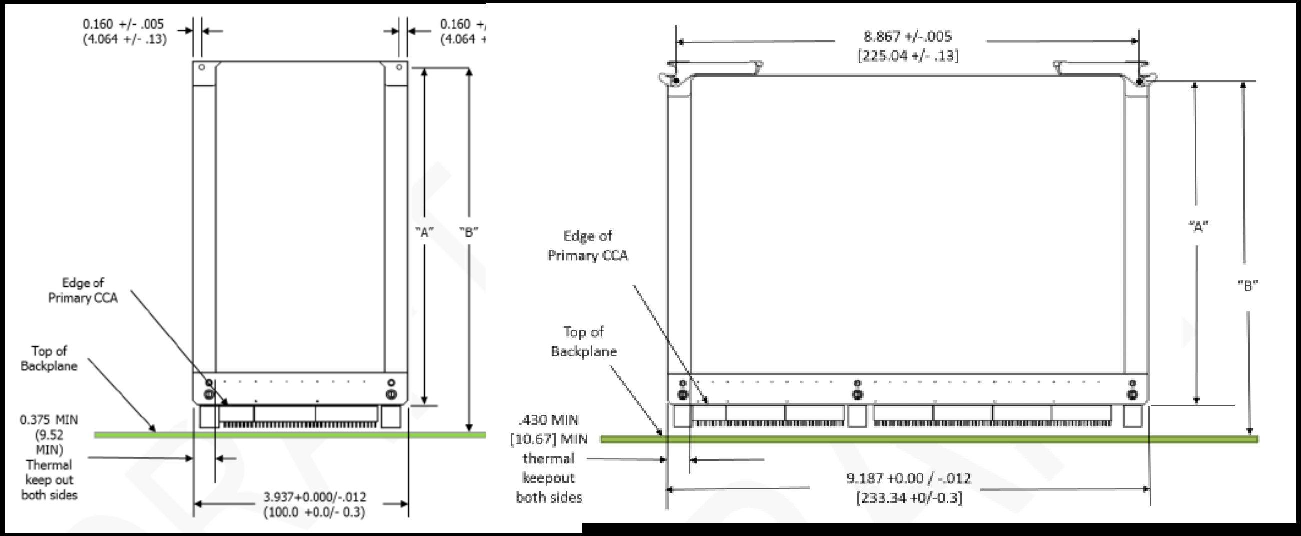
- Interconnect analysis addressed the following topics
  - Optimal interconnect standards for data plane, control plane, utility plane, and expansion plane
  - Additional low-rate interfaces for communication with simple modules
  - JTAG debug and test interface usage
  - Constraints on user defined signals to enable interoperability
  - Support for FPGA programming over the backplane
  - Utilization and allocation of interconnect on 3U and 6U modules
  - The extent to which backplane profiles influence interoperability
  - Signal integrity for high bandwidth signals
  - Backplane connector intermateability

Interconnect Analysis - Findings

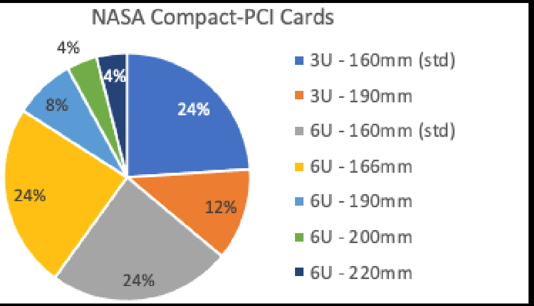
Finding	
F-19	In assessing the current VITA-78 data plane standards, SpaceFibre is a sole source solution with limited spaceflight usage, and the SRIO standard lacks industry support.
F-20	**TSN, which leverages Ethernet and is defined in multiple IEEE 802.1 standards, has broad industry engagement and support.**
F-21	**The HPSC project does not require native support for SRIO, SpaceFibre, or TTE, although these and other non-native I/O protocols can be provided at the board level using external circuitry.**
F-22	The I2C bus provided within the utility plane is capable of handling PMBus functions within the SpaceVPX chassis.
F-23	12.5 Gbps SERDES signals can be supported with a trace length of 13.5 inches, two SpaceVPX connectors, and a 22-layer printed wiring board (PWB) using Arlon material.
F-24	The VITA-78 standard allows for user defined signals to provide flexibility, but their use can hinder interoperability.
F-25	There is need to provide industry standard JESD204 interfaces to high bandwidth ADCs and DACs in excess of 1 gigasample per second (GSPS).
F-26	There is need for a low-rate I2C interface (i.e., below SpaceWire bandwidth) to provide connectivity to simple modules that can be implemented without an FPGA.
F-27	**While system management is provided via IPMI or DAP on the System Management Bus, and JTAG is included to support testing, SpaceVPX does not define a system-level test and debug scheme.**
F-28	**Industry trends are to combine control and data flow traffic on a single high-bandwidth onboard network, and one product survey respondent recommended combining control and data plane functions on SpaceFibre links.**
F-29	There are four vendors of SpaceVPX connectors, but only two offer connectors that can intermate.

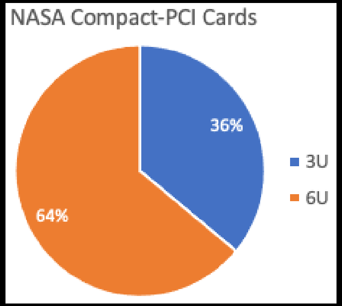
Form Factor and Daughtercard Analysis

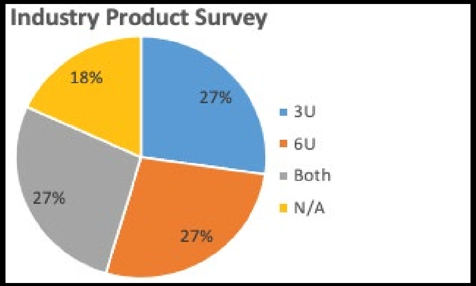
- Previous NASA missions were assessed to determine the module sizes that were used.
- Industry product surveys and use case analysis also provided data on module sizes.
- Current NASA SpaceVPX development is focused on 3U modules with a module length of 220mm.
  - SPLICE (JSC)
  - SpaceCube-V3 (GSFC)

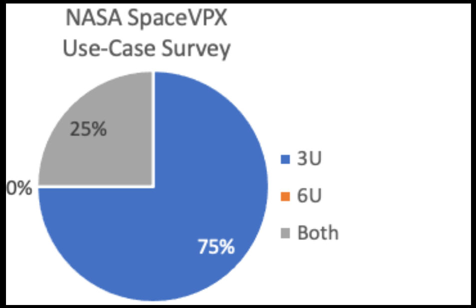


3U and 6U Slot Dimensions [VITA-78]



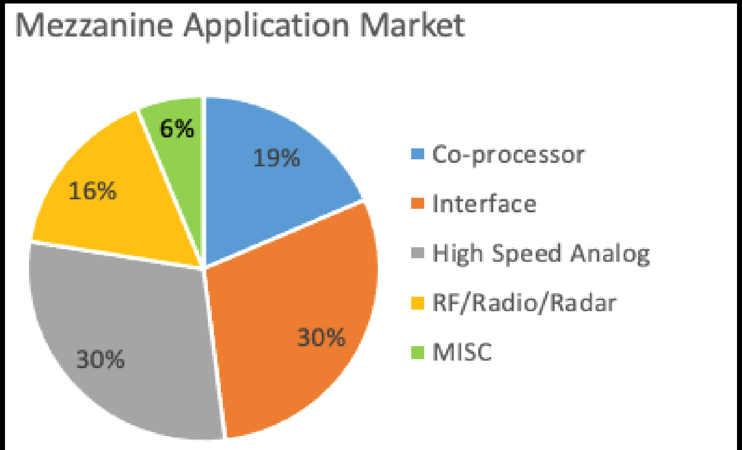


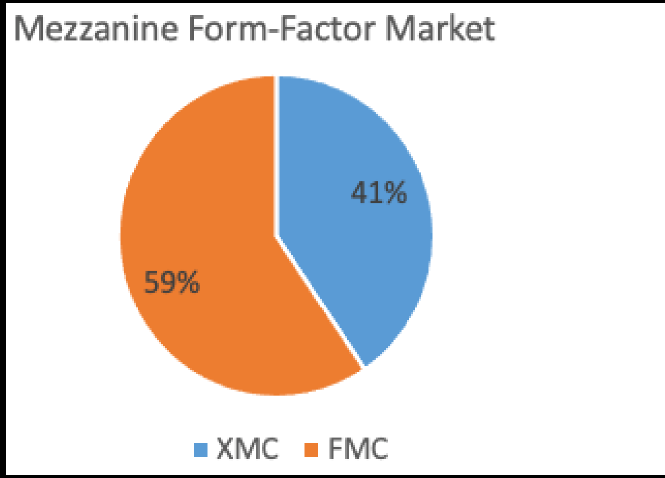




Form Factor and Daughtercard Analysis

- Daughtercards on SpaceVPX modules can provide mission unique functionality and front panel interfaces
- Within industry, the FPGA Mezzanine Card (FMC) [VITA-57.1] and Switched Mezzanine Card (XMC) [VITA-43 and 61] standards are used
- An industry survey assessed to usage and prevalence of each of these standards
- Potential SpaceVPX Daughtercard Configurations
  - A 3U base card is capable of supporting 1 x FMC, or 1 x XMC daughtercard
  - A 6U base card is capable of supporting 3 x FMC, or 2 x XMC daughtercards





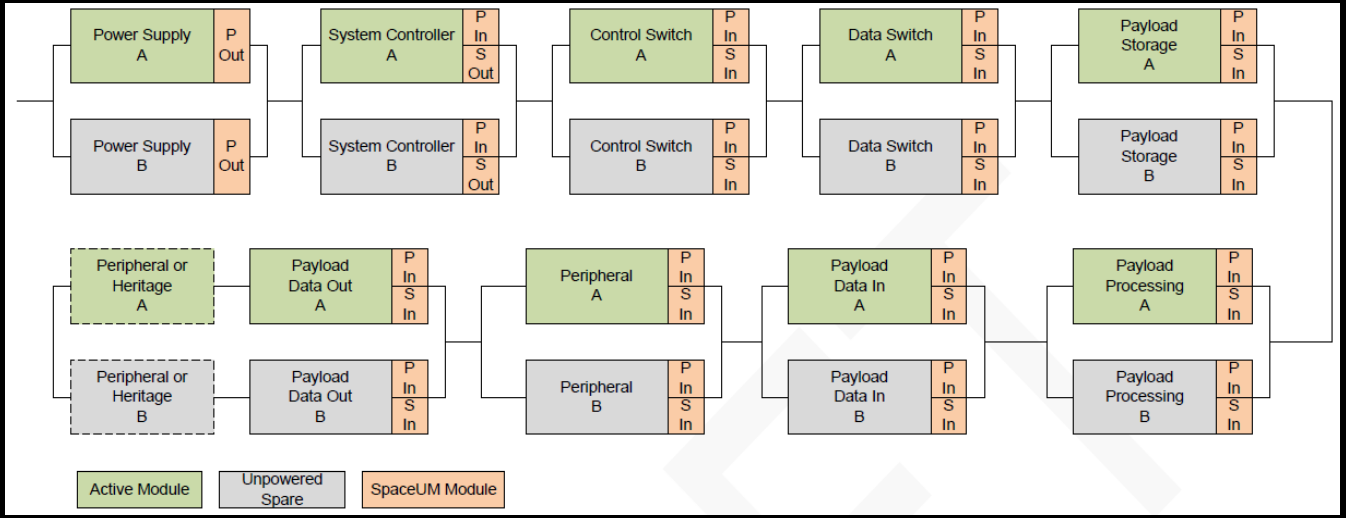
Form Factor and Daughtercard Analysis - Findings

	Finding
F-30	Commercial industry (COTS) has more FMC than XMC offerings, with the application market for mezzanine/daughtercards being interface and high-speed analog.
F-31	**NASA subsystems utilizing a backplane standard (i.e., VME, cPCI, SpaceVPX) will typically select a width (e.g., 3U, 6U, 9U) and customize the card length in a chassis to minimize SWAP-C.**
F-32	**The 3U 160mm module size is limiting for implementing processor boards with large processor packages and multiple memory banks. Project use cases at NASA (e.g., SpaceCube-V3 and SPLICE DLC) use the 3U 220mm SpaceVPX form factor.**

Fault Tolerance Analysis

- Analysis explored the following questions related to SpaceVPX fault tolerance:
  - Are the mechanisms sufficient for use cases?
    - *The mechanisms within SpaceVPX that support FDIR and redundancy management are effective building blocks to support all NASA use cases*
  - Are they sufficient for mission critical systems (i.e., systems within Class A, human-rated, or high-profile missions)?
    - *The VITA-78 standard does not inherently provide the necessary fault detection and isolation required for these applications*
    - *However, system could potentially be implemented within a single SpaceVPX chassis or across multiple chassis that could provide the necessary fault detection and isolation*
  - Are they sufficient for low SWaP constraints?
    - *SWaP constrained systems may drive the use of systems on chips (SoC) which can have several redundancy strategies available within a single device*
    - *For SWaP constrained systems, it is possible that for some missions the desired reliability can be met without invoking the explicit fault tolerance mechanisms defined in SpaceVPX*

Fault Tolerance Analysis - Findings



- VITA-78 Section 1.7 includes the typical SpaceVPX reliability model diagram
- Since the SpaceUM controls individual power and management signal distribution to the modules, SpaceUM failures can dominate the cut sets for fault tree analysis
- Essentially, a SpaceUM failure results in loss of redundancy

	Finding
F-33	Since the SpaceUM controls individual power and management signal distribution to the modules, SpaceUM failures can dominate the cut sets for fault tree analysis.
F-34	The mechanisms within SpaceVPX that support FDIR and redundancy management are effective building blocks to support all NASA use cases.

Engagement with Outside Organizations

	Finding
F-35	There is a recognition within other government agencies that SpaceVPX as specified in VITA-78 presents interoperability challenges, and interest in collaborating to refine the specification to address those challenges.

Proposed NASA SpaceVPX Specification

	Proposed NASA Specification
RT-1	**General** Support dual redundant and single string SpaceVPX systems.
RT-2	**Power distribution and management** Utilize the 5-output SpaceUM (SLT3-SUM-5S1V3A1R1M3C-14.7.2) for 3U implementations with a 5V main power voltage. Utilize the 8-output SpaceUM (SLT6-SUM-8S3V3A1B1R1M4C-10.8.1) for 6U implementations with +12, +5, and +3.3 main supply voltages.

RT-3	**Interconnect**
	Support the following interconnect protocols:
	• Data Plane – Support for Ethernet 10GBASE-KR as specified in IEEE 802.3ap with support for TSN as specified in IEEE 802.1AX, CB, AS, Qbv, Qav, Qci, Qcc, and 802.1Q clauses 8.6.5.1 and 8.6.8.2
	• Control Plane - SpaceWire as defined in ECSS-E-ST-50-12C
	• Expansion Plane – JESD204C
	• Expansion Plane – Support for PCIe Gen 3.1
	• Utility Plane – IPMI and DAP as specified in VITA-78
	• User Defined signals with the requirement that they are user programmable
	    • SERDES.- 1600mV peak-to-peak AC-coupled differential signaling; 8b/10b encoding; data rates of 1.25 Gbps, 2.5 Gbps, 3.125 Gbps, 5 Gbps, 6.25 Gbps, and 10 Gbps (note that some modules may not support all of these rates)
	    • Single ended - 2.5V LVCMOS signaling
	• Low-Rate Interconnect – I2C
	• JTAG
	• Provide pin on a front panel to disable JTAG for flight.

Proposed NASA SpaceVPX Specification

	Proposed NASA Specification
RT-4	**Form Factors and Daughtercards** Support 3U and 6U – 220mm form factors. Support for XMC and/or FMC daughtercards on SpaceVPX FPGA-based modules. Combined 3U/6U chassis as needed.
RT-5	**Fault tolerance** Adopt fault tolerance methodologies as defined in VITA-78.
RT-6	**Backplanes and Chassis** Use VITA-78 identified passive backplanes.
RT-7	**Connectors** Utilize SpaceVPX module and backplane that comply with VITA-46.
RT-8	**VITA-78 features not be used to ensure future interoperability** • Specified chassis and backplane profiles. • SRIO on data plane (can be implemented with User Defined SERDES). • SpaceFibre on data plane (can be implemented with User Defined SERDES). • System Controller interfacing to 4 SpaceUM modules (recommendation is 2). • Support for heritage cPCI modules. • Support for 2-output 3U SpaceUM (SLT3-SUM-2S3V3A1B1R1M4C-14.7.1). • Support for VBAT voltage. • System management discrete input and output interfaces. • Full latitude on user defined signal usage .

Proposed NASA SpaceVPX Specification

The following features are proposed that are not currently in VITA-78:

- Explicit support for single string systems
- Using Ethernet/TSN for data plane
- Use of PCIe 3.1 for expansion plane
- JESD-204C support for high bandwidth digitizers
- Constraints on user defined signals
- Explicit daughtercard support

Candidate Module Definitions

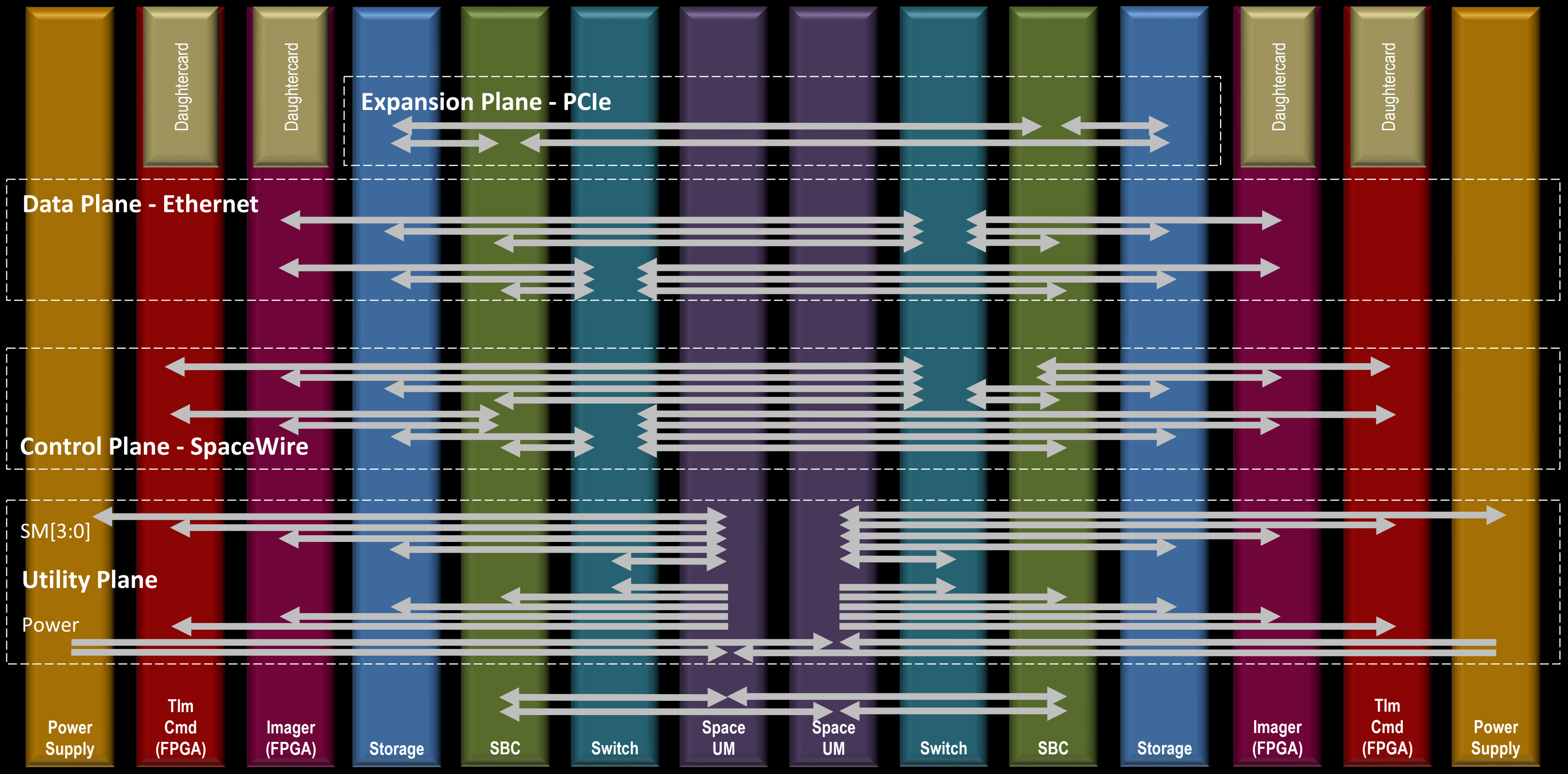
Based on the use cases and the proposed NASA SpaceVPX specification, candidate modules were defined

- Single Board Computer (SBC)
- Storage
- High Density FPGA
- Digitizer
- Low Density FPGA
- Switch

Example Systems

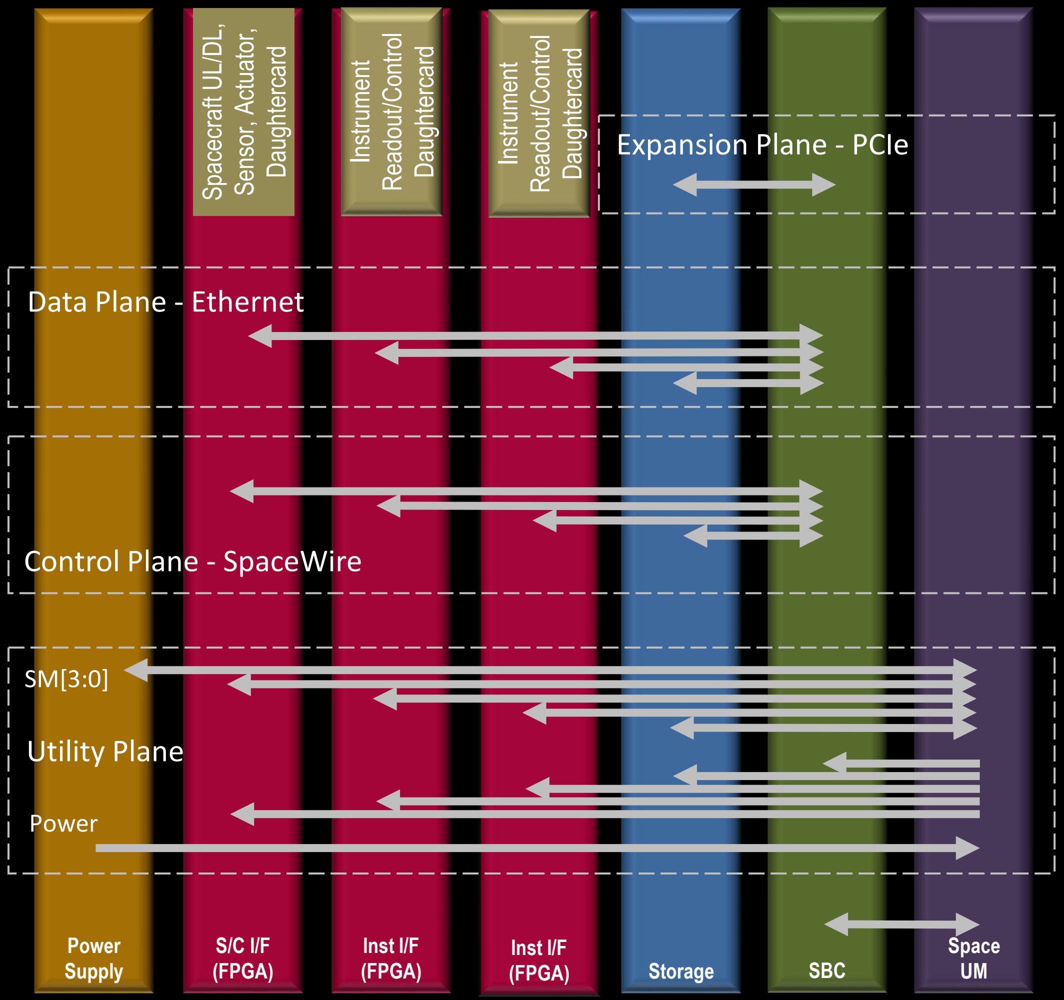
Based on the candidate module definitions and proposed NASA SpaceVPX specification, example systems were defined

- Redundant 3U system
- Single string 3U systems (smallsat avionics, instrument controller)
- Minimalist systems
- Interim systems supporting legacy cPCI modules



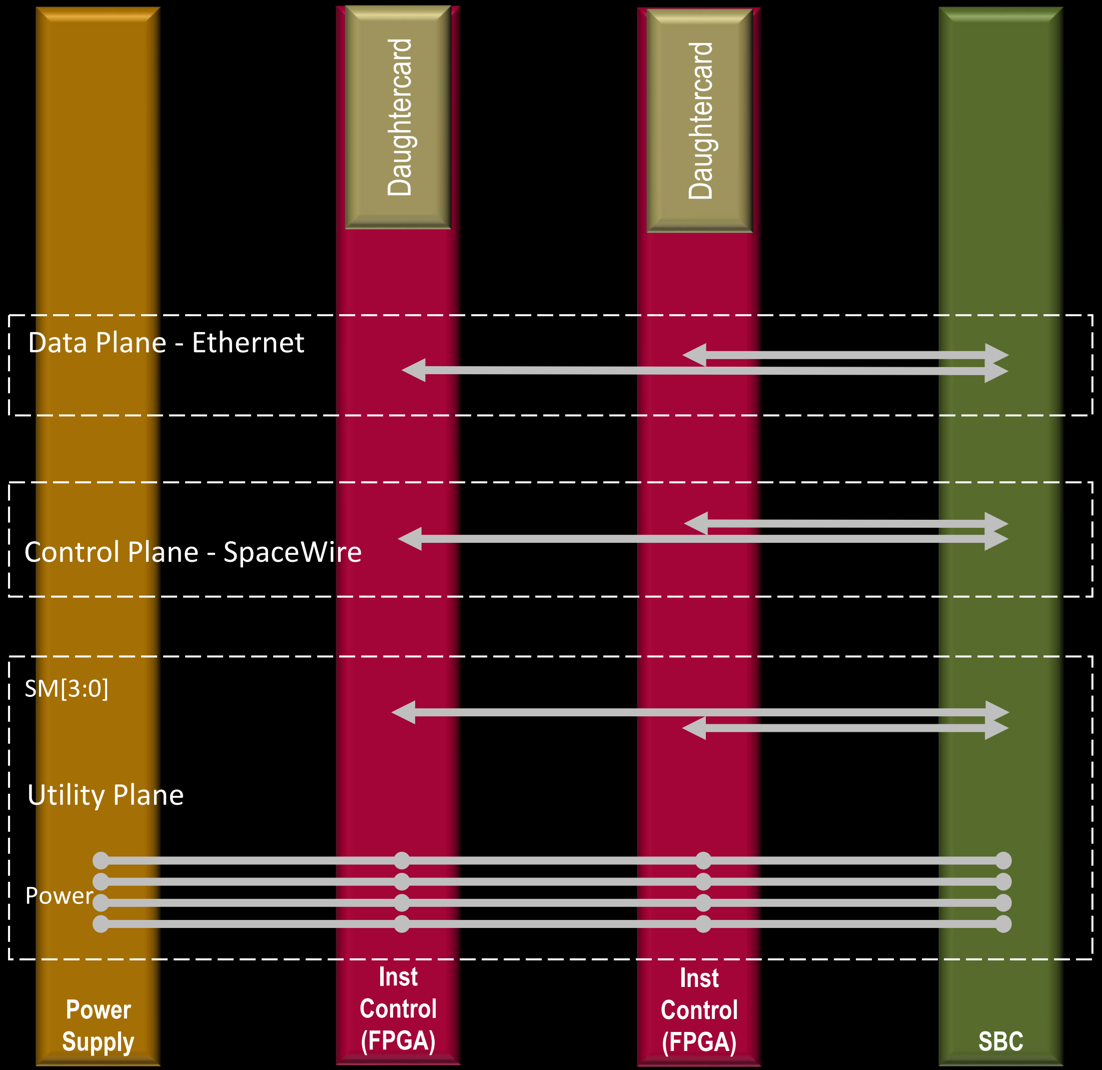
Redundant 3U System

Example Systems



Single String 3U Smallsat Avionics

Example Systems



Minimalist System

Recommendations

	Recommendation	Traceability
R-1	NASA projects and programs should standardize the use of SpaceVPX for NASA avionics systems as defined in the proposed NASA SpaceVPX specification.	
R-2	NESC and STMD should develop a NASA standard SpaceUM module architecture and reliability model.	F-33
R-3	NESC and STMD should engage with industry, other government agencies, and the SOSA™ Consortium on revision to VITA-78, and refine the module definition and interoperability (see Appendix B) and daughtercard use.	F-7, F-8, F-9, F-35
R-4	NESC and STMD should conduct a follow-on study, in collaboration with other government agencies, for a next generation avionics architecture (i.e., beyond SpaceVPX), addressing: (a) simplified interconnect with data streams combined into fewer planes, (b) alternative power management and distribution options, (c) possible adoption of PMBus, (d) support for a broader set of fault tolerance methodologies, (e) hierarchical system-level self-test and debug architectures, and (f) module-level interchangeability and reuse across NASA systems.	F-6, F-16, F-27, F-28

In Closing …

NASA has recently completed a study to assess SpaceVPX interoperability challenges and define a proposed solution

- Using the NASA study recommendations as a starting point for discussion, NASA would like to engage with the spaceflight avionics community to determine if consensus can be readily achieved on developing a SpaceVPX VITA78 ‘dot spec’ that enhances interoperability

- We welcome your input!

Questions?

Acronym List

AC	Alternating Current	I/O	Input/Output	POL	Point of Load
cPCI	Compact Peripheral Component Interconnect	JESD	Joint Electron Device Engineering Council Standard	SBC	Single Board Computer
C&DH	Command and Data Handling	JPL	Jet Propulsion Laboratory	SERDES	Serializer Deserializer
DAP	Direct Access Protocol	JTAG	Joint Test Action Group	SPLICE	Safe and Precise Landing – Integrated Capabilities Evolution
DLC	Decent and Landing Computer	LCRD	Laser Communication Relay Demonstration	SRIO	Serial RapidIO
EMIT	Earth Surface Mineral Dust Source Investigation	LEO	Low Earth Orbit	STMD	Space Technology Mission Directorate
ESPA	Evolved Expendable Launch Vehicle (EELV) Secondary Payload Adapter	LVCMOS	Low Voltage Complimentary Oxide Semiconductor	SWaP-C	Size Weight and Power, and Cost
FPGA	Field Programmable Gate Array	mV	Millivolt	TTE	Time Triggered Ethernet
FMC	FPGA Mezzanine Card	NASA	National Aeronautics and Space Administration	TSN	Time-Sensitive Networking
Gbps	Gigabits Per Second	NESC	NASA Engineering & Safety Center	VCU	Vehicle Control Unit
IEEE	Institute of Electrical and Electronics Engineers	OSAM	On-Orbit Servicing Assembly and Manufacturing	VITA	VMEbus (Versa Module Eurocard Bus) International Trade Association
IPMI	Intelligent Platform Management Interface	PCIe	Peripheral Component Interconnect Express	XMC	Express Mezzanine Card

Backup

Observations

	Observation
O-1	There is no standardized approach or best practice for FPGA programming and management based on a firm understanding of the current and emerging FPGA configuration options.
O-2	There are potential JTAG security vulnerabilities to NASA missions that have not been fully assessed.
O-3	During the SpaceVPX connector analysis, potential issues were raised regarding the attachment of SpaceVPX connectors to printed wiring boards.

Problem Statement – Defining Interoperability

- Within the context of this study, interoperability is defined as the ability for a set of SpaceVPX modules to function coherently within SpaceVPX chassis as a systems for a wide range of NASA use cases.

- Interoperability of SpaceVPX modules implies:
  - Standard power interfaces
  - Standard form factors and dimensions
  - Standard interconnect protocols for the utility, control, data, and expansion planes
  - Restricted user defined signal usage

- The chassis and backplane profiles defined in the SpaceVPX standard are not addressed in this study
  - Given the SWaP constraints of most NASA missions, it is assumed that the chassis and backplane will be designed to missions specific requirements. Hence, it is not practical to define standard NASA chassis and backplane profiles.

- It is understood that some missions may require bespoke SpaceVPX modules and implementations that are inconsistent with the recommendations of this study.
  - The study team has assumed an "80%/20%" figure of merit, where the recommendations would enable 80% of missions and the remaining 20% would require more custom implementations.

- Note that there are degrees of interoperability that are not addressed by the recommendations of this study, including:
  - "Plug and play", where device discovery enables dynamic system configuration
  - "Interchangeability", where modules from different vendors are ensured to have identical functionality and feature sets
  - Interoperability above Layer 2 (Data Link) of the OSI stack

Problem Statement – Achieving Interchangeability

- Beyond interoperability, common sparing of avionics modules for crewed missions can be enabled by interchangeability.

- Achieving interchangeability requires:
  - Common form factors
  - Common interfaces (connector types, pin assignments, signaling levels and timing, and messaging formats and protocols)
  - Common functionality and feature set

- Within SpaceVPX, a necessary step towards interchangeability is the definition of standard module profiles for specific types of modules.

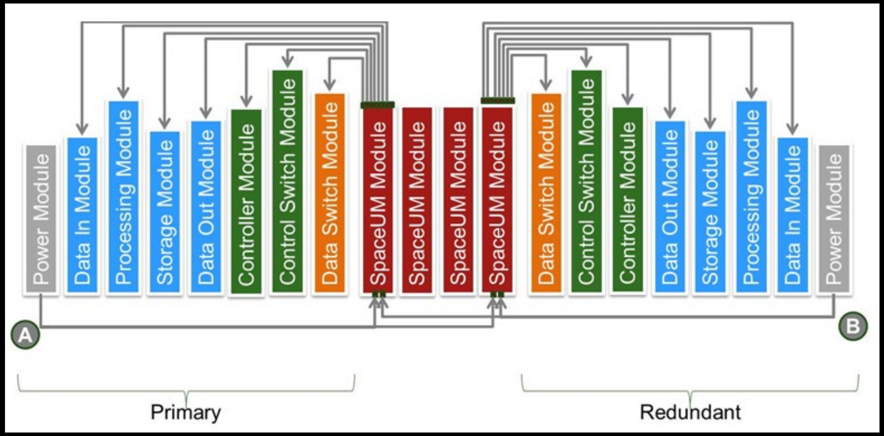
- However, interchangeability requires the specification of communication between modules at higher-levels than is defined in VITA-78.

- Interchangeability may be difficult to achieve for computing modules, in that it would require software portability.

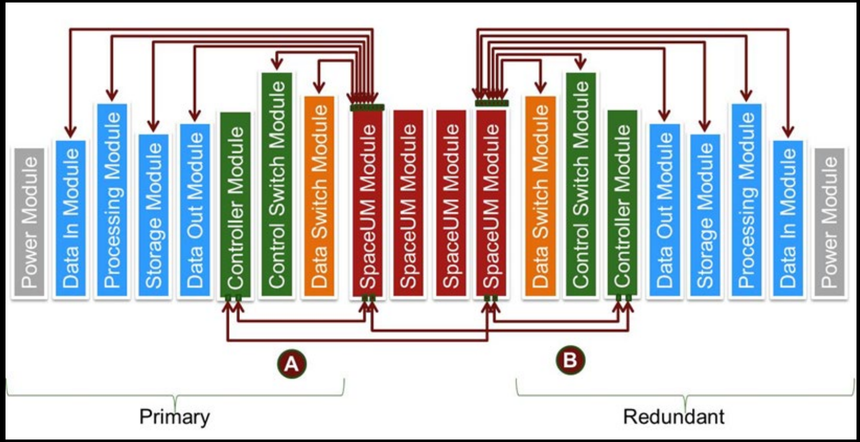
- While the proposed SpaceVPX implementations of this study do not ensure interchangeability, guidance is provided in an appendix on candidate module profiles that can be starting points for further studies to achieve module profile standardization.

Background: SpaceVPX

- SpaceVPX implements a dual redundant system
- Redundant power supplies feed power to SpaceUM modules
- Redundant System Controllers, which manage the functionality of the SpaceVPX chassis, provide control signals to SpaceUM modules
- SpaceUMs select between redundant power supplies and System Controllers, and distributes switched power and control signals radially to each of their modules



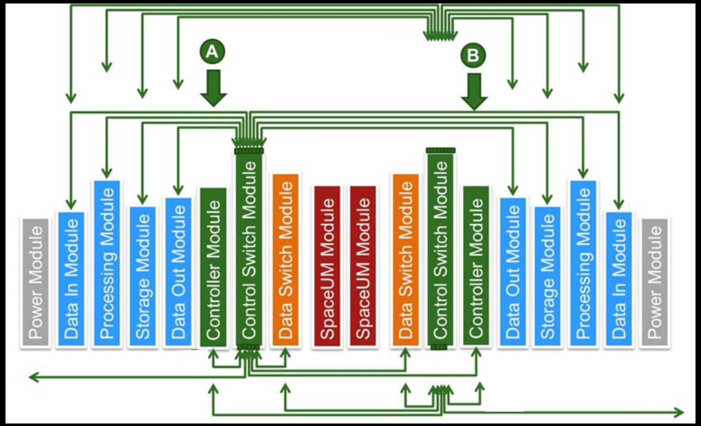
Power Plane



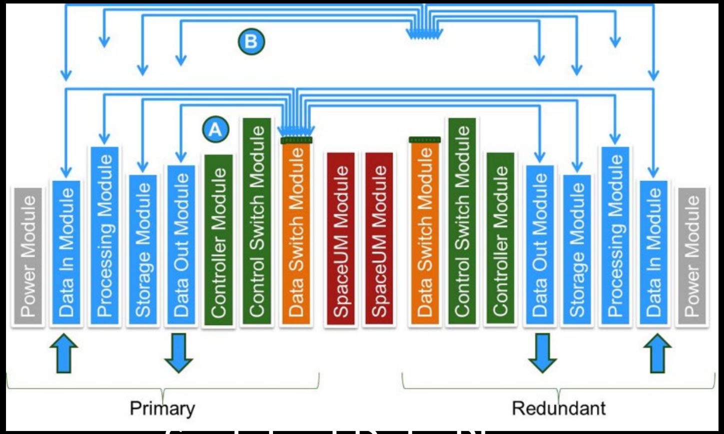
Utility Plane

Background: SpaceVPX

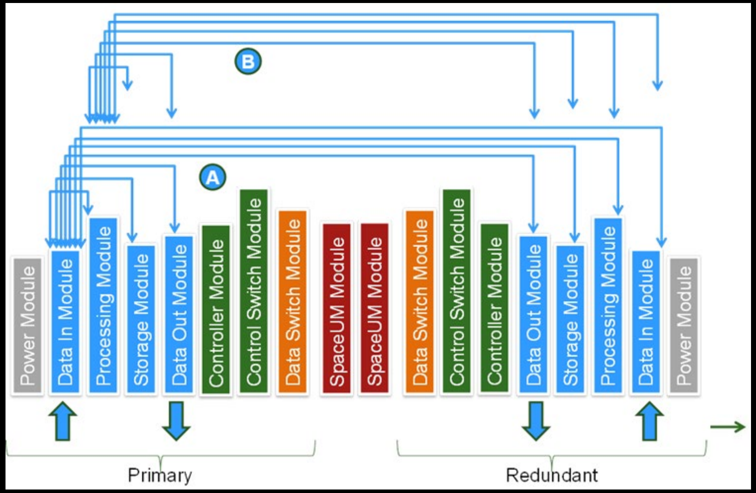
- System Controller sources the control plane, which is provided to each module radially from a Control Switch Module
- Data plane can use a switched topology, mesh topology, or a hybrid topology (not shown)



Switched Control Plane



Switched Data Plane



Mesh Data Plane

Background: SpaceVPX

- Selects between redundant power supplies and provides switched power for up to 5 modules (8 modules for 6U)
- Selects between System Controller and provides control signals for up to 5 modules (8 modules for 6U)
- Provides processing to:
  - Switch power and distribute signals to modules based on commands from the System Controller
  - Aggregate module status and provide to the System Controller