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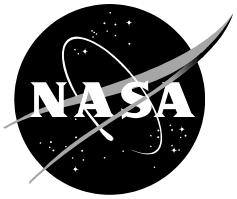

Guidelines for Screening, Lot Acceptance, and Derating for Polymer Tantalum Capacitors

Alexander A. Teverovsky

January 2023

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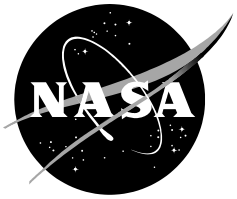

Guidelines for Screening, Lot Acceptance, and Derating for Polymer Tantalum Capacitors

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Guidelines for Screening, Lot Acceptance, and Derating for Polymer Tantalum Capacitors

1. Scope.

These guidelines have been developed for NASA space projects that are planning to use new technology hermetic and chip polymer cathode tantalum capacitors. Polymer Tantalum Capacitors (PTC) selected from MIL-PRF-32700, automotive grade (AEC-Q200) parts, or COTS+ (hi-rel COTS) capacitors should be screened and qualified as suggested in Tables 1-3 and derated per section 9 below. Screening and lot acceptance tests that were carried out for a lot that is intended for flight as a part of the manufacturing process do not need to be repeated.

Contents

2. Background and benefits of using PTCs

Evolution of tantalum capacitors goes in the direction of further improving volumetric efficiency, reducing equivalent series resistance (ESR), and increasing operating voltages. ESR is one of the most important characteristics of the parts as it determines the rate of energy delivery in the pulse-power systems and the level of ripple currents and voltages when capacitors are used for filtering in power lines. A substantial reduction of ESR has been achieved with the introduction of PTCs that employ conductive polymers as a replacement of MnO2 cathode materials in traditional chip tantalum capacitors. Manganese oxide has resistivity about 1 ohm_cm, while the resistivity of the used conductive polymers is approximately 10 times less.

Other benefits of using PTCs compared to MnO2 capacitors include a safe failure mode (no ignition), higher ripple currents, and higher frequency of operation. A smaller concentration of defects in the dielectric of PTCs results in higher breakdown voltages and less probability of infant mortality (IM) failures. The latter is due to less stressful conditions of the cathode formation. Also, PTCs, like MnO2 capacitors have a high radiation tolerance, up to 5 Mrad (Si).

A better performance and improved quality and reliability of chip polymer tantalum capacitors (CPTC) that had been achieved over the last years, made these parts not only preferred components for many commercial applications, but their employment had begun in reliability-demanding automotive, medical, military, and space systems. Currently, commercially available CPTCs have rated voltages up to 100 V and operating temperatures up to 150 °C.

Substantial efforts have been made to demonstrate compliance of CPTCs with the automotive industry requirements, AEC-Q200. A military specification for CPTCs, MIL-PRF-32700, was released in 2022 and there are several DLA drawings for commercial PTCs, e.g. 04051/52, 13030, 20021. However, these documents do not fully address issues with PTCs that might pose risks for space applications, particularly in vacuum conditions. Issues that are specific to PTCs are discussed below, and possible mitigation of the relevant risks is described in the screening, lot acceptance, and derating sections of these guidelines.

A system of screening and qualification tests in military specifications is supposed to assure reliability of components at rated conditions. Also, MIL parts are expected to operate reliably during any applications within the specified conditions. This level of confidence in quality assurance is not expected for commercial components without extensive additional tests. However, development of military specifications takes years and years more are required to start production. This timeframe might not be acceptable in a world with fast growing new technology components. A solution to this problem might be the development of screening and qualification procedures for specific space application conditions based on understanding of potential reliability issues with the part, assessments the reliability acceleration factors, and analysis of the project's Mission, Environment, Applications and Lifetime (MEAL) requirements. These guidelines are an attempt to create such procedures for polymer tantalum capacitors.

3. Specifics of PTCs

The first polymer tantalum capacitors (late 1990's) were manufactured using in-situ polymerization of poly(3,4)ethylenedioxythiophene (PEDOT) by chemical reactions between the oxidizer and monomer. A breakthrough technology in PTCs was achieved by introducing a water-soluble poly-styrene sulfonate (PSS) in the polymer composition and formation of pre-polymerized PEDOT:PSS systems. This new technology and material, that have been available since 2009, allow for development of capacitors with high voltage ratings up to 125 V, that could not be realized by old technology that employs MnO2 as a cathode material.

Although the size of particles in slurries of the pre-polymerized PEDOT/PSS is low, ~ 30 nm, it is still too large to penetrate the pellet of high-CV value capacitors and assure full surface coverage of the Ta2O5 dielectric. For this reason, the majority of capacitors rated to 10 V and less are manufactured using in-situ polymerization process. In many cases, a combination of the in-situ polymerization and pre-polymerized polymers, so called hybrid technology, is used. According to this technology, the first layers during cathode formation are made using in-situ PEDOT polymer that covers the whole surface of the Ta2O5 dielectric, including pores of the slug. Then, several layers of pre-polymerized PEDOT/PSS compositions are applied to form a relatively thick coating over the shell area of the tantalum slug. Some additives to the compositions might be used to further improve characteristics of conductive polymers and capacitors. Variety of the materials and processes used to form cathode electrodes of capacitors is greater for PTC technology compared to conventional MnO2 technology, and results in larger variations of behavior and reliability of PTCs. This complicates generalization of test results and requires a thorough quality control for each lot of capacitors.

In some instances, problems with PTCs are caused by the same features as their benefits. For example, a smaller concentration of defects in the dielectric and lower probability of IM short circuit failures do not allow using the Weibull Grading Test (WGT) that had been developed to screen out defective parts and determine the failure rate (FR) for MnO2 capacitors. Instead, a regular burn-in (BI) is used to reduce IM failures, highly accelerated life testing (HALT) is used to assess reliability acceleration factors, and life testing is used to assess FR for PTCs.

Other specifics of behavior that are different compared to MnO2 capacitors include:

- Reaction to environments (moisture and vacuum).
- Degradation at high temperatures.
- Anomalous transients (new phenomenon).
- Instability of leakage currents.
- Prevalence of wear-out (WO) failures during HALT.

3.1. Effect of environments

The presence of moisture in environments affects characteristics and behavior of PTCs to a much greater degree compared to MnO2 capacitors. For this reason, preconditioning before testing to assure dry conditions of the part is critical for proper screening and qualification of polymer capacitors for space applications.

Moisture absorption increases capacitance of the parts, and this increase is substantially greater for polymer compared to MnO2 capacitors. After saturation with moisture at 85 °C and 85% RH, that typically takes ~ 100hr, capacitance in CPTCs increases on average by 26.6% ± 8%, whereas in MnO2 capacitors the increase is approximately 10 times less, 2.5% ± 1.1%. This means that contrary to MnO2 technology, manufacturing parts with 10% and even 20% of capacitance tolerance for CPTCs might be a challenge.

Prolonged exposure to humid environments can increase ESR and cause leakage current failures. Due to the acidic reaction of PSS, long-term biased operation in the presence of moisture might result in failures related to corrosion and migration of copper from the lead frames. For this reason, substantial efforts have been made by manufacturers to improve moisture resistance of CPTCs and current automotive grade capacitors can pass biased testing at 85 °C and 85% RH for 1000 hours.

Variations of moisture content cause reproducible alterations of capacitance between minimal (after 24hr bake at 125 °C) and maximal (after one week at 85 °C and 85% RH) values. This allows for employing slugs in capacitors as moisture sensors as the kinetics of moisture diffusion can be assessed by variations of capacitance with time of exposure to humid or dry environments. Examples of variations of the characteristics of PTCs at different environmental conditions are shown in Fig. 3.1. The characteristic times of moisture desorption increases exponentially with temperature. The activation energy of this process is in the range from 0.4 to 0.5 eV. In most cases, the bake-out time necessary to assure dry conditions of the slug is 24 hours at 125 °C.

Storage in humid environments does not change ESR substantially, and for most lots of CPTCs, this parameter remains below 3X of the initial limit even after 1000 hours of storage. Variations of the dissipation factor, DF, with time of moisture sorption or desorption go through maximum, and in some cases, the level of DF_{max} exceeds 10%, which is typically the limit for this parameter. Note, that moisture can decrease the level of DCL up to three orders of magnitude. This effect is due to anomalous transients that will be discussed in section 3.3.

The effect of vacuum on CPTCs is mostly due to moisture desorption and results in decrease of capacitance and increase of DCL. The effect might result in orders of magnitude higher leakage currents in dry compared to wet conditions and is especially noticeable at low temperatures. The process of moisture sorption or desorption at room temperature might take thousands of hours. For this reason, the slug after vacuum storage or after bake will remain dry at room conditions long enough, so for the purpose of testing, vacuum conditions can be simulated by baking the parts at 125 °C for 24 hours.

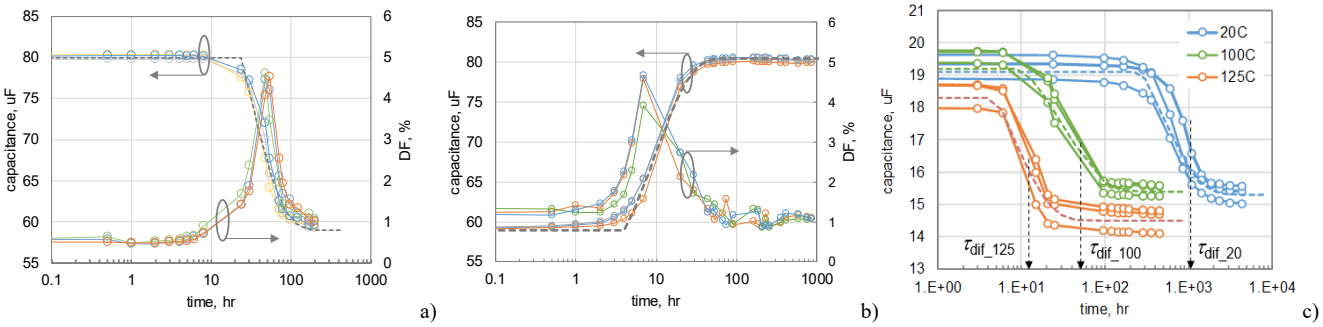

Fig.3.1. Variations of C and DF during drying at 85 °C (a) and soaking with moisture (b) at 85 °C 85% RH in 68 µF 16 V CPTCs and decreasing of capacitance for pre-humidified 15 µF 25 V CPTCs during drying at 20 °C, 100 °C, and 125 °C (c). The dashed curves are calculations based on the diffusion model describing moisture uptake or release in CPTCs.

3.2. Degradation at high temperatures

As most polymer materials, conductive polymers used in PTCs can degrade during long-term storage or operation at high temperatures. This degradation results in decrease of capacitance, increase of DF and ESR (see an example in Fig.3.2.1). Initially, operating temperatures of CPTCs were limited to 85 °C or 105 °C. However, automotive grade capacitors that can pass unbiased storage at 125 °C for 1000 hours had been available since 2014. In 2019, KEMET introduced their new automotive grade T599 series that can pass 1000-hour storage testing at 150 °C.

Experiments show that ESR is a parameter most sensitive to degradation and can increase thousands times during high temperature storage (HTS) compared to the initial value. ESR in CPTCs is increasing exponentially with time of storage after a certain incubation period (see an example in Fig.3.2.2). This increase is due to thermo-oxidative processes in conductive polymers that result in structural changes raising energy barriers for the charge transport; thus, drastically reducing conductivity of the polymers. The major path for oxygen penetration to the tantalum slug is along the molding compound/lead-frame interfaces or through the cracks in the package (see Fig.3.2.3). For this reason, the integrity of packaging and selection of the most thermally robust PEDOT:PSS systems are critical to assure stability of ESR in CPTCs.

Because of the sensitivity of CPTCs to environmental stresses, qualification procedures for these parts should include high temperature storage (HTS) testing. For automotive grade capacitors, this testing is carried out at 125 ºC for 1000 hours (Automotive Electronics Council, AEC-Q200 requirements). Some general purpose CPTCs, as well as capacitors manufactured to MIL-PRF-32700, do not have HTS requirements, but high-quality commercial parts are tested typically for 2000 hours at 105 ºC or 1000 hours at 125 ºC. According to manufacturers' specifications, post-HTS values of ESR are relaxed compared to the initial limits, from 2 to 5 times.

The incubation period of ESR degradation corresponds to the time necessary to form delamination or cracks in the case. A decrease of capacitance and increase of DF are results of the ESR degradation. The times to capacitance and DF failures are on average 3.5 and 2 times greater than for ESR. The activation energies of the degradation during HTS are from 0.38 to 0.93 eV, averaging at E_a = 0.62 ± 0.17 eV. Considering that E_a increases substantially in vacuum, and in this regard, vacuum is beneficial for reliable applications of CPTCs, successful results of 1000 hour testing at 125 ºC can assure reliable operation of capacitors for most space missions. Note that hermetically sealed PTCs have a limited amount of oxygen in the case and have a better stability of AC characteristics during HTS compared to CPTCs.

Automotive grade CPTCs typically employ better packaging materials and process control and can withstand more than 1000 hours at 125 ºC and some types may remain stable for 4000 hours at 150 ºC. For this reason, automotive grade polymer capacitors should be the prime source for selecting components for space applications.

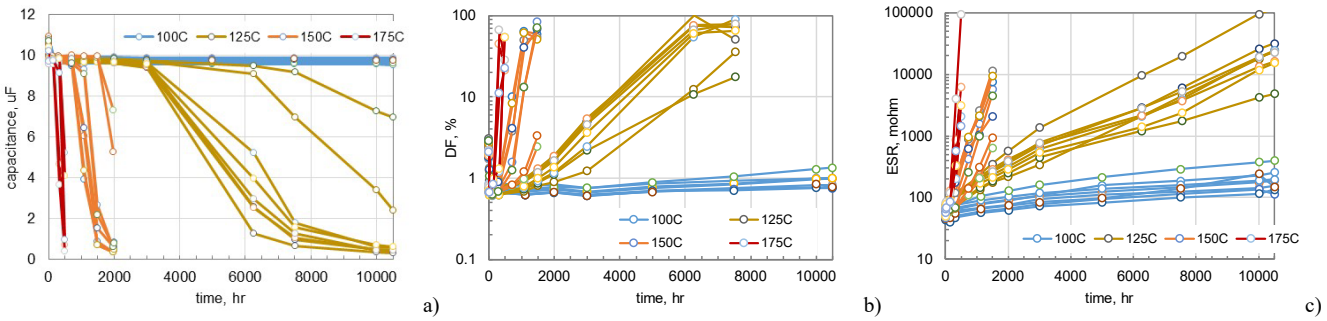

Fig.3.2.1. Examples of degradation of capacitance (a), dissipation factor (b), and equivalent series resistance (c) during HTS at 100, 125, 150, and 175 ºC for 10 µF 25 V CPTCs.

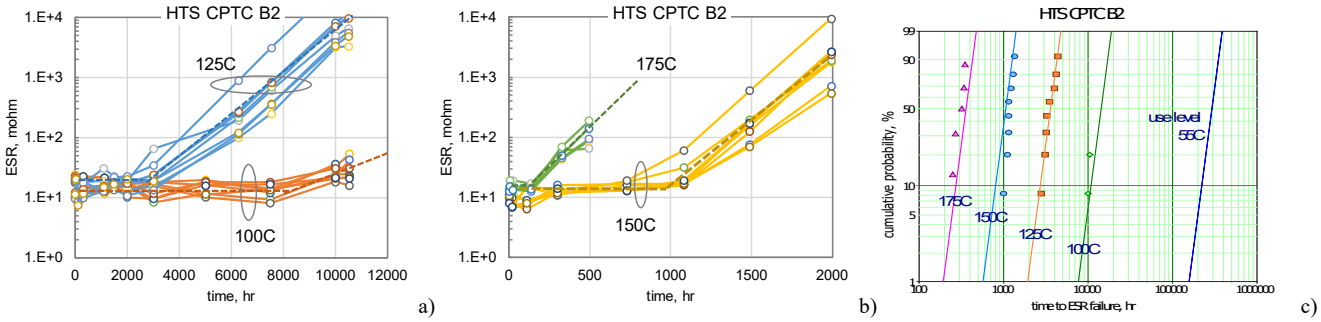

Fig.3.2.2. Examples of the effect of HTS on ESR for 220 µF 10 V capacitors at different temperatures (a, b) showing the presence on incubation periods and exponential growth of ESR after that period. Figure (c) shows distributions of times to ESR failure that allow for assessments of the probability of failure at the use temperature.

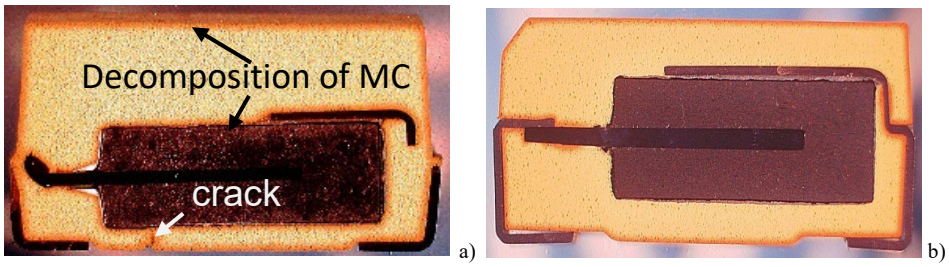

Fig.3.2.3. Cross-sections of CPTCs after high temperature storage. Discolorations show the path for oxygen penetration to the slug, along delamination between the lead frame and molding compound and through the crack.

3.3. Anomalous transients and charging currents

Applications of step voltages to capacitors result in displacement currents that reduce with time exponentially. For most tantalum capacitors these currents became negligibly small after ~1 msec. Absorption currents that follow the displacement currents are typically below a few milliamperes and decrease inversely with time up to tens to thousands of seconds. Afterwards, the currents stabilize at the level that corresponds to the intrinsic leakage of the dielectric that may be orders of magnitude below the specified direct current leakage (DCL) that in tantalum capacitors are measured after 5 min of electrification. The specified level of DCL is typically calculated as 0.01C×V for MnO2 and ten times greater, 0.1C×V, for polymer capacitors.

Displacement currents are caused by changes with time of the electric field in the dielectric. Absorption currents are due to reorientation of dipoles in the dielectric or electron trapping/release into/from the states within the dielectric or at the interface cathode/dielectric. Leakage currents are related to the intrinsic conductivity of the dielectric that is most likely due to the Schottky emission of electrons over the barrier at the cathode/dielectric interface. The first two types of the currents increase linearly with voltage and have a poor temperature dependence, whereas the leakage current increases exponentially with temperature and voltage.

All three types of currents are present in both MnO2 and polymer tantalum capacitors. However, PTCs have an additional type of currents that might reach several amperes and is typically observed between 1 msec and 0.1 sec of electrification. These currents were termed anomalous charging currents (ACC). The existence of ACC is yet another manifestation of a new phenomenon, anomalous transients that is specific to dry and discharged PTCs. This phenomenon also manifests as variations of capacitance and dissipation factor with time after voltage application and increasing currents at low temperatures (see examples in Fig. 3.3.1). Note that in the presence of moisture, PTCs behave similar to MnO2 capacitors. Modification of conductive polymers and improvements in the manufacturing processes can substantially reduce anomalies in the behavior of PTCs.

Although the nature of anomalous transients is not clearly understood, it is most likely related to the Schottky emission of charge carriers over the barrier at the conductive polymer/Ta2O5 dielectric interface that changes with time under bias. In dry and discharged PTCs, the barrier is low resulting in initially large conductivity of the dielectric. The

barrier increases with time that was explained by the orientation of polymer dipoles or by electron trapping processes resulting in rising of the barrier and reduction of the Schottky injection.

ACC is likely the most significant and important manifestation of anomalous transients because it might cause temporary shorting of the part and failures during power cycling in the system. However, currently there is no standard method to evaluate the level of ACC and even a recent military specification, MIL-PRF-32700, does not address this issue.

Problems with assessments of ACC are that the effect is divergent, changes with time due to moisture absorption, and charge accumulation during repeat testing. ACC depends also on temperature and the history of exposures to high temperatures. Anomalous transients are much more sensitive to the moisture content compared to capacitance variations. Even a relatively small amount of moisture, likely less than 10% of the amount absorbed at room conditions can suppress ACC substantially. However, exposure to high temperatures might affect ACC even for dry capacitors.

Capacitors for space applications will dry-out eventually and might cause malfunctions in systems or even fail catastrophically under power turn-on conditions. For these reasons, the level of ACC needs to be controlled. A procedure for ACC evaluation, the power surge testing (PST), is described below, and examples of current transients during PST are shown in Fig.3.3.2. Compared to the constant current and constant voltage ramp test methods, PST results in maximum energy dissipation in capacitors. The thermal stresses associated with PST may result in sharp temperature increases of the slug up to 100 - 150 °C and cause damage to the dielectric resulting in failures of capacitors as shown in Fig.3.3.2c.

Different types of PTC, different lots within the same part type, and different samples in the lot might have different levels of ACC. The value of energy dissipated during PST, E, gives an assessment of the level of ACC that does not depend on the specifics of current relaxation. However, to simplify characterization of the test results, average and standard deviations of currents measured 10 msec after pulse application, I_{10}, for a group of 5 to 10 samples can be used. The level of ACC in a particular sample reduces with repeat testing but remains relatively stable after resetting (bake at 125 °C for 15 – 24 hours). The coefficients of sample-to-sample variations within one lot are typically in the range from 5 to 50%, and the values of I_{10} for different lots of capacitors might vary from 0.01 A to more than 10 A. Variations of E are smaller than I_{10} and are relatively independent on the value of the limiting current in the power supply. The severity of ACC in different manufacturing lots of capacitors after bake at 125 °C for 24 hours can be characterized as high for parts with $I_{10} \geq 1$ A or $E \geq 1$ J, as low for parts with $I_{10} < 0.1$ A or $E < 0.1$ J, and as medium in other cases.

Anomalous currents might increase below the room temperature and become negligible at temperatures exceeding ~60 °C. Voltage has a strong effect on ACC increasing currents exponentially, so the effect might be negligibly small at derated voltages (see Fig.3.3.3).

The significance of the ACC effect in a circuit depends on specific application conditions. Lots with medium and high ACC levels require additional tests and analysis by the system design and project parts engineers to assure reliable operation throughout mission life. These lots might be used for the project at properly derated voltages, temperature and current limitations (see section 9).

3.3.1. Power Surge Testing procedure

A rated voltage should be applied from a power supply capable of increasing voltage across the part in less than 1 msec at limiting currents of ≥ 10 A. The PST cycle includes 200 msec at the rated voltage followed by 200 msec at zero voltage. The transient currents and voltages should be monitored during power on periods to calculate the dissipated energy, and measure currents at 10 msec after pulse application. These values should be recorded during the lot acceptance testing (LAT). The dissipated power is calculated by digital integration till the moment when the current decreases to 0.01A.

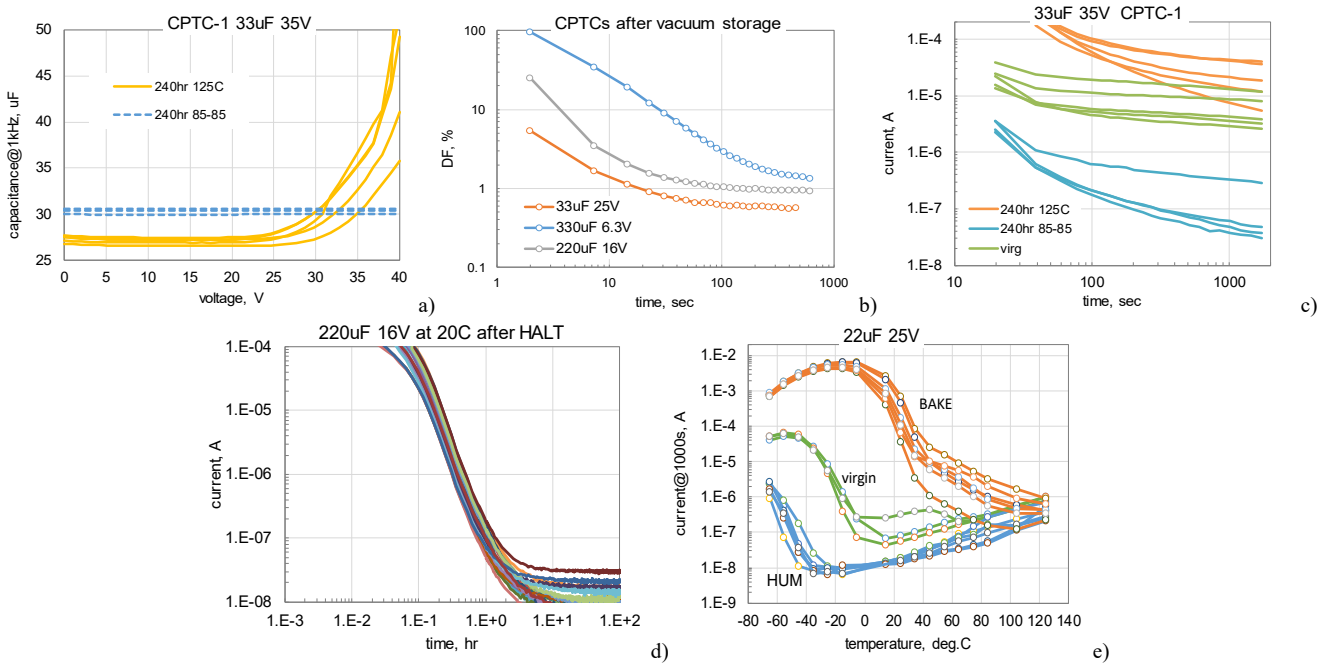

Fig 3.3.1. Examples of the anomalous transients in polymer tantalum capacitors. Voltage dependencies of capacitance for dry and wet 33 µF 35 V capacitors (a) and dissipation factors for three types of dry capacitors (b). Relaxation of currents in 33 µF 35 V capacitors with different moisture content (c). Currents in 220 µF 16 V capacitors at 22 °C, 16 V measured after HALT and 1 hour depolarization that show reduction by 4 orders of magnitude after a few hours under bias (d). Note that the initial currents that exceeded 100 µA at room temperature (Fig.d) were lower than the currents measured at 165 °C. Temperature dependence of leakage current for 22 µF 25 V capacitors after different preconditioning (e).

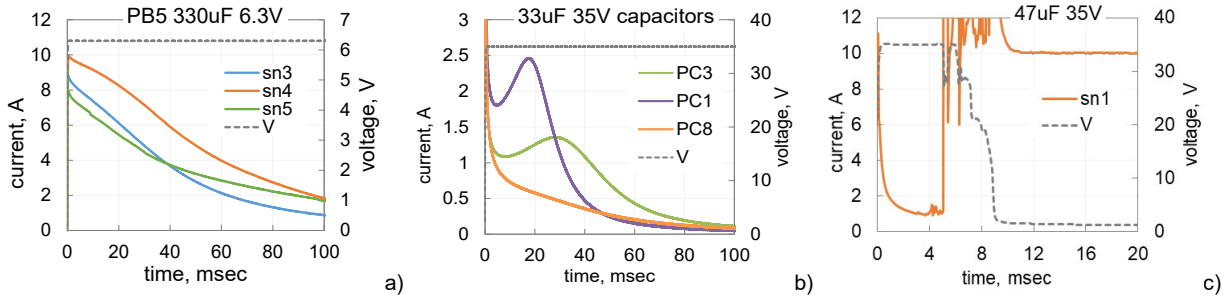

Fig. 3.3.2. Examples of current and voltage variations during PST for different types of polymer tantalum capacitors (a, b) and a failure of a 47 µF 35 V capacitor during PST (c). Note that test results in figure (a) are related to different samples within the same lot and in (b) for different part types.

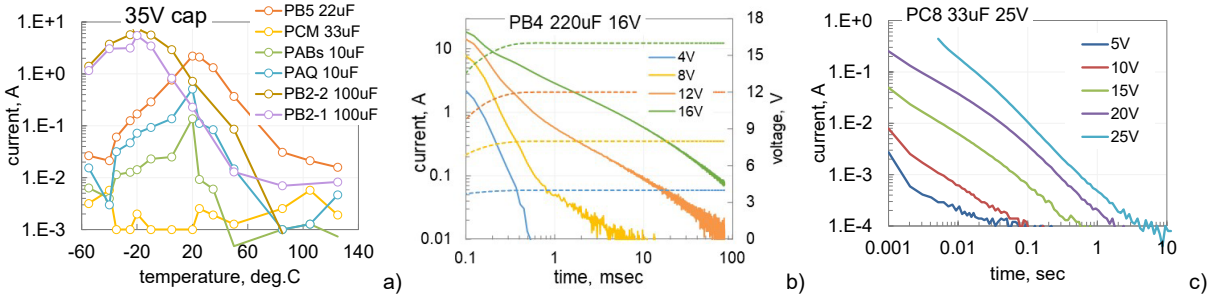

Fig.3.3.3. Temperature variations of currents measured at 10 msec for different types of polymer tantalum capacitors rated to 35 V (a) and effect of voltage on currents during PST (b, c). Dotted lines in (b) show variations of voltages during the testing.

3.4. Reliability issues with PTCs

Failures of tantalum capacitors manufactured with MnO2 cathodes were mostly due to defects in a thin Ta2O5 dielectric resulting predominantly in infant mortality (IM) failures. To remove defective parts, a special screening procedure, called Weibull Grading Test (WGT), had been developed. WGT can be considered as an accelerated test for IM failures that according to MIL-PRF-55365 is carried out for 40 hours at the rated temperature of 85 °C and voltages 20 to 50% above the rated voltage. The failure rate (FR) based on WGT data is calculated using an exponential model for the voltage acceleration factor:

$$AF_{WGT} = exp[B_{WGT} \times (u - 1)] \ , \quad (1)$$

where B_{WGT} = 18.77 is the voltage acceleration constants and u is the test voltage normalized to the rated voltage, $u = V_{test}/VR$.

Introduction of conductive polymers to replace MnO2 cathodes has reduced IM failures to the level that WGT became not applicable. Instead, IM failures of PTCs are screened out using a burn-in procedure and FR is calculated based on life test results and reliability acceleration factors.

3.4.1. Failure rate calculation

Reliability of electronic components is typically characterized by the failure rate that is calculated based on the life test results in an assumption of random failures:

$$FR = \frac{\chi^2(\alpha,(2m+2))}{2} \times \frac{1}{AF} \times \frac{1}{Nt} \quad , \quad (2)$$

where χ^2 is the chi-square function, α is the confidence level, m is the number of failures, N is the number of tested samples, t is the duration of the test in hours, and AF is the acceleration factor that depends on test voltage and temperature.

The acceleration factor can be presented as a product of temperature and voltage acceleration factors, Eq.(3). The temperature acceleration factor, AF_T, depends exponentially on temperature according to Arrhenius law, Eq.(4), where E_a is the activation energy. Note that according to some models, E_a is decreasing with applied voltage. However, Eq.(3) can be used for conservative estimations for tests at a limited range of test temperatures.

$$AF = AF_T \times AF_V \quad (3)$$

$$AT_T = \exp\left[-\frac{E_a}{k} \times \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right] \quad (4)$$

For calculations of the voltage acceleration factor, AF_V, two models, exponential and power can be used. The exponential model can be presented in a form similar to Eq.(1):

$$AF_V = exp[B \times (u_2 - u_1)] \ , \quad (5)$$

where B is the voltage acceleration constant for the exponential model.

According to MIL-PRF-32700, AF_V for PTCs is calculated using a power model:

$$AF_V = \left(\frac{u_2}{u_1}\right)^n \ , \quad (6)$$

where n is voltage acceleration constant for the power model.

Analysis shows that both models, exponential and power, can approximate results of HALT equally well. However, extrapolation of the test results to the rated and derated voltages gives orders of magnitude lower FR for the power compared to the exponential model. Because users need conservative estimations of FR, the exponential model will be used in these guidelines. Also, the exponential model agrees with the time dependent dielectric breakdown (TDDB) model for tantalum capacitors.

3.4.2. Assessments of voltage acceleration factors and useful life

Highly accelerated life tests (HALT) of polymer capacitors show that a prevailing portion of failures is caused by wear-out (WO) processes that limit the useful life of the parts. A relatively small portion of the parts failing due to IM failures does not allow for accurate estimations of AF for this failure mode, but it can be determined for WO failures. Using AF for WO failures to calculate FR per Eq.(2) can be justified by the TDDB model. Assessments using this model show that the voltage acceleration constant for IM failures can be 1.5 to 2 times greater than for WO failures, so application of AF determined for WO failures will give a conservative estimation of FR.

Typically, operating temperatures of tantalum capacitors in space instruments are below the rated temperature of 85 °C. Note that per MIL-PRF-55365, FR for MnO2 tantalum capacitors is calculated by WGT at 85 °C. For consistency, it is reasonable to use the same temperature for polymer tantalum capacitors. By limiting HALT conditions to 85 °C and carrying out testing at different stress voltages only, we can determine AF_V and the constant B as shown in Fig. 3.4.1. This procedure is similar to the one described in MIL-PRF-32700, Appendix B, with several exceptions:

I. Because different part types have different margin to breakdown voltages, the stress voltages should be at least 20% below the characteristic breakdown voltage for the lot (instead of below 2×VR per MIL-PRF-32700).

II. To get a better accuracy of AF assessments, the testing should be carried out at three levels of stresses instead of two per MIL-PRF-32700. The difference between the stress voltages is recommended ≥ 0.1VR instead of 0.2VR per MIL-PRF-32700.

III. Because moisture might affect results of HALT, the parts should be soldered onto test PWBs (soldering is optional per MIL-PRF-32700) and baked before HALT at 125 °C for 24 hours.

IV. Failures per MIL-PRF-32700 are determined as blown 1A fuses connected in series to each part. However, the failed PTCs can have resistances of dozens and hundreds of ohms, so fuses might not blow open. To increase the sensitivity to breakdown and allow for monitoring of leakage currents, fast acting 62 mA/125V fuses with resistance of 7 ohm are recommended to use during BI, life testing or HALT.

V. A procedure to determine the voltage acceleration constant B:

V.1. The times to failure (TTF) should be plotted in Weibull coordinates that allows for a simple discrimination of the type of failures. By approximating TTF distributions with strait lines we can determine parameters of the Weibull function:

$$P(t) = 1 - exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right],$$

where β is the shape (slope) and η is the scale factors.

Variations of the failure rate with time, $\lambda(t)$, for Weibull distributions can be presented as: $\lambda(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1}$.

At $\beta < 1$, $\lambda(t)$ is decreasing with time indicating IM failures, whereas at $\beta > 1$ $\lambda(t)$ is increasing, which is the major characteristic of WO failures. At $\beta = 1$, the failure rate does not depend on time thus indicating random failures.

V.2. The WO portions of the curves are determined by approximation with lines having similar slopes, β, that should exceed 1 (see Fig. 3.4.1a). Note, that the similarity of the slopes indicates similar failure mechanisms at different stress levels. The approximation can be carried out graphically, using a maximum likelihood estimation (MLE) method or appropriate software e.g., available from ReliaSoft or HBM Prenscia.

V.3. The characteristic times to failure, TTF_c, are determined at the level of 63% (see Fig. 3.4.1a).

V.4. To calculate the voltage acceleration constant B, the values of TTF_c can be plotted against $u = V_{test}/VR$ and approximated with an exponential function (see Fig. 3.4.1b).

The presence of WO failures in PTCs requires that reliability of these capacitors is characterized not only by FR that can be defined as a maximal value of FR calculated based on the results of life testing per Eq.(2), but also by the useful time, or time to the inception of WO failures, TTF_i. The latter can be determined as a time when the probability of failure at operating conditions increases to 0.1% and can be calculated as:

$$TTF_i = TTFc(u_{op}, T_{op}) \times [-\ln(0.999)]^{1/\beta} \quad (7)$$

where $TTF_c(u_{op}, T_{op})$ is the characteristic time of WO failures at operating conditions calculated based on the characteristic time at the rated conditions (85 °C and VR) and acceleration factors:

$$TTFc(Top, Vop) = TTFc(85C, VR) \times AF_V \times AF_T \quad (8)$$

The values of β and AF_V are determined as described above. Available in literature values of E_a are ranging from 0.7 to 1.4 eV. For conservative estimations, we can calculate AF_T per Eq.(4) using E_a = 0.7 eV.

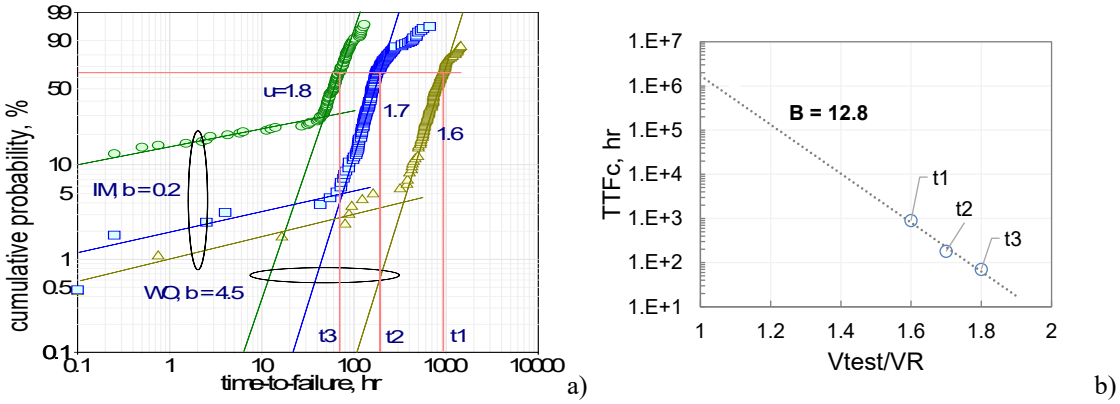

Fig. 3.4.1. An example of HALT for 150 µF 30 V capacitors at 85 °C (a) and calculation of the voltage acceleration constant B (b). Note that the characteristic time-to-failure at rated conditions for this part is 2E6 hours or 230 years, and the time to failure inception calculated per Eq.(7) is 50 years. Voltage derating to 0.8VR will increase TTF_i to 800 years.

3.4.3. Monitored BI and life testing

Some PTCs might have unstable, erratically changing or spiking leakage currents (see examples in Fig.3.4.3 and 3.4.4). The probability of spiking is lot-dependent and increases with the level and duration of stress. This behavior is a specific feature of polymer tantalum capacitors caused by a different, and probably less effective self-healing compared to MnO2 and wet tantalum capacitors. To reduce the probability of malfunction and the level of noise in sensitive electronic systems, capacitors with excessive spiking currents should be screened out by monitored burn-in that is recommended at 105 ºC, 1.1VR or 85 ºC at 1.3VR for 40 hours. Both conditions have approximately the same acceleration factors. Recommended monitored life test conditions are 85 ºC, 1.3VR for 1000 hours.

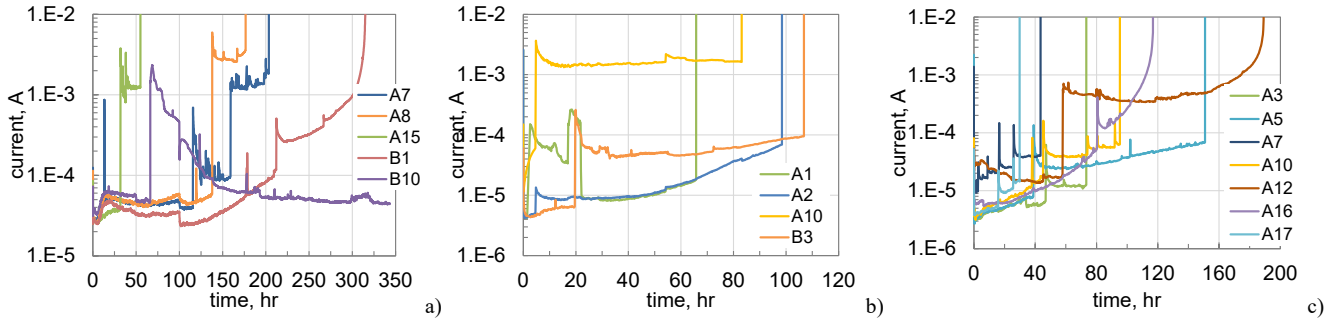

Fig. 3.4.3. Examples of current spiking before failure during HALT at 85 °C for 330 µF 16 V capacitors at u = 2.2 (a), 150 µF 30 V capacitors at u = 1.8 (b), and 150 µF 35 V capacitors at u = 1.6 (c). Parts with similar spiking that are detected during burn-in are recommended to remove from the flight lot.

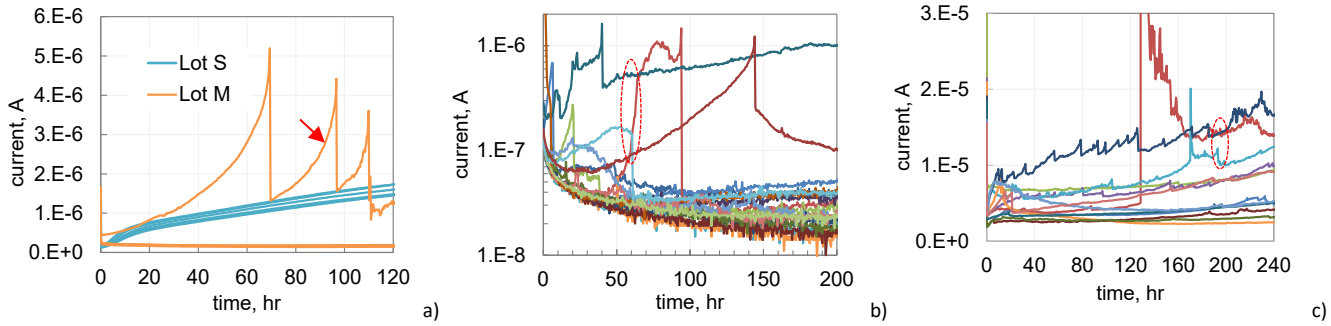

Fig. 3.4.4. Examples of monitored BI that allow to screen-out parts with excessive spiking; a) two lots of 10 µF 35 V capacitors; b) 33 µF 35 V capacitors; c) 100 µF 35 V capacitors. Samples with excessive spiking are indicated by the arrow or dotted ovals.

4. Construction Analysis/DPA

Design of PTCs is similar to conventional MnO2 tantalum capacitors except for MnO2 as a cathode layer is replaced with a conductive polymer as shown in Fig.4.1. Examples of the designs of hermetically sealed PTCs are displayed in Fig.4.2 and 4.3. The conductive polymers (PEDOT or PEDOT:PSS compositions) are black and optically might be not clearly distinguished from the carbon layer used in chip capacitors to separate conductive polymer from silver epoxy attachment and prevent migration of silver to the slug. Due to the presence of sulfur (S), areas with the polymer can be revealed in SEM using energy dispersive spectroscopy (EDS) analysis. The morphology of conductive polymers inside the pores of the slug and on the shell are shown in Fig. 4.4.

A sponge-like structure of the anode pellet, large surface area, and sub-micrometer thickness of the Ta2O5 dielectric, make detection of defects in the dielectric of tantalum capacitors practically impossible. The existing requirements for destructive physical analysis (DPA) for chip tantalum capacitors per MIL-STD-1580 are focused mostly on the integrity of the case and slug, anode riser wire welding, cathode lead-frame attachment, and delamination and cracks in the cathode layers. These requirements can be used for CPTCs in the process of construction analysis (CA) when applicable. Note, that the purpose of DPA is to verify that design, materials, and defects are compliant with the requirements for a standard part. For new technology components, the purpose of similar examinations carried out within CA is evaluation of the design and used materials to indicate potential problems with the parts that should be addressed during screening and lot acceptance tests.

Due to thermo-oxidative degradation of conductive polymers, the integrity of the case is especially important for PTCs and the thickness of the molding compound (case) above the slug should exceed 0.005” (125 um). The case integrity might be compromised during soldering or environmental stresses, so the absence of defects in the case in virgin samples does not guarantee reliable operation of the parts. For this reason, CA or DPA are recommended to carry out on samples after temperature cycling and high temperature storage (subgroup 2 of LAT in Table 3).

As a rule of thumb, the lead-frame in CPTCs is required to be connected to the slug at no less than 25% of the available slug area. However, there is no experimental justification for this requirement, and for high conductivity cathode materials, and in particular, conductive polymers, even a relatively small contact area can assure low ESR values. Requirements for the attachment are especially difficult to verify for multi-anode capacitors.

Delamination and horizontal cracks are often observed between the layers of conductive polymer in the shell area of the slug. These defects are not critical for performance of the capacitors. Vertical cracks in the shell area of the slug coating (see Fig.4.5) after long high temperature storage indicate structural changes associated with thermo-oxidative degradation rather than direct reason for parametric failures.

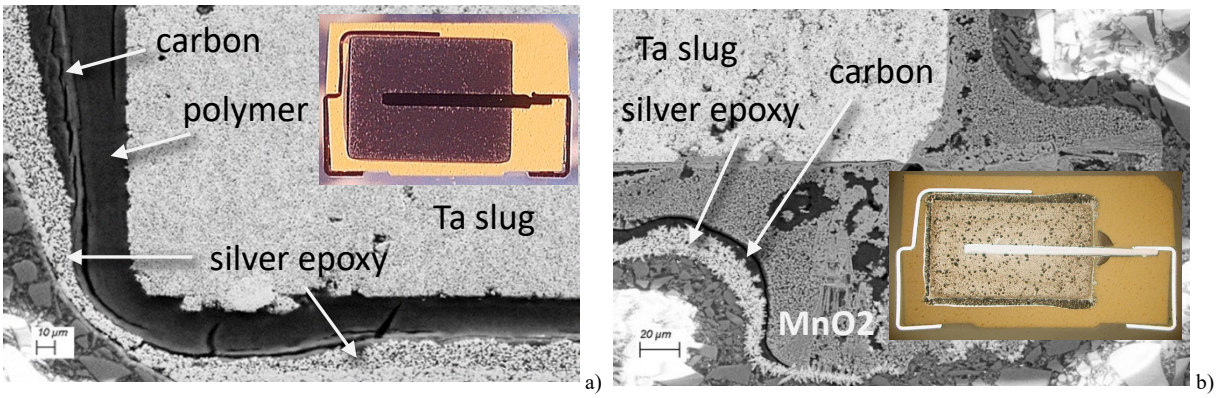

Figure 4.1. Design of chip polymer (a) and MnO2 (b) tantalum capacitors.

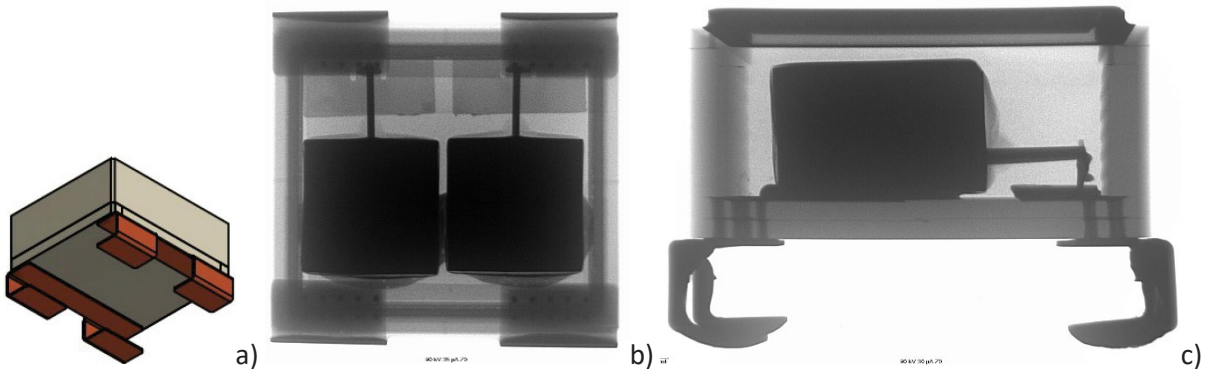

Fig. 4.2. An overall view (a) and X-ray images (b, c) of a PTC in a hermetic ceramic package. Note that the case can be filled with a foam epoxy. Radiography is useful for these parts to detect foreign materials, e.g. small metal bolls that might be generated during the riser anode wire welding.

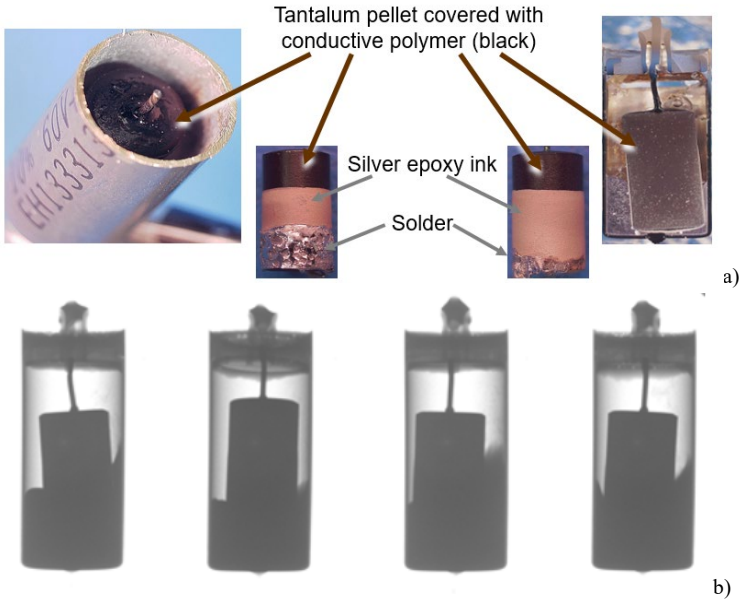

Fig. 4.3. Design of a PTC in a hermetic metal case (a) and examples of X-ray views (b) showing solder distribution and possible misalignment. Note that this design is similar to MnO2 capacitors manufactured per MIL-PRF-39003, and most DPA requirements in MIL-STD-1580 are applicable.

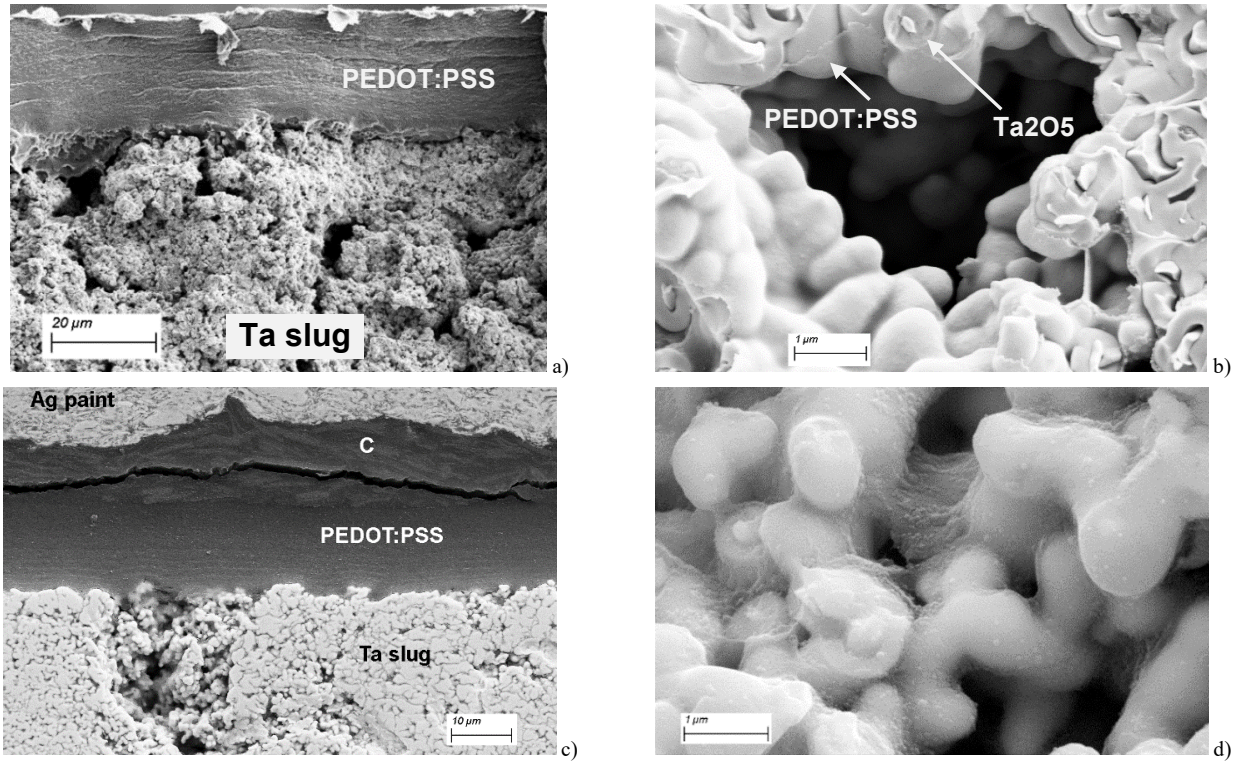

Fig. 4.4. Internal views of 35 V polymer capacitors showing the shell area (a, c) and pores of the slug (b, d). Note that the thickness of multilayer conductive polymers on the shell are ~ 20 μm, whereas it is below ~ 0.1 μm inside the pores.

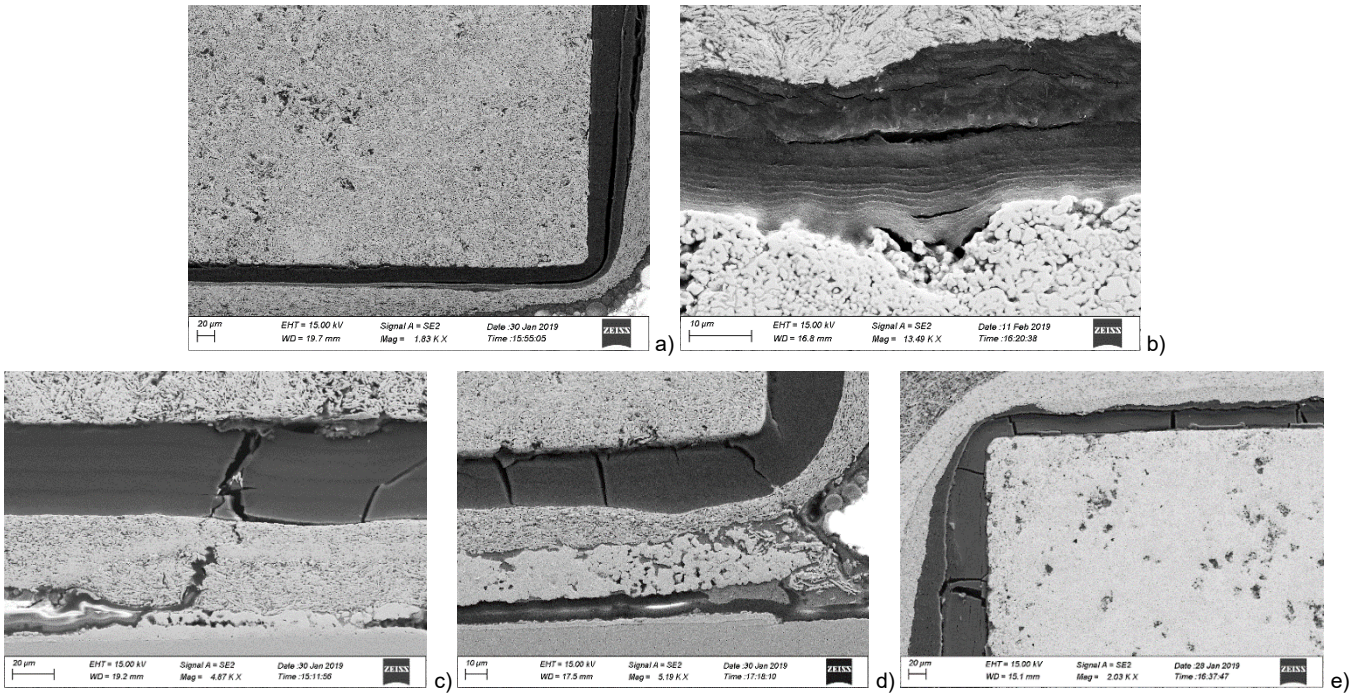

Fig.4.5. SEM views of cross-sectioned virgin (a, b) and post-HTS (c-e) samples. Note the presence of delamination and horizontal cracks in virgin capacitors and vertical cracks in samples after high-temperature storage.

5. Effect of soldering

In the process of soldering all surface mount technology (SMT) components experience significant thermo-mechanical stress that might affect their integrity and reliability. An additional problem with soldering of plastic encapsulated components is due to moisture sorption. A fast moisture release during soldering temperatures can cause cracking of the case (so-called popcorn effect), delamination between the leads and molding compound, and damage to active elements of the part. Damage to the dielectric might result in power-on catastrophic failures in tantalum capacitors.

Popcorn is a well-known effect in plastic encapsulated microcircuits (PEM) and it also occurs in chip tantalum capacitors. The porous slug of tantalum capacitors allows for absorption of substantially larger amount of moisture compared to molding compound. For this reason, tantalum capacitors may be more sensitive to soldering compared to PEMs. Due to a high hygroscopicity of conductive polymers, PTCs absorb approximately two times more moisture compared to similar MnO2 parts and for this reason they are typically labeled as moisture sensitivity level 3 (MSL3 per J-STD-020), whereas MSL1 is often used for MnO2 capacitors. Note that damage to the part caused by soldering can be revealed by surge current or power surge tests, but these tests are not required to establish MSL per MIL-PRF-32700. PTCs that were stored outside the dry hermetically sealed bags or in dry boxes with RH ≤ 10% for more than 4 days require baking for 24 hours at 125 °C for loose parts and for 1 week at 55 °C for parts in reels.

6. TEST REQUIREMENTS, Table 1

Assurance Level 1/	Screening	LAT	CA/DPA 2/
Level 1	X	X	X
Level 2	X	X	X
Level 3	X	X	

1/. Tantalum capacitors used in critical applications, e.g. in power supply systems, might require a higher level of testing compared to other components used by the project.

2/. Samples for this analysis are recommended after temperature cycling and high temperature storage (subgroup 2 of LAT in Table 3)

Here and below, the character “X” designates a recommended procedure.

7. SCREENING, Table 2

Inspection/Test	Test Methods, Conditions, and Requirements	Assurance Level		
		L1	L2	L3
Reflow conditioning	Per MIL-PRF-32700	X	X	X
1. Visual Inspection	Verify marking and workmanship. There shall be no evidence of corrosion, mechanical damage, or cracks.	X	X	
2. Radiographic Inspection	Per MIL-PRF-55365 for chip **1/**, MIL-PRF-39003 for hermetic capacitors	X	X	
3. Thermal Shock and bake	TS per MIL-PRF-32700. (5c -55 to +125C) Bake at 125C for 24 hours **2/**	X	X	
4. Initial Electrical Measurements	C, DF, ESR, DCL per MIL-PRF-32700	X		
5. Surge Current Test	Per MIL-PRF-32700 **3/** L1: -55°C ± 5°C, +25°C ± 5°C, +85°C ± 5°C L2: -55°C ± 5°C, +25°C ± 5°C, +85°C ± 5°C L3: +25°C ± 5°C	X	X	X
6. Seal Test (Hermetic Types Only)	Per MIL-PRF-39003	X	X	
7. Power Surge Test	3 cycles as described in 3.3.1 **4/**	X	X	X
8. Monitored Burn-In Voltage ageing	85C, 1.3VR, 40 hr, with current measurements every 5 min **5/** Per MIL-PRF-32700 (85C 40hr, V ≥ VR, 1A fuses)	X	X	 X
9 Final Electrical Measurements	C, DF, ESR, DCL per MIL-PRF-32700	X	X	X
10. Visual Inspection	Capacitors shall show no evidence of corrosion, cracks, or mechanical damage.	X	X	X
11. Engineering review. (Percent Defective Allowable)	PDA should be considered in conjunction with the types of failures and project's MEAL requirements.	≤10%	≤20%	

Notes:

1/ Verify that the thickness of the case above the slug in CPTCs exceeds 0.005".

2/ The purpose of bake is to assure that electrical tests are carried out on parts with minimal level of absorbed moisture**.** Parts after bake should be tested within 8 hours or kept in a dry box with RH < 10%.

3/ The parts should be tested as described in MIL-PRF-32700 except for measurements after test can be carried out after PST (step 7).

4/ The parts should be preconditioned by baking at 125 °C for 24 hour and tested by 3 PST cycles within 8 hours after the bake. Failures should be detected during the test and/or by parametric measurements after the test.

5/ Currents monitoring is recommended by using 1 to 10k current sense resistors and a scanner to determine voltage drop across the resistors. The voltage drop should not exceed 5% of the test voltage. Capacitors with the out-of-family (e.g., determined by the 3-sigma criterion) and unstable currents similar to those shown in Fig.3.4.3 and 3.4.4 should be removed from the flight lot. It is possible to use fast blow fuses with resistance exceeding 5 ohm in lieu of resistors.

8. LOT ACCEPTANCE TEST, Table 3

Inspection/Test	Test Methods, Conditions, and Requirements	Assurance Level		
		L1	L2	L3
Group 1	Mechanical and prohibited materials inspections	6(0)	6(0)	3(0)
1. Visual Inspection	Verify conformance to mechanical dimensions. Get overall pictures of the parts.	X	X	X
2. Pure tin	Per MIL-PRF-32700	X	X	
Group 2	TC and High Temperature Storage	77(0)	40(0)	20(0)
Temperature Cycling	10 cycles -55C to +125C **1/**	X	X	X
High Temperature Storage	1000 hr at 125C for L1 and at $T_{op\ max}$ +20C for L2 projects **2/**	X	X	
Post-TC/storage tests electrical measurements	PST, C, DF, ESR, DCL (within 8 hours after storage)	X	X	X
	+Seal Test (hermetic types only) per MIL-PRF-39003	X	X	X
Group 3	Ripple currents, PST, and stability at high and low temperatures **3/**	10(0)	10(0)	10(0)
Ripple current	Temperature rise should be below 10C at $I_{ripple\_test} = 1.2 \times I_{ripple\_op}$ **4/**	X	X	
Power Surge Test (PST) **5/**	L1: -55C, -25C, 0, +25C, +50C	X		
	L2: $T_{op\ max}$, -25C, and +25C		X	
	L3: +25C			X
Stability at low and high temperatures	Per MIL-PRF-32700, except for DCL should be measured at all temperatures **6/**	X	X	NA
Group 4 (hermetic parts only)	Random vibration testing. **7/** Per MIL-STD-202, TM214, test condition II-E (19.6 rms g), 1.5hr in two directions, last 30 min. – monitored. DCL, C, and DF to specification.	6(0)	6(0)	NA
Group 5	Reliability assessments **8/**	280	100	0
Voltage acceleration factor	At 85C and 3 voltage levels **9/**	60x3	X	
Monitored life test	1000hr at 85C 1.3 VR **10/**	100	60	
Failure rate at rated conditions (85C, VR)	As described in 3.4.1 **11/**	< 10 FIT	< 10 FIT	< 100 FIT
Useful life at application conditions (T_{op}, V_{op})	As described in 3.4.2 **11/**	>3MD	>3MD	>3MD
Group 6	Moisture resistance test **12/**	20 (0)	20(0)	NA
Biased humidity	85C 85% RH at VR for 168 hr. per MIL-PRF-32700	X	X	

Notes

1/ The suggested are base-line conditions for TC. The number of cycles and temperature range can be increased based on the project mission requirements.

2/ Capacitors manufactured for automotive industry per AEC-Q200 supposed to withstand 1000 hour storage at 125 °C (77 samples with zero failures). Post-HTS values of ESR should be below $3xESR_{limit}$. TC might create cracks or delamination in the case that accelerates thermo-oxidative degradation of the conductive polymer, and for this reason, HTS should be carried out after temperature cycling test.

3/ Parts for this test group should be soldered onto a test PWB according to MSL and recommendations of the manufacturers.

4/ This test should be carried out if ripple currents during applications exceed 50% of the values specified in the data sheet for the part. Currently, ripple current testing is not required per MIL-PRF-32700, but limits for the ripple currents exist in the commercial data sheets. High ripple currents can cause rising of the temperature and thus reduce reliability of the parts. The temperature rise should be determined at the application frequency and I_{ripple_test} that exceeds the ripple current during applications by 20%.

5/ The purpose of this test is to assess anomalous transient currents (ACC) at different temperatures using a procedure described in section 3.3.1. Ten samples preconditioned by baking at 125 °C for 24 hours should be tested consequently at -55, -25, 0, +25, and +50 °C (for L1 projects). The test should be carried out within 8 hours after bake. Average values and standard deviations of the 10 msec currents or dissipated energy should be documented and used to characterize the level of ACC for the lot. Parts with $I_{10} \geq 1$ A or $Q \geq 1$ J indicate high ACC level and with $I_{10} < 0.1$ A or $Q < 0.1$ J indicate low ACC level. Lots with medium and high ACC levels require additional tests and analysis considering MEAL by the system design and project parts engineers to assure reliable operation throughout the mission.

6/ Measurements of DCL at low temperatures are not required for MnO2 cathode capacitors (per MIL-PRF-32535) because they decrease orders of magnitude below the value specified at room conditions. For PTCs, due to anomalous transient effect, currents at low temperatures might significantly exceed currents at high temperatures and must be controlled. Note, that this requirement is absent in MIL-PRF-32700. After measurements of the currents at each temperature, the parts should be depolarized at 0V for at least 5 min. The acceptability of test results should be evaluated during the engineering review based on the project's MEAL requirements.

7/ According to NASA requirements all space units suppose to pass a random vibration test that simulates stresses during spacecraft launch. The level of vibration depends on the type of the launch vehicle, but typically Mission Assurance Requirements (MAR) acceptance conditions for space projects include testing at 14.1 rms g. To assure a certain margin to the box-level testing, it is recommended that all hermetically sealed PTCs pass random vibration test at 19.6 rms g (test condition II E per MIL-STD-202).

8/ CPTCs should be preconditioned per the specified MSL, soldered on test PWBs, and baked after soldering at 125 °C for 24 hours to assure dry conditions of the parts. The tests should start within 8 hours after bake.

9/ Voltage acceleration factors should be determined as described in 3.4.2. AF_V for L2 projects can be calculated based on the generic manufacturer's data.

10/ Monitored life test are recommended for L1 and L2 projects only (scanning every 30 min). Life test results carried out per MIL-PRF-32700 can be accepted for L3 projects.

11/ The failure rate and useful life should be calculated as described in 3.4.1. The FR is calculated at the rated conditions, but the useful life is assessed for the operating conditions based on MEAL. The unit for FR is failures in time (FIT), 1 FIT = 1E-9 1/hr = 0.0001%/1000hr.
Note that the highest FR for tantalum capacitors manufactured to MIL-PRF-32700 is 0.001%/1000hr or 10 FIT (level Z).
The useful life time should exceed 3 times the mission duration (MD).
For L3 projects conservative estimations for the failure rate and useful life time can be made using the voltage acceleration constant $B = 7$ and $E_a = 0.7$ eV.

12/ Although moisture resistance of components used in space is not as critical as for terrestrial applications, exposure to humid conditions is possible during the ground phase storage and integration and testing (I&T) periods. This requires assessments of the moisture resistance for PTCs used in space. The existing automotive grade PTCs (77 samples) can withstand 1000 hours biased testing at 85 °C/85% RH at rated voltages (AEC-Q200 requirements). MIL-

PRF-32700 requires testing at similar conditions for 500 hours for 18 samples only. The suggested Moisture Resistance Test (MRT) is similar to MIL-PRF-32700 except for shorter duration, larger sample size, and contrary to MIL-PRF-32700 that allows one failure out of 18 tested samples, no failures allowed.

9. DERATING, Table 4

The table below presents baseline recommendations for operating voltage, currents, and temperature deratings. Depending on the project's MEAL, specifics of the part performance, confidence in information regarding possible degradation and failure mechanisms, the derating requirements can be reevaluated.

		Chip PTCs	Hermetic PTCs
Maximum Operating Voltage	**1/**	0.6VR	0.6VR
Maximum Case Temperature	**2/**	T_{c_max} = 85 °C	T_{c_max} = 105 °C
Maximum Surge Current	**3/**	$I_{max} = VR/(1+ESR_{spec})$	$I_{max} = VR/(1+ESR_{spec})$
Maximum Ripple Current	**4/**	$T_{case} - T_{amb}$ = 10 °C	$T_{case} - T_{amb}$ = 10 °C

Notes:

1/ The maximum operating voltage is the sum of the peak AC ripple and DC polarizing voltages. The operating voltage is limited to further increase reliability during long-term DC biased operations, reduce surge currents, and anomalous charging currents during power-on processes. The reliability gain (decrease of the failure rate or increase of useful life) caused by voltage derating can be calculated per Eq.(5) or estimated using Fig. 9.1.a. Note that conservative estimations can be made assuming $B = 7$.

2/ The maximum case temperature is limited to prevent thermal and thermo-oxidative degradation of conductive polymers and to increase reliability under biased operations. The reliability gain of the temperature decrease can be calculated at different activation energies per Eq.(4) or estimated using Fig. 9.1.b. Conservative estimations can be made assuming $E_a = 0.7$ eV.

3/ During screening, the parts are tested by surge current spikes that should exceed $I_{max} = VR/(1+ESR_{spec})$, where ESR_{spec} is the specified maximal value of ESR for the part. Note, that current spikes with similar amplitudes occur during power-on and power-off cycles, but failures are mostly due to the power-on cycles because the breakdown happens at lower voltages when the voltage rises instantly across the capacitor. During applications, the power-on surge current is limited by the actual *ESR* that might be much smaller than the specified value, ESR_{spec}. In this case, even at derated voltages the actual current spike, $I = V_{op}/ESR$, might be greater than I_{max} used during screening. To limit the surge current for a capacitor of value *C* during applications, the rate of voltage increase across the part should be limited by the power supply (soft power-on circuits) with $dV/dt < I_{max}/C$, or by adding a resistor connected in series to the part, $R \geq V_{op}/I_{max}$.

4/ Capacitors operating at high ripple currents might have reduced reliability due to self-heating. For this reason, the self-heating is recommended to limit to 10 °C for parts operating at $T_{amb} \geq T_{c\_max}$ -10. This requirement can be relaxed at $T_{amb} < T_{c\_max}$ -10. Note, that temperature rising in vacuum can be larger than in air environments. The temperature rise can be estimated as $\Delta T = I^2_{ripple} \times ESR \times R_\theta$, where I_{ripple} is the ripple current and R_θ is the thermal resistance of the part that depends on the size of the part, mounting conditions, and environments. The value of ΔT can be determined experimentally, e.g. using an IR camera. For rough estimations, the value of R_θ can be assumed exceeding 40 K/W.

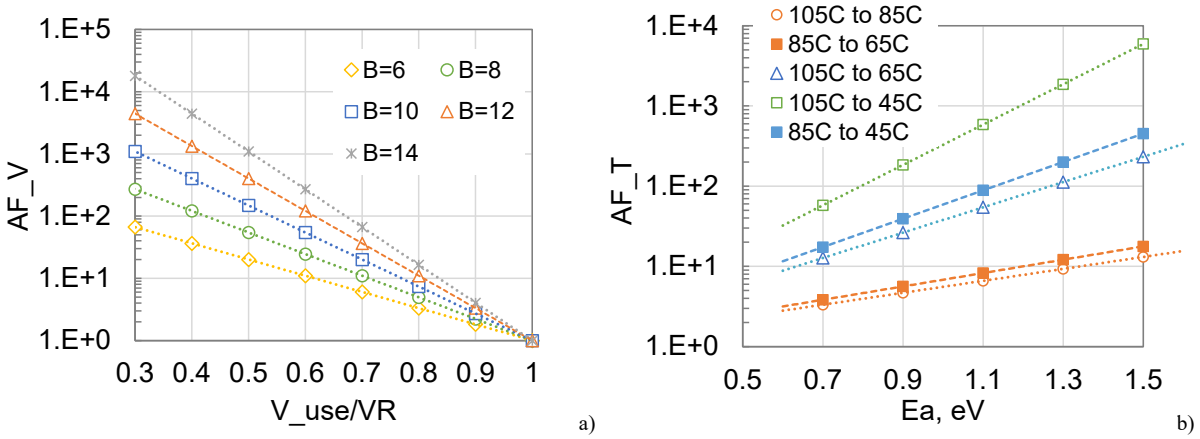

Figure 9.1. Acceleration factors for voltage derating at different voltage acceleration constants *B* (a) and for temperature reduction at different reliability activation energies (b). The legend in (b) gives examples of the initial and derated temperatures.

10. ACRONYMS

AC	alternating current	**MD**	mission duration
ACC	anomalous charging currents	**MEAL**	Mission, Environment, Applications and Lifetime
AF	acceleration factor	**MLE**	maximum likelihood estimation
BI	burn-in	**MRT**	Moisture Resistance Test
CA	construction analysis	**MSL**	moisture sensitivity level
COTS	commercial-off-the-shelf	**PEDOT**	poly(3,4)ethylenedioxythiophene
CPTC	chip polymer tantalum capacitors	**PEM**	plastic encapsulated microcircuits
DC	direct current	**PSS**	poly-styrene sulfonate
DCL	direct current leakage	**PST**	power surge testing
DF	dissipation factor	**PTC**	polymer tantalum capacitors
DPA	destructive physical analysis	**PWB**	printed wiring board
EDS	energy dispersive spectroscopy	**RH**	relative humidity
ESR	equivalent series resistance	**SEM**	scanning electron microscopy
FIT	failures-in-time	**SMT**	surface mount technology
FR	failure rate	**TC**	temperature cycling
FR	failure rate	**TDDB**	time dependent dielectric breakdown
HALT	highly accelerated life testing	**TTF**	time-to-failure
HTS	high temperature storage	**VR**	voltage rating
IM	infant mortality	**WGT**	Weibull Grading Test
LAT	lot acceptance testing	**WO**	wear-out
MAR	Mission Assurance Requirements		