A real-time optical ground receiver for photon starved environments

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ABSTRACT

The National Aeronautics and Space Administration (NASA) Glenn Research Center (GRC) has developed a photon-counting optical ground receiver for pulse-position modulated signals. The real-time receiver system includes a fiber interconnect, superconducting nanowire single-photon detectors (SNSPDs), and a real-time field programmable gate array (FPGA) based receiver. The fiber interconnect and SNSPDs are implemented with two different configurations. In the first, a 7-channel few-mode fiber photonic lantern couples the light from the telescope to 7 single-pixel few-mode fiber coupled SNSPDs. In the second configuration, a few-mode fiber couples light to a 16-pixel monolithic SNSPD array. The real-time FPGA-based receiver performs combining of up to 16 SNSPD channels, symbol timing recovery, demodulation, and decoding. The system is scalable with data rates ranging from 20 Mbps to 267 Mbps. It is compliant with the Consultative Committee for Space Data Systems (CCSDS) Optical Communications Coding and Synchronization Standard. This standard will be used in NASA deep space and other low photon flux missions, such as in the Orion Artemis-2 Optical Communications System (O2O) demonstration, planned for the first crewed flight of Orion. This paper describes the scalable real-time optical receiver system and presents characterization test results.

Keywords: Optical communications, pulse-position modulation

1. INTRODUCTION

The National Aeronautics and Space Administration (NASA) is planning to use the Consultative Committee for Space Data Systems (CCSDS) Optical Communications High Photon Efficiency (HPE) Standard[1] in future missions requiring photon-counting optical communication systems. Planned missions include the Optical Artemis-2 Orion (O2O)[2] communications demonstration on the first crewed flight of the Artemis program as well as the Psyche[3] mission into deep space. The CCSDS HPE standard uses serially concatenated pulse-position modulation (SCPPM), with code rates of 1/3, 1/2, or 2/3 and pulse-position modulation (PPM) orders of 4, 8, 16, 32, 64, 128, and 256. PPM pulse widths range from 512 ns to 125 ps so that the maximum data rate supported is ~2 Gbps.

The NASA Glenn Research Center (GRC) has designed and built a photon-counting receiver using commercial off the shelf (COTS) components, so that the system can be replicated and installed in ground stations for use in future missions requiring photon-counting optical communications. The receiver consists of a fiber interconnect, superconducting nanowire single-photon counting detectors (SNSPDs), and a field programmable gate array (FPGA) based receive modem. The receiver is designed to be compatible with the CCSDS Optical Communications HPE Standard, with a maximum 500 ps slot and data rates up to 533 Mbps. The current system supports data rates up to 267 Mbps.

The ground receiver key subsystems are described in Section 2. The system characterization test setup is presented in Section 3. Section 4 describes system performance characterization results.

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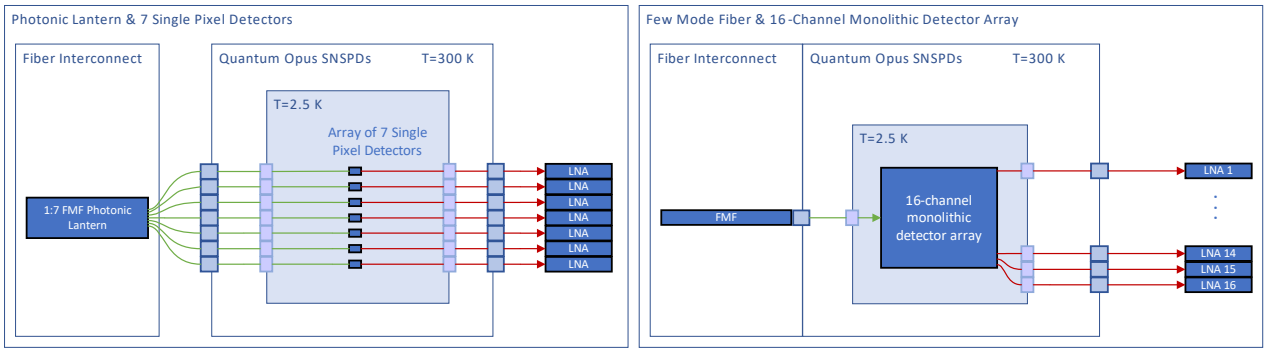
2. REAL TIME OPTICAL RECEIVER SYSTEM DESCRIPTION

The real-time photon-counting ground receiver connects to the backend optics after the telescope in an optical ground station. The receiver consists of a fiber interconnect, SNSPDs, and an FPGA-based receive modem. Each subsystem is described below.

2.1 Fiber Interconnect and Detectors

Two fiber/detector architectures are being prototyped and tested in the laboratory[4]. The first architecture, depicted in Figure 1 (a), consists of a few-mode fiber (FMF) photonic lantern with one multi-mode input and seven FMF outputs in which each output is individually coupled to an SNSPD. Conversely, the second architecture consists of a single FMF coupled to a multi-channel SNSPD array, as depicted in Figure 1 (b). In both cases, the few-mode fiber is 20-μm graded-index core, with a numerical aperture (NA) of 0.19, supporting propagation of up to six LP-modes, LP_{01}, $LP_{11e/o}$, $LP_{21e/o}$, and LP_{02}. For the photonic lantern, the seven FMF output fibers have been adiabatically tapered over a length of 70 mm to form a single-core, multi-mode input approximately 55 μm in diameter[5]. After connectorization and packaging into a metal tube, the input and taper section are ~ 180 mm in length. Since each output FMF supports six LP modes, the photonic lantern in total can couple 42 modes, not including polarization. The photonic lantern can be scaled by changing the number of output fibers.



(a) (b)

Figure 1. Two fiber interconnect and SNSPD architectures. (a) photonic lantern paired with seven single-pixel detectors; (b) a few-mode fiber paired with a 16-channel monolithic detector array.

For the photonic lantern architecture, the SNSPDs in use are commercial devices and have been characterized previously[6,7]. For convenience, the salient features are summarized. The SNSPDs are butt-coupled to the FMFs, which have been AR-coated to reduce blackbody background counts, and enclosed in a cryocooler operating at 2.5 K with the cryocooler encased in a connectorized box to be rack-mountable. Each device is a meandered nanowire approximately 14 μm in diameter, with a central operating wavelength of 1.55 μm, current biased with a DC-coupled preamplifier stage, and readout through room temperature low-noise amplifiers (LNAs). Detection efficiency is referenced to the front panel connector, and for best polarization found to be nearly 80-82% at a background/dark count rate of approximately 3000 cps, with the deconvolved detection jitter in the range of 60 – 80 ps full width at half maximum (FWHM). Output pulses have a rise time of about 850 ps, a 1/*e* reset time on the order of 15 ns, and each SNSPD has a count rate of 20 Mcps at 50% maximum efficiency with a saturated count rate approaching 60 Mcps or more.

In the second architecture, with a single FMF, the SNSPD is a commercially fabricated multi-channel array, with a scalable number of sub-elements. The SNSPD has 16 sub-elements linearly arrayed, with each sub-element 16 μm x 1 μm in size for a total 16 μm x 16 μm device. Each SNSPD in the array is individually biased and read out, using identical electronics to the other system architecture, for a total of 16 output channels. As in the other architecture, the FMF has been AR-coated to reduce background counts and is butt-coupled to the SNSPD array operating at 2.5 K in the same cryostat. After device characterization[8], maximum detection efficiency was found to be approximately 83% with a background/dark count rate of between 3 and 10 kcps, and 75 – 95 ps FWHM detection jitter. Pulse rise times are on average 500 ps, with 1/*e* reset times in the 5 – 8 ns range. The total count rate at 3 dB loss is 500 Mcps, and a saturated total count rate nearly 1 Gcps, with negligible channel crosstalk probability.

2.2 FPGA-based Receiver

The FPGA-based receiver is implemented on a COTS FPGA development platform. The system uses two FPGA cards housed in a Micro Telecommunications Architecture (MicroTCA) chassis. One FPGA card is used for detector channel combining, symbol timing recovery, codeword alignment, and symbol deinterleavering. The other FPGA card is used for iterative decoding, derandomization and deslicing. Additional cards could be added to the chassis to scale the system to higher data rates. A block diagram of the system is shown in Figure 2.

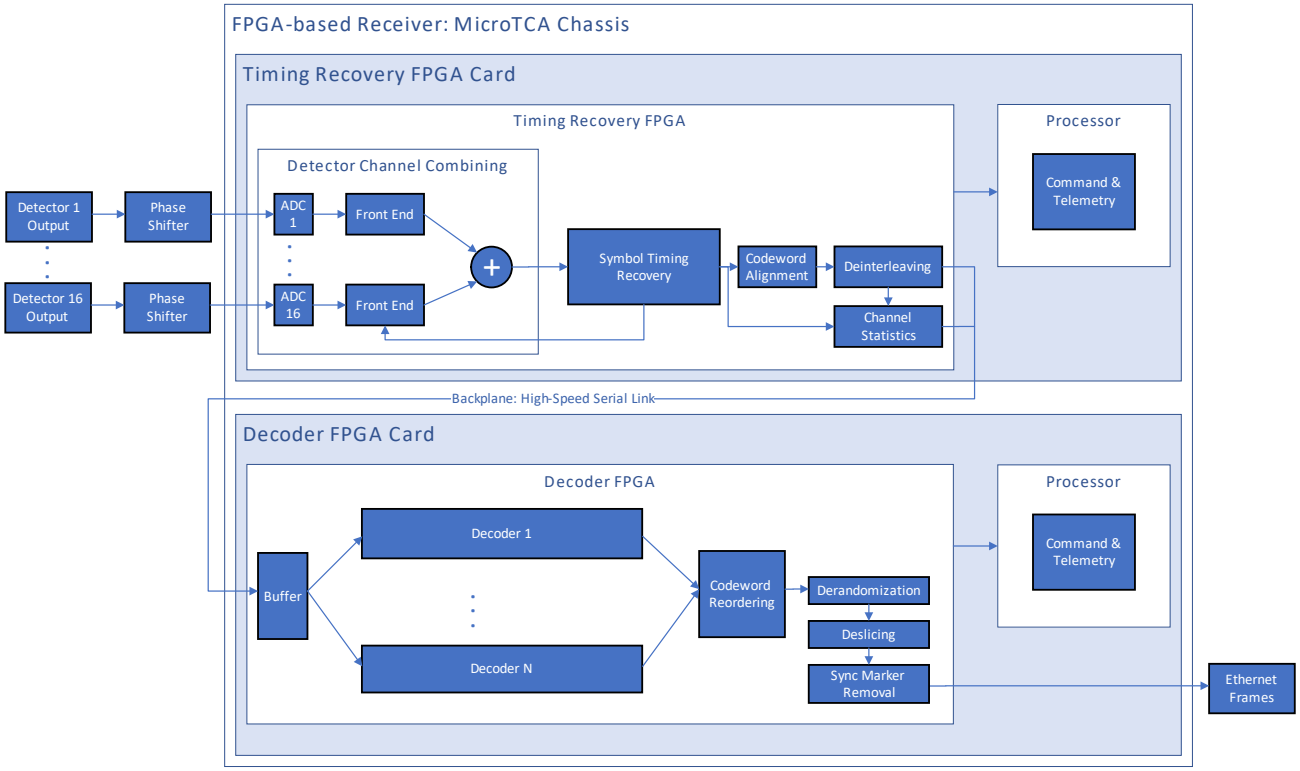


Figure 2. Block diagram of the FPGA-based receive modem.

The timing recovery loop is implemented on a Xilinx Radio Frequency System-on-Chip FPGA with 16 analog to digital converters (ADCs). The detector channels are time-aligned outside the FPGA with mechanical phase shifters. The ADCs on the timing recovery FPGA sample the output of each detector channel individually. The photons are counted and combined digitally before symbol timing recovery[9] is performed. The timing recovery loop front end uses the phase error fed back from the symbol timing recovery module to interpolate between the detector samples at the slot boundary. After the timing recovery loop, codeword alignment is performed using an approximation to a maximum likelihood correlator with scaling[10]. The received channel statistics, including the mean photons per signal slot, K_s, and the mean background photons per slot, K_b, are also calculated. A histogram is generated of the received slot counts over 32,768 consecutive symbols. K_b is calculated from the average photon counts in the guard band and K_s is calculated from the difference of the average photon counts in the signal slots and guard band. Convolutional deinterleaving is implemented utilizing an external DDR4 memory operating at 2400 MHz[11]. The deinterleaved symbols with 3 bits per slot and the received channel statistics are sent over the backplane on a high-speed serial link to the decoder FPGA. The timing recovery FPGA can be reconfigured in real time with a different PPM order, slot width, and several different deinterleaver sizes.

The SCPPM decoder is implemented on a Xilinx Virtex 7 FPGA. Using the channel statistics, the decoder calculates the 8-bit slot log-likelihood ratios for valid input codeword slot counts. Then the decoder performs queuing of the input codewords, iterative Bahl, Cocke, Jelinek, and Raviv (BCJR) decoding[12] with multiple decoder instances, output codeword reordering, derandomization, deslicing, and removes transfer frame synchronization markers. The received data is sent out of the chassis in Ethernet packets. The base decoder code is the same for all PPM orders and code rates, but the CCSDS mode is selected at build time.

The decoder FPGA can also receive slot counts and channel statistics from an external device over Ethernet. This enables independent characterization of the SCPPM decoder performance using a software model to generate slot counts and channel statistics prior to integration with the system.

Each FPGA card contains a processor, which is used to command the FPGA and report telemetry. The telemetry data adheres to a client-server networked architecture through hypertext transfer protocols (HTTP) and utilizes standard data formats, such as plaintext or JavaScript Object Notation (JSON). The control software, written in C/C++, was built on NASA's Space Telecommunications Radio System (STRS)[13] standard and interacts with the underlying processor to send commands to and receive telemetry from the FPGA through memory-mapped registers.

3. TEST SETUP DESCRIPTION

A block diagram of the test setup is shown in Figure 3. The test optical transmitter is used to emulate the signal sent from the spacecraft. The signal is sent through free-space path loss emulation and into the real time optical receiver system. The test transmitter and receiver system use a common 10 MHz clock reference for system characterization.

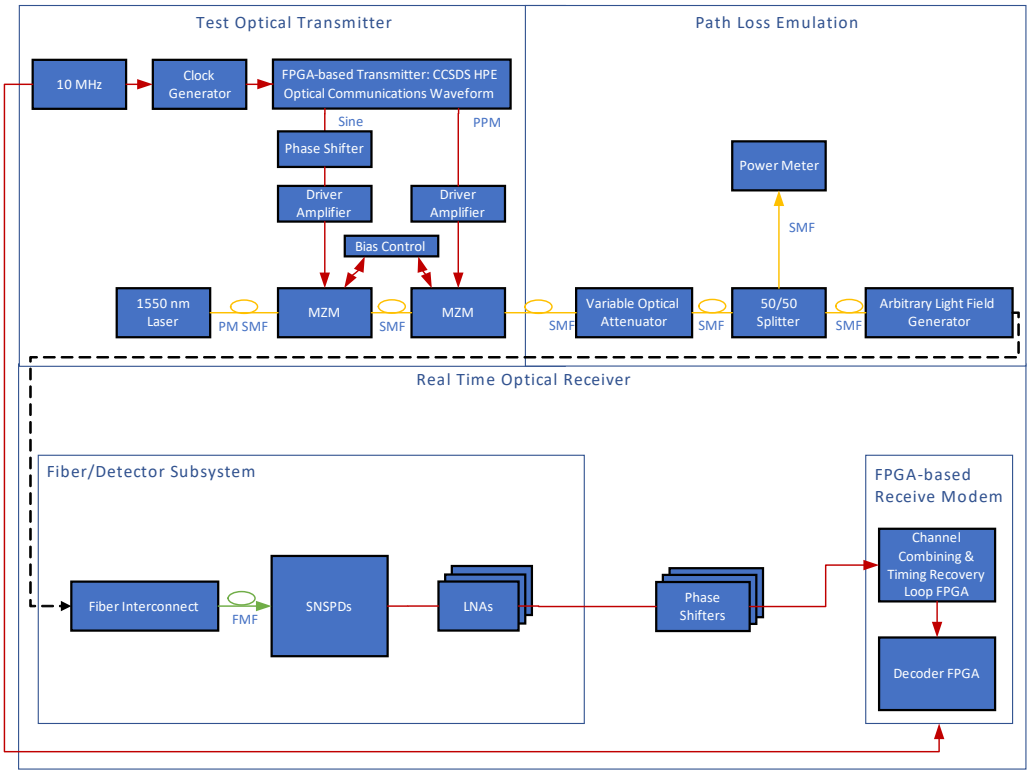


Figure 3. Block diagram of the real time optical receiver system within the optical communications test bed.

3.1 Test Optical Transmitter

The test transmitter generates the PPM signal sent on the downlink to the ground optical receiver. It consists of the FPGA-based transmitter, a laser, and a pulse carving electro-optic modulator system.

The FPGA-based transmitter accepts Ethernet frames and performs slicing, randomization, SCPPM encoding, Cyclic Redundancy Check (CRC) attachment, convolutional channel interleaving, codeword synchronization marker insertion, modulation, and guard slot insertion in compliance with the CCSDS HPE standard. It also generates a square wave at the same frequency as the PPM slot clock. The square wave is low-pass filtered to generate a sine wave which is used to carve

the data with the Mach-Zehnder modulators (MZM). Both the PPM and sine wave signal are sent out the FPGA using the onboard gigabit transceivers.

The modulated optical signal is generated with two MZMs connected serially. The first MZM is fed optically with a continuous wave polarized laser source and modulated with the sine wave signal generated by the FPGA-based transmitter. An inline mechanical phase shifter is used for fine tuning the phase alignment between the sine wave and PPM signals. A small amount of the optical output is tapped and measured for bias control feedback. The average feedback power at the quadrature point is determined during initialization and this level is maintained with a proportional-integral (PI) control loop.

The second MZM is fed with the optical output of the first MZM and modulated with the electrical PPM signal generated by the FPGA-based transmitter. A small portion of the optical output is tapped and measured for bias control feedback. This average power is minimized by the controller using the gradient descent technique[14] with a five-point stencil derivative. Minimization of the average output power places the off slots near the null point of the modulator. This approximation is more accurate for higher PPM orders (16 or greater) as the minimum power is closer to zero. The optical intensity of the pulsed slots is controlled by the amplitude of the electrical input signal and is optimized when the peak potential is near the V_π of the MZM.

3.2 Path Loss Emulation

The free-space path loss is emulated using a variable optical attenuator (VOA). The power into the receiver system is measured with a power meter. No additional background noise is added so the noise received is determined by the extinction ratio of the test optical transmitter.

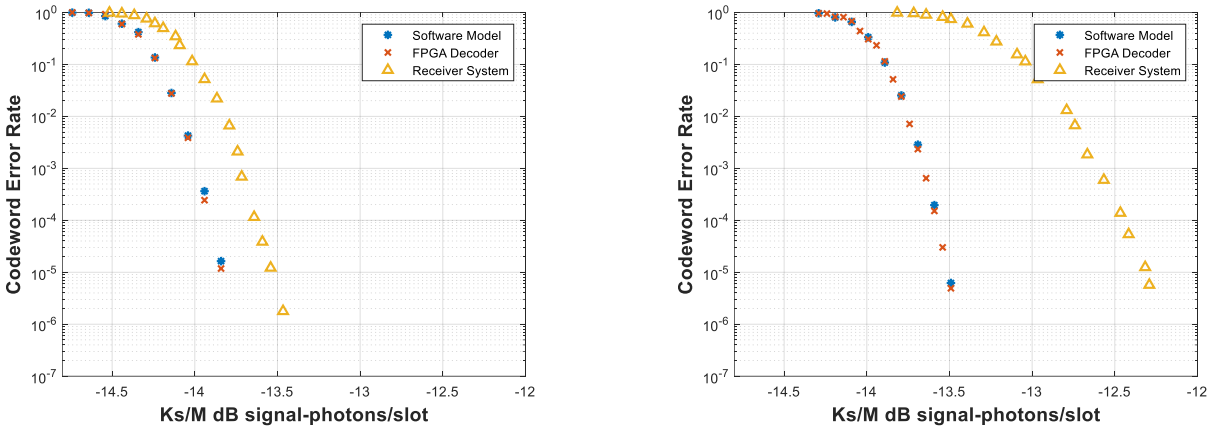
After the VOA, the light is delivered via a fiber to the Arbitrary Light Field Generator (ALF-G)[15,16], which is used to generate a flat-top beam profile. At the output of the ALF-G, the flat-top beam is focused into the receiver fiber interconnect. For the data presented in this paper, the light was focused with an NA that maximizes the throughput for an atmospherically disturbed beam with a $D/r_0=9$ (the predicted worst-case condition at the ground station site). The NAs that produce the maximum throughput for this condition are 0.13 for the photonic lantern and 0.18 for the FMF. However, these NAs do not produce the maximum throughput for the flat-top beam profile. This has a larger effect on the photonic lantern, decreasing the throughput by ~2.1 dBm compared to a ~0.15 dBm decrease for the FMF. A more detailed and comprehensive study on loss differences between the FMF and the photonic lantern has been discussed previously[4].

4. SYSTEM CHARACTERIZATION RESULTS

System characterization results are presented in this section for both fiber/detector architectures with the FPGA-based receive modem. The waveform modes tested are the PPM-16, code rate 1/3, 500 ps slot, 133 Mbps data rate mode; and the PPM-16, code rate 1/2, 500 ps slot, 200 Mbps data rate mode. Codeword error rate (CWER) curves were measured. The fiber/detector subsystem loss and the detector jitter and FPGA implementation loss were calculated.

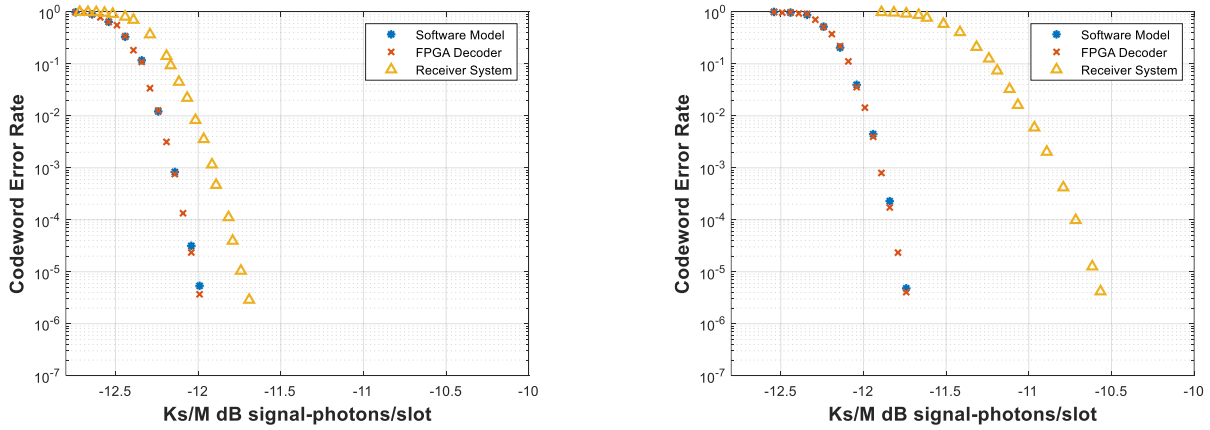
The receiver system codeword error rate curves are shown in Figures 4 and Figure 5. Each point on the codeword error rate curve contains at least one minute of data and a minimum of 100 codeword errors. The average K_s from each minute is used to place the codeword error rate data into K_s bins sized 0.025 dB apart. The binning method is used to compensate for modulator drift and variability in the bias point. The bias controller re-biases the MZMs every minute in between data collection. Codeword error rate curves with the decoder software model using 8-bit log-likelihood ratios and with the decoder FPGA implementation only are also plotted in the figures. The curves show that the FPGA decoder implementation matches the software model very closely. The receiver system has approximately 0.3 dB of implementation loss for the photonic lantern + 7 single-pixel detectors and 1.2 dB of implementation loss for the FMF + 16-pixel array. This implementation loss includes FPGA implementation loss and detector jitter.

Additional test results are summarized in Table 1. The fiber interconnect and detector loss (including efficiency, polarization loss, and blocking loss) is around 3-4 dB higher for the photonic lantern + 7 single-pixel detectors than the FMF + 16-pixel array. The measured K_b is 4-5 dB higher for the FMF + 16-pixel array. After accounting for the mismatch between the flat-top beam profile and the fiber interconnect NA, the two architectures perform within 3 dB of each other, depending on the mode. The required input power for a 10^{-5} codeword error rate is about 1-3 dB higher for the photonic lantern + 7 single-pixel detectors than for the FMF + 16-pixel array.



(a) (b)

Figure 4. Codeword error rate curves for the PPM-16, code rate 1/3, 500 ps slot, 130 Mbps mode. (a) photonic lantern + 7 single-pixel detectors (b) few-mode fiber + 16-pixel array.



(a) (b)

Figure 5. Codeword error rate curves for the PPM-16, code rate 1/2, 500 ps slot, 200 Mbps mode. (a) photonic lantern + 7 single-pixel detectors (b) few-mode fiber + 16-pixel array.

Table 1. System characterization results for the photonic lantern + 7 single-pixel detectors (PL) and the FMF + 16-pixel array (A).

PPM Order	Code Rate	Data Rate (Mbps)	Detector Jitter & FPGA Implementation Loss (dB)		Fiber & Detector Loss (dB)		Measured K_b at 10^{-5} CWER (dB photons/slot)		Required Input Power at 10^{-5} CWER (dBm)	
			PL	A	PL	A	PL	A	PL	A
PPM-16	1/3	133	0.3	1.2	8.0	3.2	-27.2	-22.0	-72.2	-75.5
PPM-16	1/2	200	0.3	1.2	9.6	3.5	-24.7	-20.8	-68.7	-73.5

5. CONCLUSION

A photon-counting optical receiver compatible with the CCSDS HPE standard was designed and built using mainly COTS parts. Two fiber/detector architectures were tested in the system with two CCSDS HPE modes. The FMF + 16-pixel array has about 1 dB more implementation loss than the photonic lantern + 7 single-pixel detectors, but the fiber interconnect + detector loss is 3-4 dB higher for the photonic lantern + 7 single-pixel detectors. When operating in an optical ground station where the photonic lantern numeric aperture is matched to turbulence conditions, it is expected that both architectures will perform within 3 dB of each other when operating a 10^{-5} codeword error rate. In the future, NASA GRC plans to demonstrate this ground receiver with the O2O mission on Artemis-2 at the Low-Cost Optical Terminal (LCOT) ground station in collaboration with the NASA Goddard Space Flight Center[17].

6. ACKNOWLEDGEMENTS

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