Recent Progress in Extreme Environment Durable SiC JFET-R Integrated Circuit Technology

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Abstract

This work updates recent progress made by NASA Glenn Research Center on further advancement of its uniquely durable silicon carbide junction field effect transistor and resistor (SiC JFET-R) integrated circuit (IC) technology since HiTEC 2021. Key fabrication process improvements compared to earlier NASA Glenn IC prototype runs have been ascertained via extensive "back end of line" (BEOL) processing experiments conducted on practice wafers over the past two years. The resulting changes to the BEOL process flow employed in the fabrication of "Generation 12" SiC JFET-R wafers are described. The NASA Glenn SiC JFET-R IC prototype "Generation 12" chipset design realizes significantly higher complexity digital and analog integrated ICs aimed at flexibly implementing a broad variety of mission-enabling extreme-environment electronics demonstrations. SPICE simulations have verified circuit designs ranging from simple amplification of analog sensor signals up through long-duration Venus lander operations and microprocessor-based of electric motor drive.

Key words

Silicon Carbide, Integrated Circuit, JFET, SiC, Microprocessor, Interconnect

I. Introduction

At HiTEC 2018, NASA Glenn reported the first ICs to demonstrate more than a year of stable operation at 500 °C [1]. These "IC Generation 10" prototype ICs are based upon highly robust silicon carbide Junction Field Effect Transistor & Resistor (SiC JFET-R) devices interconnected by two-level $TaSi_2$ metallization passivated with SiO_2/Si_3N_4 dielectric stack. While these early prototype SiC JFET-R chips can perform important electronic functions (such as ring oscillators, logic flip-flops, and high-T sensor signal amplification) far broader circuit capabilities and benefits will be enabled by upscaling chip complexities.

As reported at HiTEC 2021, the "IC Generation 11" NASA Glenn prototype SiC JFET-R run demonstrated more than 4-fold increase in chip complexity primarily facilitated by halving the SiC resistor width dimension (to 3 μm) and increasing the die size (to 4.65 x 4.65 mm) [2]. Initial demonstrations of a 998-bit Read Only Memory (ROM) chip and an 8-bit sigma-delta analog to digital converter (ADC) at 500 °C were reported, but IC Gen. 11 failed to achieve the prolonged 500 °C operation and high yield metrics of IC Gen. 10. IC Gen. 11 attempted to implement interconnect processing revisions aimed at further improving IC durability and yield that instead resulted in undesired degradation of both these key performance metrics [2,3].

To achieve advanced (mission driven) improvements in IC complexity and performance, IC Gen. 12 further increases chip size (to 5 mm x 5 mm) and reduced feature sizes compared to IC Gen. 11 [2]. Even with IC Gen 10 record-breaking demonstrations of prolonged 500 °C durability, a minority percentage of IC Gen. 10 chips tested at 500 °C suffered from sudden and unpredictable "infant" failures, initiated by dielectric layer crack formation, that would likely preclude actual deployment into high-reliability

aerospace applications [1,4]. Therefore, further understanding and resolution of remaining interconnect processing and high-T durability challenges is crucial to the continued advancement of durable SiC JFET-R ICs towards reliable harsh-environment aerospace application infusion.

This HiTEC 2023 paper summarizes recent progress made by NASA Glenn on advancing SiC JFET-R IC technology. As detailed in the following sections, this progress includes (1) results of key processing experiments that further developed the "Back End of Line" (BEOL) interconnect processing to be employed during the completion of the IC Gen. 12 wafer run, and (2) the multi-functional capabilities of the IC Gen. 12 chipset.

II. BEOL Interconnect Process Experiment

Previously reported NASA Glenn IC Gen. 11 results [3] revealed dramatic differences in interconnect stack thermal (including cycling) durability with the addition of a 67 nm thick Si_3N_4 layer between Metal1 and Metal2 that was not present in earlier NASA JFET-R IC generations. Those results in large part motivated the broader experimental study of Si_3N_4 layer permutations described in this section.

A. BEOL Test Experimental

Six different metal/dielectric interconnect stack structures were respectively carried out on six SiC test wafers. Fig. 1 presents a simplified cross-sectional schematic depiction of the six variations of the two-metal-level interconnect/dielectric stacks studied. These six structures (designated "BEOL1" through "BEOL6") are all compatible with the interconnect and bond pad process flow employed for preceding two-level interconnect NASA Glenn SiC JFET-R IC generations [1-7]. The salient differences between the six structures studied are the locations of 0.1 µm thick Si_3N_4 layers (depicted in red in Fig. 1, always sandwiched in the middle of ≥ 0.4 µm thick SiO_2 layers depicted in blue) in addition to two thicknesses (0.4 µm or 0.6 µm) for two of the SiO_2 layers. Dry etches and metal

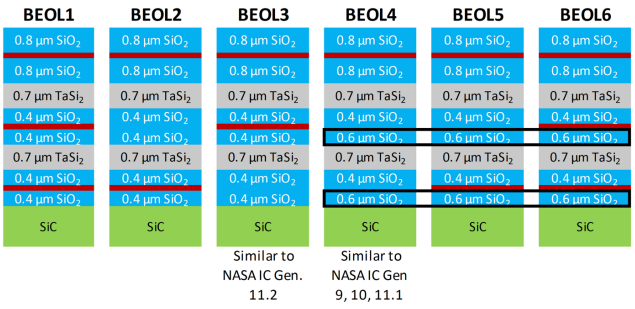

Fig. 1. Simplified cross-sections of the six interconnect layer structures studied in the BEOL test experiment. Each red line denotes where a 0.1 µm thick layer of low-stress LPCVD Si_3N_4 was deposited.

layer depositions were carried out in succession using single-wafer systems, which permitted minor process adjustments, but this also resulted in evidence of process drift during some six-wafer process step sequences. Simultaneous/batch deposition was employed for dielectric layer depositions (to the extent the different layer structures of Fig. 1 permitted).

For experimental consistency with the IC Gen. 12 wafers, the six starting 4H-SiC substrates employed for this BEOL study were implanted with phosphorous at 600 °C (1.2 x 10^{15} cm^{-2} @ 180 keV, 6.0 x 10^{14} cm^{-2} @ 130 keV, 6.7 x 10^{14} cm^{-2} @ 80 keV, 3.9 x 10^{14} cm^{-2} @ 40 keV), activation annealed (1360 °C for 100 hours in N_2 while capped with 1 µm SiO_2 that is subsequently stripped), and mesa-pattern etched (depth ~ 0.9 µm) to provide SiC surface n-type conductivity and topography mimicking those of the partially fabricated IC Gen. 12 wafers [1,2,6,7]. Many interconnect/via test patterns derived/modified from IC Gen. 12 mask layouts were employed along with additional test structures (such as larger-area Meta1 to Metal2 capacitors) not found in the IC Gen. 12 design. Aside from the BEOL4 wafer that was n-type without any epilayers, the remaining five BEOL test wafers featured homoepitaxial n-channel (0.6 µm, 1 x 10^{17} cm^{-3}) residing on top of p-type (4 µm, 5 x 10^{16} cm^{-3}) layer to facilitate pn-junction mesa device isolation.

Except for film thicknesses, the 720 °C Low-Pressure Chemical Vapor Deposition (LPCVD) SiO_2 deposition process was effectively unchanged from IC Gen. 10 & 11 [1-6]. Stoichiometric 0.1 µm thick Si_3N_4 layers were also deposited using 25 sccm SiH_2Cl_2 : 75 sccm NH_3 via LPCVD at 800 °C instead of 720 °C employed in IC Gen. 10 & 11 [9]. A new $TaSi_2$ metal sputtering process that lowers post-anneal film stress [10] was also adopted for this study.

The dimensional shrink combined with higher circuit complexity for IC Gen. 12 drove the development of an "all dry" Reactive Ion Etch (RIE) for the Via1 etch conducted at 50 mTorr in 30.5 sccm C_4F_8 : 35 sccm Ar 50 W plasma that replaced the SF_6/Ar RIE "dry" + 6:1 buffered oxide etchant (BOE) "wet" IC Gen. 10 & 11 Via 1 etch process [1]. The subsequently sputter-deposited ~ 30 nm Ti followed by ~0.13 µm $TaSi_2$ ohmic contact film thicknesses were also reduced from IC Gen. 10 & 11 [1] towards improving liftoff patterning yield. The C_4F_8/Ar etch also offers higher selectivity against over-etch into underlying Metal1 $TaSi_2$ at the completion of the Via2 etch.

It is worth noting that for wafers BEOL1 & 2 the C_4F_8/Ar RIE was attempted for the Via3 etch that penetrates all the stacked dielectric layers to expose the SiC surface for subsequent Iridium Interfacial Stack (IrIS) durable bond pad metal deposition [1,8,11]. It was found that this much deeper/longer (~4X than Via1/Via2) etch of large-area features produced an undesirably degraded SiC surface morphology that may have arisen due to polymer formation in this dry-etch chemistry [12]. As a result, the Via3 etch for

the remaining wafers was carried out by dry etching through the bottom-most Si_3N_4 layer followed by wet (6:1 BOE, ultrasonically agitated) etch to expose the SiC surface for subsequent IrIS bond pad stack deposition (i.e., the same bond pad Via3 etching approach used for IC Gen. 10 & 11 [1]).

B. BEOL Test Characterization

The BEOL test wafers were microscopically inspected at various stages of the fabrication process, and 25 °C electrical probe testing was also conducted following completion of Via1, Via2, and bond pad patterning steps. An automated probing system with DC source-measure units comprehensively mapped device current-voltage-resistance across all BEOL test wafers following bond pad patterning.

Fig. 2 presents a dramatic-contrast example (not statistically representative) from optical microscope inspections carried out after deposition of the final SiO_2 layers (prior to bond pad via and metal stack processing). Dielectric cracking and associated film discoloration is readily evident in the Fig. 2a photo of the BEOL5 sample (a portion of a prototype ROM chip near the wafer center) while the Fig. 2b photo of the exactly corresponding region on the BEOL6 sample exhibits no microscopically observable evidence of dielectric cracking.

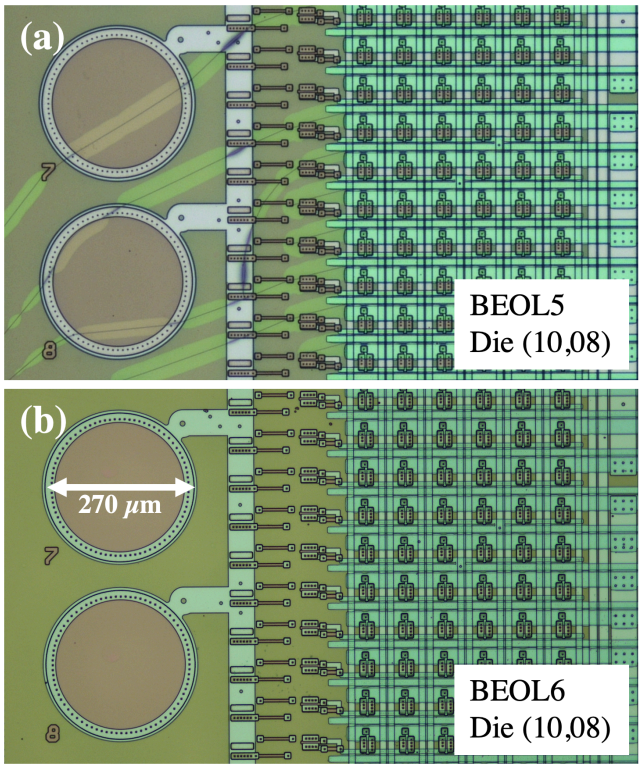

Fig. 2. Optical microscope photos of the identical regions of (a) BEOL5 and (b) BEOL6 recorded following deposition of the final 0.8 μm SiO_2 layer. This region of the BEOL5 wafer exhibited abundant dielectric layer cracks while no dielectric layer cracks are visible for same location on the BEOL6 wafer.

No cracks were observed immediately prior to the topmost Si_3N_4 layer deposition, but cracks visible after this final nitride deposition account for the vast majority (if not all) of the cracks seen after BEOL test process completion. Fig. 3 graphically maps the number of cracks manually counted within each 5 mm x 5 mm die region using optical microscopy for the upper right quadrants of the six BEOL test wafers following the completion of bond pad patterning. The BEOL1 and BEOL6 wafers that uniquely contain three separate Si_3N_4 layers exhibit the lowest observed crack populations, the majority of which reside within 8 mm of the wafer edge. For the remaining other wafers, the crack density is highest near the wafer center suggesting that wafer-scale film stress might play a role in the observed crack formation.

Electrical probe-testing conducted immediately following SiC contact liftoff patterning revealed that the Via1 etch had failed to completely penetrate the bottom SiO_2 layer to reach the implanted SiC surface for the central regions of BEOL wafers 1, 2, 5 and 6, despite etch time adjustments intended to account for the added thickness of the Si_3N_4 layers on these wafers. This behavior has been attributed to slightly (unanticipated) reduced dry etch rate for SiO_2 layers subjected to (i.e., beneath) Si_3N_4 layer depositions combined with the known etch rate non-uniformity (slower etching at wafer center compared to wafer periphery) of NASA Glenn's parallel-plate RIE system. Since metal contacts reaching SiC through the Via1 etch hole are necessary for all bond pad electrical connections to/from the test chip at the end of fabrication [8], the central regions of BEOL 1, 2, 5, and 6 finished wafers electrically mapped as non-conducting due to the undesired remaining SiO_2. Therefore, these insulating central wafer regions were excluded from electrical analysis.

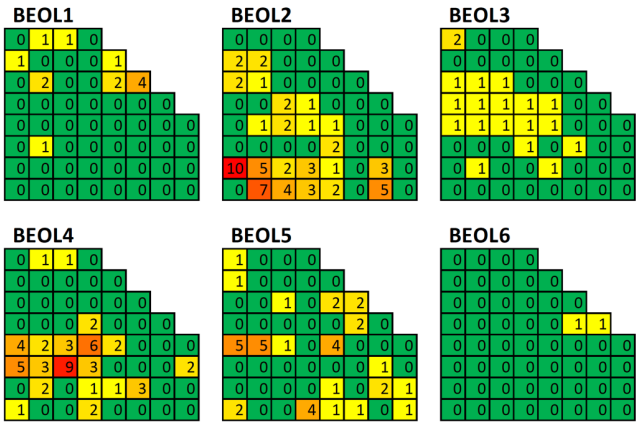

Fig. 3. Data maps of the upper right quadrant of each of the six BEOL test wafers summarizing the number of dielectric cracks manually detected by optical microscopy within each 5 mm x 5 mm die area following bond pad etching. The lower left box of each map corresponds to Die (09,09) whose lower left corner corresponds to the wafer center.

Another non-ideality encountered is varying degrees of ballooning/widening of metal trace features that has been attributed to varying degrees of photoresist reflow that occurred during the metal patterning RIE steps.

Table 1 compares selected 25 °C electrical data measured from key test structures amongst the BEOL wafers during automated probe-test mapping. All devices falling within the "Analysis Exclusion Radius" (from the wafer center) shown in the top data row are excluded as these were compromised by the incomplete Via1 etch described above. Table 1 also excludes the BEOL4 wafer that cannot be usefully mapped and compared since it lacks pn junctions for sufficient electrical isolation of individual devices.

The unshaded (upper) data rows of Table I compare average sheet and contact resistance properties, including the sheet resistances extracted from Metal1 and Metal2 test traces that ran over flat topography compared to traces that ran over arrays of underlying mesa topography. While significant variation in quantities across the 5 BEOL wafers (columns) are apparent for some measurements (rows), the observed spreads would have had negligible impact on Gen. 12 IC performance. There is anecdotal evidence that processing drift/adjustments over the course of sequentially (six-times) repeating single-wafer-tool process steps contributed to some of the observed parameter spreads. For example, varied amounts of photoresist removal (impacting $TaSi_2$ trace thickness and morphology) and photoresist reflow (impacting $TaSi_2$ trace lateral extent) were noted during metal etching sequences that would somewhat affect metal sheet resistance (R_{Sheet}) values shown in Table I.

TABLE I
SUMMARY OF SELECTED 25 °C BEOL TEST ELECTRICAL WAFER MAP MEASUREMENTS

Test	BEOL1	BEOL2	BEOL3	BEOL5	BEOL6
Analysis Exclusion Radius (r) Due To Incomplete Via1 Etch	35 mm	25 mm	0 mm	20 mm	25 mm
Metal 1 Over Flat Topography Avg. R_{Sheet}	1.9 Ω/sq.	1.4 Ω/sq.	1.4 Ω/sq.	0.82 Ω/sq.	0.92 Ω/sq.
Metal1 Over Mesa Topograpy Avg. R_{Sheet}	2.1 Ω/sq.	3.1 Ω/sq.	2.6 Ω/sq.	1.2 Ω/sq.	1.7 Ω/sq.
Metal 2 Over Flat Topography Avg. R_{Sheet}	0.97 Ω/sq.	1.2 Ω/sq.	0.89 Ω/sq.	0.91 Ω/sq.	0.94 Ω/sq.
Metal2 Over Mesa Topography Avg. R_{Sheet}	2.3 Ω/sq.	2.1 Ω/sq.	1.5 Ω/sq.	1.3 Ω/sq.	2.1 Ω/sq.
Source/Drain Implant Avg. R_{Sheet}	540 Ω/sq.	560 Ω/sq.	432 Ω/sq.	530 Ω/sq.	350 Ω/sq.
Avg. Specific Contact Resistivity	62 $\mu\Omega$-cm^2	140 $\mu\Omega$-cm^2	80 $\mu\Omega$-cm^2	110 $\mu\Omega$-cm^2	150 $\mu\Omega$-cm^2
9μm Metal1+2 Long Trace Conduction % Yield (R < 5 kΩ)	88%	98%	98%	79%	100%
9μm Metal1+2 Long Trace Conduction Avg. R	2.0 kΩ	2.5 kΩ	1.7 kΩ	1.1 kΩ	1.5 kΩ
45μm Metal1+2 Long Trace Conduction % Yield (R < 1 kΩ)	87%	96%	91%	91%	97%
45μm Metal1+2 Long Trace Conduction Avg. R	320 Ω	420 Ω	240 Ω	200 Ω	300 Ω
128 SiC R+Metal1 Chain Conduction % Yield (R < 200 kΩ)	82%	86%	79%	96%	100%
128 SiC Resistor+Metal1 Chain Conduction Avg. R	100 kΩ	67 kΩ	68 kΩ	60 kΩ	51 kΩ
Metal1 to Metal2 Interconnect Isolation %Yeild (R > 1 GΩ)	100%	99%	97%	91%	99%
Metal1 to Metal2 Interconnect Isolation Avg. R	21 GΩ	33 GΩ	68 GΩ	53 GΩ	74 GΩ

Shaded rows are "ROM" BEOL test chip measurements.

The shaded lower rows of Table 1 focus on measurements of both conduction and isolation (to 50 V DC) of interconnect test structures residing on the "ROM" BEOL test chip design. This benchmark chip was derived by slightly altering the interconnect/via mask pattern of the 2 kbit ROM chip that is the most complex chip of the IC Gen. 12 prototype run. Worst-case interconnect test traces/devices include long Metal1 and Metal2 ("Metal1+2 Long", both 45 µm wide power bus as well as 9 µm wide signal) traces spanning most of the 5 mm die dimension that crosses overhead of hundreds of underlying topological features in the same manner (i.e., same layout design) as will occur on the IC Gen. 12 ROM chip itself. The BEOL6 wafer exhibited the overall highest yield of long-trace ROM interconnect test structures.

C. BEOL Test Summary Discussion

Even though the BEOL test chips remain to be packaged and tested at elevated temperature, important findings of this experiment are nevertheless already evident. First and foremost, the suppression of dielectric cracking as well as highest overall "ROM" interconnect test electrical yields in the BEOL6 wafer has warranted its selection as the basis (with corrections for via and metal etch issues noted above) for finishing the IC Gen. 12 fabrication run.

It is also worth noting that the BEOL3 cross-section in Fig. 1 is structurally very similar to IC Gen. 11.2, which probe-tested as completely failed at 25 °C due to open-circuit metal-crack failures wherever Metal2 crossed over oxide topography imparted by underlying mesas and/or Metal1 traces [3]. However, there is no electrical evidence in the BEOL probe-test data that the IC 11.2 Metal2 cracking failure mechanism was replicated in any of the 25 °C probed BEOL test wafers. This suggests that implemented deposition process revisions, including the revised $TaSi_2$ sputter process reported in [10], significantly impacted the observed BEOL test results in addition to the different interconnect layer-structures with different locations of Si_3N_4. Since detrimental effects of stress usually increase with film thickness, it is counterintuitively noteworthy that the slightly thicker BEOL6 3-nitride-layer stack yielded the best results over the slightly thinner BEOL1 3-nitride-layer stack.

III. Gen. 12 Chip Library

This section briefly overviews general capabilities of Application Specific Integrated Circuit (ASIC) Gen. 12 chip designs presently undergoing fabrication at NASA Glenn. These chips are intended to uniquely bring new electronics

capability for long-term operation to 500 °C mission environments. The first-order SPICE transistor/resistor models and layout rules employed in designing the IC Gen. 12 chip library have been posted online by NASA Glenn since April 2019 [5]. These IC Gen. 12 chip designs have been simulated in SPICE at 25 °C, 460 °C (Venus surface temperature) and 500 °C to function with negligible change to signal voltages (consistent with prior SiC JFET-R experimental test results [13]). Owing to 4H-SiC conduction temperature behavior, the IC operating power and frequency performance decreases by a factor of roughly 4 to 5 as temperature increases from 25 °C to 500 °C. SiC JFET-R logic operates near 0 V to -10 V signals using V_{DD} near +25 V and V_{SS} near -25 V power supplies [5]. Simpler ASICs were implemented in 24-pad 2.5 mm x 2.5 mm chip frames while more complicated chips reside in 5 mm x 5 mm die with either 56, 62, or 72 pads. The ceramic high temperature packages custom-designed for these chips are described in a separate paper at this conference [14].

A. Microprocessor

Two of the IC Gen. 12 chips are designed for packaging together to implement a basic yet highly capable/versatile microcontroller with functional similarity to the MC14500B Industrial Control Unit developed by Motorola Corporation in 1977 [15]. The simplified Transport Triggered Architecture logic approach, instruction set, and functional examples of microcontroller programming and use will be described elsewhere [16]. At 460 °C (Venus's surface temperature), SPICE simulations indicate the microprocessor will consume roughly 1.3 W of power.

B. Memory (RAM and ROM)

The 2-kbit (128 x 16-bit) Read Only Memory (ROM) and 248-bit (31 x 8-bit) Random Access Memory (RAM) chips were both designed to function in concert with the IC Gen. 12 microprocessor. The ROM is mask-layout coded with multiple programs for running diagnostic and hardware demonstrations which SPICE predicts will consume almost 1 W of power at 460 °C. One of the RAM designs implements a shared read/write data bus with tri-state buffer architecture that will permit systems of multiple SiC IC Gen. 12 memory chips to function using a common data bus. The other RAM design employs separate read and write data busses and consumes roughly 1.2 W power when SPICE simulated at 460 °C.

C. Venus Lander ASICs

Custom IC Gen. 12 chips were designed around demonstrating the Long-Lived In-Situ Solar System Explorer (LLISSE) concept as an initial mission to greatly extend the duration of observational science possible from the 92 atmosphere, 460 °C corrosive environment on the surface of Venus [17]. The LLISSE chip designs are primarily driven by the need to minimize power consumption given the long mission duration (up to 60 Earth days) combined with small lander battery size constraints. Therefore, flip-flops are employed to implement minimal-power state machine control logic to collect and transmit unbuffered sensor data instead of more power-hungry microprocessor and memory buffer ICs. The "LLISSE-TD" (Tech Demo) ASIC chip is designed to convert 4 channels of amplified analog sensor input into 6 data bits per channel with 2-bit channel identification tag to serial data bitstream as the core circuitry for a first/lowest-power technology demonstration Venus lander mission. A correspondingly more capable (but higher power cost) bitstream of 16 sensor channels at 8 bits/channel was also designed using a "LLISSE-16" control ASIC in concert with a pair of "DAQ/MUX8" chips. Both LLISSE approaches employ a Successive Approximation Analog to Digital Conversion (SA ADC) circuit topology. Nearly a dozen different low-power analog op-amp based custom ASICs were designed for interfacing a variety of developmental harsh-environment sensors to the LLISSE ADC topology.

D. Multi-Chip Demonstrators

Additional IC Gen. 12 chips were designed to support construction of a variety of multi-chip harsh-environment demonstration systems. These include simple logic gates, flip flops, ring-oscillator clocks, counters, latches, level shifters, tri-state buffers, digital and analog multiplexors, and a JFET chip designed for paralleling into higher current switching modules (up to ~ 1 Amp at 25 °C). It worth noting that IC Gen. 12 clock chip frequencies are un-referenced, below 1 MHz, and substantially affected by temperature (decreasing by factor of 4 to 5 with temperature rise from 25 °C to 500 °C). Generation of relatively temperature independent and frequency-referenced clock signals remains an unmet technology gap for this extreme temperature range.

Using the IC Gen. 12 chipset, a remarkably broad variety of system/subsystem demonstration circuits have been designed and simulated in SPICE. Multi-chip LLISSE-TD and LLISSE-16 core control/ADC boards have been simulated to autonomously run these lower-power missions. The simulated LLISSE-TD board consists of four IC Gen. 12 chips that measure, amplify, digitize, and serial ping battery voltage, battery current, and temperature using less than 400 mW at 460 °C (excluding the 100 MHz radio transmitter under separate development based upon higher-frequency/power SiC bipolar junction transistors). On the higher end (of both power and complexity), a stepper-motor based line-scanner imaging system has also been designed and simulated using the IC Gen. 12 chipset (including microprocessor and ROM).

The details of various circuits and simulations as well as to technical data sheets for specific IC Gen. 12 chips will be reported in the future as results from corresponding experimental hardware demonstrations become available. Successful 500 °C circuit demonstrations will hinge upon ceramic packaging and circuit boards with sufficiently low parasitic 500 °C leakage currents.

IV. Conclusion

This report has overviewed major aspects of technical progress on SiC JFET-R technology development by NASA Glenn Research Center since HiTEC 2021. As described above in Section III, the IC Gen. 12 represents the most functionally capable SiC JFET-R ICs designed to date. The successful realization of these chips would be enabling for multiple applications including Venus surface exploration. However, circuit functionality at 500 °C is of little value if that functionality does not approach the operational lifetime needed by each respective application. The work described in Section II of this report provides crucial learning towards yielding IC Gen. 12 chips that are long-term durable at 500 °C, especially in terms of minimizing dielectric layer cracks known to be detrimental to SiC JFET-R extreme-environment durability [1-4]. However, as of this writing, the 500 °C durability of the most promising "BEOL6" interconnect process remains to be experimentally verified. Furthermore, the BEOL6 interconnect process remains to be executed on the IC Gen. 12 wafers. For the IC Gen. 12 chipset to bring its promised advances to extreme-temperature capabilities, these chips must first demonstrate stable long-term operation in application-relevant thermal environment. Subsequent technology transfer of a proven-stable JFET-R fabrication process to commercial foundry manufacturing environment is considered paramount to future widespread accessibility and application infusion.

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