Ionizing Radiation Effects on Hole Collection Backside-Illuminated P-Type Deep-Trench Pinned Photo-MOS Pixels under Image Acquisition

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***Abstract*—Dark current degradation, origins, and annealing behavior after x-ray irradiation are studied in a P-type, hole collecting, backside-illuminated image sensor currently being developed at STMicroelectronics and based on deep-trenched photo-MOS pixels. Different biasing conditions during irradiation, i.e. grounded or biased and sequenced, are compared. The dark current increase with total ionizing dose (TID) and the dark current annealing behavior seem to be driven by the backside interface between the P-epitaxy of the pixels and the ONO stack. Despite still being under development, this pixel architecture already exhibits both very good electro-optical performance and a better radiation hardness than pinned photodiode-based CMOS Image sensors that benefit from the same advanced CIS processing technologies. At high total dose range, the photogate challenges custom Radiation-Hardened-by-Design photodiodes by exhibiting a comparable radiation tolerance while bringing new features such as high-resolution or Correlated Double Sampling.**

***Index Terms*—CMOS Image Sensor (CIS), Total Ionizing Dose (TID), Metal-Oxide-Semiconductor (MOS), Interface-States, Oxide-Traps, Capacitive Deep Trench Isolation (CDTI), X-rays.**

I. Introduction

RADIATION tolerant high-resolution image sensors are receiving a rising interest in numerous applications involving harsh radiation environments including space [1] [2] [3], nuclear power plants [4] [5], and high energy physics research facilities [6] [7]. For those applications, custom radiation-hardened CMOS Image Sensors (CISs) are often used where customer grade CIS cannot be operated due to the high accumulated dose [8] (i.e. Total Ionizing Dose/Displacement Damage Dose).

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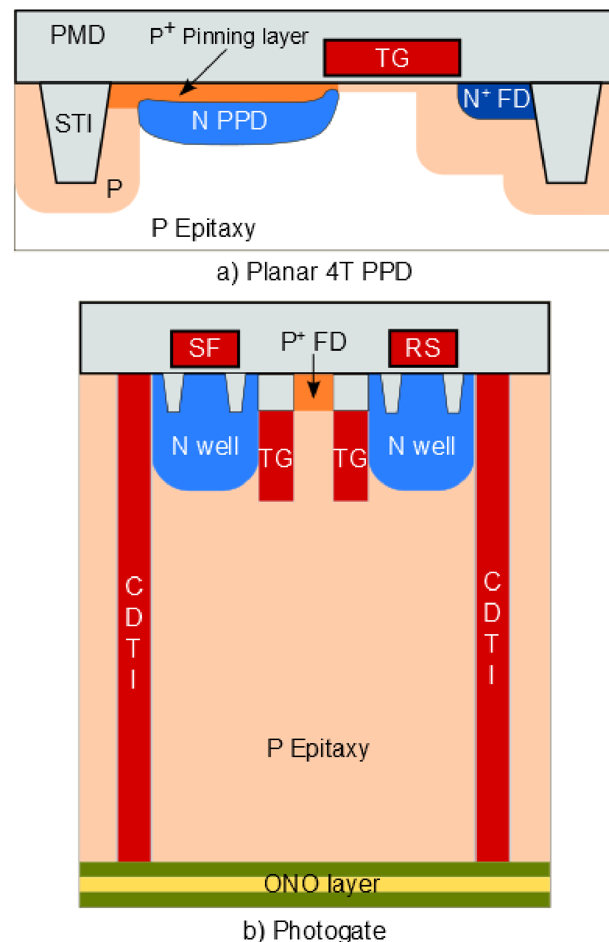

Fig. 1. Cross-section of a) a classical 4T planar Pinned-Photodiode (PPD), and b) the photogate under study.

In this context, the development of a radiation hardened pixel following the state-of-the-art customer grade CIS pitch reduction and electro-optical performance would unlock imaging at higher resolution and would be of interest for a broad panel of applications.

Recently, STMicroelectronics has disclosed a novel p-type trench-pinned photo-MOS device, also referred to as photogate [9]. This photogate has been shown to present very promising electro-optical characteristics both before and after irradiation, challenging state-of-the-art n-type Radiation Hardening By

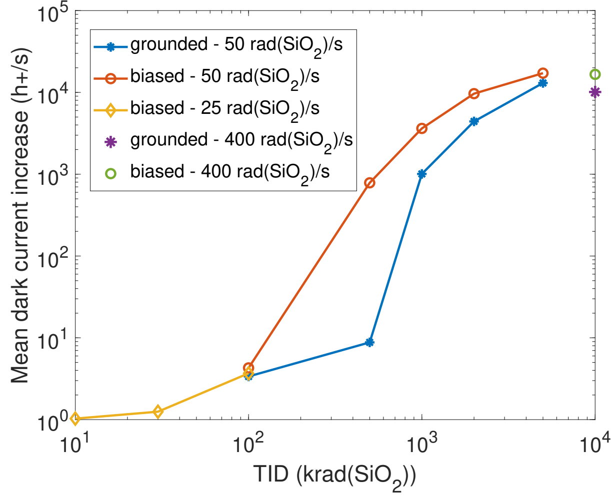

Fig. 2. Evolution of the mean dark current at 22 °C of grounded and biased photogates with TID. Each color line represents a different device. V_{CDTI} = 3.5 V.

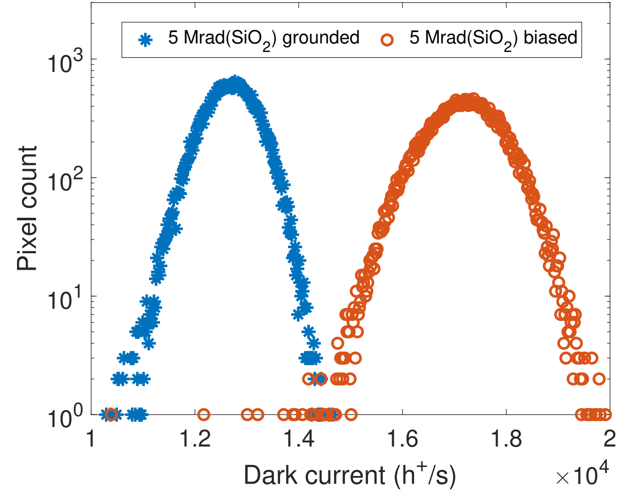

Fig. 3. Histogram of the dark current increase at 22 °C of a grounded and a biased photogate at 5 Mrad(SiO_2). V_{CDTI} = 3.5 V.

Design (RHBD) image sensors [10]. This pixel design benefits from advanced CIS processing technology and moves from planar to three-dimensional pixels, thus reducing the pixel pitch. A cross section of the photogate is shown in Fig. 1 b). A good radiation tolerance was demonstrated after Co60 gamma rays and fusion neutron irradiations [10]. As a preliminary test, that first irradiation campaign was performed with grounded photogates. Results point out a significant reverse annealing effect after irradiation, meaning that the dark current keeps increasing over time after irradiation. Reverse annealing is generally not expected in CIS and that observation was one of the starting points for this study.

This paper further studies the TID-induced dark current contribution in biased photogates, completing the previous study presented in [10] by analyzing the effects of the bias as well as the annealing behavior when performing accelerated ageing. The objective is to have a better understanding of the mechanisms at the origin of the dark current in this technology and responsible for the reverse annealing previously reported.

TABLE I
PHOTOGATE PIXEL PERFORMANCES, FROM [9]

Pixel	P-type, BSI, 2 μm pitch
CVF	90 $\mu V/h^+$
Saturation charge	13,000 h^+
Quantum Efficiency (550nm)	80%
Photo-Response Non-Uniformity	0.5%
Dark current at 60 °C	5.3 h^+/s
Lag	$< 1\,h^+$
Temporal noise floor	2 h^+
Dynamic range	75

II. Experimental Details

A. Device Description

As described in [9] [10], the photogate is a p-type Backside-Illuminated (BSI) pixel fabricated in the STMicroelectronics 90 nm image sensor technology node, implementing dedicated process steps optimized for the p-type pixel and with a 2 µm pitch [9]. Its performances were detailed in [9] and are summarized here in Table. I. As shown in Fig. 1 b illustrating the cross-section of the photogate, the photogate is built from a p-type epitaxial silicon layer of 3.5 µm. It collects and stores photo-generated holes. This pixel is based on a trench-pinned photo-MOS with Capacitive Deep Trench Isolation (CDTI) sidewalls. CDTI sidewalls are made of polysilicon trenches surrounded by oxide liners.

Applying a positive bias to the CDTI allows creating an inversion layer of electrons filling the interface states along the sidewalls. The intent is to limit the dark charges generation. To achieve the same objective, the backside Si/SiO_2 interface is passivated by integrating a positively-charged Oxide-Nitride-Oxide (ONO) layer as reported in [11]. The positive charges trapped in the ONO stack induce a charge inversion layer along the backside surface, joining the one previously described on the CDTI sidewalls. Moreover, this ONO layer also acts as an anti-reflective coating optimized for visible light transmission. In the photogate, the passivation of the oxides interface states is achieved by electrostatic means to maintain surface inversion. Instead of using pinning implants of opposite type kept in accumulation as found in classical planar PPD (Fig. 1 a)), the photogate uses active bias for CDTI sidewalls and a positively charged ONO stack.

For charge transfer, the photogate includes a vertical Transfer Gate (TG) between the photo-MOS and the Floating Diffusion (FD). The reset and the readout are performed by separate p-type transistors named Reset (RS) and Source Follower (SF) respectively. This architecture also allows to perform Correlated Double Sampling (CDS) to remove kTC noise and reduce Fixed-Patern Noise (FPN) [12].

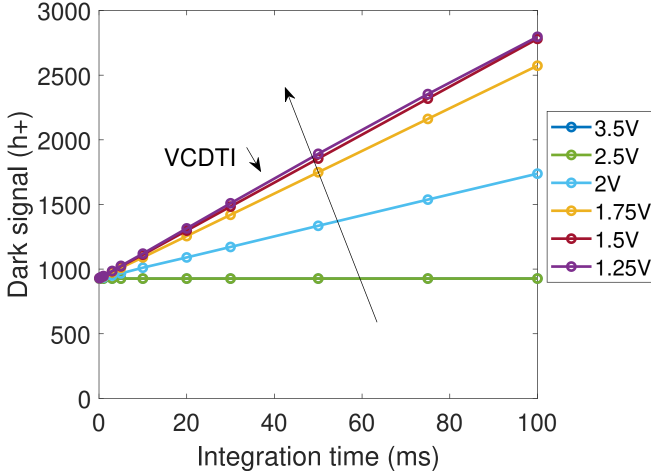

Fig. 4. Evolution of the signal in a photogate before irradiation as a function of the integration time for different CDTI bias voltage (V_{CDTI}). Y-axis values have an electrical offset of 85 mV corresponding to 944 holes.

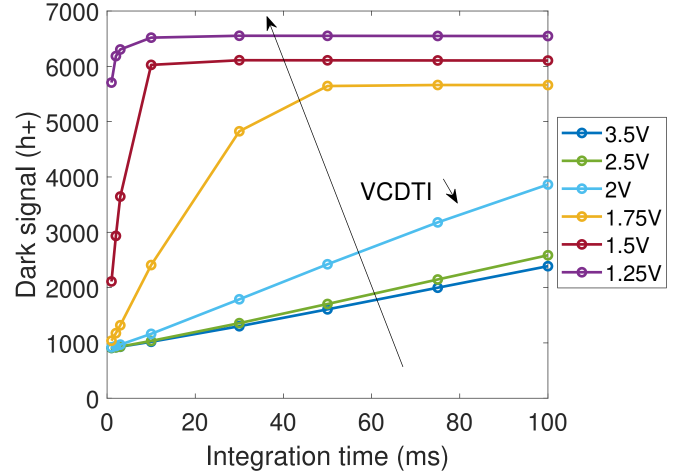

Fig. 5. Evolution of the signal in a photogate at 10 Mrad(SiO_2) as a function of the integration time for different CDTI bias voltage (V_{CDTI}). Y-axis values have an electrical offset of 85 mV corresponding to 944 holes.

B. Irradiation and measurement parameters

The photogates were irradiated at room temperature (20±3 °C) using a tungsten X-ray tube. The dosimetry is assured by a calibrated ionizing chamber dosimeter. The homogeneity of the dose within the sensitive area of the devices under test is expected to be greater than 95 %. Both biased and grounded photogates have been used for comparison. During irradiation, biased photogates were also sequenced consistent with standard operation using a connection cord of 2 m from the proximity board toward the irradiation chamber allowing the remote operation of the CIS. The TID ranges from 10 krad(SiO_2) to 10 Mrad(SiO_2). Three dose rates of 25, 50 and 400 rad(SiO_2)/s were used.

After irradiation, all measurements are performed at 22 °C (chip temperature measured with a thermocouple) in a temperature controlled chamber comprising both the proximity board and the CIS. For dark current measurements, the connection extension cord is not used in order to assure optimal CIS operation. Measurements are made after one hour of unbiased annealing at room temperature (20±3 °C). To further study the reverse annealing, two sets of photogates were placed grounded in an oven at 100 °C for 1 week (168 hours), as per a typical space-grade ageing. Their dark current has been measured after an additional 12 hours of unbiased cooling at 22 °C.

III. Results

The focus will be set on the dark-current since it is the parameter whose degradation will impact this sensor's performances the most according to [10]. It should be mentioned at this point that even at the highest dose explored (10 Mrad(SiO_2)), other parameters (lag, charge to voltage conversion gain) did not show significant variation and that all the tested sensors were still sensitive to light and able to acquire images.

A. Dark current evolution with TID

Fig. 2 shows the increase of the mean dark current of a grounded photogate (grounded) and a biased photogate (biased) with TID. The dark current of the biased photogate is systematically higher than the one achieved in the grounded photogate. The highest difference is reached at 500 krad(SiO_2) with 8.8 h^+/s for the grounded photogate and 785 h^+/s for the biased photogate. Whereas it is known that biasing conditions are key for studying transistor degradation, it is very uncommon to observe such a wide discrepancy for a pixel level parameter. For higher TID, at 5 Mrad(SiO_2), the difference between the grounded and the biased sensor shrinks down to a factor of 1.3, as visible in Fig. 3. Post-radiation device-to-device variability wasn't explored and could partially explain the difference at 500 krad(SiO_2). However, all the devices came from the same wafer and exhibited low variability before irradiation (<5%). For the two samples irradiated at 400 rad(SiO_2)/s in one time up to 10 Mrad(SiO_2), the dark current increase is roughly equal to the one observed on the samples that were irradiated by successive steps up to 5 Mrad(SiO_2) at 50 rad(SiO_2)/s. It isn't possible to conclude on any dose rate effects since the annealing history of the two different sets of sensors are drastically different.

These results show that biasing the sensor during irradiation accelerates the degradation of the photogates at the earliest stage of the irradiation but that at high dose (TID>5 Mrad(SiO_2)), one can expect that the biasing condition can be considered as a simple offset. In other words, the dose threshold at which the dark current increases significantly will be reached sooner for a biased photogate.

An additional sample was irradiated while being biased at a lower dose rate of 25 rad(SiO_2)/s up to 100 krad(SiO_2) in order to assess the dark current increase in the dose range of typical space applications. For all the samples tested, the dark current increase at 100 krad(SiO_2) did not exceed 5 h^+/s before annealing.

Finally, it can also be noted that the degradation of dark current obtained at 5 Mrad(SiO_2) in Fig. 3 is uniform due

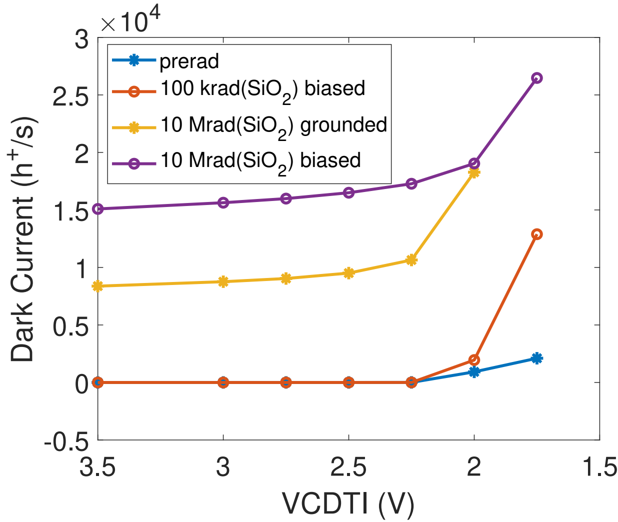

Fig. 6. Evolution of the dark current in the photogate as a function of the CDTI bias voltage (V_{CDTI}). The dark current increases abruptly when the CDTI sidewalls lose their passivation.

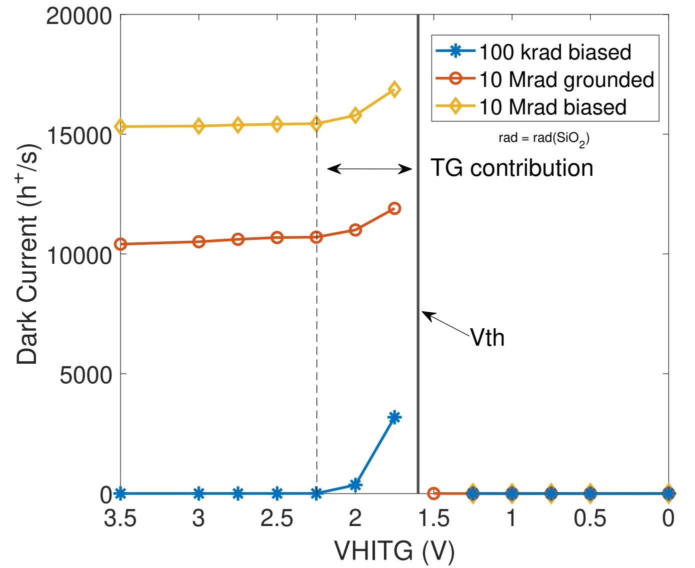

Fig. 7. Evolution of the dark current in the photogate as a function of the Transfer-Gate bias voltage during signal integration (V_{HITG}). V_{CDTI} = 3.5 V.

to the distributions' Gaussian shape. It can also be seen from the dark current distributions that there is no obvious Electric-Field-Enhancement (EFE) at play because EFE would distort an uniform, TID induced Gaussian distribution toward high dark current values [13] [14]. The absence of obvious EFE is important because the electric field created by the CDTIs could have been responsible for EFE. On the other hand, the absence of highly doped implant in or near the charge collection and storage volume is a good thing to limit the electric field and potential EFE effects.

B. CDTI bias effects

Fig. 4 and Fig. 5 show an example of the evolution of the signal in the photogate before irradiation and after 10 Mrad(SiO_2) as a function of the integration time for different values of V_{CDTI}, the bias voltage of the CDTI.

Several effects can be observed. First, as V_{CDTI} decreases, the surface inversion of the CDTI sidewalls is lost, thus explaining the slope increase as the charges generated by the defects of the Si/SiO_2 interface start to be collected. In Fig. 5 the saturation level, in other words the maximum amount of charge that can be stored in the photogate, is higher for low values of V_{CDTI}. This can be explained because the charge storage volume is less constrained at lower values of V_{CDTI}.

Fig. 6 illustrates the evolution of the dark current in the photogate (the slope in the linear part of the curves in Fig. 5) as a function of V_{CDTI}. The inversion threshold can be identified around 2.25 V before irradiation and shows minimal shift up to 10 Mrad(SiO_2), independent of the biasing condition.

These results demonstrate a very high radiation hardness of the technique used here to mitigate the dark current contribution of the lateral interfaces of this pixel.

C. Transfer-Gate bias effects

Following the same approach as for the CDTIs, the dark-current of the photogate is extracted as a function of the Transfer-Gate voltage during integration of the signal, V_{HITG}. The results are reported in Fig. 7, where three regimes can be identified. Between 3.5 V and 2.25 V, the TG is properly inverted and the dark current is almost constant with V_{HITG}. Between 2.25 V and 1.6 V, the strong inversion of the TG is lost and the contribution of the TG oxide rises with decreasing V_{HITG}. Beyond the threshold voltage of the TG, around 1.6 V, the charge collection volume meets the sense node and since the sense node is continuously reset during integration, all the collected charges are flushed, leading to zero dark-current. Up to 10 Mrad(SiO_2), no obvious shift of the threshold voltage of the Transfer-Gate is observed, independent of the biasing conditions.

D. Annealing

The second objective of this test campaign is to further study the reverse annealing effect observed in [10] that has been previously attributed to the Si/SO_2 interfaces between the P epitaxy and the bottom SiO_2 layer of the ONO stack (Fig. 1.b)).

Fig. 8 reports the dark current histogram obtained for irradiated photogates with TID level close to typical space mission doses of 100 krad(SiO_2). It can be observed that the dark current distributions after irradiation are quite similar for both the biased and grounded photogates but that the reverse annealing effect is much worse on the biased photogate. This result indicates that the mechanisms responsible for the stabilized dark current increase, obtained after annealing, are sensitive to the biasing conditions.

The results obtained for photogates irradiated at 1 Mrad(SiO_2) are shown in Fig. 9. Again, the dark current after irradiation is greater for the biased photogate than for the grounded photogate. However, the annealing behavior is notably different for the two devices and also

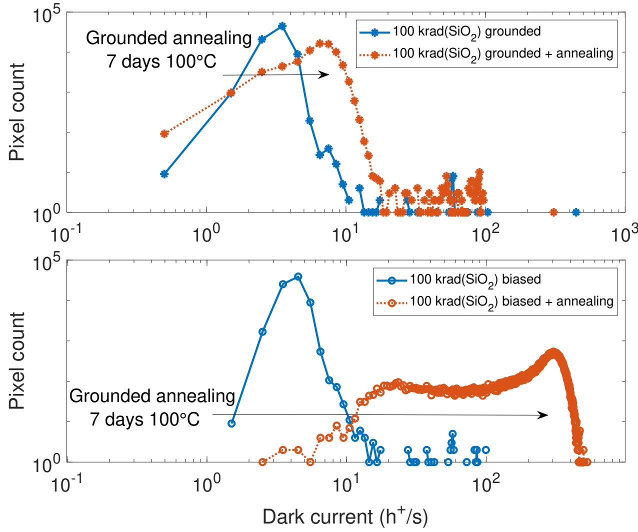

Fig. 8. Histograms of dark current for a grounded and a biased photogate at 100 krad(SiO_2), after irradiation and after annealing at 100 °C for one week. All sensors were grounded during annealing.

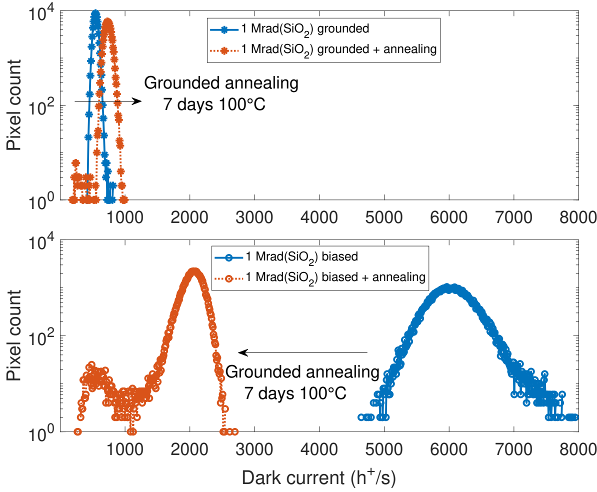

Fig. 9. Histograms of dark current for a grounded and a biased photogate at 1 Mrad(SiO_2), after irradiation and after annealing at 100 °C for one week. All sensors were grounded during annealing.

departs from what has been previously reported in [10]. For the grounded photogate, the annealing induces an increase of the dark current by a factor 1.4 whereas for the biased photogate, the annealing induces a decrease of the dark current by a factor 3.

IV. Discussion

A. Dark-Current Origins

Understanding the origin of the dark current in irradiated photogates is essential in order to improve the device's radiation tolerance that is already promising in the range of dose tested so far. As seen Fig. 10, the photogate dark current degradation is less important than in n-type planar pinned photodiode-based CMOS Image sensors. At high TID, the photogate challenges custom Radiation-Hardened-by-Design photodiodes by exhibiting a comparable degradation but also benefits from advanced CIS processing allowing pixel-pitch reduction and a layout compatible with Correlated Double Sampling [10] [12].

In [10], the Si/SiO_2 interface under the ONO stack has been pointed out as the most likely source of dark current but other sources such as the CDTI sidewalls, the Transfer-Gate oxides could also contribute. Bulk defects in the P-epitaxy can be considered negligible: the dark-current before irradiation is extremely low ($<1\,\mathrm{h^+/s}$), thus showing the quality of the P-epitaxy, and the X-rays used in this study do not induce displacement damage.

The nominal voltage for the CDTI and for the TG during integration is 3.5V. Fig. 6 and Fig. 7 thus shows that the TG and CDTIs sidewalls are far from the inversion threshold at all dose levels that were investigated. At 10 Mrad(SiO_2) it can be seen both for the CDTI and TG that the dark current does increase a little with the decreasing gate voltage when the MOS structure is in inversion. The dark current at an Si/SiO_2 interface is proportional to the Shockley-Read-Hall (SRH) generation-recombination rate U, and to the interface-state density N_{it}:

$$I_{dark} \propto U \times N_{it}. \tag{1}$$

For mid-gap defects and assuming $\sigma_n = \sigma_p = \sigma$, the generation rate in depletion can be expressed as [18]:

$$U_{dep} = \frac{1}{2}\sigma v_{th}\sqrt{N_c N_v} e^{-\frac{E_g}{2kT}}, \tag{2}$$

with σ the capture cross-section for holes and electrons, v_{th} the thermal velocity, N_c and N_v the effective densities of states in the conduction and valence bands respectively, E_g the silicon bandgap, k the Boltzman constant, and T the temperature. Assuming that in inversion $n >> n_i$ and $p = 0$, the generation rate in inversion can be expressed as [18]:

$$U_{inv} = \frac{1}{n_{inv}}\sigma v_{th} N_c N_v e^{-\frac{E_g}{kT}}, \tag{3}$$

with n_{inv} the concentration of electrons in the inversion channel. The ratio between U_{dep} and U_{inv} then gives:

$$\frac{U_{dep}}{U_{inv}} = \frac{n_{inv}}{2\sqrt{N_c N_v}} e^{\frac{E_g}{2kT}} = \frac{n_{inv}}{2n_i} >> 1, \tag{4}$$

So although inverted interfaces can still generate charges, the resulting dark current is expected to be orders of magnitude lower than the dark current coming from a depleted interface. The CDTI sidewalls and TG oxides thus shouldn't be the main contributors to the high dark current increase observed here after a few hundreds of krad(SiO_2).

The fact that the biasing conditions of the device minimally impacts the functioning of both the CDTI and the TG (no significant threshold shift) points out that the state of the backside interface after irradiation is then most likely driving the dark-current increase in the device. An optimisation of the thickness of the different layers of the ONO stack is currently ongoing but the use of transparent thin film electrodes [19]

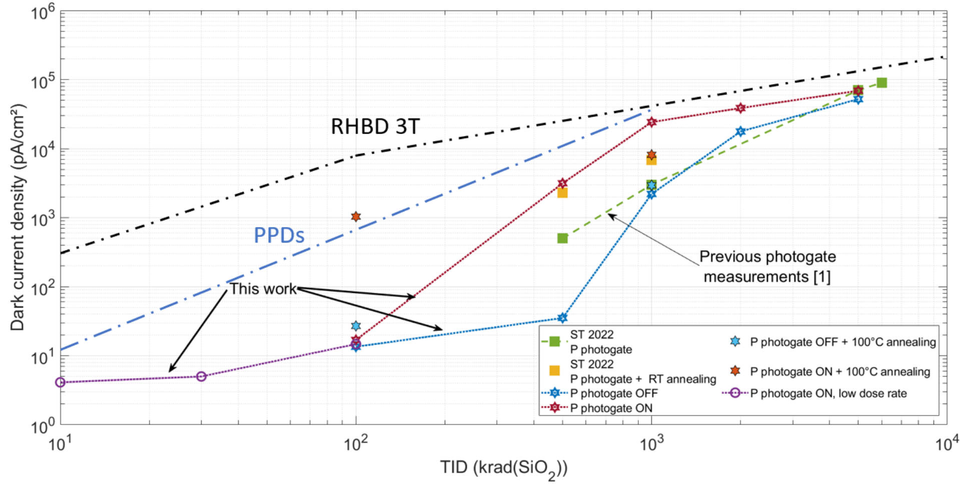

Fig. 10. TID-induced dark current benchmark of the p-photogate pixel with n-type planar Pinned-PhotoDiodes (PPDs) and Radiation Hardened By Design 3-transistor pixels (RHBD 3T) from the literature. The envelopes for the PPDs and RHBD 3Ts were plotted based on values extracted from [4], [5], [15]–[17]. Adapted from [10].

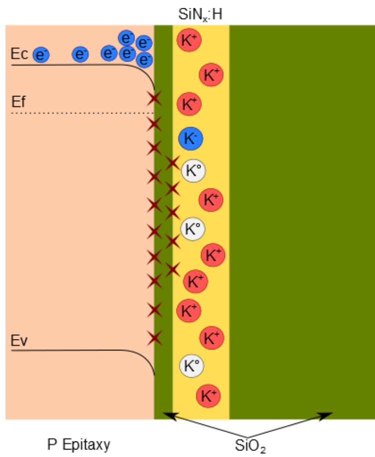

Fig. 11. Detailed view of the ONO stack. The "K" rounds represent the K centers inside the SiN_x:H layer that can either be neutral, positively charged or negatively charged. The red crosses represent interface defects. Before irradiation, the positively charged SiN_x:H stack induces a field passivation of the Si/SiO_2 interface by creating an electron sheet along this interface.

[20] could also be investigated in order to achieve a bias controlled passivation of the backside interface while maintaining a good Quantum-Efficiency.

B. Annealing behavior

The ONO stack structure is illustrated on Fig. 11. The positive charge of the stack is carried by the SiN_x:H layer, thanks to K centers (silicon dangling bonds back-bonded to three nitrogen atoms) that can either be neutral, positively charged or negatively charged [21]. It can be seen in [11], [21] that the charge state of a SiN_x:H layer does not vary over time at room temperature, but that very high temperature annealing (400 °C) could reduce the charge concentration. It is also pointed out that both positively and negatively charged K centers lose their charge in a few minutes under UV exposition. One can thus expect that the charge state of the ONO stack of the photogates will change during X-ray or gamma irradiation.

Results obtained in [10] and in this work reveal the complex interactions between the interface-states concentration, N_{IT}, at the Si/SiO_2 interface on one hand, and the total charge, Q_{tot} of the ONO stack on the other hand, both during irradiation and annealing. The evolution of this total charge during irradiation is also uncertain. The SiN_x:H layer charge Q_K is expected to decrease and the concentration of interface-states, which are mostly acceptors and thus negatively charged, to increase, thus decreasing the total charge. On the other hand, both the SiO_2 layers trap positive charges Q_{OT}, leading to an increase of the total charge. Annealing should however lead to a decrease of the charge concentration in both the SiN_x:H and SiO_2 layers and may thus induce a progressive loss of the inversion layer at the Si/SiO_2 interface.

The buildup and annealing of interface-states is very dependent of the bias and temperature conditions, as seen in [22] [23] [24]. It is also reported that the hydrogen concentrations in the Si, SiO_2 and surrounding materials greatly affect the annealing of interface-states and it can be noted that the SiN_x:H layer in between the two SiO_2 layers is rich in hydrogen. Since Ref. [22] and references therein report that post-irradiation bakes of grounded devices lead to more efficient interface-states annealing and since interface-states annealing has already been reported in thick oxides during grounded annealing at 100 °C [25] [26], it is assumed that in the case reported here, the concentration of interface-states N_{IT} will decrease during grounded annealing.

To illustrate the Si/SiO_2 backside interface's surface potential evolution during irradiation and annealing, the backside interface is considered as an ideal NMOS. The effects of the variation of Q_{OT}, Q_K,and N_{IT} on this ideal NMOS I-V characteristic are presented in Fig. 12 and Fig. 13. In an ideal NMOS, N_{IT} are known to decrease the subthreshold slope while trapped and fixed charges are known to induce a lateral shift of the I-V characteristic [27].

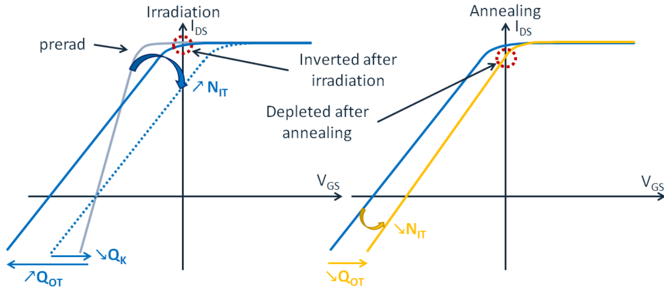

Fig. 12. Illustration of the effects of the evolution of the SiN_x:H charge (Q_K), the radiation induced oxide-trap charges (Q_{OT}) and the concentration of interface-states N_{it} during irradiation and high temperature annealing on ideal I-V curves of the backside interface. Case where the interface is still inverted after irradiation and becomes depleted after annealing.

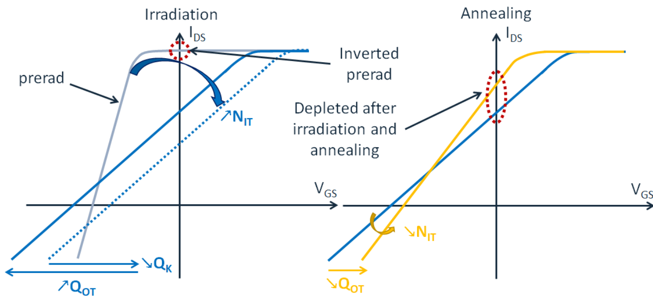

Fig. 13. Illustration of the effects of the evolution of the SiN_x:H charge (Q_K), the radiation induced oxide-trap charges (Q_{OT}) and the concentration of interface-states N_{it} during irradiation and high temperature annealing on ideal I-V curves of the backside interface. Case where the interface is already depleted after irradiation and remains as is after annealing.

Fig. 12 illustrates the case were the backside interface is still inverted after irradiation but becomes depleted after annealing. During irradiation, the reduction of Q_K will shift the I-V curve to the right, the increase of Q_{OT} will induce a shift to the left and the increase of N_{IT} will flatten the subthreshold slope. As the dark current is barely increasing up to a few hundreds of krad, and according to Eq.(1) the small dark current increase 1 h after irradiation is likely coming from the increase of N_{IT} in inverted interfaces (Eq.(3)). The annealing will however reduce Q_{OT} thus shifting the I-V characteristic to the right. The backside interface may end up in depletion after annealing. The resulting abrupt increase of U ($U_{dep} >> U_{inv}$) will then drive the increase of I_{dark} despite the decrease of N_{IT}. This scenario would explain the important rebound of the dark-current observed after annealing of the biased sample at 100 krad(SiO_2) in Fig. 8.

Fig. 13 illustrates the case were the backside interface is already depleted after irradiation. This time, because the interface is depleted both before and after annealing, the decrease of N_{IT} during the grounded annealing directly reflects on I_{dark} according to Eq.(1). This scenario would explain why the dark-current in the biased sample irradiated at 1 Mrad(SiO_2) decrease after annealing in Fig. 9.

In fact, because the values of N_{IT}, Q_{OT} and Q_K are unknown after irradiation and because the kinetics of the evolution of these quantities during grounded annealing is hard to evaluate, it is almost impossible to predict with precision how the annealing will affect the dark current. However, the annealing behavior in Fig. 8 and Fig. 9 allows to identify a few trends.

First, it is clear that biasing the device during irradiation has a strong impact on N_{IT} and Q_{OT}, and possibly on Q_K. Indeed, all samples underwent the same annealing process but the biased and grounded samples had a different response at the two doses tested, thus showing that the starting point before annealing was different for each sample in both cases.

The annealing behavior of the grounded sample at 1 Mrad(SiO_2) is also of interest. Although the high value of I_{dark} after irradiation suggests that some part of the backside interface is depleted, the annealing does not decrease the dark current as depicted in the case of Fig. 13. The dark current of this sample increases after annealing however the relative increase isn't as big as what as been observed for the biased sample at 100 krad(SiO_2) ($\times$1.4 against $\times$ 70 respectively). Since annealing of N_{IT} and Q_{OT} have opposite effects on the resulting dark current degradation a case in between the two cases presented in Fig. 12 and Fig. 13 were the interface is already depleted after irradiation but the dark current still gets worse during annealing is possible. One could expect that after a certain amount of TID induced degradation of this backside interface, the dark current will start to decrease during grounded annealing, independently of the biasing conditions during irradiation.

Finally, grounded annealing of samples irradiated at higher dose should help to corroborate the hypothesis proposed here and biased annealing should also be performed as it may lead to different results and may also be a more realistic way of aging the device.

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VI. Conclusion

X-ray induced TID effects were studied in a novel p-type trench-pinned photo-MOS device under development at STMicroelectronics. The focus was made on the radiation induced dark current increase, the dark current origin after irradiation, and the annealing behavior. The effects of operating the device under nominal biasing and sequencing conditions during irradiation were also studied.

The biasing condition of the device is shown to have an effect on the degradation rate of the device: the dark-current in biased photogates increases faster than in a grounded photogate.

The reverse annealing effect observed in [10] is confirmed but a new annealing behavior is seen while performing high temperature accelerated annealing (7 days at 100 °C). Depending on the absorbed dose level, a large enhancement or

reduction of the dark current is observed after annealing and an hypothesis on the evolution of the state of the backside interface during irradiation and annealing is proposed to explain these annealing behaviors.

These results confirm and clarify the prominent role of the backside interface between the silicon epitaxy and the ONO stack which is identified as driving both the dark current degradation and the annealing behavior.

At this stage of development and despite the sensitivity on irradiation and annealing conditions, this technology still exhibits a higher radiation hardness than more conventional image sensor technologies with equivalent electro-optical performances. At high total dose range, photogates and custom Radiation-Hardened-by-Design 3-transistors photodiodes exhibit a comparable radiation tolerance but the latter do not benefit from customer-grade pixel pitch reduction or Correlated Double Sampling. The novel pixel architecture based on 2 µm pitch, BSI P-type photogates offers promising results up to 10 Mrad(SiO_2) to create high-performance, high-resolution, and radiation-tolerant image sensors.

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