Recent Progress in Extreme Environment Durable SiC JFET-R Integrated Circuit Technology

Philip G. Neudeck[1], David J. Spry[1], Michael J. Krasowski[1], Carl W. Chang[2], José M. Gonzalez[2], Srihari Rajgopal[1], Norman F. Prokop[1], Lawrence C. Greer[1], Dorothy Lukco[2], Shamir Maldonado-Rivera[1], and Christina M. Adams[1]

[1]NASA Glenn Research Center
[2]HX5, LLC
Cleveland, Ohio USA

2023 International Conference and Exhibition on High Temperature Electronics (HiTEC)
Albuquerque, New Mexico USA
April 18-20, 2023

NASA Glenn SiC Electronics and Sensors Website: https://go.nasa.gov/sic
NASA Glenn SiC JFET IC Technology Guide: https://go.nasa.gov/jfetic
NASA Glenn Microsystems Fabrication Lab Website: https://www1.grc.nasa.gov/facilities/microfab/

PS–03876–0223

Acknowledgement

This work was conducted by The NASA John H. Glenn Research Center in Cleveland, OH USA with funding from the NASA Science Mission Directorate under the High Operating Temperature Technology (HOTTech) and Long-Lived In-Situ Solar System Explorer (LLISSE) projects.

Ohio Aerospace Institute
Liangyu Chen

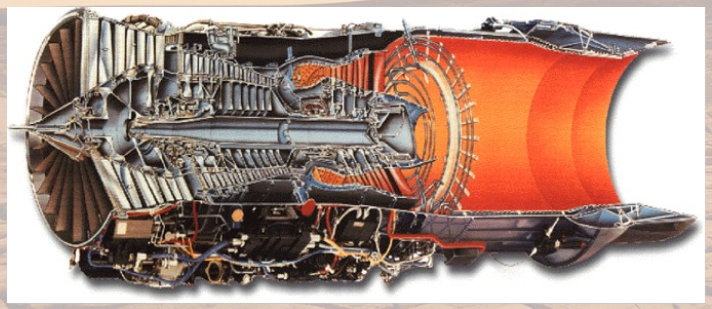
HX5 Sierra (NASA Glenn)
Kelley Moses
Michelle Mrdenovich
Arianna Miller
Wentworth John

Jacobs Technology
Frank Lam
Tiffany Vanderwyst

NASA Glenn Research Center
Gary Hunter
Andrew Trunek
Robert Buttler
Stephanie Booth
Robert Okojie
Diana Centeno-Gomez
Michael Lienhard
Jennifer Xu
Tibor Kremic

High-T Electronics Benefits to NASA Missions

Intelligent Propulsion Systems

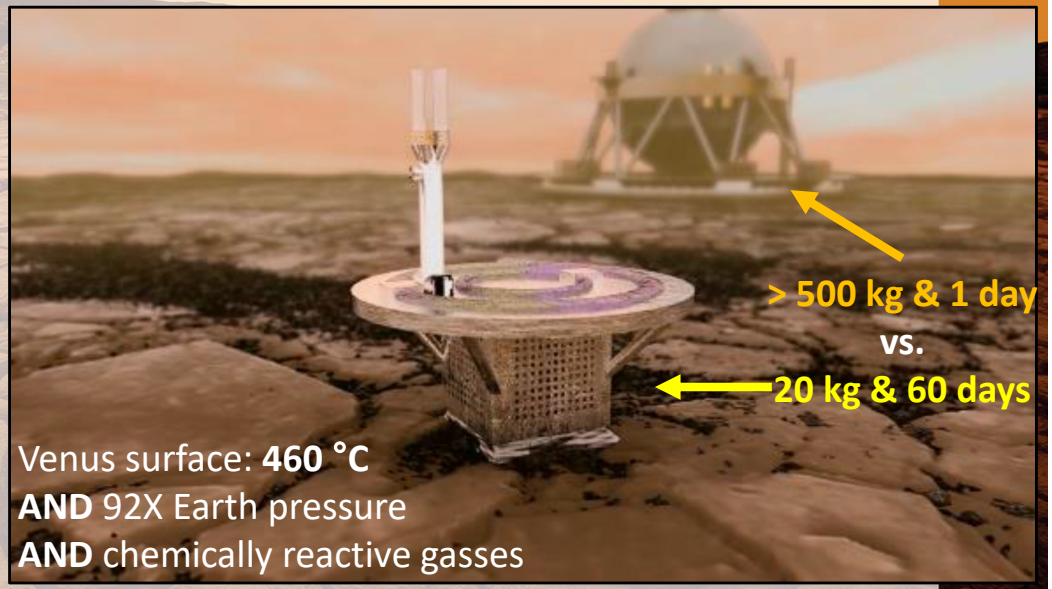


T > 450 °C sensors with electronics in key engine areas for realizing advanced concepts in distributed control and compressor/combustion instability detection and avoidance for improving engine performance

- Thrust to weight ratio
- Fuel efficiency & emissions

Power devices for aerospace electric propulsion and actuation

Venus Exploration Landers[1]



Long duration landers require electronics that endure the Venus surface environment

[1] T. Kremic and G. W. Hunter, Bulletin of the American Astronomical Society, vol. 53, (2021)

Outline

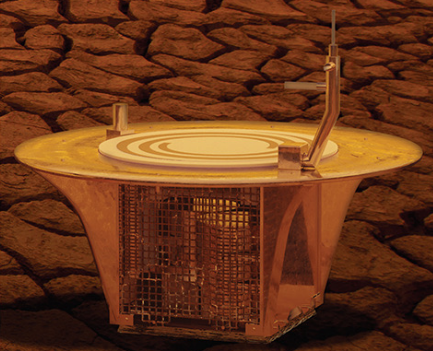
National Aeronautics and Space Administration

“Learn by doing” development of 500 °C Durable SiC JFET-R Integrated Circuits

Unique durability foundation of NASA Glenn SiC JFET-R IC
- Unmatched 500 °C and Venus Durability (IC Gen. 10)
- Interconnect crack failure issue (IC Gen. 11 worse than IC Gen. 10)

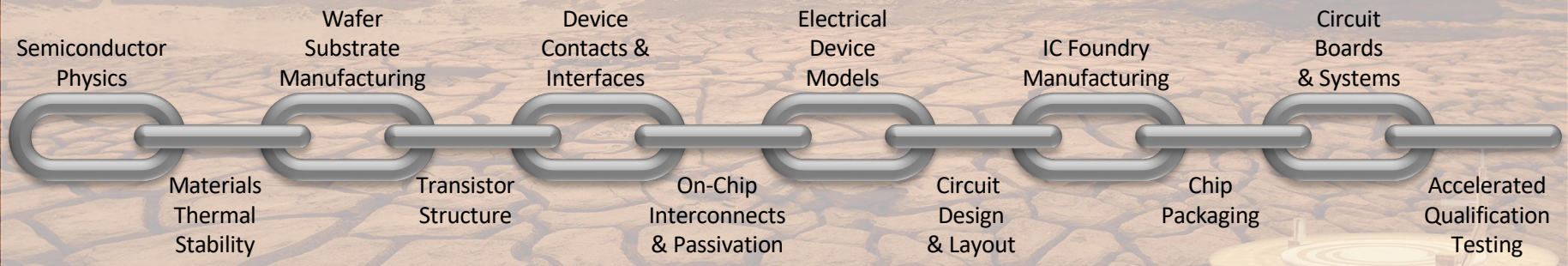
Recent progress made since HiTEC 2021
- BEOL process development towards interconnect crack suppression
- IC Gen. 12 chip and circuit board designs
  - Venus lander electronics (digital and analog)
  - Simple microprocessor supporting robotic seeking operations

Planned next steps
- Oven-test BEOL test chips with packaging & circuit boards
- Finish IC Gen. 12 wafer fabrication based upon BEOL6 process
- Package and test IC Gen. 12 chips and circuit board demonstrations
- Tech transfer towards “ecosystem” of durable ICs manufacturing & infusion



IC Electronics Technology Chain

Chain that is taken for granted at conventional temperatures **is far from trivial to expand to temperature extremes.**

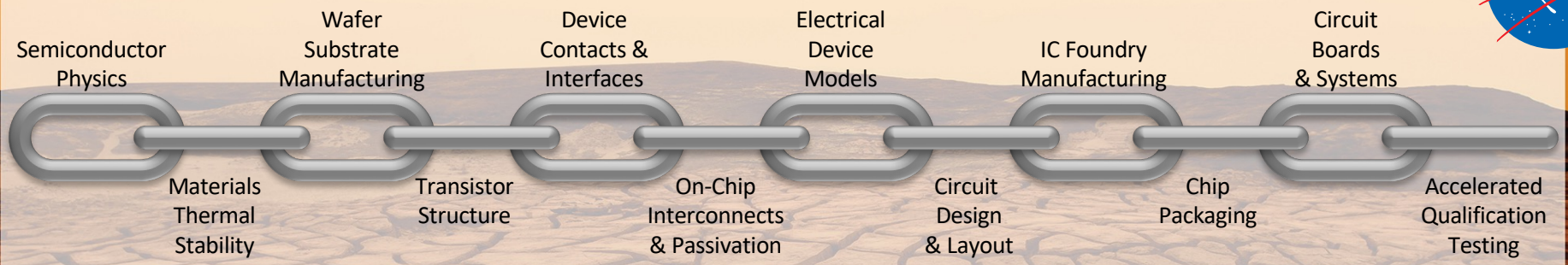


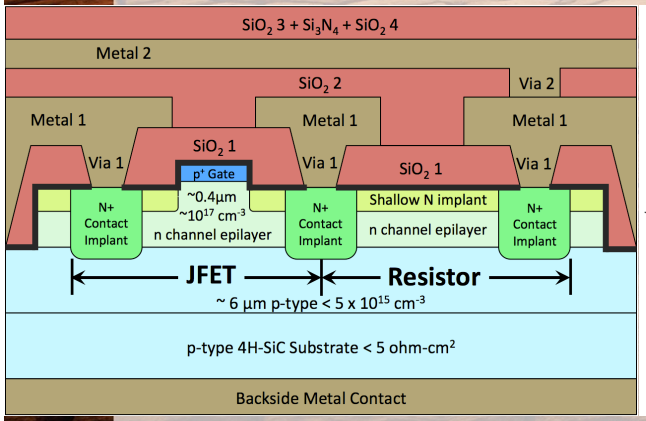
Any single weak link will prevent practical infusion and deployment of electronics.

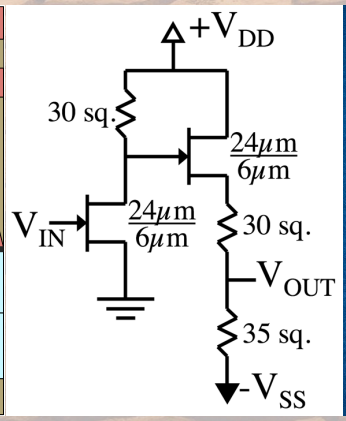
IN THE DESIRED APPLICATION ENVIRONMENT, ALL LINKS MUST

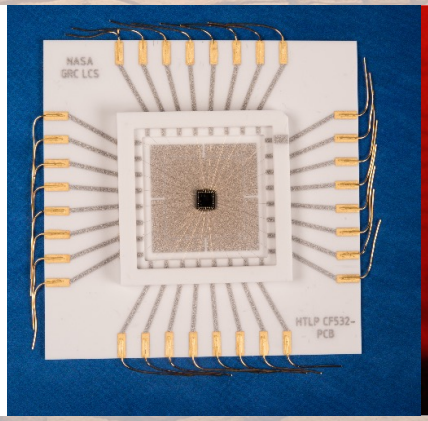
1. FUNCTION INTEGRATED TOGETHER
2. BE PROVEN LONG-TERM DURABLE/STABLE - WITH MARGIN!

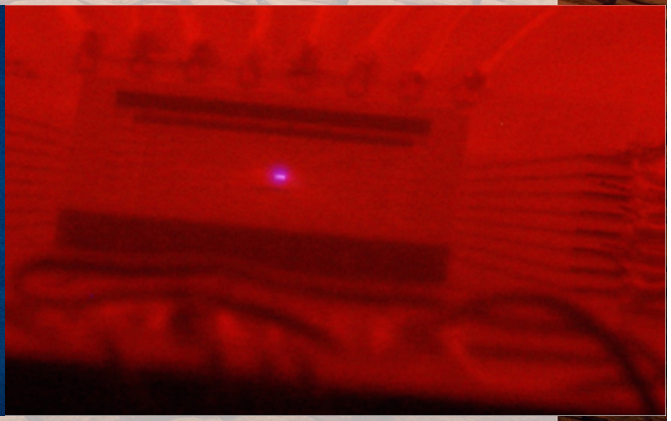
High Temperature Electronics Technology Chain







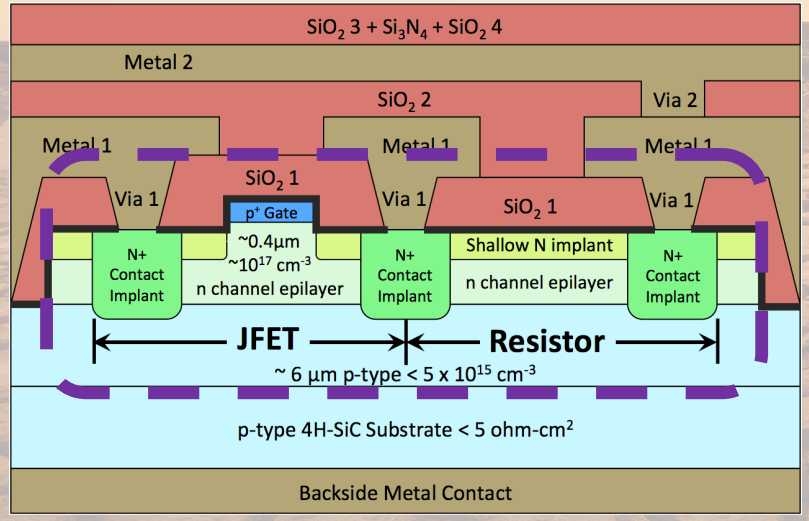




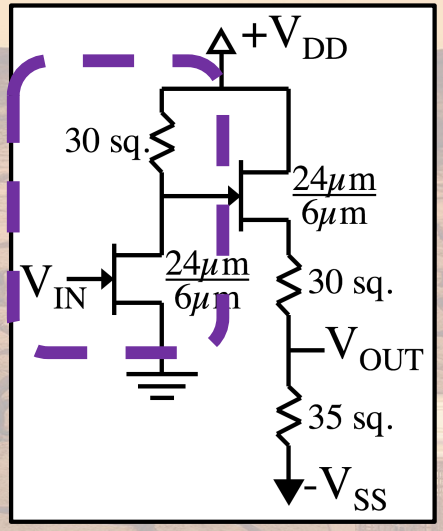
"Learn by Doing" Prototype SiC Design, Fab, Package, & Test Workflow

Basic Device & Circuit Approach[1,2]

JFET and Resistor (JFET-R) Device Cross-Sections



NOT Logic Gate Schematic

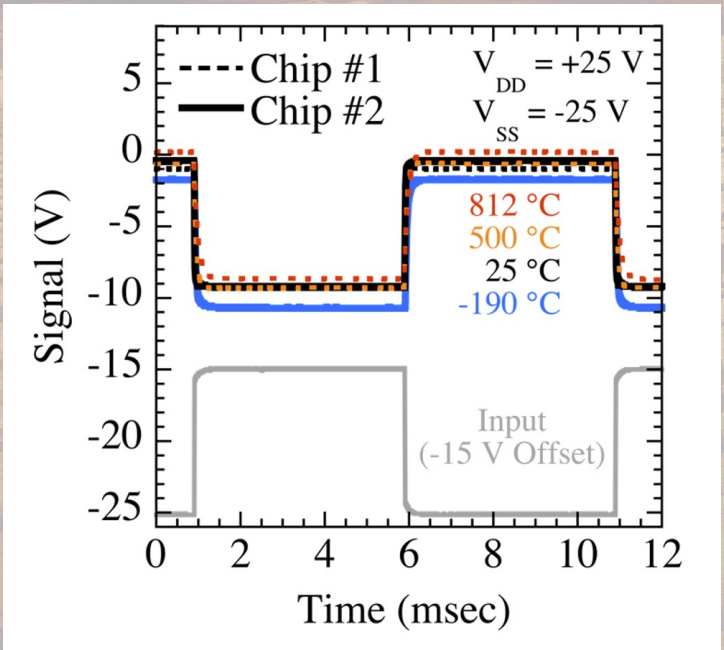


- **Resistors made with same epi as JFET → well-matched T dependence**
- Layout ratio-based circuit design (not absolute component values)
- Negative threshold voltage V_T → negative signal voltages (roughly -1V to -10V logic)
- Typical V_{DD} = +25 V, V_{SS} = -25V Chip backside is biased at V_{SS}

[1]M. J. Krasowski, US Patent 7,688,117 (2010).
[2]P. G. Neudeck, et al., Proc. IMAPS High Temperature Electronics Conf., 2016, pp. 263-271.

-190 °C to +812 °C and Rad Hard "Go Anywhere" Functionality[1,2]

(NASA Glenn IC Generation 10.1 NOT Gate Testing)



- 1000 °C temperature span WITHOUT changing signal/supply input voltages!
- SiC JFET-R ICs function in cold environments WITHOUT "cold start" issues.
- Temperature-accelerated 800 °C lifetime testing for long-duration 500 °C missions.
- Straightforward functional yield screening at 25 °C (on-wafer probe test).
- Radiation Tested > 7 Mrad(Si) & LET 86 MeV-cm^2/mg

[1]Neudeck, Spry, Krasowski, Prokop, Chen, Materials Science Forum, vol. 963, pp. 813-817 (2019).
[2]Lauenstein et al. IEEE Radiation Effects Data Workshop (2019) https://ntrs.nasa.gov/citations/20190031951

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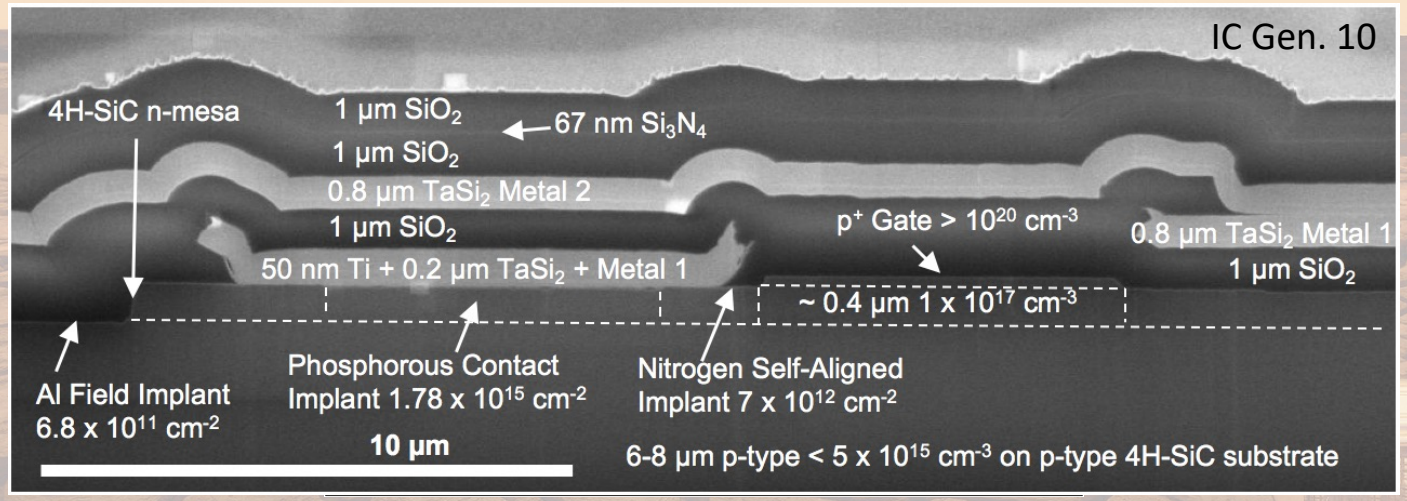
500 °C Stable Two Levels Interconnect[1]

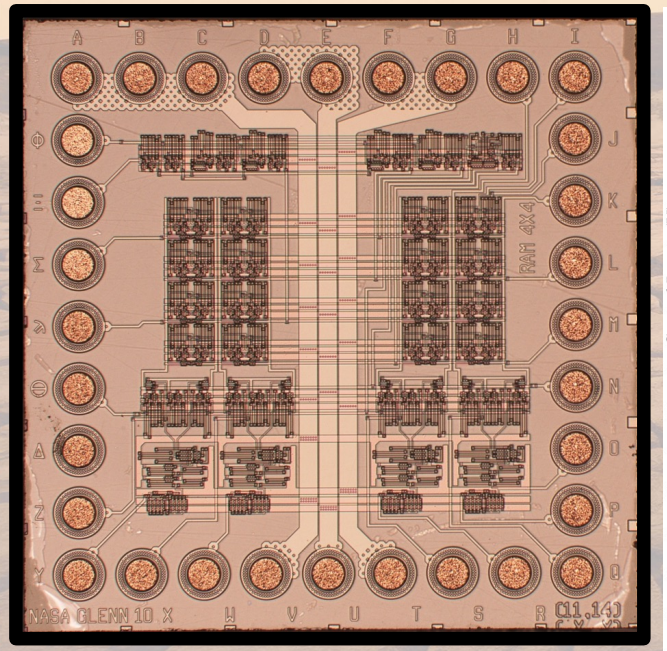


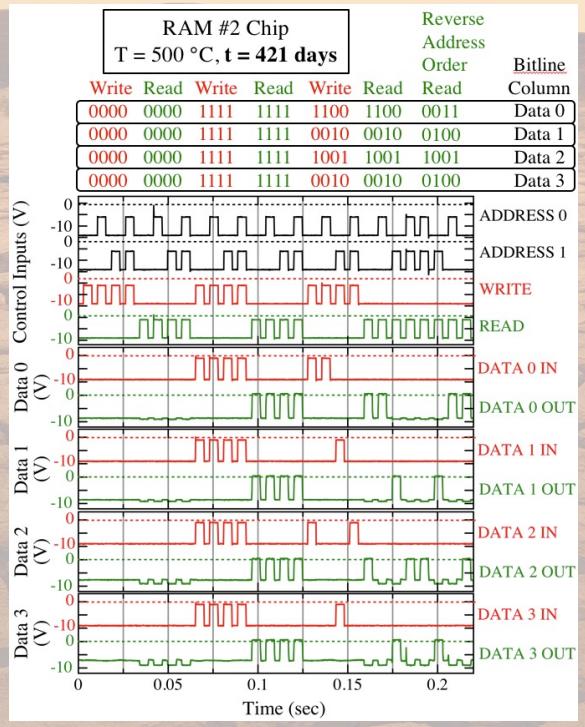
IC processing and materials compatible with SiC power device tools & manufacturing

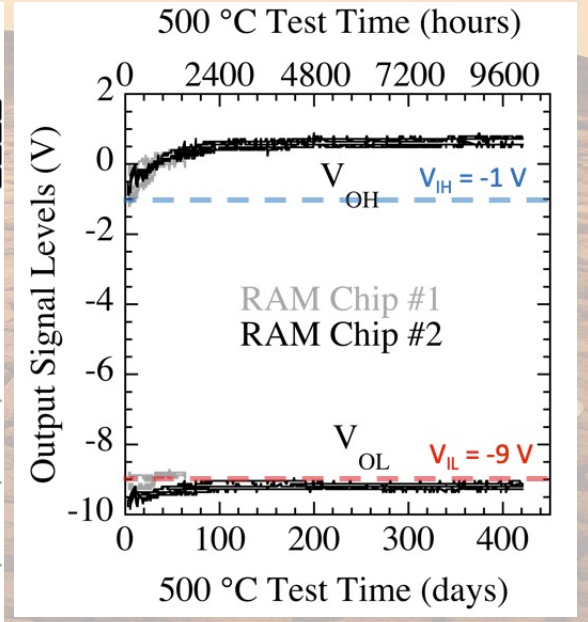
- Close-proximity sputtering of $TaSi_2$ (21mm target to substrate spacing)
- LPCVD tetraethyl orthosilicate (TEOS) and Si_3N_4 layers deposited at 720 °C
- **All interconnect completely buried/passivated beneath dielectric.**

[1]P. G. Neudeck, D. J. Spry, et al., 2018 IMAPS High Temperature Electronics Conf. pp. 71-78

500 °C Durable NASA Glenn Gen. 10 SiC JFET-R RAM Chip[1]







No other transistor IC technology reported near these extreme environment durability results.

[1]P. G. Neudeck, et al., 2018 IMAPS High Temperature Electronics Conf. pp. 71-78

IC Gen. 10 Primary Limitation

Sudden and unpredictable "open-circuit" failures occur due to dielectric crack formation[1,2].

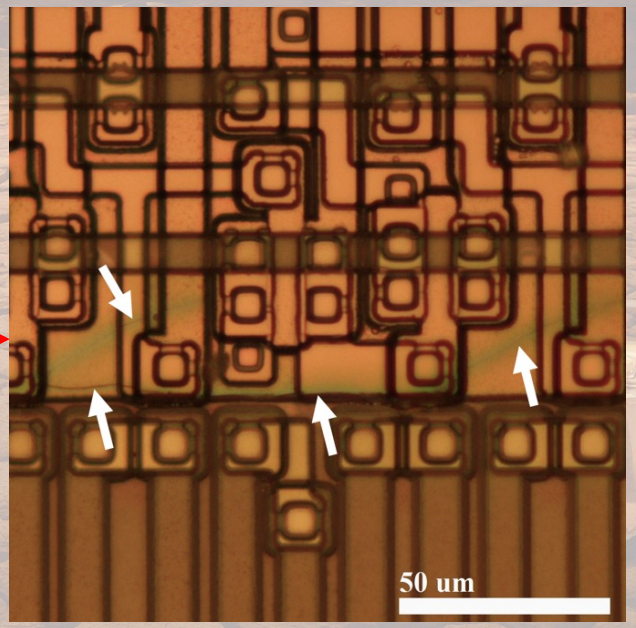
- Unacceptable random failure risk for missions

Table I. 500 °C JFET IC Test Summary

Packaged IC Sample	*r* (mm)	500 °C Time	Test Status
RAM #1	13.4	63 days	Suspended
RAM #2	6.7	420 days	Running
Clock #1	24.2	19 days	Failed
Clock #2	15.3	437 days	Running
Clock #3A	12.4	403 days	Running
Clock #3B	12.4	403 days	Running
Clock #3C	13.4	87 days	Failed

Above table is the total oven-test data set for complicated Gen. 10 ICs.

- Much larger quantities of oven-tests needed to meet standard practices/statistics for aerospace-mission qualification of ICs.



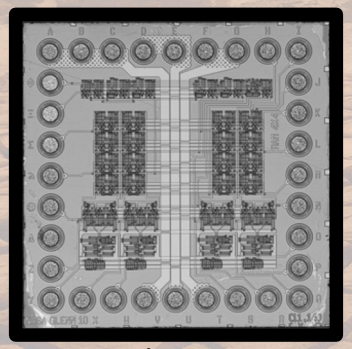
White arrows denote examples of dielectric cracks and metal trace discoloration/oxidation are observed in the oven-failed Clock #1 IC.

[1]D. J. Spry, et al., Proc. IMAPS High Temperature Electronics Conf., 2016, pp. 249-256.
[2]P. G. Neudeck, et al., Proc. IMAPS High Temperature Electronics Conf., 2018, pp. 71-78.

Upscaling from MSI to LSI

"IC Gen. 10" (2017)

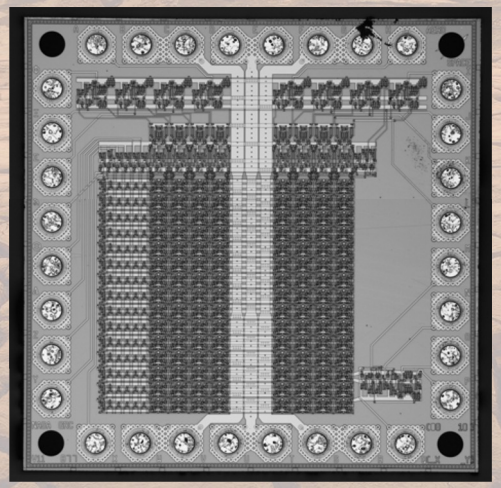
16-bit RAM



12 mW/bit @ 500 °C

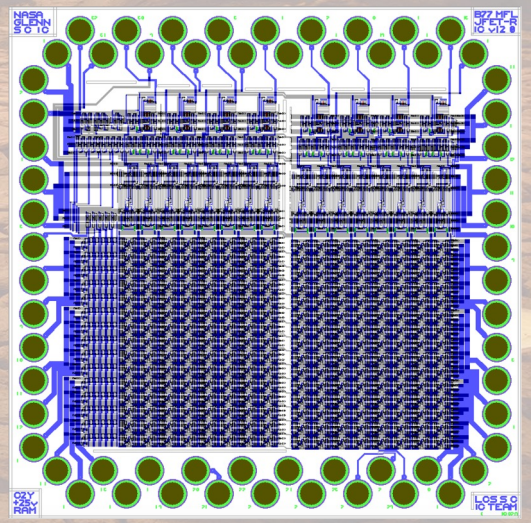
"IC Gen. 11" (2019)

120-bit RAM, ~ 1000 JFETs



"IC Gen. 12" (2023*)

248-bit RAM, ~ 2000 JFETs



	Gen. 10	Gen. 11	Gen. 12
Gate Length	6 µm	6 µm	3 µm
Res. Width	6 µm	3 µm	2 µm
Contact Via	6 µm	6 µm	3 µm
JFETs/Chip	~ 200	~ 1000	~ 2500
Die Width	3 mm	4.65 mm	5 mm
Year	2017	2019	2023*

Higher chip complexity → Higher application functionality.

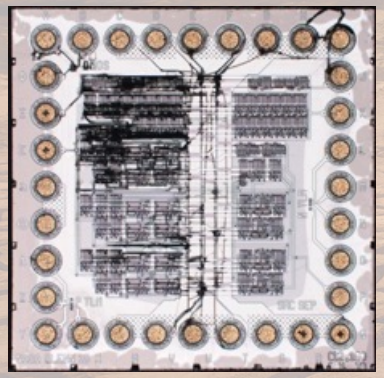
* Delayed by COVID-19 NASA Glenn SiC lab closure.

10-cycle "Accelerated Aging" **720 °C** Anneal Test Results[1]

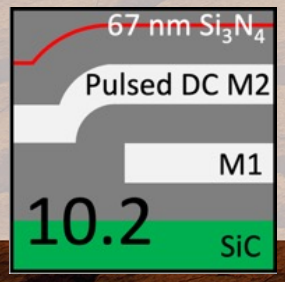
[1]D. Spry et al., Materials Science Forum, vol. 1004, pp. 1148-1155 (2020)

Cracks & Oxidation

500 °C Durable IC

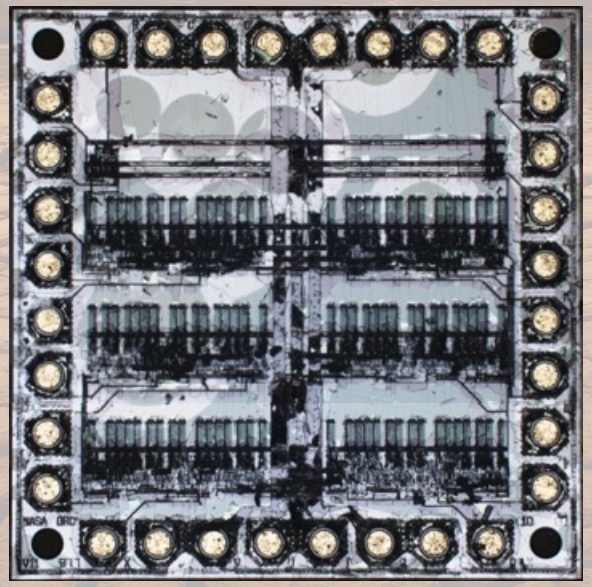


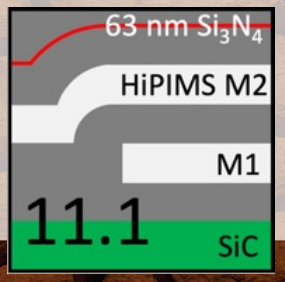
1 mm



Cracks & Oxidation

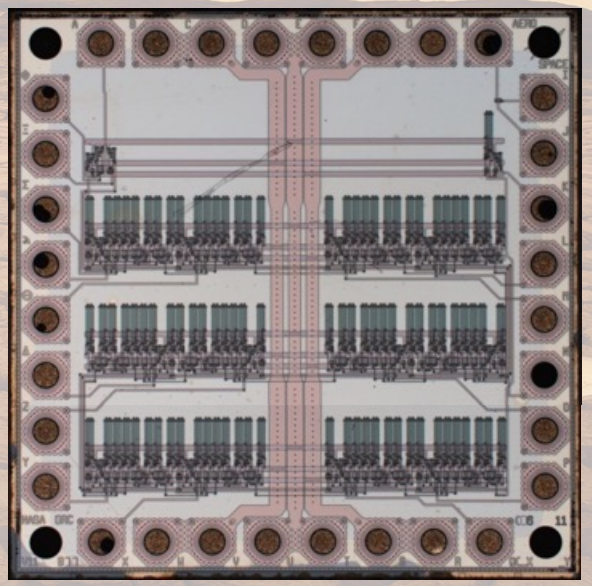
NOT 500 °C durable

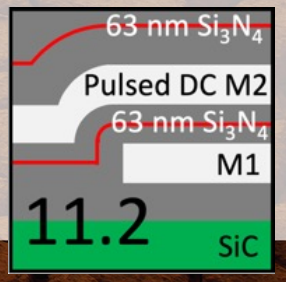




No Cracks, No Oxidation

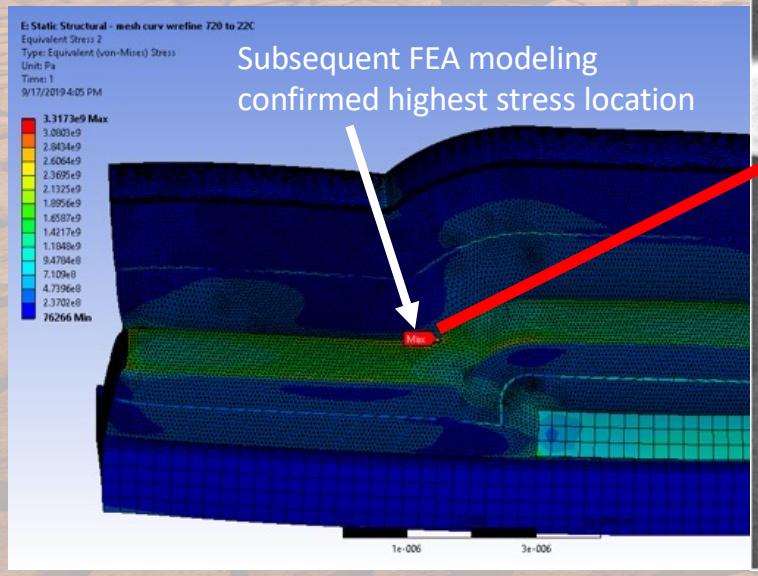
NOT 25 °C Functional

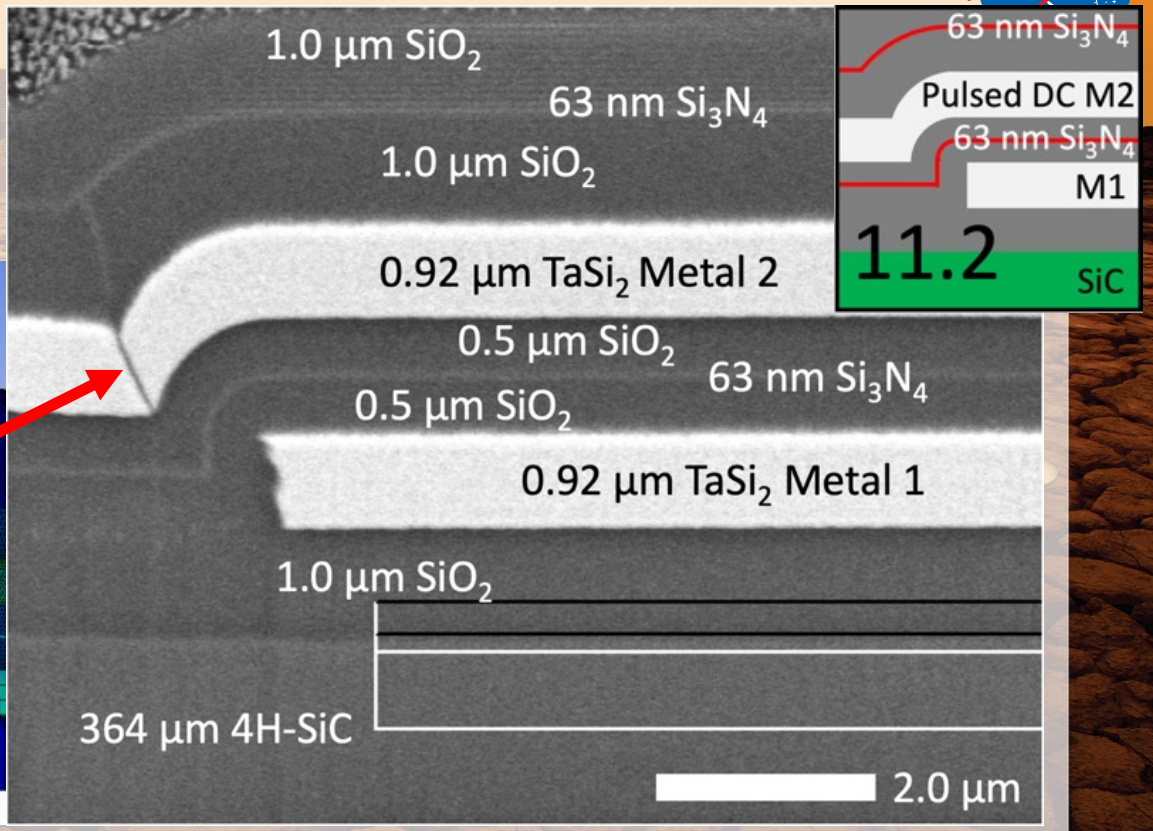




IC Gen. 11.2 – IC-Killing Metal 2 Crack[1]

As seen in the microscopic cross-sections, metal cracks opened in all Metal2 traces running over topology during final Si_3N_4 720 °C deposition, resulting in electrical failure of all the large integrated circuits.





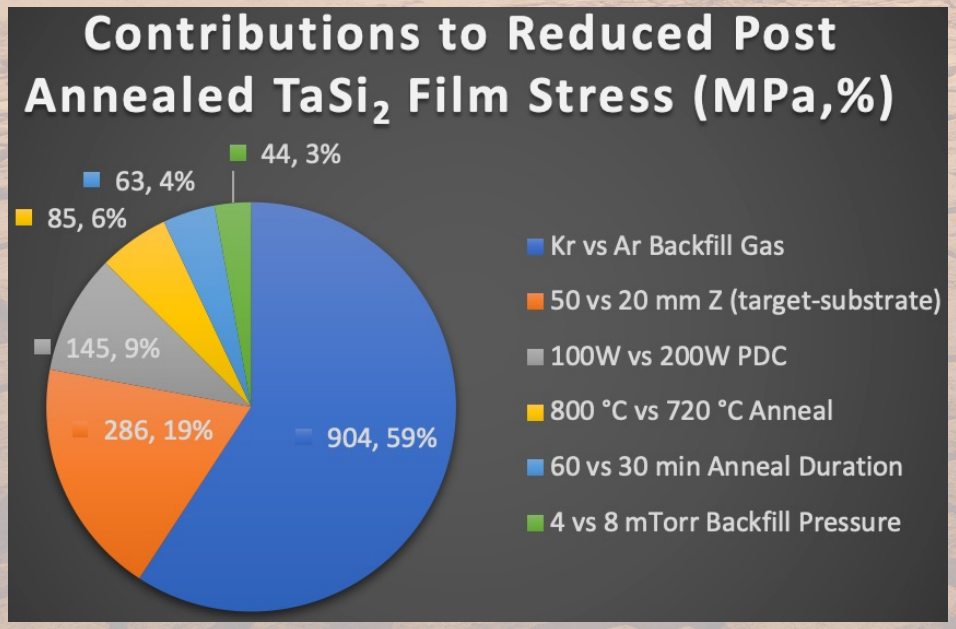
[1] D. Spry, P. Neudeck, C. Chang, Mat. Sci. Forum 1004 pp. 1148-1155 (2020)

Back End Of Line (BEOL) Interconnect Process Experiments

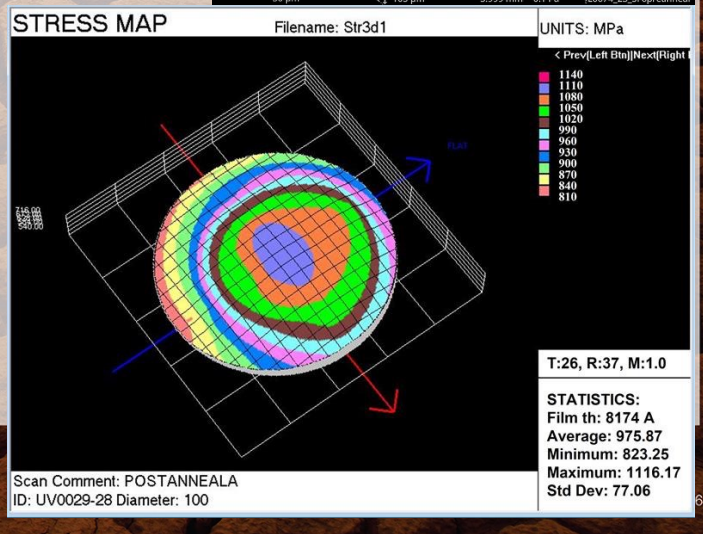
Post-COVID experimental work towards retiring JFET-R IC interconnect cracking issues

Phase 1: Improved $TaSi_2$ metal properties (to avoid metal crack failure)[1]

- ✓ $TaSi_2$ film stress more than halved
- ✓ Eliminated cracks, droplets, other morphological defects
- ✓ Verified functional up to 1000 °C over vertical via etch topography



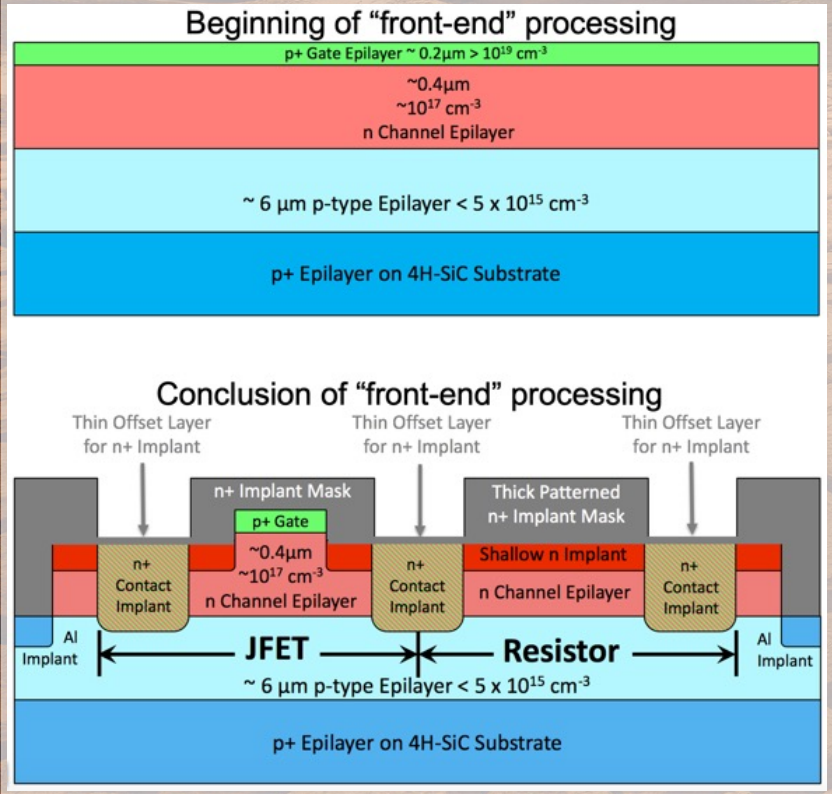
$TaSi_2$ metal test trace snaking through 1µm deep SiO_2 trenches



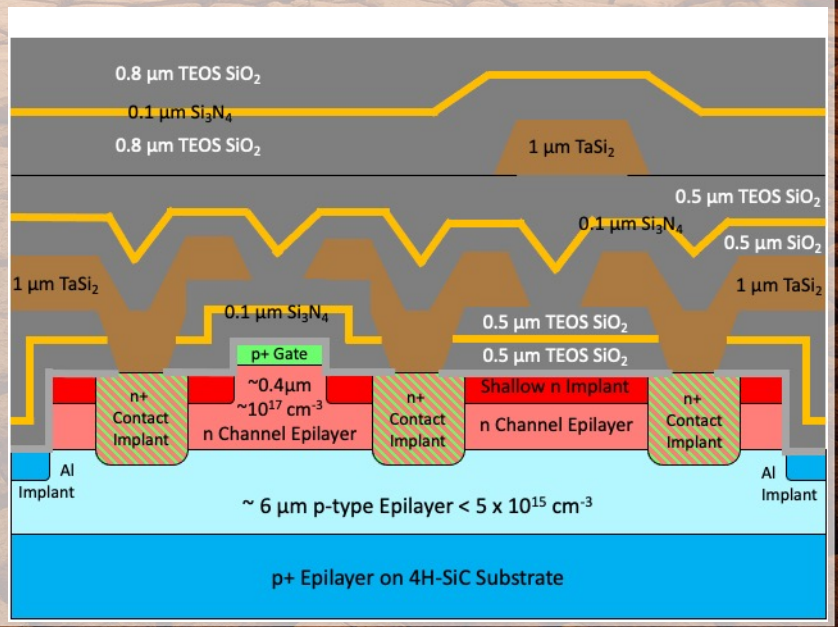
[1]D. Spry et al., to appear in Mat. Sci. Forum, 2023

NASA Glenn SiC JFET-R Fabrication Process

Cross-sectional depiction of
"Front End of Line" (FEOL) process



Cross-sectional depiction following
"Back End of Line" (BEOL) process

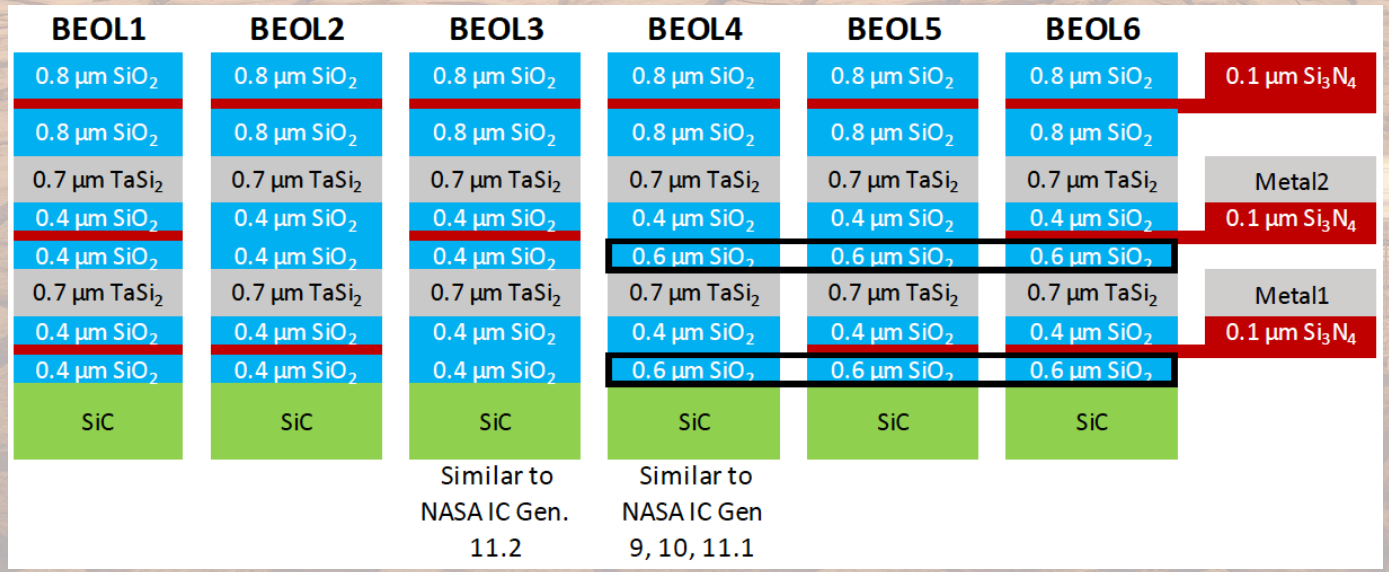


Back End Of Line (BEOL) Interconnect Process Experiments

Post-COVID experimental work towards retiring JFET-R IC interconnect cracking issues

Phase 2: Experimental "test flights" of six different BEOL interconnect stack structures on SiC wafers

- Full interconnect trial fabrication run (from dummy SiC wafers through 500 °C oven-testing)
- Realistic SiC epilayers, mesas, ion implants, bond pads, and mask layouts found on IC Gen. 12
- Ascertain interconnect process of lowest dielectric crack density and highest electrical yield
- Deliver SiC resistor test chips of identical bond pad layout as IC Gen. 12 for verification of packaging, multi-chip boards, and high temperature testing (by NASA and external partners)



Back End Of Line (BEOL) Interconnect Process Experiments

Post-COVID experimental work towards retiring JFET-R IC interconnect cracking issues

Phase 2 Experimental Results: BEOL6 is best process

- Fewest observed cracks, all confined to wafer edge
- Highest electrical probe-test yield

Quarter-wafer region maps showing optically counted number of cracks observed on each 5 mm x 5 mm die

BEOL1

0	1	1	0				
1	0	0	0	1			
0	2	0	0	2	4		
0	0	0	0	0	0	0	
0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

BEOL2

0	0	0	0				
2	2	0	0	0			
2	1	0	0	0	0		
0	0	2	1	0	0	0	
0	1	2	1	1	0	0	0
0	0	0	0	2	0	0	0
10	5	2	3	1	0	3	0
0	7	4	3	2	0	5	0

BEOL3

2	0	0	0				
0	0	0	0	0			
1	1	1	0	0	0		
1	1	1	1	1	0	0	
1	1	1	1	1	0	0	0
0	0	0	1	0	1	0	0
0	1	0	0	1	0	0	0
0	0	0	0	0	0	0	0

BEOL4

0	1	1	0				
0	0	0	0	0			
0	0	0	0	0	0		
0	0	0	2	0	0	0	
4	2	3	6	2	0	0	0
5	3	9	3	0	0	0	2
0	2	0	1	1	3	0	0
1	0	0	2	0	0	0	0

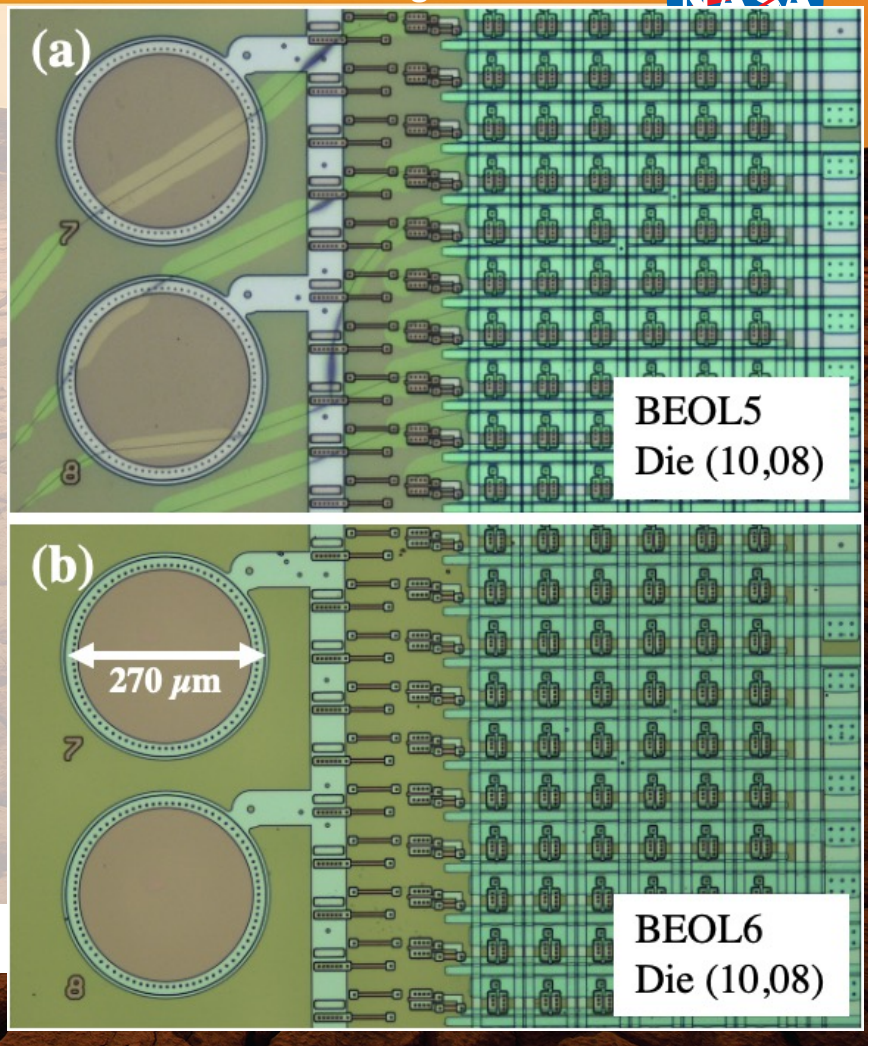
BEOL5

1	0	0	0				
1	0	0	0	0			
0	0	1	0	2	2		
0	0	0	0	0	2	0	
5	5	1	0	4	0	0	0
0	0	0	0	0	0	1	0
0	0	0	0	1	0	2	1
2	0	0	4	1	1	0	1

BEOL6

0	0	0	0				
0	0	0	0	0			
0	0	0	0	0	0		
0	0	0	0	0	1	1	
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Dicing, packaging & oven testing remains to be conducted



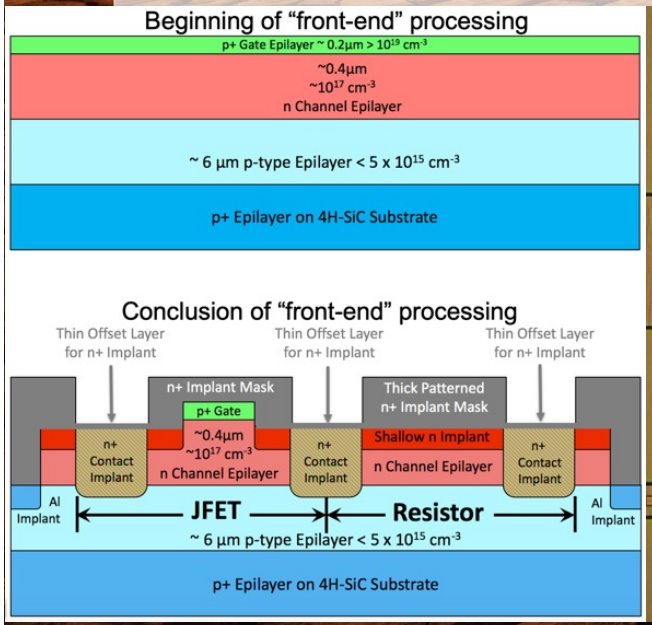
IC Gen. 12 Front End Of Line (FEOL) Processing

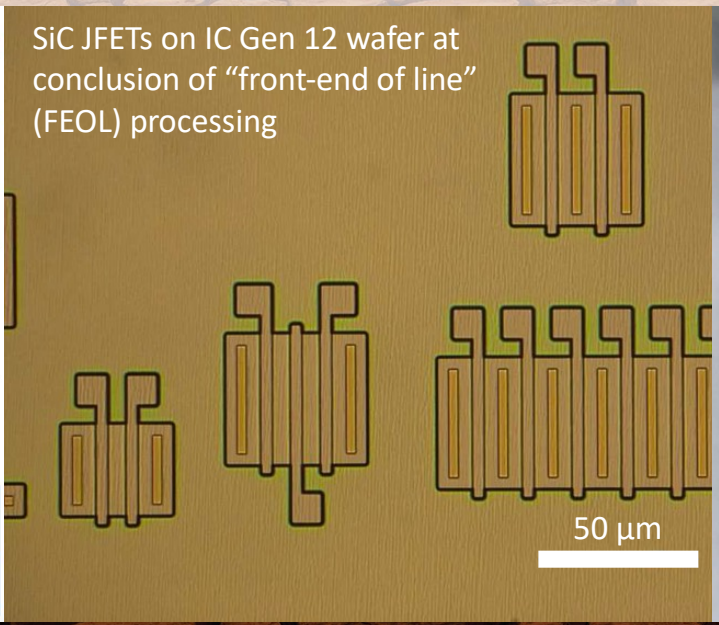
Batch of six 100-mm diameter 4H-SiC wafers

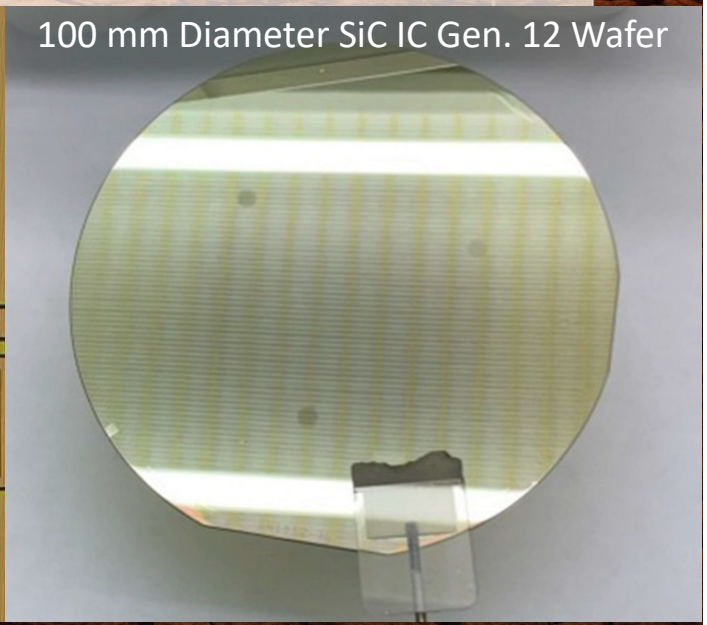
- Wafer size and batch size increases compared to IC Gen. 11 wafer run (batch of four 75-mm diameter wafers).
- Custom 5-epilayer structure with tight control of n-type and p-type layers.
- Starting SiC epi-wafers procured from Cree/Wolfspeed ($55K = $9.23K/wafer).

"Front-end" processing (that forms SiC JFETs and SiC resistors on wafers) successfully outsourced and completed.

- SiC JFET-R front-end process flow already patent-protected, published, and well within basic SiC wafer foundry capabilities.
- Competitive $281K procurement awarded to Alion/General Electric (GE) team Nov. 2019.
- **Front-end processing (with 7 major processing steps and 4 mask levels) finished May 2020 despite COVID-19.**



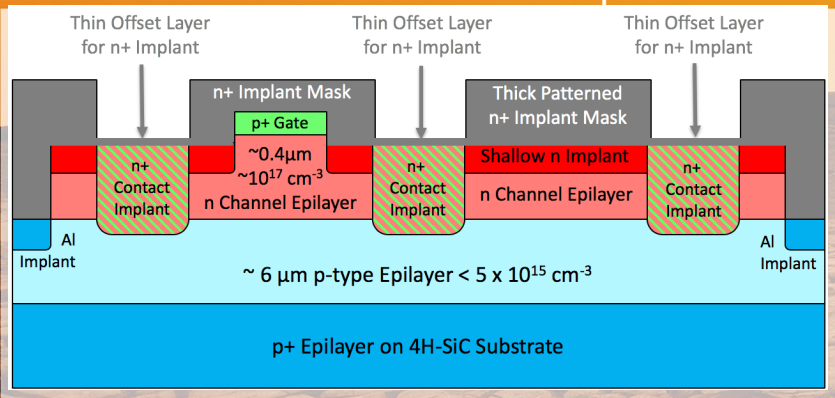




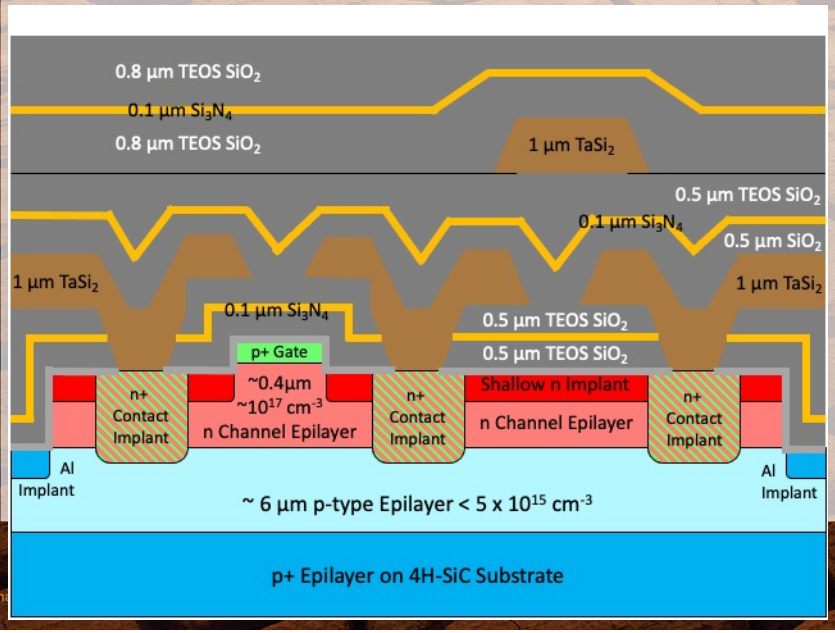
IC Gen. 12 Back End Of Line (BEOL) Processing

Builds the chip interconnects, bond pads, and backside metal

BEOL Start



BEOL End



BEOL Process Improvements for IC Gen. 12

(Critically important learning from the BEOL test run)

1. Dielectric cracks suppressed by insertion of three 0.1 µm stoichiometric Si_3N_4 layers sandwiched between thicker SiO_2 layers.

2. $TaSi_2$ Metal1 and Metal2interconnect film stress halved by changed sputter deposition parameters[1].

3. All dry C_4F_8/Ar Reactive Ion Etch process developed and debugged for higher-yield smaller-dimension IC Gen. 12 via etches.

4. Ti + $TaSi_2$ ohmic contact metal film thickness reduced for better liftoff pattern yield.

BEOL test run has greatly reduced the risk of major IC Gen. 12 interconnect fabrication failure.

[1]D. Spry et al., to appear in Materials Science Forum (2023)

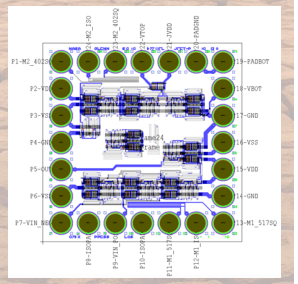
IC Gen. 12 Chipset Overview

50 Application Specific Integrate Circuit (ASIC) chip designs are being fabricated in IC Gen. 12

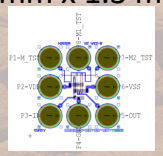
Including:

- Microprocessor dual-chip (assembly language)
- 8-bit analog to digital (serial output), digital to analog
- 2-kbit mask-programmed ROM, 248-bit RAM
- Venus lander control and analog-to-digital conversion
    - 4-channel 6-bit “Tech Demo”
    - 16-channel 8-bit “Exploration Mission”
    - Microseconds to hours clock/timer
- Venus imager array signal processing
- 12 customized analog sensor amps (op-amp based)
    - Wind, pressure, temperature, gas, & battery
- Power JFET chips for paralleling in power module
- External customer Space Act Agreement chips
    - Makel Engineering (NASA/MEI designed chip)
    - Ozark IC (Ozark IC designed chip)
    - Draper Labs (Draper designed half-chip)
- Miscellaneous logic (gates, flip flops, multiplexors, tri-states), analog (op-amp), and process test chips

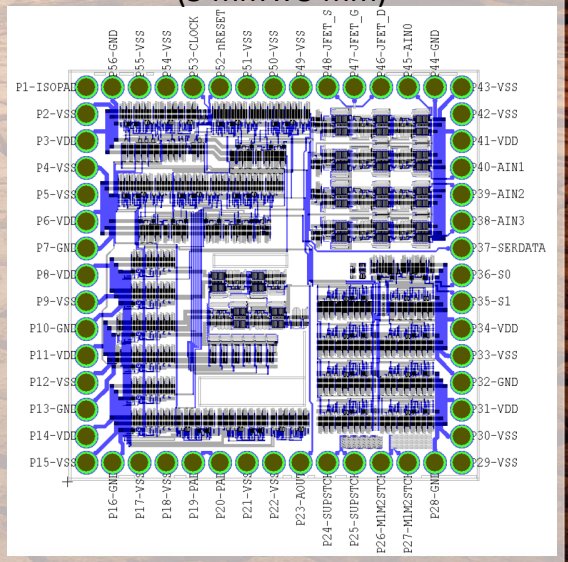
Pressure Sensor ASIC
(2.5 mm x 2.5 mm)



NOT Gate Chip
(1.3 mm x 1.3 mm)

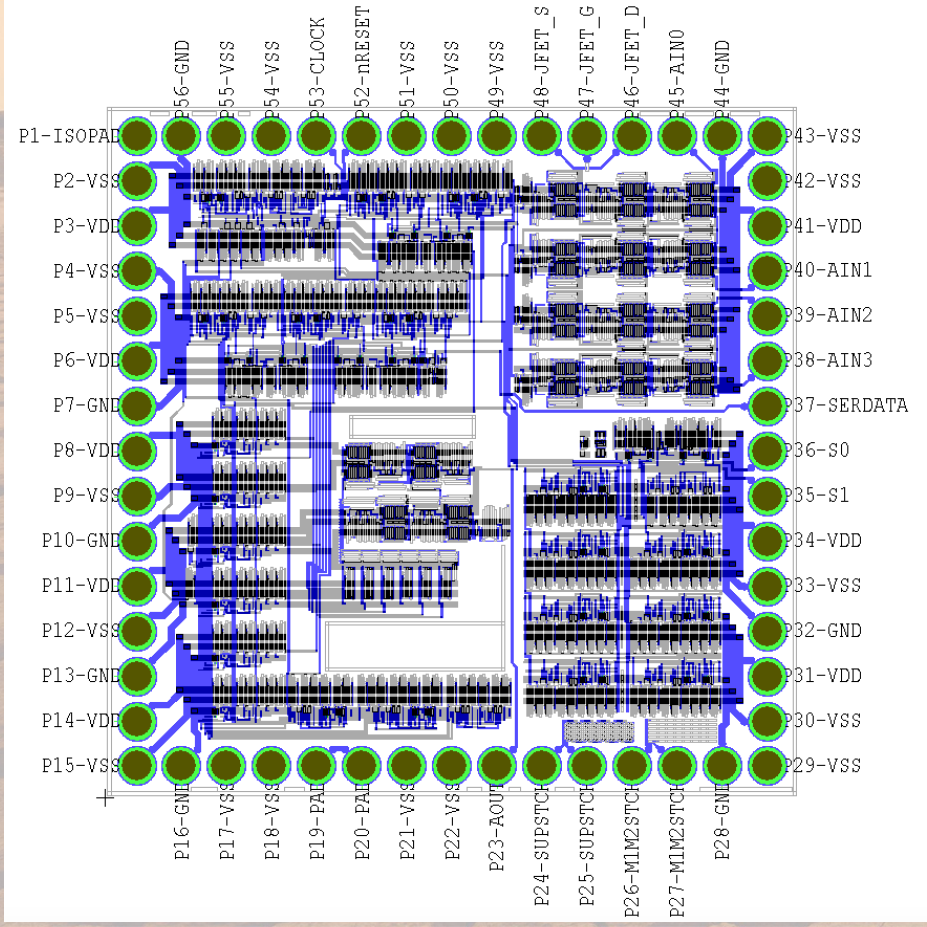


Venus Lander Control ASIC
(5 mm x 5 mm)

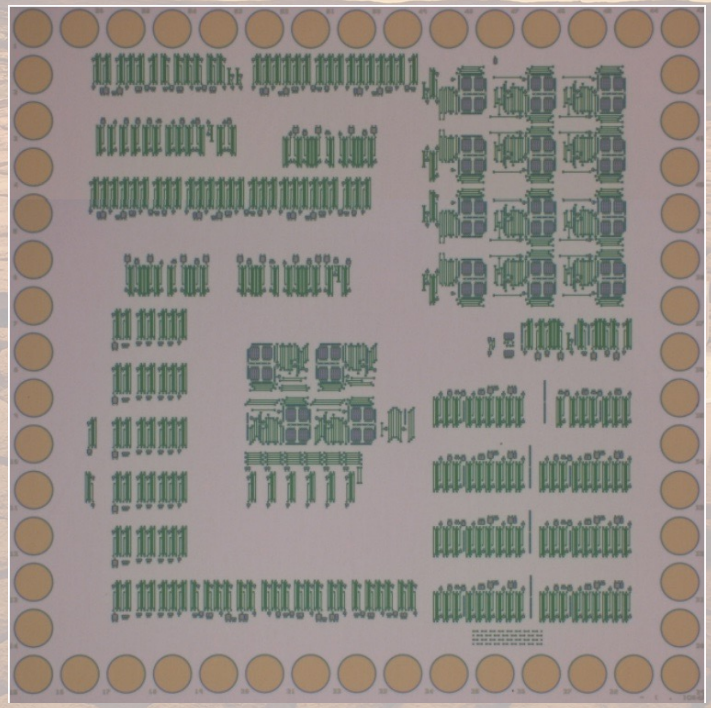


IC Gen 12 LLISSE-TD Chip

Low-power simple state-machine control chip for Venus lander technology demonstration mission



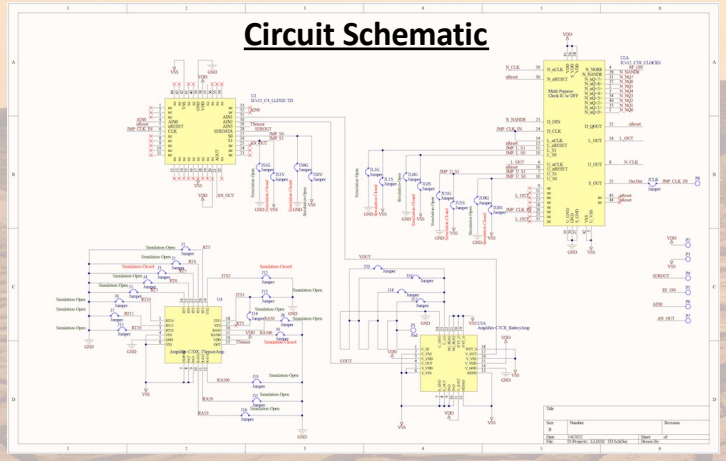
Chip after FEOL processing, ready for BEOL interconnect processing



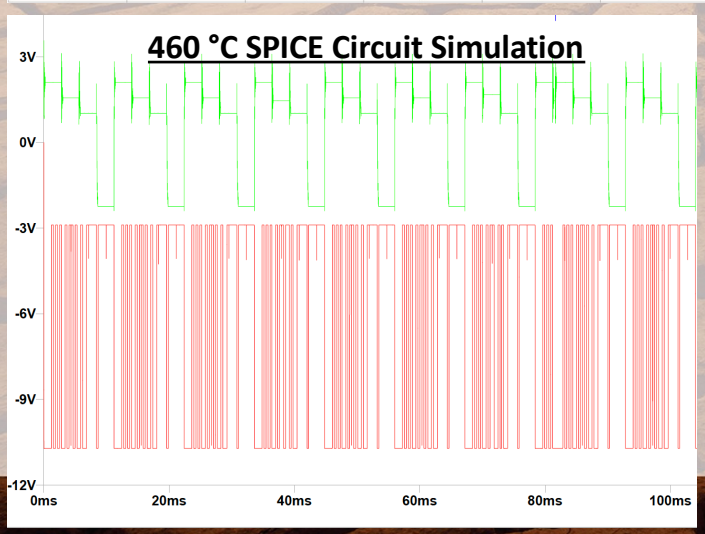
LLISSE Tech Demo (TD) Control Demonstration Board

Accomplishes timing, control, and digitization for Venus lander technology demonstration mission

Circuit Schematic



460 °C SPICE Circuit Simulation



DAC output wave

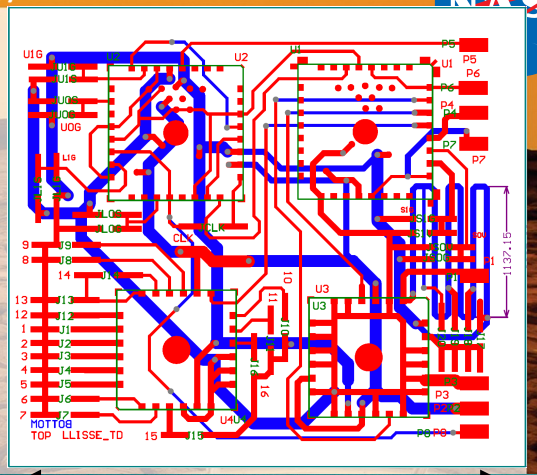
Output data bitstream

Circuit Board Layout

2-sided with through vias

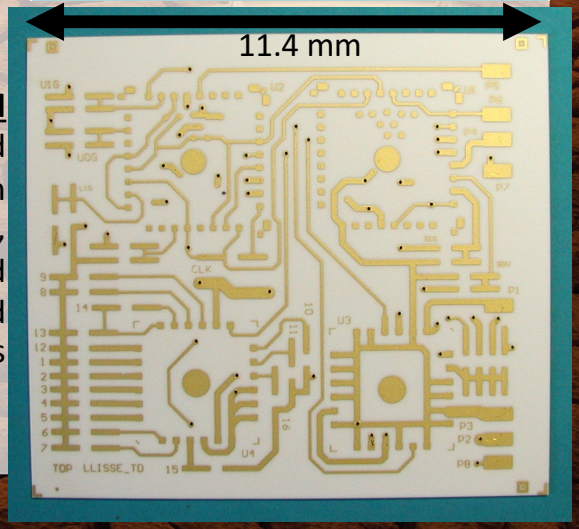
4 chips

11.4 cm x 10.1 cm



Circuit Board

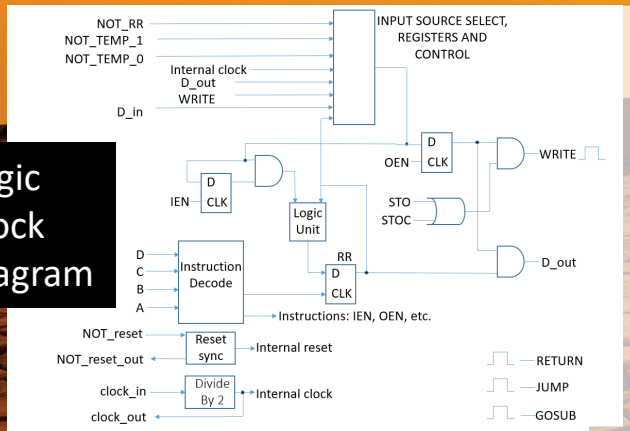
Manufactured by Thick Film Technology, Inc., to be populated with packaged IC Gen. 12 chips



IC Gen. 12 SiC Microprocessor

Extreme Environment Programmed Operations

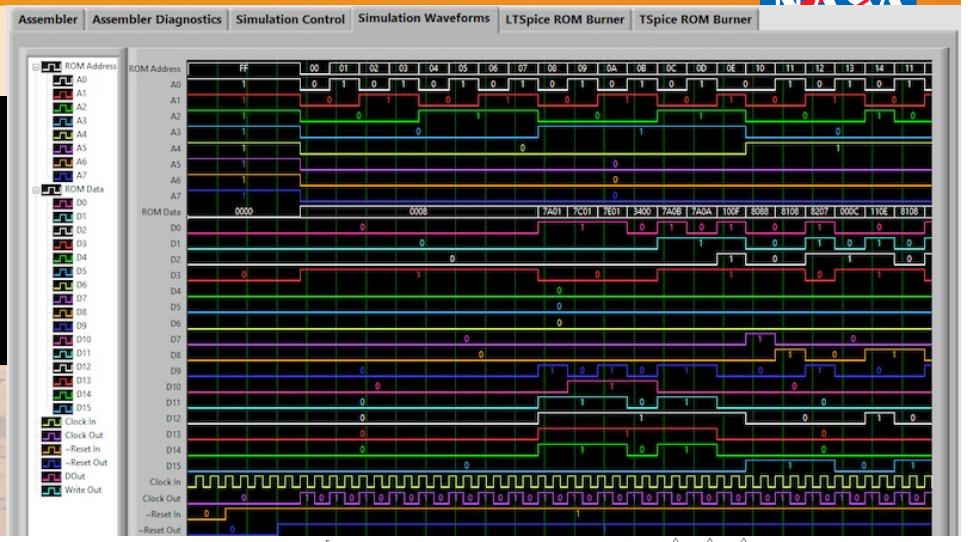
Logic Block Diagram



OP CODE (DCBA)	OPERAND	OPERATION
0000	XOR	If **RR** ≠ **D_in**, then, **RR** → 1
0001	XNOR	If **RR** = **D_in**, then, **RR** → 1
0010	AND	**RR** · **D_in** → **RR**
0011	NAND	$\overline{RR \cdot D\_in}$ → **RR**
0100	OR	**RR** + **D_in** → **RR**
0101	NOR	$\overline{RR + D\_in}$ → **RR**
0110	LD	**D_in** → **RR**
0111	LDC	$\overline{D\_in}$ → **RR**
1000	STO	**RR** → **D_out**, **WRITE** → Π
1001	STOC	$\overline{RR}$ → **D_out**, **WRITE** → Π
1010	IEN	**D_in** → **IEN**
1011	OEN	**D_in** → **OEN**
1100	SKZ	Skip next instruction IF **RR** = 0
1101	RTN	**RETURN** Flag → Π, skip next instruction
1110	JMP	**JUMP** Flag → Π
1111	GOSUB	**GOSUB** Flag → Π

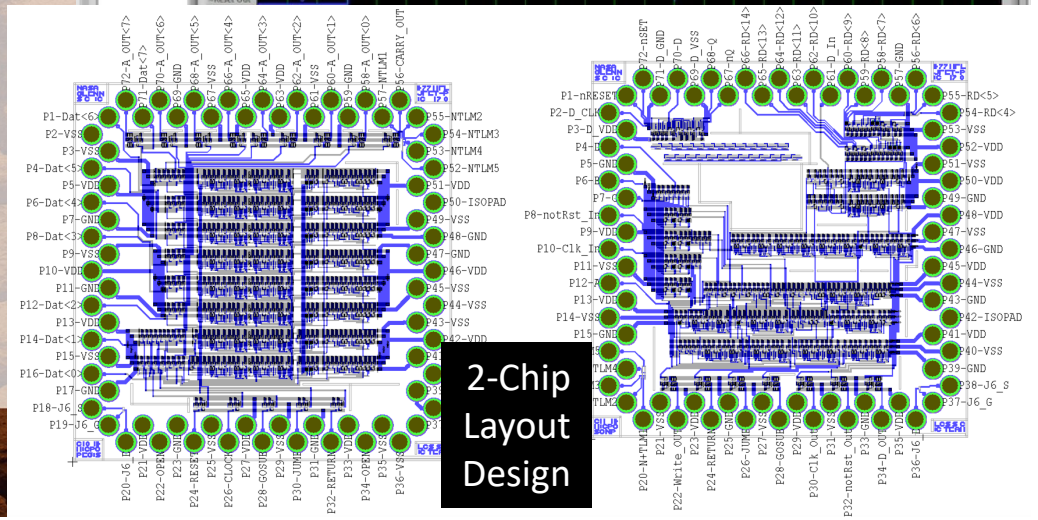
Instruction Set

Integrated Development Environment (IDE)
- Assembler
- Logic Simulator
- ROM Programmer



Transport Triggered Architecture

1.3 W @ 460 °C (SPICE Simulation)



2-Chip Layout Design

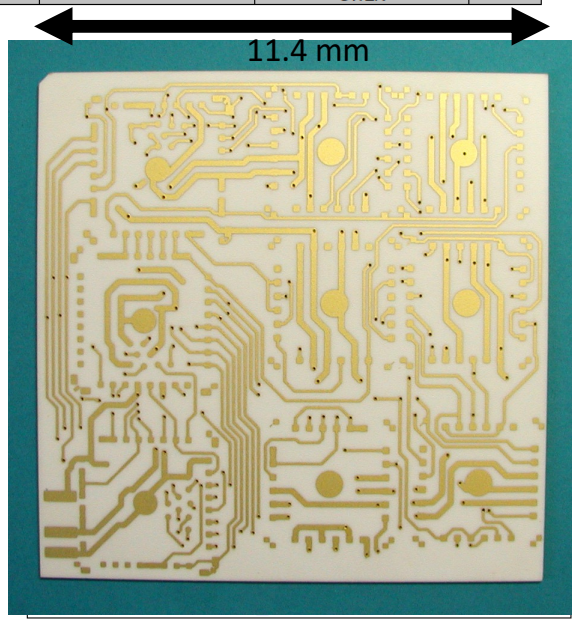
Microprocessor-Based Motor Control Demo Board

2-stepper-motor robot can follow line on floor using left, right, and front optical sensors

IC Gen 12 chip list & 2-sided circuit board

Bill Of Materials

Line #	Designator	Comment	Quantity
1	48EdgeConnector	z48pinEdgeConnector_Simulation	1
2	U1	ICv12_C11_MicroSeq	1
3	U2	ICv12_C10_MicroReg	1
4	U3, U6	ICv12_C13AY_Quad 2-1 Mux	2
5	U4	ICv12_C13C_1:8 Mux	1
6	U5, U8	ICv12_C13BY D Flip Flop Bank	2
7	U7, U10	8:1 Mux with NAND	2
8	U9	ICv12_C1X_ROM_LINE_FOLLOWER	1



Portion of assembly program compiled & built into IC Gen. 12 chip

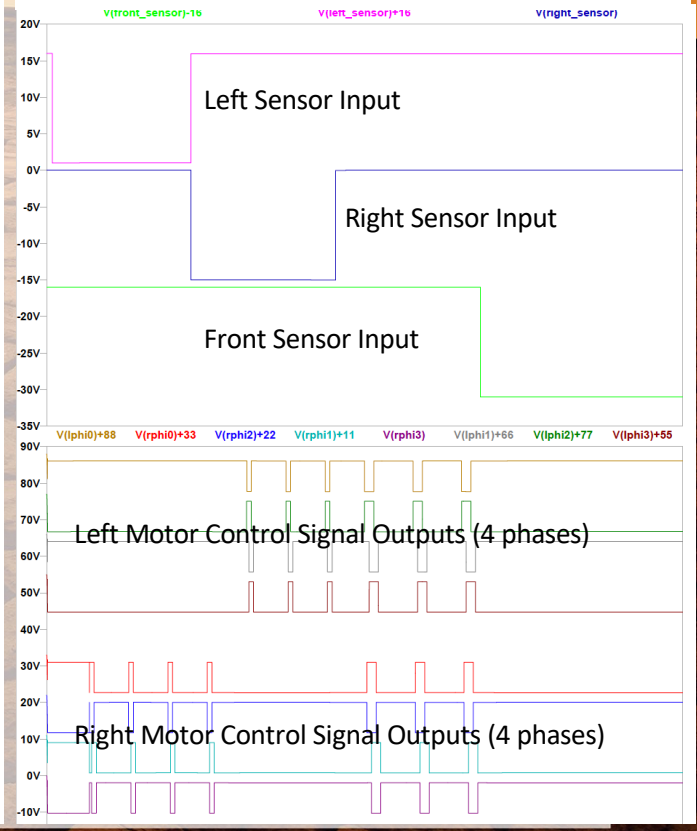
```
; Valentino Braitenberg vehicle program
; Robot follows a black tape on a shiny floor, or vice versa.

%ORG $00 ;address of first line of code is $00
%LEFT EQU $00 ;source address of LEFT eye
%RIGHT EQU $01 ;source address of RIGHT eye
%FRONT EQU $02 ;source address of FRONT eye
%RIGHTMOTOR EQU $01 ;address of LEFTMOTOR stepper
%LEFTMOTOR EQU $02 ;address of RIGHTMOTOR stepper

;main program
;
Start: nxor RR,RR ;make a 1
ien RR ;also use it to enable inputs
oen RR ;use it to enable outputs
top: ldc_e RR,(FRONT) ;Read /FRONT eye
skz ;If result is 1 (no obstacle) then skip loopback
and continue
jmp top ;loopback

FORWARD: stoc_e (LEFTMOTOR),RR ;RR contains a 1
sto_e (RIGHTMOTOR),RR
stoc_e (LEFTMOTOR),RR
sto_e (RIGHTMOTOR),RR
stoc_e (LEFTMOTOR),RR
sto_e (RIGHTMOTOR),RR
stoc_e (LEFTMOTOR),RR
sto_e (RIGHTMOTOR),RR
jmp top
```

SPICE circuit simulation of stepper motors controlled by sensor inputs



SiC power modules needed to switch each stepper motor phase on/off

Summary

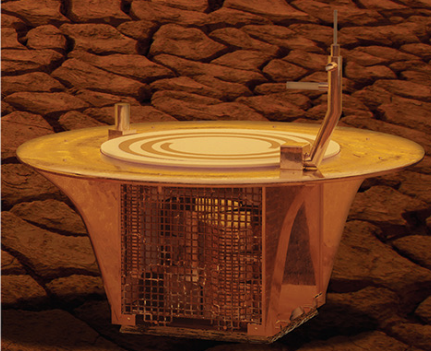
National Aeronautics and Space Administration

“Learn by doing” development of 500 °C Durable SiC JFET-R Integrated Circuits

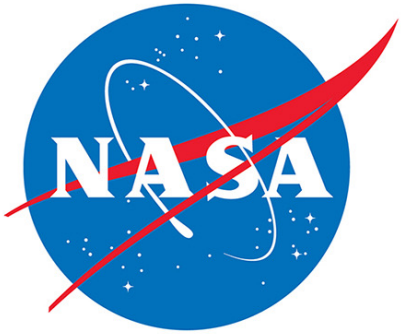
Unique durability foundation of NASA Glenn SiC JFET-R IC
- Unmatched 500 °C and Venus Durability (IC Gen. 10)
- Interconnect crack failure issue (IC Gen. 11 worse than IC Gen. 10)

Recent progress made since HiTEC 2021
- BEOL process development towards interconnect crack suppression
- IC Gen. 12 chip and circuit board designs
  - Venus lander electronics (digital and analog)
  - Simple microprocessor supporting robotic seeking operations

Planned next steps
- Oven-test BEOL test chips with packaging & circuit boards
- Finish IC Gen. 12 wafer fabrication based upon BEOL6 process
- Package and test IC Gen. 12 chips and circuit board demonstrations
- Tech transfer towards “ecosystem” of durable ICs manufacturing & infusion

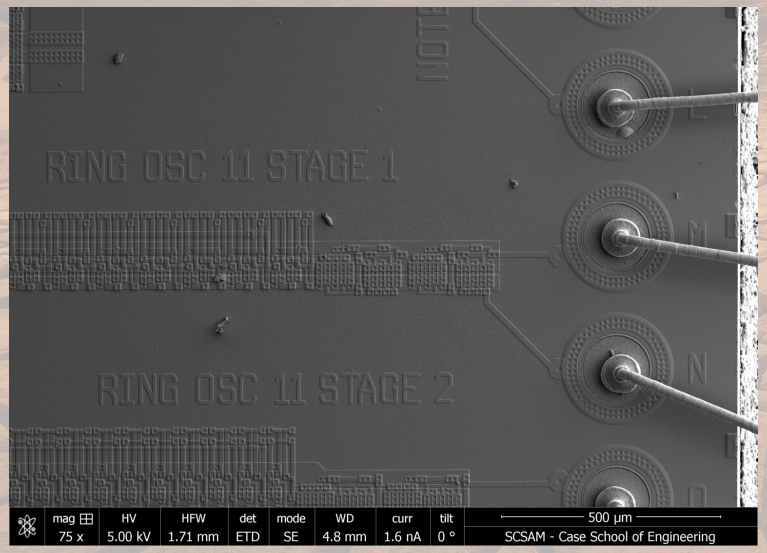


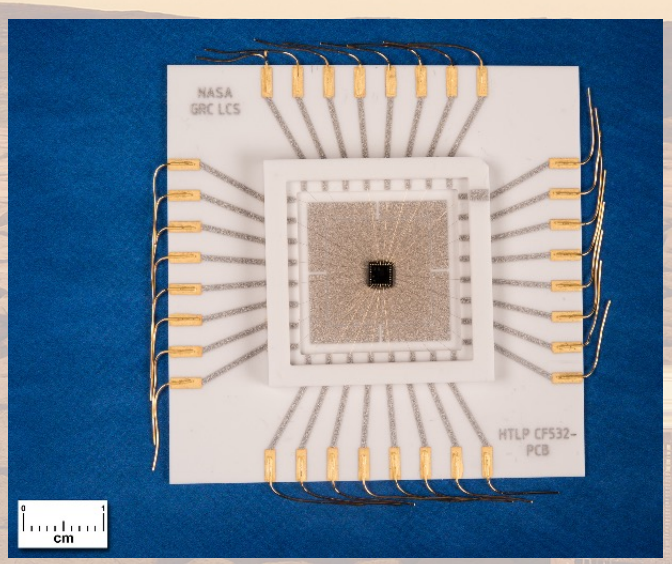
PS–03876–0223



NASA Glenn SiC Team Website: https://go.nasa.gov/sic
NASA Glenn SiC JFET IC Technology Guide: https://go.nasa.gov/jfetic
NASA Glenn Microsystems Fabrication Lab: https://www1.grc.nasa.gov/facilities/microfab/

500 °C Stable Bond Pads and Packaging[1,2]





- "IrIS" bond pad metal stack anchored directly to SiC[1]
- Pt thick-film traces, Au/Pt pads, Au die attach (600 °C), and Au ball bonding[2]

[1]D. Spry & D. Lukco, J. Electronic Materials 41 p. 915 (2012)
[2]L. Chen, et al., Proc. 2016 IMAPS High Temperature Electronics Conf. pp. 66-72

Remaining IC Gen. 12 Process Flow

IC Gen. 12 interconnect fabrication steps presently remaining:

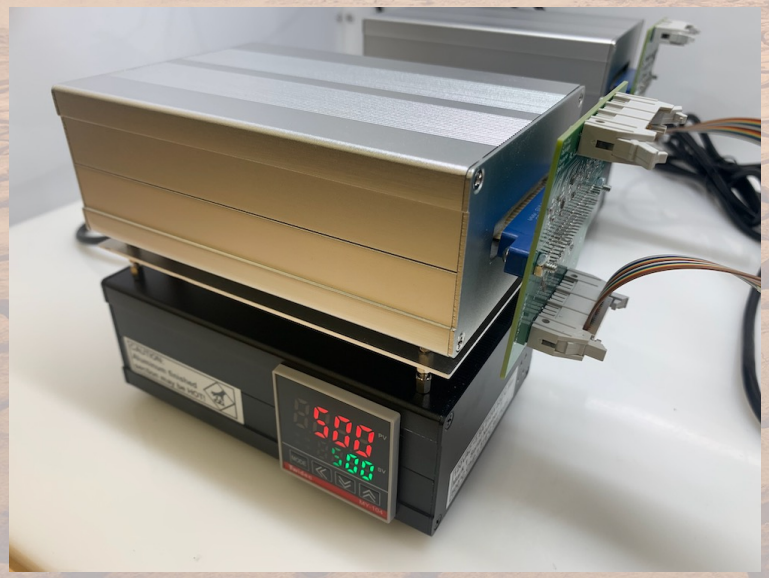
1. 1st dielectric layer (0.5 µm SiO_2 / 0.1 µm Si_3N_4 / 0.5 µm SiO_2) deposition (by GE)
2. Via1 patterned etch through 1st dielectric layer
3. Ohmic contact deposition and liftoff (same mask as Via1 etch)
4. Metal1 $TaSi_2$ interconnect deposition and etch patterning
5. 2nd dielectric layer (0.5 µm SiO_2 / 0.1 µm Si_3N_4 / 0.5 µm SiO_2) deposition (by GE)
6. Via2 patterned etch through 2nd dielectric layer
7. Metal2 $TaSi_2$ interconnect deposition and etch patterning
8. 3rd dielectric layer (0.8 µm SiO_2 / 0.1 µm Si_3N_4 / 0.8 µm SiO_2) deposition (by GE)
9. Bond pad Via3 patterned etch through all three dielectric layers
10. Deposition and etch patterning of Venus-durable bond pad "IrIS" metal stack
11. Etch removal of all three dielectric layers from wafer backside
12. Shadow-mask pattern deposition of Venus-durable "IrIS" backside metal stack
13. Deposition and liftoff patterning of gold wire bonding pad cap metal
14. 720 °C final wafer tube furnace anneal

Estimated completion date: Summer 2023

SiC IC Oven Testing Laboratory Upgrade (Phase 1)

Improved T ≥ 460 °C IC electrical testing statistics data needed for mission infusion

- PXI instrument chassis hardware and software setup for parallel-testing (future 32 ovens capacity)
- First 8 “Mark 1” next-generation small/compact test ovens constructed and installed
  - Rapid heating & cooling (for thermal cycling tests) and power-efficient



Packaged BEOL test chips will be 500 °C tested/cycled first, until IC Gen. 12 chips become available.

Mark 1 oven design and construction by Stephanie Booth and David Spy

IC Gen. 12 Chip Documentation

(Example: LLISSE Clock Chip C3X)

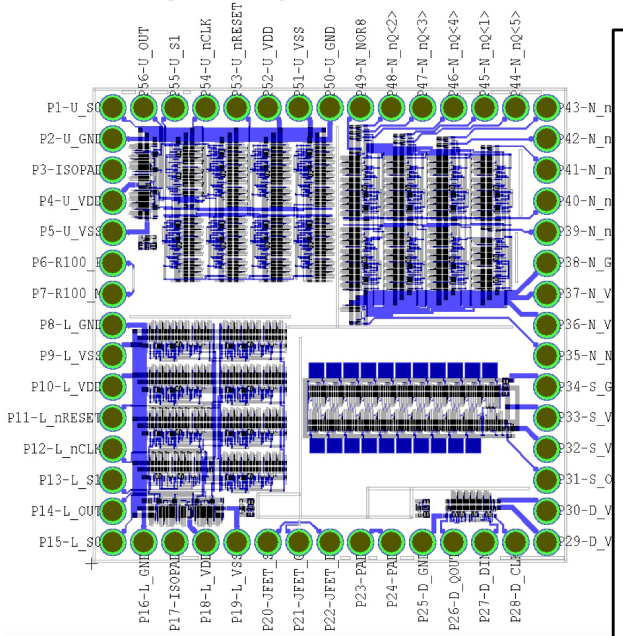
Chip Name: C3X_CLOCKS_ULP

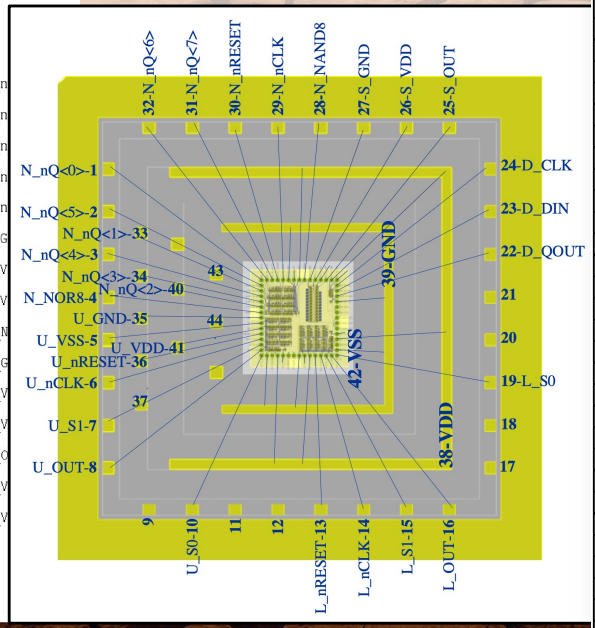
This chip contains the following 5 independent integrated circuits (ICs):

1. 21-Stage Ring Oscillator Clock (denoted with "S" pads).
2. Selectable Frequency Divider/counter (denoted by "U" pads).
3. Selectable Frequency Divider/counter (denoted by "L" pads).
4. Start- and End-State 8-bit Counter (denoted by "N" pads).
5. D-Flip Flop (denoted by "D" pads).

Depending upon how the ICs are interconnected at the package level, these 5 ICs provide "ultra-low power" base clock and control signals for running state machines (e.g., LLISSE). Each independent IC functions using logic signals near -10V for logic 0/low, 0V for logic 1/high, and each IC is independently powered using VDD near +25V, VSS near -25V, and GND pads.

C3X_CLOCKS_ULP Chip Bond Pad Map (56-Pad Frame):





Chip datasheets:

- Functional descriptions
- Chip & high-T ceramic package pinouts
- Schematic/block diagrams

SPICE models

HT Pkg Pin #	Chip Pad #	Terminal Abbreviation	Signal Description
10	1	U_S0	Input frequency division selection Bit0 for "U" Frequency Divider IC (-10V to 0V Logic)
39	2	U_GND	0V Ground for "U" Frequency Divider IC
38	4	U_VDD	+25V Power for "U" Frequency Divider IC
42	5	U_VSS	-25V Power for "U" Frequency Divider IC
39	8	L_GND	0V Ground for "L" Frequency Divider IC
42	9	L_VSS	-25V Power for "L" Frequency Divider IC
38	10	L_VDD	+25V Power for "L" Frequency Divider IC
13	11	L_nRESET	Input NOT RESET active low reset for "L" Frequency Divider IC (-10V to 0V Logic)
14	12	L_nCLK	Input clock signal to be divided by "L" Frequency Divider IC (-10V to 0V Logic)
15	13	L_S1	Input frequency division selection Bit1 for "L" Frequency Divider IC (-10V to 0V Logic)
16	14	L_OUT	Ouput frequency divided clock signal from "L" Frequency Divider IC (-10V to 0V Logic)
19	15	L_S0	Input frequency division selection Bit0 for "L" Frequency Divider IC (-10V to 0V Logic)
39	16	L_GND	0V Ground for "L" Frequency Divider IC
38	18	L_VDD	-25V Power for "L" Frequency Divider IC
42	19	L_VSS	+25V Power for "L" Frequency Divider IC
39	25	D_GND	0V Ground for D Flip Flop IC
22	26	D_QOUT	Output Q for D Flip Flop IC (-10V to 0V Logic)
23	27	D_DIN	Input D for D Flip Flop IC (-10V to 0V Logic)
24	28	D_CLK	Input clock for D Flip Flop IC (-10V to 0V Logic)
42	29	D_VSS	-25V Power for D Flip Flop IC (-10V to 0V Logic)
38	30	D_VDD	+25V Power for D Flip Flop IC (-10V to 0V Logic)
25	31	S_OUT	Output for "S" Ring Oscillator Clock IC (-10V to 0V Logic)
42	32	S_VSS	-25V Power for "S" Ring Oscillator Clock IC
26	33	S_VDD	+25V Power for "S" Ring Oscillator Clock IC
27	34	S_GND	0V Ground for "S" Ring Osillator Clock IC
28	35	N_NAND8	Output of 8-input NAND for "N" 8-bit Counter IC (-10V to 0V Logic), high at count=255
38	36	N_VDD	+25V Power for "N" 8-bit Counter IC
42	37	N_VSS	-25V Power for "N" 8-bit Counter IC
39	38	N_GND	0V Ground for "N" 8-bit Counter IC
29	39	N_nCLK	Input clock for "N" 8-bit Counter IC (-10V to 0V Logic)
30	40	N_nRESET	Input NOT RESET active low reset for "N" 8-bit Counter IC (-10V to 0V Logic)
31	41	N_nQ<7>	Output NOT Bit7 for "N" 8-bit Counter IC (-10V to 0V Logic)
32	42	N_nQ<6>	Output NOT Bit6 for "N" 8-bit Counter IC (-10V to 0V Logic)
1	43	N_nQ<0>	Output NOT Bit0 for "N" 8-bit Counter IC (-10V to 0V Logic)
2	44	N_nQ<5>	Output NOT Bit5 for "N" 8-bit Counter IC (-10V to 0V Logic)
33	45	N_nQ<1>	Output NOT Bit1 for "N" 8-bit Counter IC (-10V to 0V Logic)
3	46	N_nQ<4>	Output NOT Bit4 for "N" 8-bit Counter IC (-10V to 0V Logic)
34	47	N_nQ<3>	Output NOT Bit3 for "N" 8-bit Counter IC (-10V to 0V Logic)
40	48	N_nQ<2>	Output NOT Bit2 for "N" 8-bit Counter IC (-10V to 0V Logic)
4	49	N_NOR8	Output of 8-input NOR for "N" 8-bit counter IC (-10V to 0V Logic), high at count=0
35	50	U_GND	0V Ground for "U" Frequency Divider IC
5	51	U_VSS	-25V Power for "U" Frequency Divider IC
41	52	U_VDD	+25V Power for "U" Frequency Divider IC
36	53	U_nRESET	Input NOT RESET active low reset for "U" Frequency Divider IC (-10V to 0V Logic)
6	54	U_nCLK	Input clock signal to be divided by "U" Frequency Divider IC (-10V to 0V Logic)
7	55	U_S1	Input frequency division selection Bit1 for "U" Frequency Divider IC (-10V to 0V Logic)
8	56	U_OUT	Ouput frequency divided clock signal from "U" Frequency Divider IC (-10V to 0V Logic)

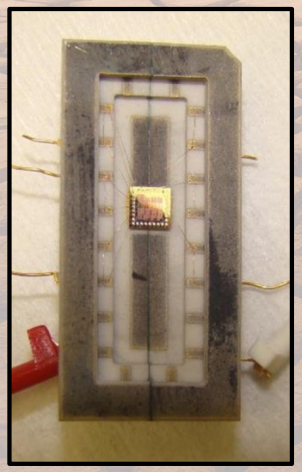
60 Day SiC Integrated Circuit Venus Test (in GEER)[1]

Two NASA Glenn SiC IC Gen. 10 circuits passed 60 days of stable electrical operation **directly exposed to the Venus surface environment** (no package lid).

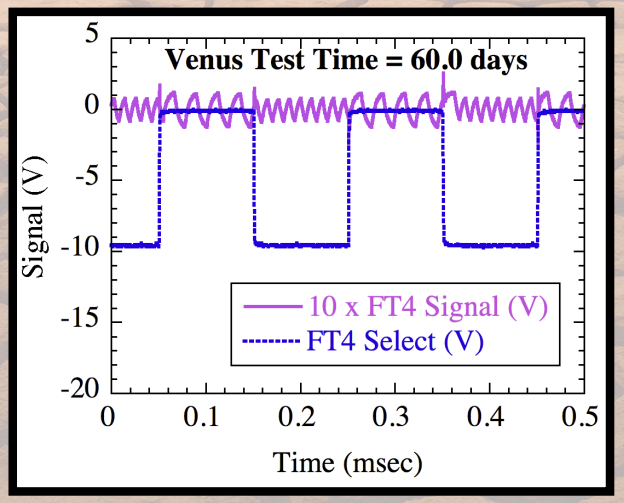
User-selectable ÷2/÷4 clock oscillator demonstration IC (175 transistors).

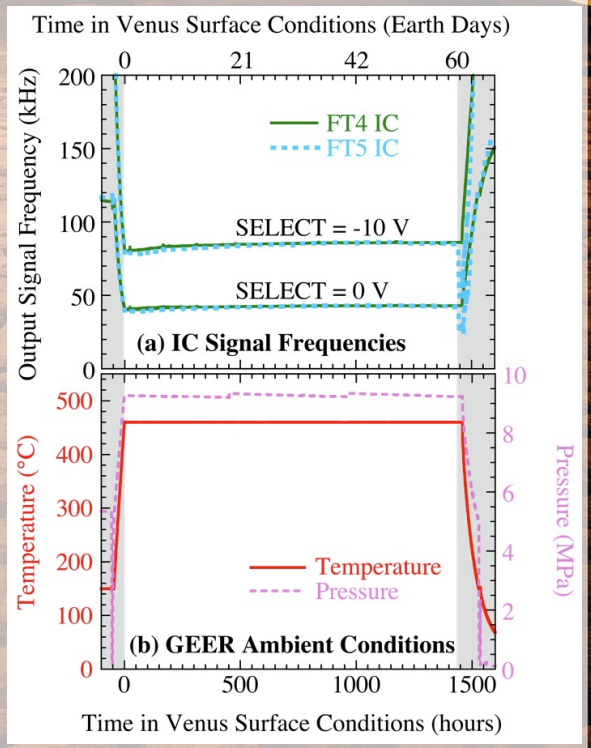
Before GEER

60 days GEER



Input and Output IC Waveforms

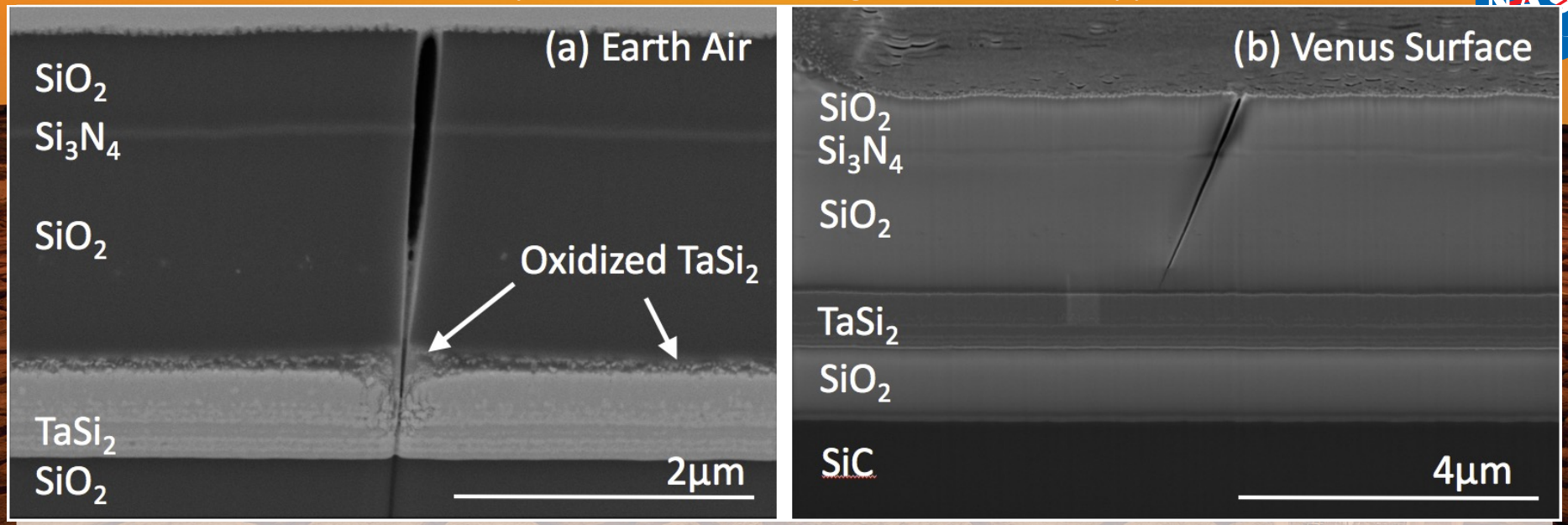




[1]Neudeck et al., IEEE J. Electron Devices Soc., vol. 7 p. 100 (2018).

Earth vs. Venus High Temperature Dielectric Crack Behavior Difference*

Studied by cross-sectional scanning electron microscopy



(a) In Earth air, the crack allows the top surface of the $TaSi_2$ film to oxidize which exacerbates metal failure.

(b) In Venus surface environment, the crack reaches the top of the $TaSi_2$ but does not propagate through the $TaSi_2$ and there is no observable evidence of $TaSi_2$ film oxidation.

*D. Spry et al., Mat. Sci. Forum vol. 924 pp. 949-952 (2018)