Electrical and Dielectric Characterizations of HTCC Electronic Packages for High Temperature Harsh Environment Applications

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Abstract
A prototype high temperature co-fired ceramic (HTCC) alumina packaging system composed of a 32-I/Os package and a compatible circuit board was previously developed and demonstrated for long term operation in 500 °C environments. The electrical / dielectric parasitic parameters of that chip level package were characterized and reported. This co-fired packaging system with platinum (Pt) conductor has successfully facilitated tests of silicon carbide (SiC) analog and digital integrated circuits (ICs) developed at NASA GRC at 500°C for up to 10,000 hours in ambient oven environment and 60 earth days in Venus surface environment with simulated temperature, pressure, and chemical constituents. Based on these previous results, this paper introduces new designs of Pt-HTCC packages with 16, 24, and 44 I/Os for packaging a new generation SiC ICs with 8, 24, 56, 62, and 72 I/Os to be tested in high temperature harsh environments. The package with 44 I/Os is specifically designed for the new SiC ICs with 56, 62, and 72-I/Os and electrical connection needs, the power pads of this package are consolidated, and an array of I/O pads distributed on separated vertical levels (inside the package) is used to control the overall package dimensions and mitigate the parasitic effects at high temperatures. This paper will present the detailed design of these chip-level packages and results of electrical and dielectric characterization of these newly fabricated chip-level Pt-HTCC packages.

Key words
High temperature, packaging, HTCC, Venus, SiC, harsh environment, 500 °C.

I. Introduction
High temperature electronics can find many desired applications in both aeronautics and space exploration [1,2,3], NASA is developing silicon carbide (SiC) electronics [4,5] including packaging technology to meet these needs. A prototype high temperature co-fired ceramic (HTCC) alumina packaging system composed of a 32-I/Os packages [6] and compatible circuit boards [7] was previously developed and demonstrated for continued long term operation in 500 °C environments. The electrical and dielectric parasitic parameters of that chip level package were characterized and reported [6]. Compatible chip level packaging technology including thick-film paste based die-attach scheme and Au alloy wire-bonding have also been developed in parallel [7]. This packaging system with co-fired platinum (Pt) conductor has successfully facilitated tests of SiC analog and digital integrated circuits (ICs) developed in NASA GRC at 500°C for up to 10,000 hours in ambient oven environment [8,9,10] and 60 earth days in Venus surface environment with simulated temperature, pressure, and chemical constituents [11,12]. This Pt/HTCC alumina material system is compatible with industrial high temperature co-fired (HTCC) process [6,13]. Based on these previous results, this paper introduces newly designed Pt-HTCC packages with 16, 24, and 44 I/Os for packaging the next generation SiC ICs with 8, 24, 56, 62, and 72 I/Os. Among these packages, the CF544 package with 44 I/Os is specifically designed for new SiC ICs with 56-, 62-, and 72-I/O, and consolidated DC bias connections. An array of I/O pads distributed on separated vertical levels (inside the package) is used to control the overall package dimensions and mitigate the parasitic effects at high temperatures. This paper introduces these newly fabricated chip-level Pt-HTCC packages and presents results of electrical and dielectric characterization of these newly fabricated packages.

II. Package Designs
All the ceramic chip-level packages introduced in this paper are made of multilayers 92% alumina with co-fired surface Pt metallization and conductive Pt vias ($\leq 0.35\Omega$) using a standard high temperature co-fire process. Package lids are made of the same material system and process. All three packages composed of 12 layers of laminated alumina tape are 0.084 in thick after firing, and compatible lids composed

of 5 layers of laminated alumina tape are 0.035 in thick after firing, with each layer of alumina about 0.007 in thick after firing. The surface exposed Pt (~5.1 micrometers thick) pads are electroplated with a thin Au over layer ~ 100 micro inches thick for die-attach and wire-bonding. A notch is designed to indicate the sequence of I/O assignment (Figures 1-3). In addition to the originally designed metallization patterns, Pt traces (most of them) sandwiched in alumina layers are added for electroplating Au on most exposed surface Pt metallization pads and traces. The various package designs based on Pt/HTCC alumina material system are implemented for different SiC ICs. Lids for these packages are also metallized for EM (electromagnetic) shielding.

A. CF516 Package with 16 I/Os

Packages with 16 I/Os (pins), denoted by CF516, are designed for one or two of 5 mm x 5mm SiC die(s) with 8 bond-pads. It measures 1.05 in x 0.57 in x 0.084 in and the lid has the same lateral dimensions with 0.035 in thickness. Each die-attach pad on the package floor fits a 5 mm x 5mm die with extra surrounding metallization edges for flexible wire-bonding to any wire-bond-pad(s) for SiC die backside metallization bias or chip shielding. Two die-attach pads are electrically connected together also with the conductive seal ring on the top surface of package walls through a Pt trace sandwiched between alumina layers (not shown). Wire-bond pads measures 0.030 in x 0.045 in with 0.09 in spacing, as shown in Fig. 1a. The bond pads on the backside of the package are shown in Fig. 1b; the metallization pads on the backside for connections to circuit board measure 0.06 in x 0.060 in with 0.06 in spacing. Each pad on the backside is connected to the corresponding wire-bond pad inside the package through Pt via. Two round shaped pads on the package backside are for mount on a circuit board [7], two pads are connected with each other for plating purpose.

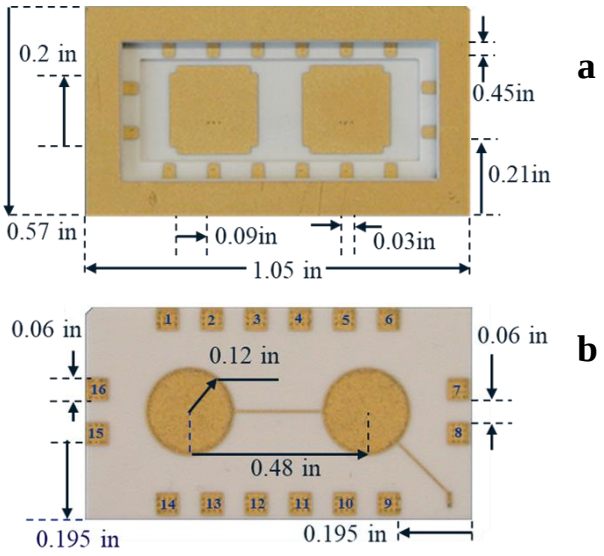

Figure 1: Top and bottom views of CF516 package. 1a shows the top side of the package without a lid, 1b shows the package backside. The package is 0.084 in thick.

B. CF524 Package with 24 I/Os

Packages with 24 I/Os (pins), denoted by CF524, are designed for 2.4 mm x 2.4 mm SiC die(s) with 24 bond-pads. It measures 1.05 in x 1.05 in x 0.084 in (thick) and the lid has the same lateral dimensions with 0.035 in thickness. The die-attach pad fits a 2.4 mm x 2.4mm die with extra surrounding metallization edges for flexible wire-bonding to any wire-bond-pad(s) for SiC die backside metallization bias or EM shielding. The die-attach pad is electrically connected to the conductive seal ring on the top surface of package walls through a Pt trace sandwiched between alumina layers and conductive Pt vias. Wire-bond pads measures 0.030 in x 0.045 in with 0.09 in spacing, as shown in Fig. 2a. The bond pads on the backside of the package are shown in Fig. 2b; the metallization pads on the package

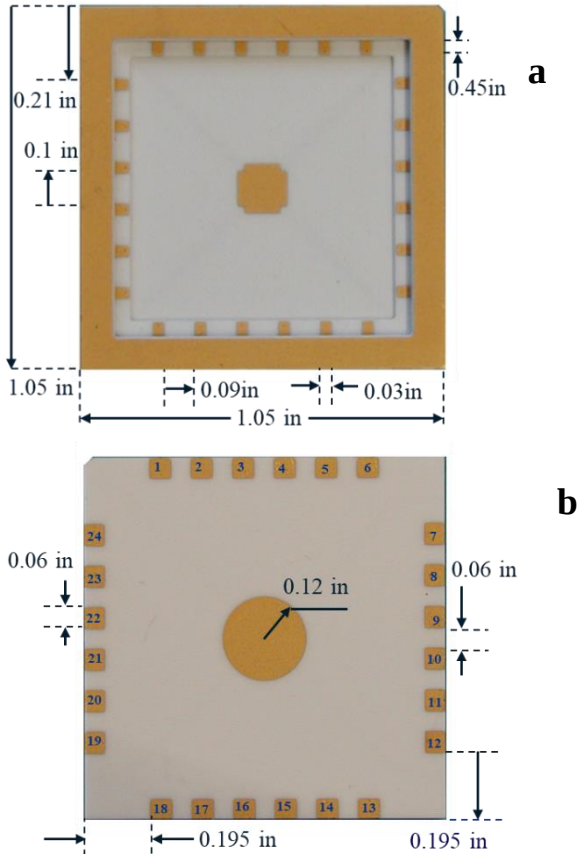

Figure 2: Top and bottom views of CF524 package. 2a shows the top side of the package without a lid, 2b shows the package backside. The package is 0.084 in thick.

backside for connections to circuit board measure 0.06 in x 0.06 in with 0.06 in spacing. Each pad on the backside is connected to the corresponding wire-bond pad inside the package through Pt via. The round shaped pad in the center of the package backside is for mounting the package on a circuit board [7].

C. CF544 Package with 44 I/Os

Packages with 44 I/Os (pins), denoted by CF544, are designed for 5 mm x 5 mm SiC die(s) with the number of bond-pads up to 72. It measures 1.18 in x 1.18 in x 0.084 in (thick), the lid has the same lateral dimensions with 0.035 in thickness. The die-attach pad fits a 5 mm x 5 mm die with extra surrounding metallization edges for flexible wire-bonding to any wire-bond-pad(s) for SiC die backside metallization bias or EM shielding. This package design varies in significant ways from CF516 and CF524 packages. This package is specially designed for packaging SiC dies with needs of multiple groups of power pads to be connected to Vdd, Vss, and Ground. To provide with flexibility of wire-bonding design for multiple kinds of SiC dies, DC power connections for Vss, Ground, and Vdd are consolidated respectively. Vss trace is surrounding the die attach pad, two "U" shaped traces are designed for ground and Vdd connections, respectively, as shown in Figure 3a. The ground trace is electrically connected to the conductive seal ring on the top surface of package walls through a Pt trace (not shown) sandwiched between alumina layers for EM shielding.

An array of I/O pads, at "north" quad, distributed on three vertical levels (Figure 3a) is used to control the overall package dimensions and mitigate the parasitic effects at high temperatures. Wire-bond pads measure 0.0275 in x 0.0275 in. The spacing between the pads along edges is 0.077 in, and the distances between inner array wire-bond pads are all above 0.055 in, as shown in Fig. 3b. Figure 3a also shows two Pt pads without Au coating, these two pads are for assisting wire-bonding as "middle islands" not connected to any metallization pads on the package backside. On the backside of the package, the metallization pads along package edges for connections to circuit board measures 0.055 in x 0.055 in with 0.055 in spacing, as shown in Fig. 3b, and the diameter of round shaped inner bond pads is 0.055 in with over 0.055 in spacing between pads. Each pad on the backside is connected to the corresponding wire-bond pad inside the package through Pt via. The round shaped big pad in the center (Figure 3b) is for mounting the package on a circuit board [7].

III. Electrical Characterization

Temperature dependent electrical and dielectric parameters such as parasitic AC conductance and capacitance between selected neighboring I/Os of these packages were measured by AC impedance analyzer at frequencies of 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz from 550ºC to room temperature with steps of 50 °C. During the testing, the package was soaked in a temperature-controlled air ambient oven with electrical resistive heating coils embedded through two sidewalls of the oven chamber. The packages were directly connected to 0.25mm diameter Au wires with lengths of approximately 15 cm which connected to 1 m long, 50 Ω RG 58C/U standard coaxial cables located outside of the oven. An Agilent 4294A impedance analyzer was used to measure the inter I/O AC conductance and capacitance based on a parallel RC circuit model. The AC conductance measures the dielectric loss as well as leakage of the ceramic substrate material, and the capacitance measures the dielectric polarization of the substrate

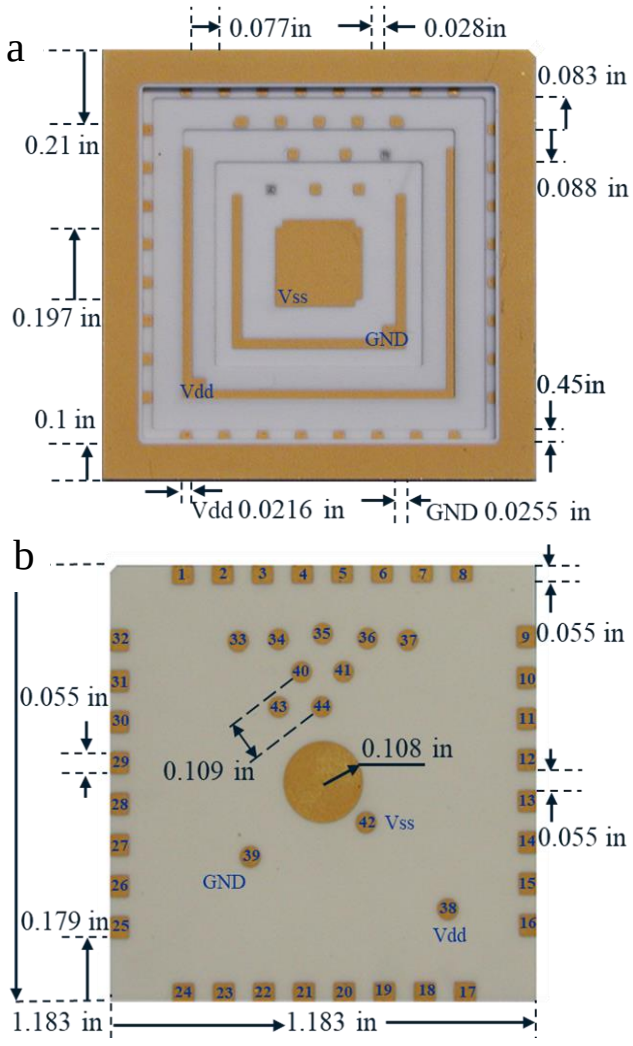

Figure 3: Top and bottom views of CF544 package. 3a shows the top side of the package without a lid, 3b shows the package backside. The package is 0.084 in thick.

material. Both were measured with small (500 mV) AC signals in a frequency window of 10Hz at test frequencies. 'Near' DC insulation resistance between selected neighboring I/Os under DC bias up to ±15V (a span of 30V) was assessed by the slope of the measured current - voltage (I-V) curve (scanned at 60 Hz) using a Sony/Techtronix 370A curve tracer. The minimal measurable current limit of the curve tracer is 0.1 µA.

Temperature dependent DC leakage currents between Vdd and GND traces, and Vdd-GND traces of CF544 package, were measured using a Kiethley Instruments 2410 Source-Measurement Unit controlled by a PC, with 35V DC bias, from room temperature to 800 °C, with steps of 100 °C, in air ambient.

The packages were heated at 550 °C for 72 hours immediately preceding AC and most DC parameter measurements.

Both DC and AC parameters of the chip-level packages were measured without the package lid. Since the measured AC parasitic parameters of the packages are small and comparable to the contributions from gold wires connecting the package inside the oven to coaxial cables outside the oven leading to the impedance meter/analyzer, the parallel RC (capacitance and conductance) parameters between gold wires (without a package) were measured separately and the values were subtracted from the data including the package for more precise measurement / assessment of package AC parasitic parameters. Above the frequency of 1MHz, it became more difficult to compensate the parasitic effects of the wiring in the oven, especially under low package conductance. The oven power was briefly switched off, with negligible temperature change, during each measurement to reduce AC interference from the filaments in the oven.

IV. Electrical Parameters

A. CF516 Package with 16 I/Os

Table 1 shows the results of parasitic capacitance (upper number) in unit of pF and parallel AC conductance (lower number) upper limit in unit of µS between I/O1 and neighboring I/O2 (see Figure 1b) with I/O1 connected to the seal ring on the package wall using wire-bonding. The capacitance data are rounded to one digit with ± 0.5pF measurement error, and any capacitance below 1 pF is rounded to 1pF. The parasitic capacitance between I/O 1and I/O2 in the entire temperature and frequency ranges is between ~1pF and 2pF, trending higher at lower frequencies and higher temperatures. This trend is consistent with the dependence of dielectric constant of the alumina material on frequency and temperature reported earlier [13].

Table 1: CF516 package (without a lid on) parasitic capacitance (upper) in unit of pF and AC conductance (lower) in unit of µS between I/O1 and I/O2. I/O1 is connected to die attach pads and the seal ring. Contributions of gold wires have been subtracted.

T (ºC) / f (Hz)	T_R	50	100	150	200	250	300	350	400	450	500	550
100	1	1	1	1	1	1	1	1	1	2	2	2
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
1K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
10K	1	1	1	1	1	1	1	1	1	1	1	2
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.05	<0.01	<0.01
100K	1	1	1	1	1	1	1	1	1	1	1	1
	0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.05	<0.05	<0.05
1M	1	1	1	1	1	1	1	1	1	1	1	1
	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05	<0.1	<0.1	<0.1

Table 2: CF516 package (without a lid on) parasitic capacitance (upper) in unit of pF and AC conductance (lower) in unit of µS between I/O2 and I/O3. Contributions of gold wires have been subtracted.

T (ºC) / f (Hz)	T_R	50	100	150	200	250	300	350	400	450	500	550
100	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
1K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
10K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
100K	1	1	1	1	1	1	1	1	1	1	1	1
	0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.01	<0.01
1M	1	1	1	1	1	1	1	1	1	1	1	1
	<0.01	<0.05	<0.05	<0.05	<0.05	<0.01	<0.01	<0.01	<0.05	<0.05	<0.05	<0.05

Considering the high impedance analyzer measurement error (>10%) for high impedance (low capacitance and conductance) range (Agilent 4294A Precision Impedance Analyzer Operation Manual), and a four-wire customer (wiring) fixture was used for test, the measured conductance data (the measured conductance of package I/Os with Au wires minus the measured conductance of Au connecting wires) and 20% of the higher directly measured conductance data (either of the package with wires or wires only) are compared, whichever is higher is rounded to 0.005μS, 0.01 μS, 0.05 μS, or 0.1 μS, and denoted as an upper limit in the data tables. All the conductance data below 0.005μS are denoted as < 0.005μS, for simplicity, in Table 1. The measured parasitic capacitance and conductance data of other two packages are all presented in the same way. Basically, at 1 MHz and high temperatures at 450 °C, 500 °C, and 550 °C the conductance is the highest. This is also consistent with material AC conductivity data of the alumina material reported earlier [14].

Table 2 shows the results of parasitic parallel capacitance (upper number) in unit of pF and upper AC conductance (lower number) limit in unit of μS between I/O2 and neighboring I/O3 of CF516 package (see Figure 1a and b). The parasitic capacitance is only 1 pF at all frequencies and temperatures, the capacitances at the high temperature and low frequency ends are lower compared with the capacitance between I/O1 – I/O2. This can be attributed to the fact that I/O1 is connected to larger metallization area, so the parasitic parameters between I/O1-I/O2 are expected to be higher.

The conductance between I/O2 – I/O3 in the entire temperature and frequency ranges are < 0.05 μS as shown in Table 2. Overall, the conductance data between I/O2-I/O3 are either equivalent to or lower than the conductance of I/O1-I/O2 at a same frequency and temperature measurement point. This can also be interpreted by the larger metallization area of I/O1 connected compared to I/O2 and I/O3. Overall, the parasitic conductance tends to higher at high temperature and high frequency ends.

The DC leakage currents, measured using the curve tracer, between I/O1-I/O2 and I/O2-I/O3 with ±15V bias at all test temperatures are all at or below the curve tracer current detection limit of 0.1 μA. It is equivalent to ≥ 150 MΩ for both I/O1-I/O2 and I/O2-I/O3.

B. CF524 Package with 24 I/Os

Table 3 shows the results of parasitic capacitance (upper number) in unit of pF and parallel AC conductance (lower number) upper limit in unit of μS between I/O1 and neighboring I/O2 (see Figure 2) with I/O1 connection to the seal ring on the package wall using wire-bonding. The capacitance data are round to one digit with ± 0.5 pF measurement error, and any capacitance below 1 pF is

Table 3: CF524 package (without a lid on) parasitic capacitance (upper) in unit of pF and AC conductance (lower) in unit of μS between I/O1 and I/O2. I/O1 is connected to die attach pads and the seal ring. Contributions of gold wires have been subtracted.

T (ºC) / f (Hz)	T_R	50	100	150	200	250	300	350	400	450	500	550
10	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
1K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
10K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
100K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.05
1M	1	1	1	1	1	1	1	1	1	1	1	1
	<0.01	<0.01	<0.01	<0.05	<0.05	<0.01	<0.01	<0.01	<0.05	<0.05	<0.05	<0.05

Table 4: CF524 package (without a lid on) parasitic capacitance (upper) in unit of pF and AC conductance (lower) in unit of μS between I/O2 and I/O3 of. Contributions of gold wires have been subtracted.

T (ºC) / f (Hz)	T_R	50	100	150	200	250	300	350	400	450	500	550
100 -242	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
1K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
10K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
100K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.01	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
1M	1	1	1	1	1	1	1	1	1	1	1	1
	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05	<0.01	<0.05	<0.05	<0.05	<0.05

Table 5: CF544 package (without a lid on) parasitic capacitance (upper) in unit of pF and AC conductance (lower) in unit of µS between I/O1 and I/O2. I/O1 is connected to die attach pads and the seal ring. Contributions of gold wires have been subtracted.

T (°C) / f (Hz)	T_R	50	100	150	200	250	300	350	400	450	500	550
100	1	1	1	1	1	1	1	1	2	2	1	2
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
1K	1	1	1	1	1	1	1	1	1	1	2	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
10K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
100K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.05
1M	1	1	1	1	1	1	1	1	1	1	1	1
	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05

Table 6: CF544 package (without a lid on) parasitic capacitance (upper) in unit of pF and AC conductance (lower) in unit of µS between I/O2 and I/O3 of. Contributions of gold wires have been subtracted.

T (°C) / f (Hz)	T_R	50	100	150	200	250	300	350	400	450	500	550
100	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
1K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
10K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005	<0.005
100K	1	1	1	1	1	1	1	1	1	1	1	1
	<0.005	<0.005	<0.005	<0.005	<0.01	<0.005	<0.005	<0.005	<0.005	<0.01	<0.005	<0.005
1M	1	1	1	1	1	1	1	1	1	1	1	1
	<0.05	<0.05	<0.01	<0.01	<0.05	<0.05	<0.05	<0.05	<0.05	<0.01	<0.05	<0.05

rounded to 1pF. The parasitic capacitances between I/O1 and I/O2 in the temperature and frequency ranges are either less or rounded to 1pF. Compared with package with 16 pads, the maximum capacitance of I/O1-I/O2 is lower. The conductances of I/O1-I/O2 in entire test temperature and frequency ranges are all below 0.05 µS, it is lower than the maximum I/O1-I/O2 conductance of CF516 package with 16 pads. Both pad dimensions and spacing between pads of 16-pad package are the same as those of CF524 package; the differences of parasitic parameters may be due to the shorter distance between the die-attach pads and wire-bond pads of 16-pad package, as well as the larger metallized die-attach pad of 16-pad package.

Table 4 shows the parasitic parameters of I/O3-I/O4 of CF524 package, the parasitic parameters at high temperature are not much different from the data of I/O1-I/O2. Overall, the parasitic conductance tends to be higher at high temperature and high frequency ends, this is consistent with the dielectric loss data of HTCC alumina.

The DC resistances measured using a curve tracer (not shown) of both I/O1-I/O2 and I/O3-I/O4 in a range of ±15V bias at all test temperatures are 150 MΩ or above.

C. CF544 Package with 44 I/Os

Table 5 and 6 show the parasitic capacitance and conductance parameters of I/O1-I/O2 and I/O10-I/O11, respectively. I/O1 is connected to the package seal ring with wire-bonding, so it is connected to the ground trace as well (testing the GND power trace impact on neighboring I/Os AC parasitic effects). The maximum parasitic capacitance of I/O1-I/O2 at high temperature and low frequency ends is 2pF. It is slightly higher than the maximum capacitance of I/O10-I/O11 (this is a "normal" pair of neighboring pads) since I/O1 was connected to a larger metallization area. The parasitic conductance parameters of I/O1-I/O2 at 1 MHz and 450 °C-500 °C do not show difference from those of I/O10-I/O11 at the same temperature and frequency range may be due to error margin adopted.

The DC resistances measured using a curve tracer (not shown), of both I/O1-I/O2 and I/O10-I/O11 between ±15V bias at all test temperatures are 150 MΩ or above.

The metallization areas of power bus traces (Vdd pad, GND trace, and Vss trace) are much bigger compared with other pads, so the DC leakage currents between Vdd- and GND-pads as well as Vss- and GND-pads at elevated temperatures need to be examined. Figure 4 shows the CF544 package DC leakage currents compared with previously reported 32-I/O package. Leakage currents through CF544 power bus traces, Vdd-GND and Vss -GND, with 35V DC bias are not significantly any more than other isolated I/Os of (a different) CF544 package or previously measured leakage current of a 32-I/O package as effectively all data (at same

temperature) plot on top of each other, as shown in Figure 4.

V. Conclusion

Base on a previously tested Pt-HTTCC material system three kinds of new chip level packages have been designed and fabricated using commercial HTCC source for next generation of SiC high temperature ICs currently being developed at NASA GRC. These packages include one design for two of 5 mm x 5mm SiC ICs with 8-pad each, one design for one 2.4 mm x 2.4 mm SiC IC die with 24 pads, and one design for one 5 mm x 5mm SiC ICs with up to 72 bond-pads. The package with 44 I/Os provides consolidated DC power connection traces specially designed for a group of SiC ICs. AC dielectric properties of parallel RC parasitic parameters and DC insulation resistance between typical neighboring I/Os have been measured in a temperature range from room temperature to 550 °C at low frequencies. The parasitic capacitance tends to higher at high temperature and low frequency ends while parasitic conductance tends to be higher at high temperature high frequency ends. The maximum parasitic capacitance between neighboring I/Os of these packages is 2pF ± 0.5pF, and the maximum parasitic conductance of neighboring I/Os of these packages is less than 0.1μS (equivalent to resistance over 10MΩ) for small AC signals. The AC parasitic parameters, especially those of "normal" neighboring I/Os, of three packages are not much different from each other, this could be due to the same (or close) metallization pads dimensions and spacing between pads were used in three package designs and high effective error bars are used to present the parasitic data. The DC insulation resistance under ±15V bias of all measured I/O pairs of all three packages are above 150MΩ. The DC leakages between the power bus traces of CF544 package are also very low and ignorable. These parasitic parameters indicate that these Pt/HTCC packages can be used for many envisioned high temperature SiC ICs in development at NASA GRC. These chip level packages will be tested with SiC ICs in near future.

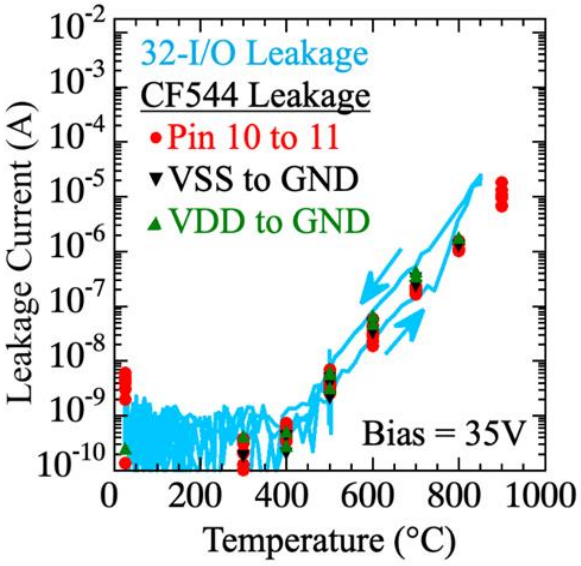

Figure 4: CF544 package DC leakage currents compared with previously reported 32-I/O package. Leakage currents through CF544 power bus traces are not significantly any more than other isolated I/Os as the data effectively all plot on top of each other.

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