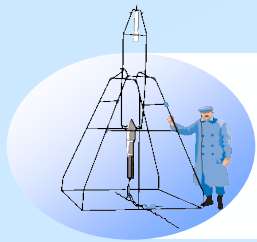


Development of a Transition-Edge Sensor Anti-Coincidence Detector for a Probe Class Mission

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Overview

- **Objective**

- The objective of this 1-year IRAD proposal is to mature the technical readiness level (TRL) of an anticoincidence detector for the Line Emission Mapper (LEM) probe class mission concept from TRL-3 to TRL-5.

- **Driver/ Need/ Benefit**

- LEM is an X-ray probe class mission concept to study galaxy evolution. The anti-co will detect and flag any events that could be confused with a science photon in the 0.2-2 keV signal band of LEM.
- The focal plane for LEM requires a larger anti-co detector than ATHENA and XRISM while maintaining or exceeding their high-speed response, presenting a challenge for claiming technical readiness at the time of the announcement of opportunity (AO).
- The payoff is a leading role for GSFC in a window-opening X-ray spectroscopy mission that will launch early in the next decade.

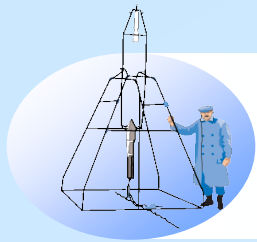




- **Summarized Description**

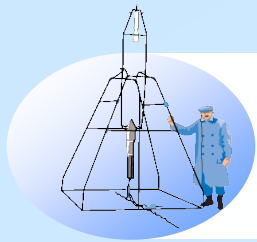
- Our combination of fabrication and testing leverage the ATHENA program and knowledge of the earlier anti-co prototyping effort.
- We have tasks for fabrication, test, and modelling efforts that develop in parallel and then converge to complete TRL-5 requirements that we have identified.
- Device fabrication, testing, and other needed verifications will be completed in time for an anticipated probe AO towards the end of 2023.





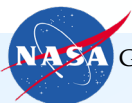
Accomplishments

- **Accomplishments**
 - Masks were drawn and printed
 - Modeling was done to determine the target heater resistance using COMSOL.
 - First iteration of fullscale anti-co prototype fabrication – 1st device yielded.
 - COMSOL vibration modelling of prototype anti-co is underway.
- **Significance of the results**
 - Scalability to full size prototype (4 cm scale) needed for TRL-5. The fabrication uses standard Athena processing and Al fin deposition.
 - Heater allows local control of substrate temperature independently of the main ADR bath temperature.



Accomplishments cont'd

- **Future plans for the remainder of the year**
 - Testing of first iteration prototype.
 - Start second iteration of prototype fabrication.
 - Testing on full-scale anti-co prototype.
- Started a collaboration with Stanford University and Northwestern University – using tungsten (has been demonstrate to work) TES instead of Mo/Au. This could be used to demonstrate TRL-5 sooner in case our Mo/Au doesn't work in time for the proposal.

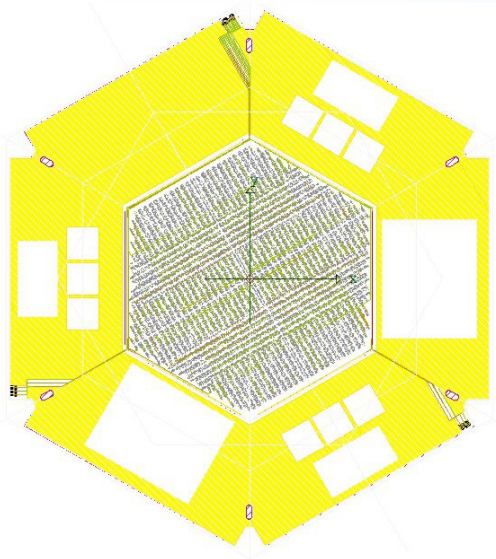




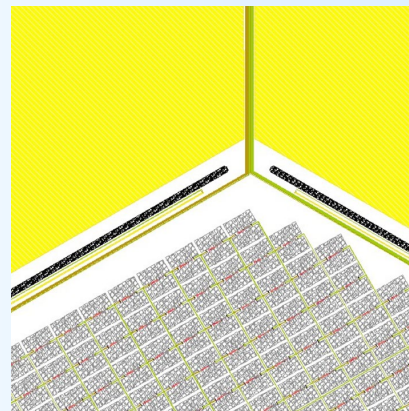
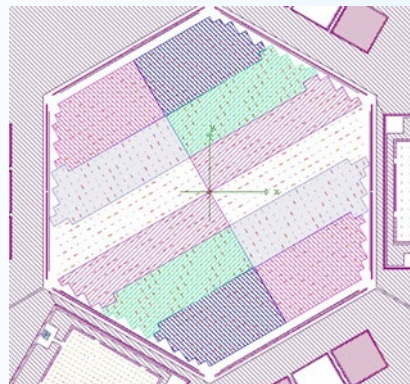
Milestones and Deliverables

MILESTONE 1: Masks were drawn and printed.

Full chip CAD drawing



Shaded regions show areas covered by parallel TES with common bias lines



Closeup on one corner of the inner hex shows the basic components of the device

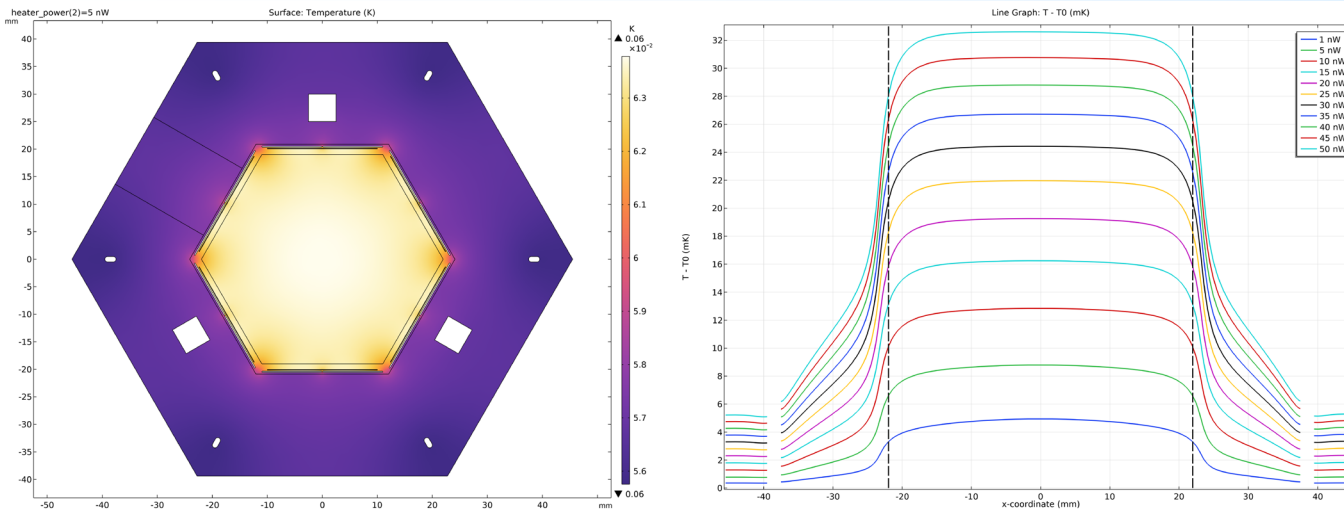
Closeup of a unit cell



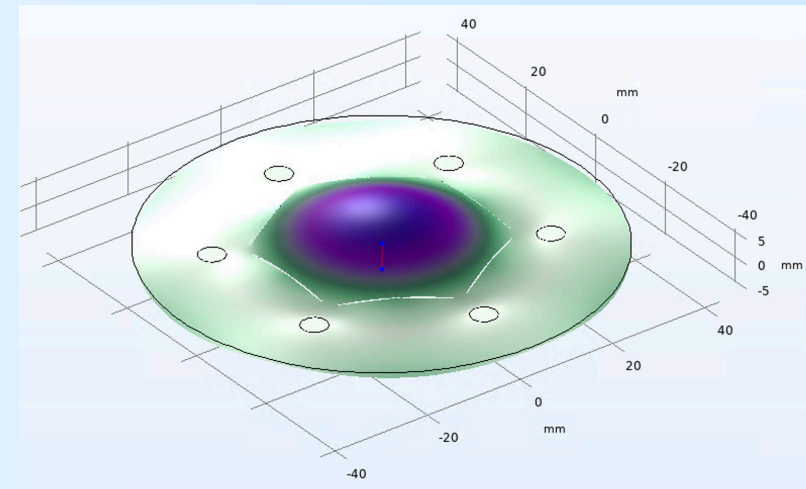


Milestones and Deliverables cont'd

MILESTONE 2: COMSOL modelling was done to determine the target heater resistance and the first vibration eigenfrequency.

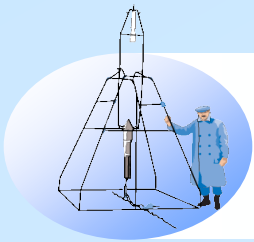


The change in temperature from T_0 (55mK) vs the x position along a line at $y = 0$ for the full wafer (i.e. ± 4.5 cm). The temperature rise at 50 nW input power is ~ 32 mK for most of TES array, so that is up to ~ 87 mK.



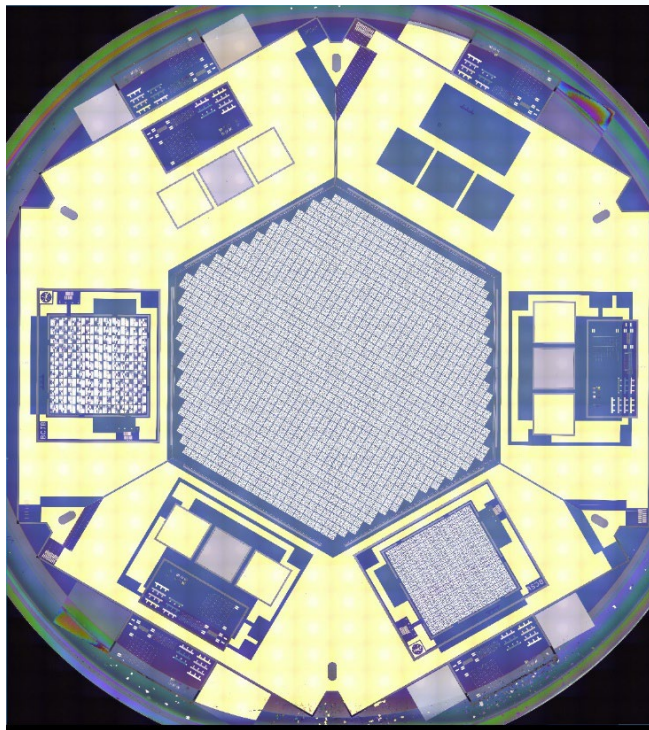
Approximate LEM anti-co with 1st eigen frequency of 1.2 kHz

Heater allows local control of substrate temperature independently of the main ADR bath temperature.

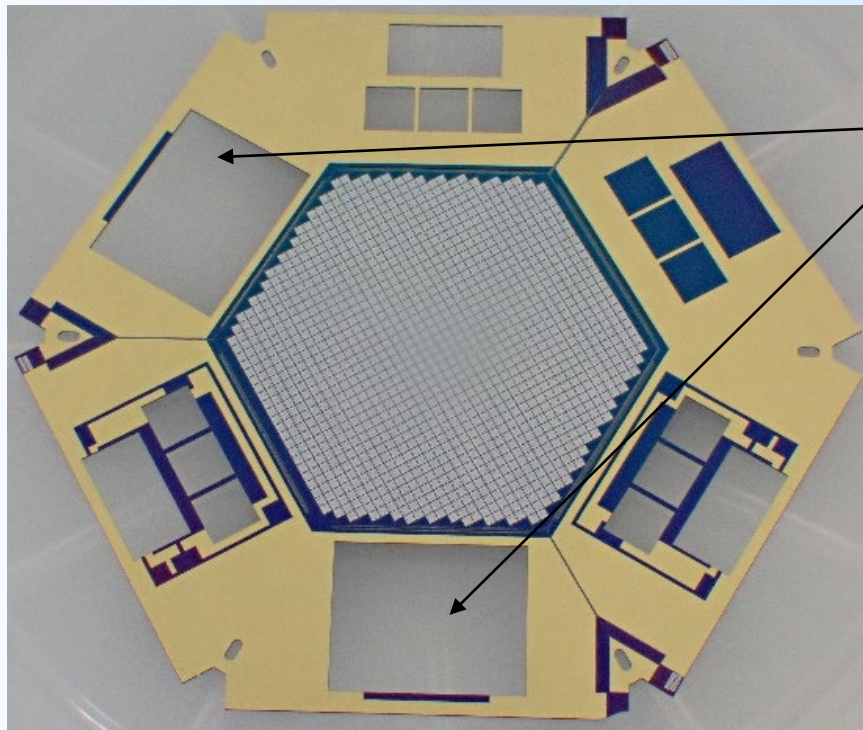


Milestones and Deliverables cont'd

MILESTONE 3: First iteration of fullscale anti-co prototype fabrication – 1st device yielded.



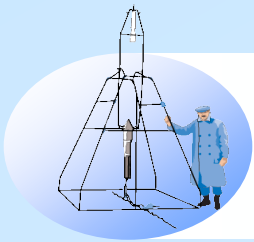
Wafer during fabrication.



Antico prototype delivered for testing

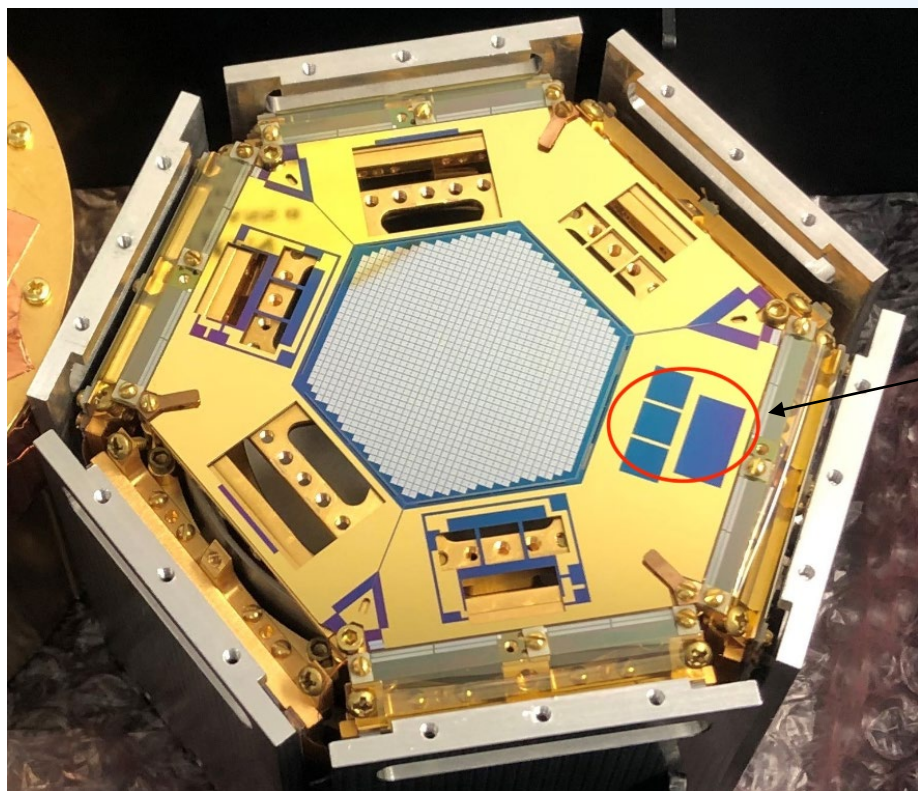
Interior chips yielded for process monitoring.

Scalability to full size prototype (4 cm scale) needed for TRL-5. The fabrication uses standard Athena processing and Al fin deposition.



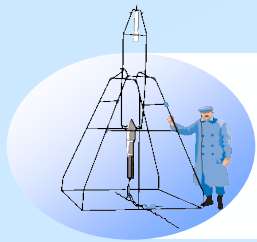
Milestones and Deliverables cont'd

- **ISSUES:**



Needs another
cut out here

- Excessive back etch – fixture for securing the wafer during etching block the areas that require etching, so the wafer had to be rotated intermittently to yield, causing overetching.
- The 1st yielded chip is not fully compatible with the testing set-up.
- We also meant to investigate different internal segmentation.



Future / Next Steps

- **What potential customers or follow-on funding sources are there for this technology?**
 - LEM proposal submission will be on September 2023, followed by Phase A study (March 2024 - April 2025).
 - We anticipate pursuing additional IRAD support for FY24, to drive the technology to TRL 6 – critical to Phase A study.
 - We expect future funds from Phase B study.
- **How should GSFC's investment in your technology be leveraged to further improve our competitive posture in this area?**
 - This antico is specific for LEM, but we can learn enough physics (threshold energy, response time and reset time) to develop antico for other future missions.