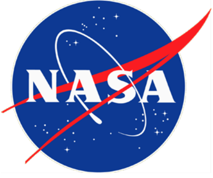

NASA Electronic Parts and Packaging (NEPP) Program

Updates on Capacitors' Tasks

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Abstract

This presentation gives an overview of the current status for 2023 NEPP tasks:

- Guidelines for Screening and Qualification of Polymer Tantalum Capacitors;
- Evaluation of Polymer Multilayer (NanoLam) Capacitors for Space Applications;
- New Passives for Space: Hermetic Al Electrolytic Capacitors.

List of Acronyms

AC	Alternative Current	**ESR**	Equivalent Series Resistance
ACC	Anomalous Charging Current	**HALT**	Highly Accelerated Life Testing
AEC	Aluminum Electrolytic Capacitor	**HSHLD**	High Sensitivity Helium Leak Detection
AF	Acceleration Factor	**HTS**	High Temperature Storage
AT	Anomalous Transient	**LT**	Life Test
CVCM	Collected Volatile Condensable Materials	**MEAL**	Mission, Environment, Applications and Lifetime
DC	Direct Current	**PTC**	Polymer Tantalum Capacitor
DF	Dissipation Factor	**S&Q**	Screening and Qualification
DLA	Defense Logistics Agency	**SAE**	Society of American Engineers
DWG	Drawing	**SCD**	Source Control Drawing
NLE	NanoLam Element	**TEC**	Tantalum Electrolytic Capacitor

Outline

I. Guidelines for Screening and Qualification of PTCs:
  - A blueprint for SCD
  - Derating

II. Evaluation of Polymer Multilayer (NanoLam) Capacitors for Space Applications
  - Specifics of the NanoLam technology
  - Degradation processes
  - Reliability assessment

III. New Passives for Space: Hermetic Al Electrolytic Capacitors
  - Perspectives for space applications
  - Reliability issues:
    - HALT
    - Long-term storage
    - Hermeticity

Guidelines for PTCs

- The document explains specifics of S&Q procedures for PTCs.
- The requirements are presented in Tables compliant with NASA-STD-8739.11.
- The guidelines are currently discussed in the SAE Polymer Tantalum Capacitor User Forum.
- The document allows flexibility based on MEAL and can be used as a blueprint for SCD.

Guidelines for Screening, Lot Acceptance, and Derating for Polymer Tantalum Capacitors

1. Scope.

These guidelines have been developed for NASA space projects that are planning to use new technology hermetic and chip polymer cathode tantalum capacitors. Polymer Tantalum Capacitors (PTC) selected from MIL-PRF-32700, automotive grade (AEC-Q200) parts, or COTS+ (hi-rel COTS) capacitors should be screened and qualified as suggested in Tables 1-3 and derated per section 9 below. Screening and lot acceptance tests that were carried out for a lot that is intended for flight as a part of the manufacturing process do not need to be repeated.

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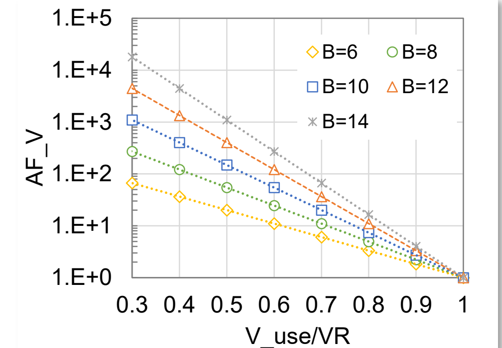
Guidelines: Voltage Derating

- Two approaches: rule-based and knowledge-based.
- Depending on the project's MEAL, specifics of the part performance, confidence in information regarding models for possible degradation and failure mechanisms, the derating requirements can be reevaluated.

$$AF_V = exp[B \times (u_2 - u_1)]$$

¤	Chip·PTCs¤	Hermetic·PTCs¤
Maximum·Operating·Voltage········1/¤	0.6VR¤	0.6VR¤
Maximum·Case·Temperature········2/¤	T_{c_max}·=·85·°C¤	T_{c_max}·=·105·°C¤
Maximum·Surge·Current···············3/¤	I_{max}·=·VR/(1+ESR_{spec})¤	I_{max}·=·VR/(1+ESR_{spec})¤
Maximum·Ripple·Current··············4/¤	T_{case}·-·T_{amb}·=·10·°C¤	T_{case}·-·T_{amb}·=·10·°C¤



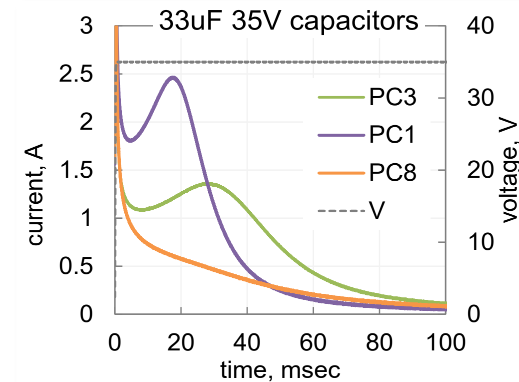
1/ V_{op} is limited to further increase reliability during long-term DC biased operations, reduce surge currents, and ACC during power-on processes.

The reliability gain (decrease of the failure rate or increase of useful life) caused by voltage derating can be calculated.

Conservative estimations can be made assuming $B = 7$.

Guidelines: Derating for ACC

¤	Chip·PTCs¤	Hermetic·PTCs¤
Maximum·Operating·Voltage·······1/¤	0.6VR¤	0.6VR¤
Maximum·Case·Temperature·······2/¤	$T_{c,max}$ = 85 °C¤	$T_{c,max}$ = 105 °C¤
Maximum·Surge·Current··············3/¤	I_{max} = VR/(1+ESR_{spec})¤	I_{max} = VR/(1+ESR_{spec})¤
Maximum·Ripple·Current·············4/¤	T_{case} - T_{amb} = 10 °C¤	T_{case} - T_{amb} = 10 °C¤



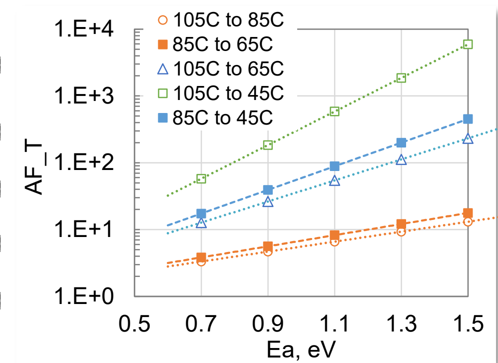
3.3.1. Power Surge Testing procedure

Preconditioning: 125 °C for 24 hour; testing within 8 hours.
Screening: VR should be applied from a PS capable of increasing voltage across the part in less than 1 msec at limiting currents of ≥ 10 A. A PST cycle includes 200 msec at VR followed by 200 msec at 0V.
LAT: Same + transient currents and voltages should be monitored during power on periods to calculate the dissipated energy, and measure currents at 10 msec after pulse application. The dissipated power is calculated by digital integration till the moment when the currents decrease to 0.01A.

- ✓ Three ACC levels: high (I_{10} ≥ 1A or U_d ≥ 1J), low (I_{10} < 0.1A or U_d < 0.1J), and medium.
- ✓ ACC decreases with voltage exponentially → Voltage derating is the most powerful tool to reduce ACC.
- ✓ The necessary voltage derating depends on ACC level and MEAL.

Guidelines: Temperature Derating

	Chip PTCs	Hermetic PTCs
Maximum Operating Voltage 1/	0.6VR	0.6VR
Maximum Case Temperature 2/	T_{c_max} = 85 °C	T_{c_max} = 105 °C
Maximum Surge Current 3/	I_{max} = VR/(1+ESR_{spec})	I_{max} = VR/(1+ESR_{spec})
Maximum Ripple Current 4/	T_{case} - T_{amb} = 10 °C	T_{case} - T_{amb} = 10 °C



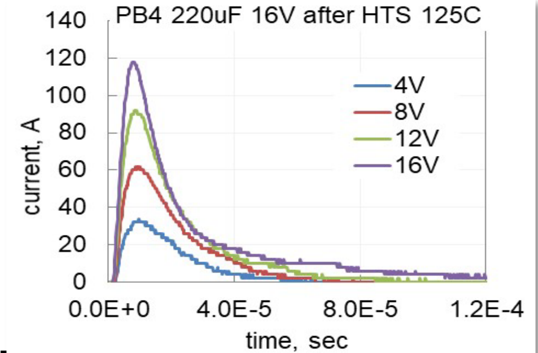
2/ T_{max} is limited to prevent thermo-oxidative degradation of conductive polymers and to increase reliability under biased operations. The reliability gain of the temperature decrease can be calculated at different activation energies. Conservative estimations can be made assuming $E_a = 0.7$ eV.

4/ Capacitors operating at high ripple currents might have reduced reliability due to self-heating. For this reason, the self-heating is recommended to limit to 10 °C for parts operating at $T_{amb} \geq T_{c_max}$ -10. This requirement can be relaxed at $T_{amb} < T_{c_max}$ -10. Note, that temperature rising in vacuum can be larger than in air environments.

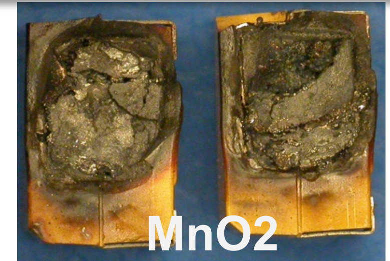
The temperature rise can be estimated as $\Delta T = I^2_{ripple} \times ESR \times R_\theta$, where I_{ripple} is the ripple current and R_θ is the thermal resistance of the part that depends on the size of the part, mounting conditions, and environments. The value of ΔT can be determined experimentally, e.g. using an IR camera.

Guidelines: Derating of Surge Currents

¤	Chip PTCs	Hermetic PTCs
Maximum Operating Voltage 1/	0.6VR	0.6VR
Maximum Case Temperature 2/	$T_{c,max}$ = 85 °C	$T_{c,max}$ = 105 °C
Maximum Surge Current 3/	I_{max} = VR/(1+ESR_{spec})	I_{max} = VR/(1+ESR_{spec})
Maximum Ripple Current 4/	T_{case} - T_{amb} = 10 °C	T_{case} - T_{amb} = 10 °C



- History of requirements for circuit resistance:
  - In the 1960s: 3 Ω per each volt of operating voltage.
  - By the 1980s: 1 Ω per each volt.
  - From the 1990s: 0.1 Ω per volt or 1 ohm, whichever is greater.
  - EEE-INST-002, 2003: The effective series resistance shall be at least 0.1 ohms per volt or 1 ohm, whichever is greater, for L2, and at least 0.3 ohms per volt or 1 ohm whichever is greater, for L1 applications.
  - NASA-STD-8739.11 - Surge current shall be limited to $V_{rated}/(1+ESR_{cap})$, where V_{rated} = V_{rated} at 85°C and ESR_{cap} = ESR_{max} (?)

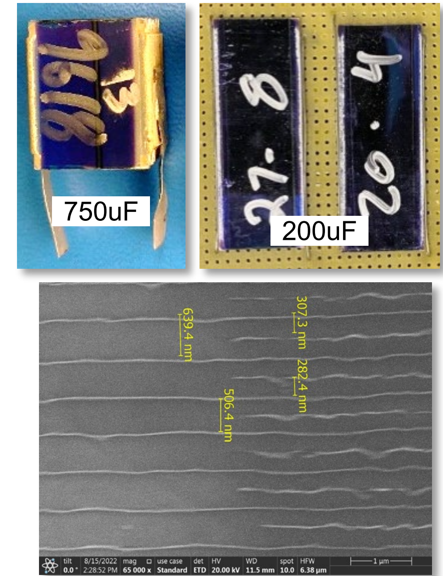


- The guidelines suggest simple assessments to assure that surge currents during applications do not exceed currents during screening: $I_{appl.} < I_{test}$

NanoLam Capacitors: Design, Technology

- Acrylate-based vapor deposited by e-beam films and Al metallization in a single vacuum process.
- Technology is adaptable for a wide range of specifications: *C* up to 1 mF, voltages up to 450V and T_{op} > 125C.
- Devices are intended for applications in various space power systems.
- NanoLam capacitors may be a replacement for polymer film, electrolytic, and stacked ceramic capacitors saving significant volume and mass.

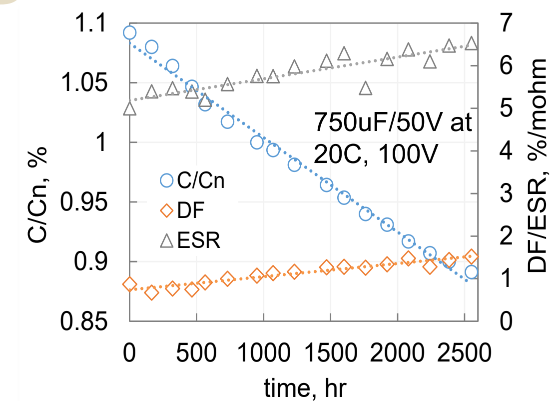
Engineering units of 50V NL capacitors, NLE

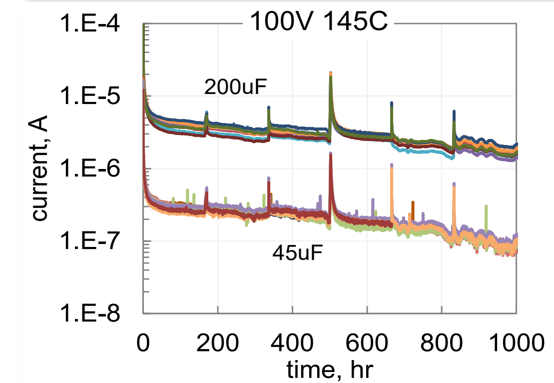


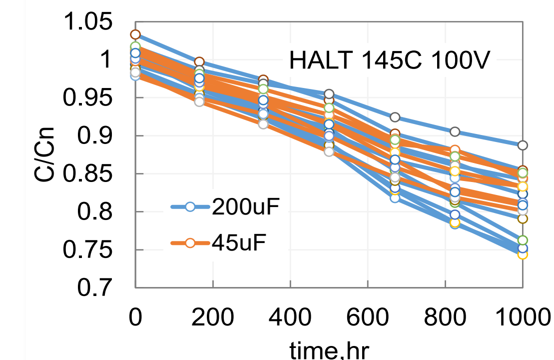
✓ <u>The purpose of this task:</u>
- evaluation of the efficiency of self-healing;
- development of methods for reliability prediction;
- assessments of degradation processes, acceleration factors, and failure modes.

NanoLam Capacitors: Degradation

- Degradation is due to self-healing processes that cause a decrease of C and increase of DF and ESR.
- Soft parametric failures rather than catastrophic short or open circuit conditions.
- Major problems with reliability assessment/prediction:
  - Selection of sensitive characteristics and levels of stress.
  - Effect of moisture on degradation processes.
- Preliminary results of NLE testing:
  - Degradation process can be characterized by the rate of capacitance decrease.
  - No catastrophic failures during HALT at 145C 2VR.
  - Currents are consistently decreasing with time of HALT.
  - A relatively small spread of capacitance degradation rates.
- Moisture can affect the rate of degradation and cause catastrophic failures.



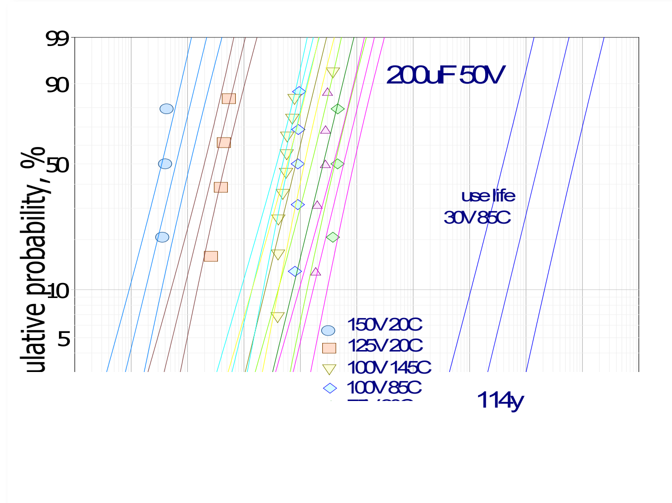




NanoLam Capacitors: Reliability

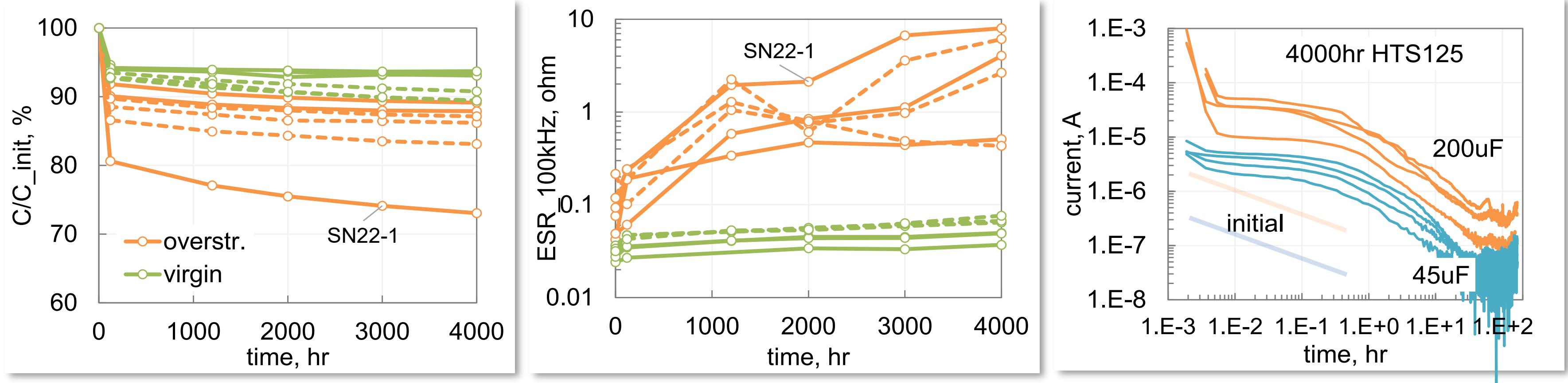
- A power law, $AF_V \sim (V_{op}/VR)^n$, is typically used to describe voltage dependence of the degradation rate.
- Temperature effect is described by either Arrhenius law, $AF_T \sim exp(-E_a/k(1/T_1-1/T_2))$, or exponential function, $AF_T \sim 2^{((T1-T2)/\Delta T)}$. [$\Delta T$ =10C → E_a= 0.68eV]
- A wide range of n *(1.8 – 9.4)* and E_a (0.08-1.5eV) for different polymer materials and part types requires assessments of AFs for NL capacitors.

Parametric TTFs during HALT were approximated using a general Weibull log-linear model



- ✓ Preliminary results indicate high values of n (8.7 - 9.5) and low E_a (<~0.1eV).
- ✓ Useful life for 50V elements exceeds 100 years at 30V and 85C.

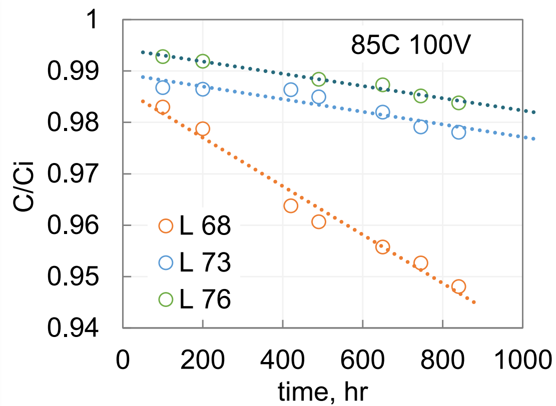
NanoLam Capacitors: HTS



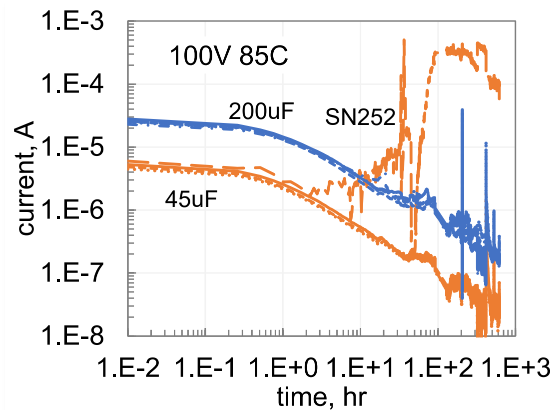
- ✓ HTS results in degradation for overstressed (150V, 28hr) parts, but no significant changes during 4000 hours at 125C for virgin elements.
- ✓ Degradation of leakage currents is likely reversible and caused by the same mechanism as in other types of capacitors.

NanoLam Capacitors: Problems

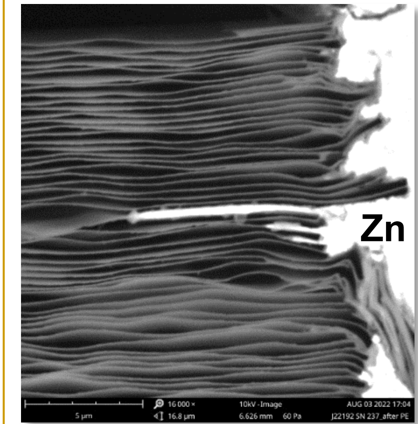
Lot-to-lot variations



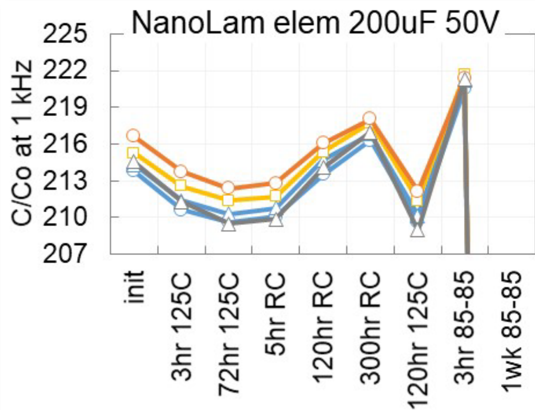
Anomalies in leakage currents

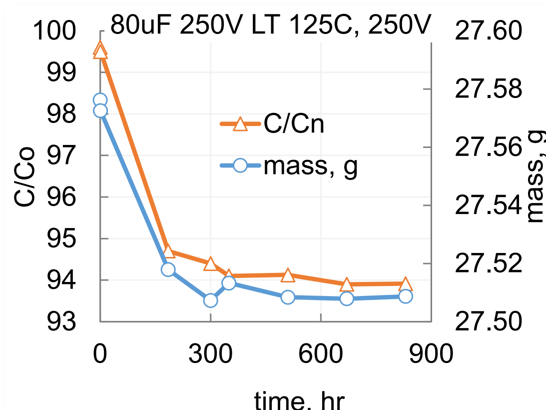


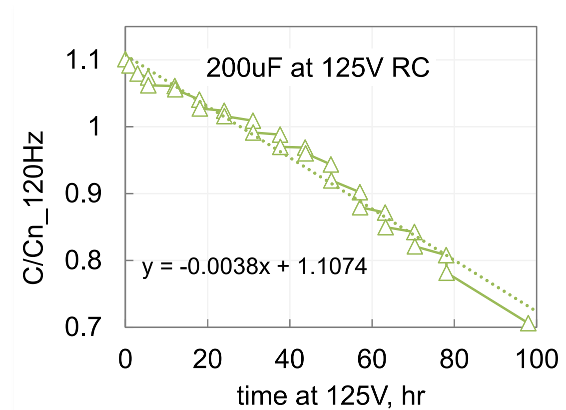
Use of Zinc



Effect of moisture







To be presented by Alexander Teverovsky at the NEPP Electronics Technology Workshop (ETW), Greenbelt, MD, June 12-15, 2023

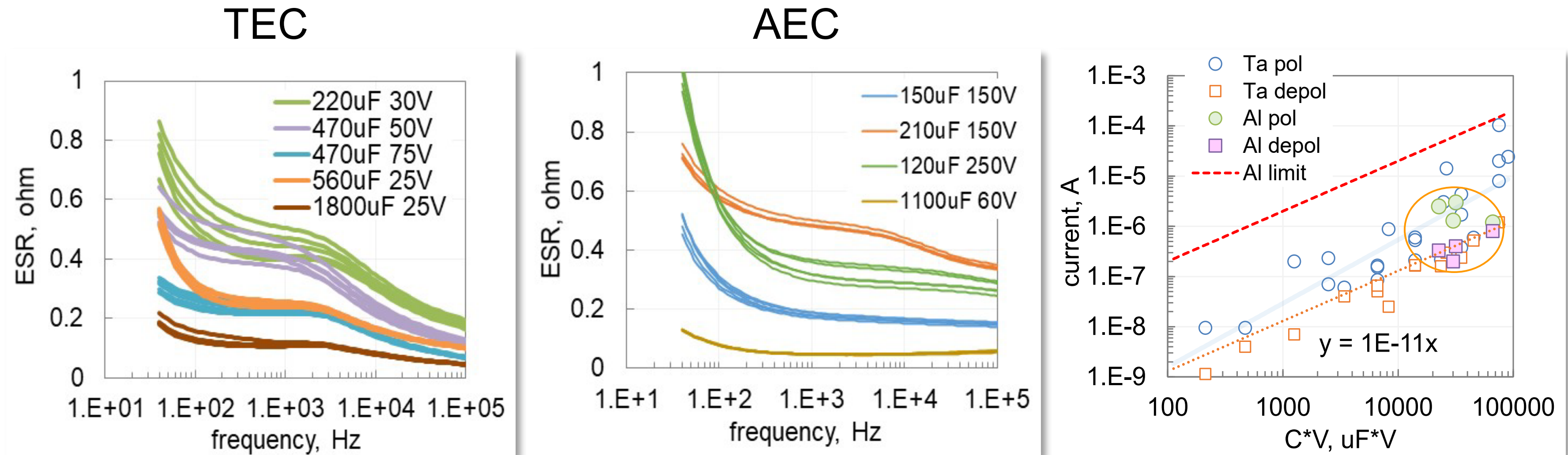
Backup

Hermetic Aluminum Electrolytic Capacitors

- Benefits of hermetic AEC compared to TEC:
  - Availability to higher voltages: capacitance up to 3200µF, voltage up to 250V.
  - no or reverse derating (?).
- Hermetic AEC are used in hi-rel applications since 1990s (DLA DWG #05019 since 2006).
- Reliability models for non-hermetic AEC might be not applicable.
- Reliability concerns:
  - Leakage currents and gas generation during operation.
  - Degradation during long-term storage (oxide dissolving?).
  - Hermeticity initially and after environmental stresses.

- ✓ Considering successful use of TEC in space systems, the purpose of this task is to compare quality of AEC and TEC.
- ✓ Comparison includes assessments of hermeticity, AC and DC characteristics, degradation processes during HALT and HTS.

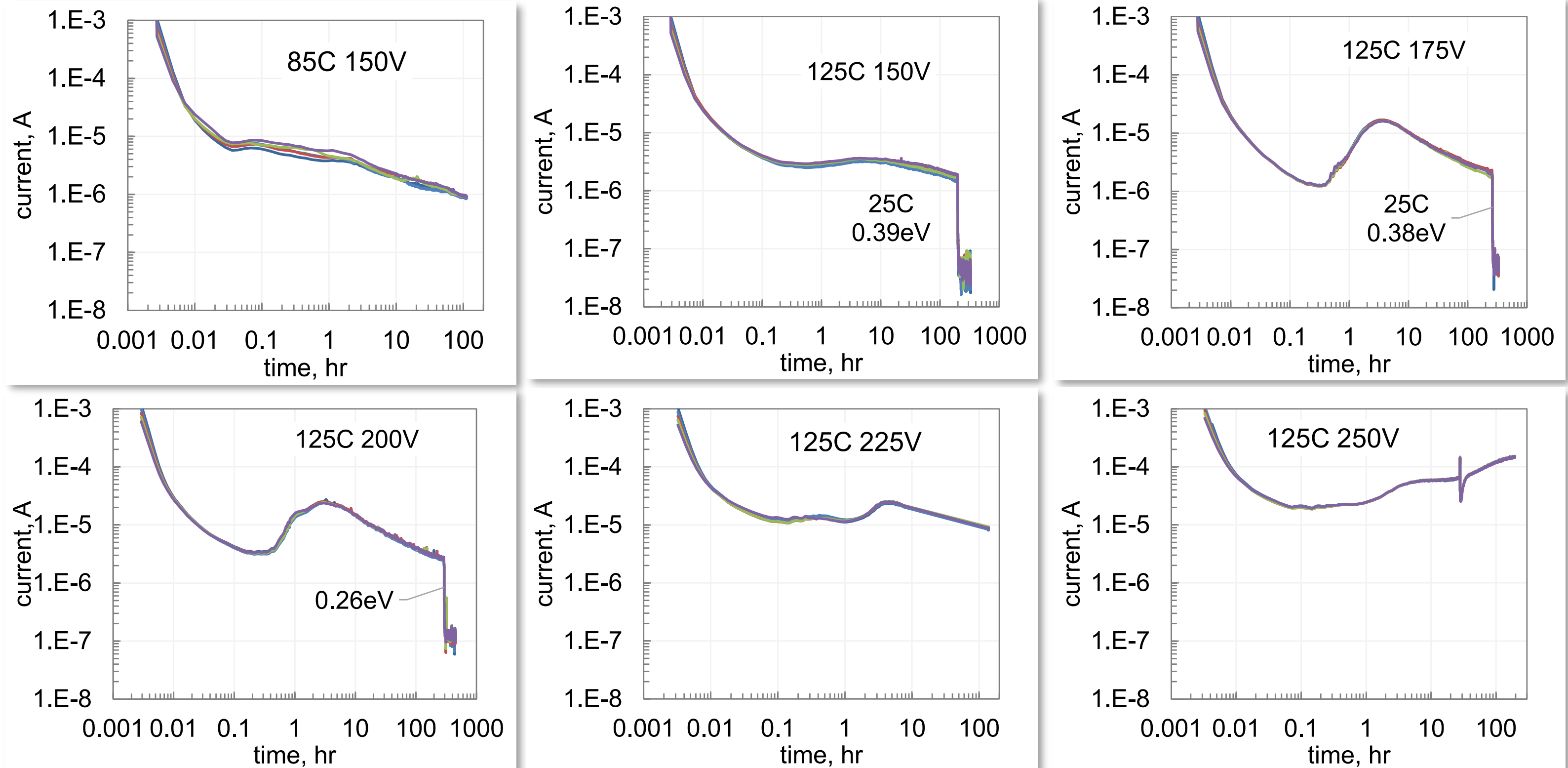
Characteristics of AEC and TEC



✓ Hermetically sealed tantalum and aluminum capacitors have similar frequency dependencies of ESR and similar levels of polarization and depolarization currents.

Effect of HALT

Leakage currents in 210uF 150V AEC during step-stress HALT



- ✓ No degradation of AC characteristics and decrease of post-HALT leakage currents.
- ✓ Humps on I-t curves are indications of oxide growth → easy to reform.

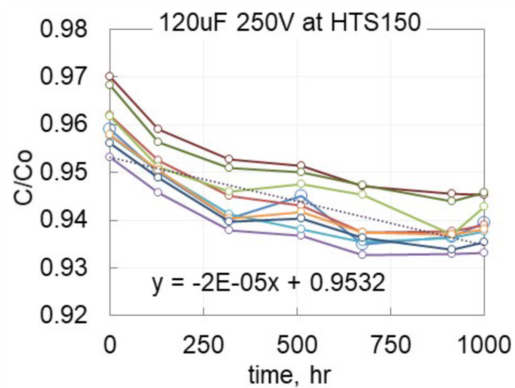
Effect of HALT, Cont'd

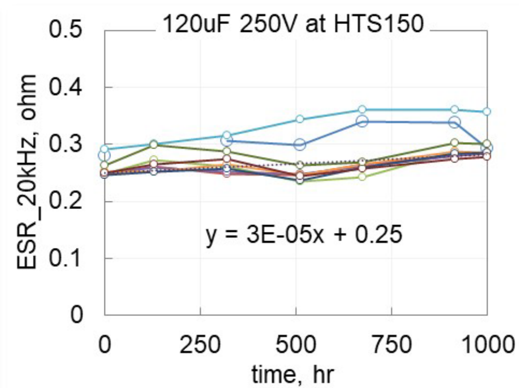
One out of 5 samples had electrolyte leak after 200hr HALT at 125C 225V

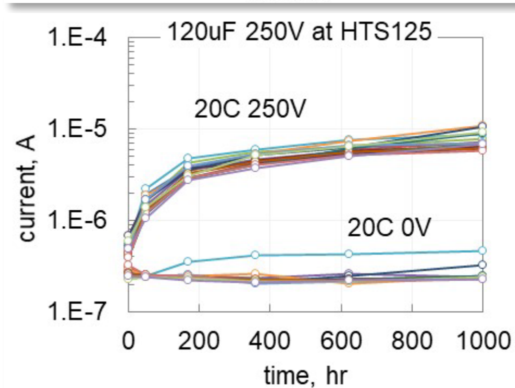
- ✓ HALT might not degrade electrical characteristics of hermetic AECs but result in gas generation and cracking at the solder joints.

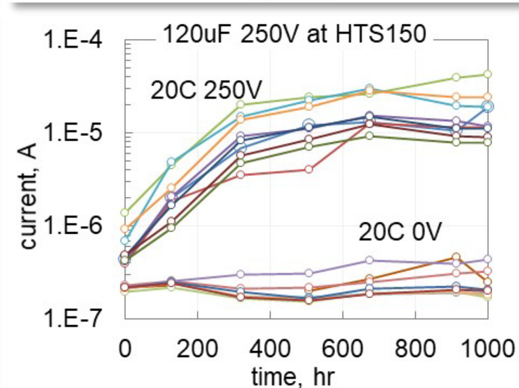
Effect of HTS

- Degradation in regular AEC during HTS is commonly explained by evaporation of electrolyte and dissolving of the oxide.
- Existing requirements for the shelf life (100hr at 85C per MIL-PRF-62G; 500hr at 125C per DWD#05019; 1000hr/125C per AEC-Q200) do not guarantee reliability of the parts after long-term storage.





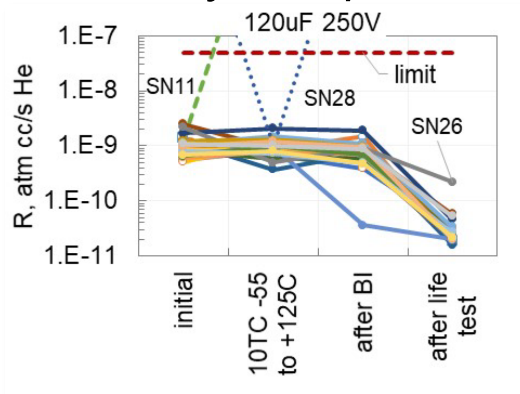




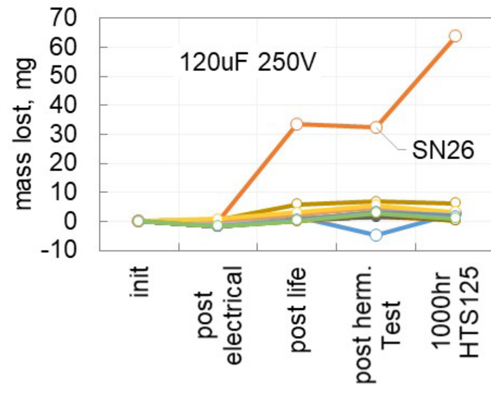
- ✓ Leakage currents are stabilizing with time.
- ✓ Decrease of C rules out the dissolving model.
- ✓ Comparative analysis of degradation of leakage currents in AEC and TEC indicate similar mechanisms that can be explained by the presence of deep traps.

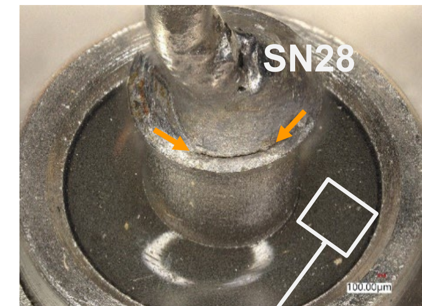
Hermeticity and Evaporation of Electrolyte

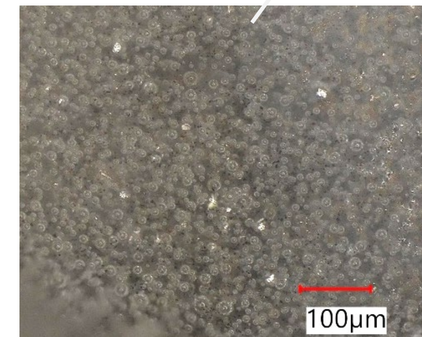
Hermeticity leak per HSHLD

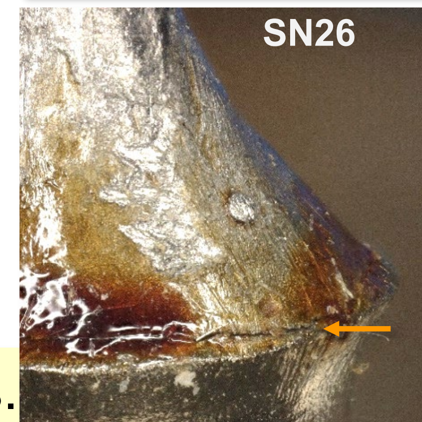


Mass variations









* BI: 96hr 85C 250V, LT: 125C 1000hr 250V.

** SN11 had no defects; SN 28 and SN26 had cracks.

- ❑ Problem with He testers: sorption in porous glass.
- ❑ How much electrolyte can be lost?
  - Up to 100 mg does not cause parametric failures.
  - Formal outgassing requirements: CVCM=0.1%M=28mg

✓ Helium testing might result in false gross leak failures.

✓ Hermeticity can be compromised in the process of operation/storage.

✓ More analysis is necessary to select adequate method of testing and requirements for hermeticity assurance.

Future Work on Capacitors

- Polymer Tantalum Capacitors
  - Discussions on S&Q procedures including metrics for ACC and derating requirements;
  - Development of SCD/MIL spec for space (?)
- NanoLam Capacitors
  - Effect of moisture;
  - Effect of radiation;
  - Post-stress degradation of leakage currents;
  - Evaluation of assembled units (?)
  - Reliability acceleration factors;
  - Suggestions for S&Q procedures (?)
- Hermetic Aluminum Electrolytic Capacitors
  - Methods for hermeticity assessments
  - Effect of random vibration
  - Degradation during High Temperature Storage
  - Suggestions for S&Q procedures (?)