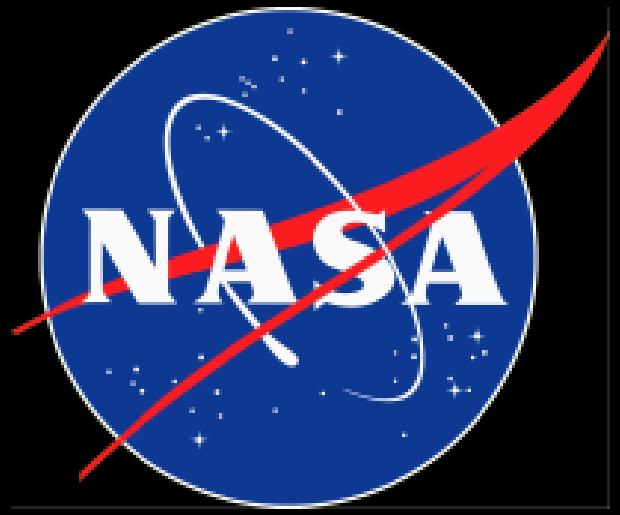

Update on NEPP SEE FPGA Test and Analysis Featuring:

The Lattice Avant TSMC 16 nm FinFet, The Xilinx TSMC 7nm Versal AIE Core, and Fluence to Failure Applied Methodologies

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Acronyms

Acronym	Description	Acronym	Description	Acronym	Description
A	Current: Amps	lb	lower bound	RPP	Rectangular parallelpiped
AI	Artificial Intelligence	LBNL	Lawrence Berkeley National Laboratory	SEE	single event effect
AIE	Artificial Intelligence Engine	LET	linear event transfer	SEF	single event failure
BIST	Built in self test	LUT	Look Up Table	SEFI	single event functional interrupt
BRAM	embedded static random-access memory	LVDS	low Voltage Differential Signaling	SERDES	serializer -deserializer
CCIX	Interconnect consortium	MFTF	mean fluence to failure	SET	single event transient
CLB	configurable logic block	MIPI	mobile industry processor interface	SEU	single even upset
CMOS	Complementary MOSFET	n	number of events	SLS	Space Launch System
CXL	Compute express link	NoC	network on chip	SoC	system on chip
DDR4	Double Data Rate 4 Synchronous Dynamic Random-Access Memory	P	probability	SRAM	static random access memory
		PLL	Phase locked loop		
DFF	Flip-flop	PCIe	Peripheral Component Interconnect Express	T	number of experiments
DSP	Digital signal processor	PL	FPGA programmable logic	ub	upper bound
DUT	device under test	PS	FPGA processing block	wDMA	Direct memory access
FPGA	Field programmable gate array	P_{effect}	Probability an event can exist through system topology	μ	mean
FTF	fluence to failure	P_{gen}	Probability an event can occur from ionization	σ	cross section
G	Giga	$P_{observe}$	Probability an event can can be observed	Φ	fluence
Gb/s	Gigabits/second	REAG	Radiation Effects and Analysis Group	Qcoll	Collection charge
GPIO	general purpose input/output	RF	radio frequency	Qcrit	Critical charge
GR	global route	RHA	Radiation Hardness Assurance	twidth	Transient width
HBM	High Bandwidth Memory	Rpw	Parasitic resistor p-well	Vac	Voltage anode-cathode
I2C	I squared C bus	Rnw	Parasitic resistor n-well	Vdd	Supply voltage
I/O	input/output	RMA	Representative Mission Application	Vss	ground
IP	Intellectual property	SR	Shift register	Vccint	Internal voltage domain

Reevaluating NEPP Role in SoC/FPGA SEE Data Collection

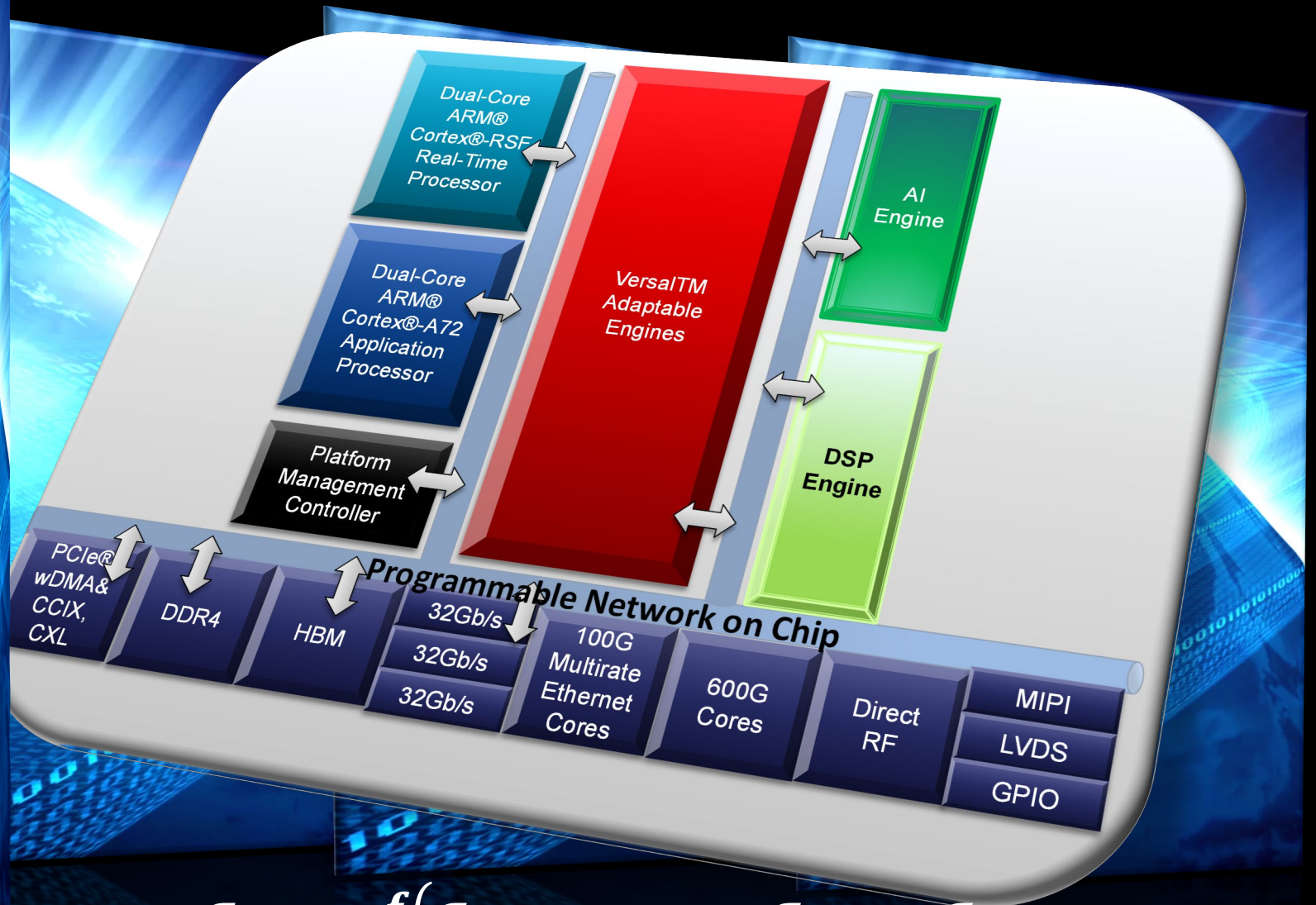
RMA: Representative mission application
SLS : Space Launch system

- Traditionally [1]:
  - **First look**:
    - Rough idea of device behavior.
    - Helps to steer other data collection campaigns.
  - **Generic data set:**
    - Mostly fine-grain test structures: (configuration, shift registers, embedded RAM, math-blocks, counters, etc.)
    - Some mid-grain test structures: (SERDES, IP blocks, etc.)
    - Used for (piecemeal) RMA extrapolation.
- **Test-as-you-fly:**
  - First campaign in 2010 for NASA SLS Program… FPGA embedded processor SEE fluence to failure (FTF).
  - Not usually under NEPP because it is generally program/mission driven.

Limited beam time and advanced technologies… time to reevaluate test methods and generic data sets.

[1]Melanie Berg et. al, "FPGA SEU Radiation Test Guidelines:" https://nepp.nasa.gov/files/23779/fpga_radiation_test_guidelines_2012.pdf

Challenges for SEE Test and Analysis of New Generation SoC/FPGA



- Cannot test every fine grain (basic mechanism).
- Not all basic mechanisms are linearly extrapolatable (topology matters).
- SoCs contain significant amount of embedded circuitry (hidden logic).
- Hidden circuits are complex and require complex test methods.
- Increased focus on $\sigma_{HiddenLogic}$

$$\sigma_{SEF} = f\left(\sigma_{configuration}, \sigma_{BRAM}, \sigma_{functionalLogic}, \sigma_{HiddenLogic}\right)$$

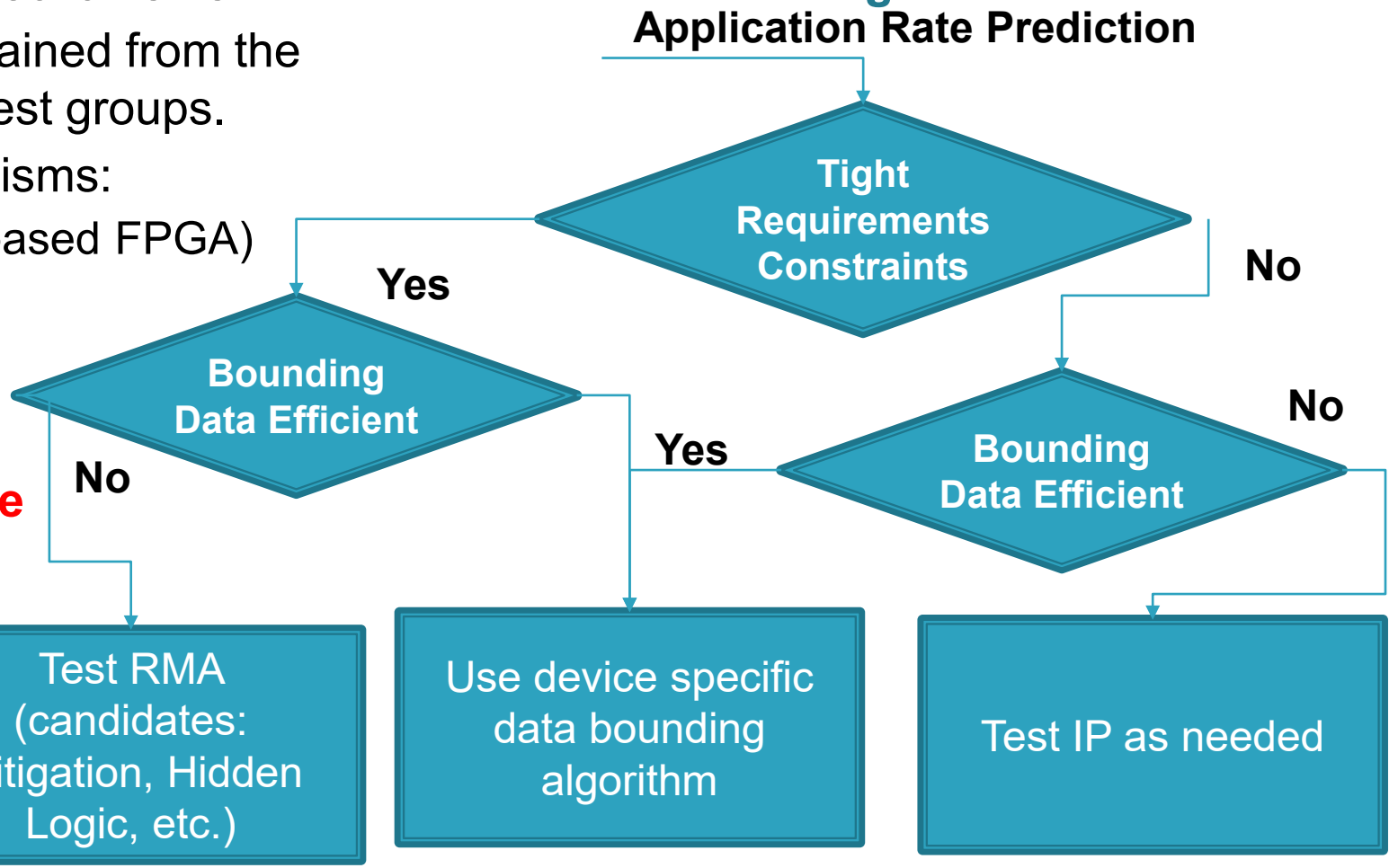
NEPP Meeting SoC/FPGA SEE Challenge

- Redefine SoC/FPGA intent:
  - No longer a study for technology nodes.
  - The goal is to obtain data that can be used/extrapolated to mission applications for failure rate analysis.
- Redefine generic data sets for today's SoC/FPGA devices:
  - **Enhance bounding metrics** and application.
  - **Increase course-grain** and mid-grain test structure experiments.
- Streamline test campaigns … reduce number of test trips (reduce facility time):
  - Reusability
  - Automation
  - Preparation
- Research alternate methods for SEE prediction:
  - **Low Level:** Other groups are studying alternate methods for basic mechanisms/discrete components.
  - **High Level:** Other groups are studying system modeling techniques (MBSE).
  - Neither studies have the details required for SoC/FPGA failure analysis**… SoC/FPGA require their own study for SEE prediction and behavioral analysis.**

Bounding versus Extrapolation

- Error rate bounding requires knowledge (and proof) of dominant SEE failure mechanisms.
- Bounding information can be obtained from the manufacturer or other radiation test groups.
- Most common bounding mechanisms:
  - Configuration memory (SRAM-based FPGA)
  - Flip-flops (Flash-based FPGA)
- **Linear transformation**
- **No concept of topology**
- **Expected to be an overestimate**

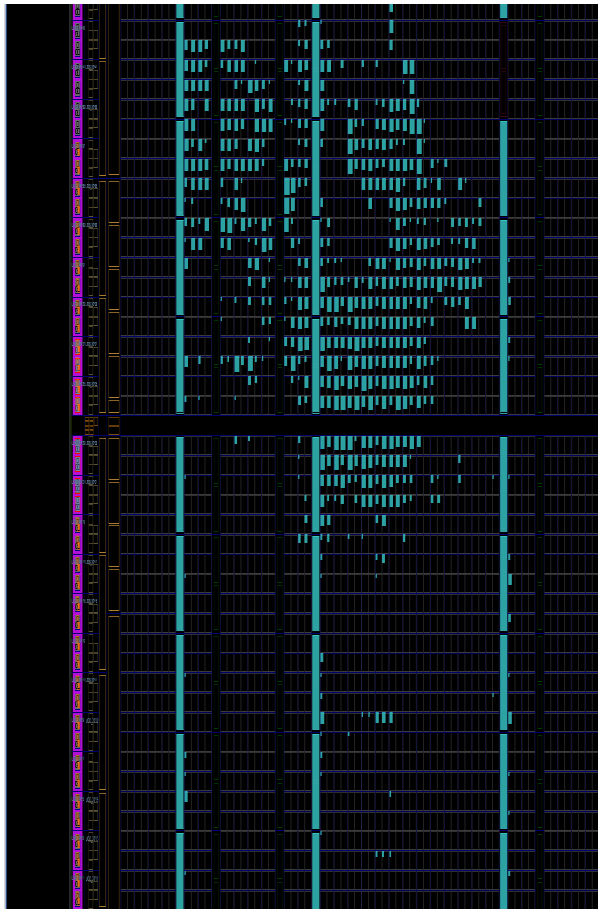
How does bounding fit into RHA?



$$Error\ Rate = \#(Dominant\_mechanism) \times error\_rate(Dominant\_mechanism)$$

An Example of When to Use Homogeneous Testing and Linear Bounding

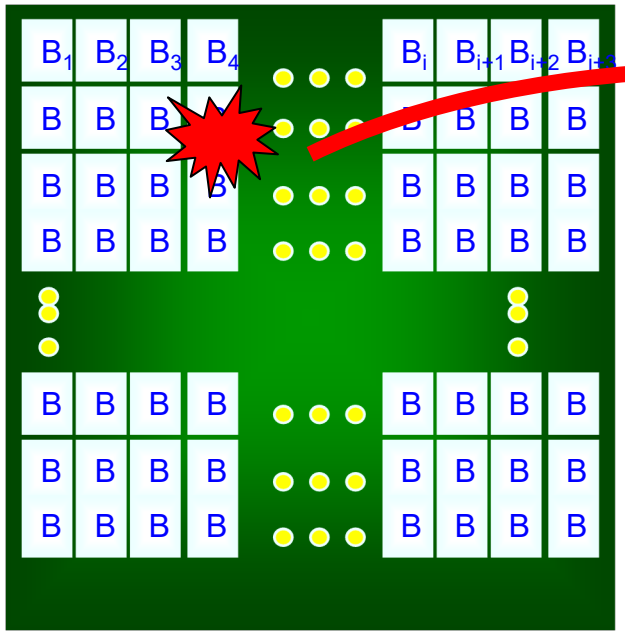
$$\sigma_{SEF} = f\left(\sigma_{configuration}, \sigma_{BRAM}, \sigma_{functionalLogic}, \sigma_{HiddenLogic}\right)$$

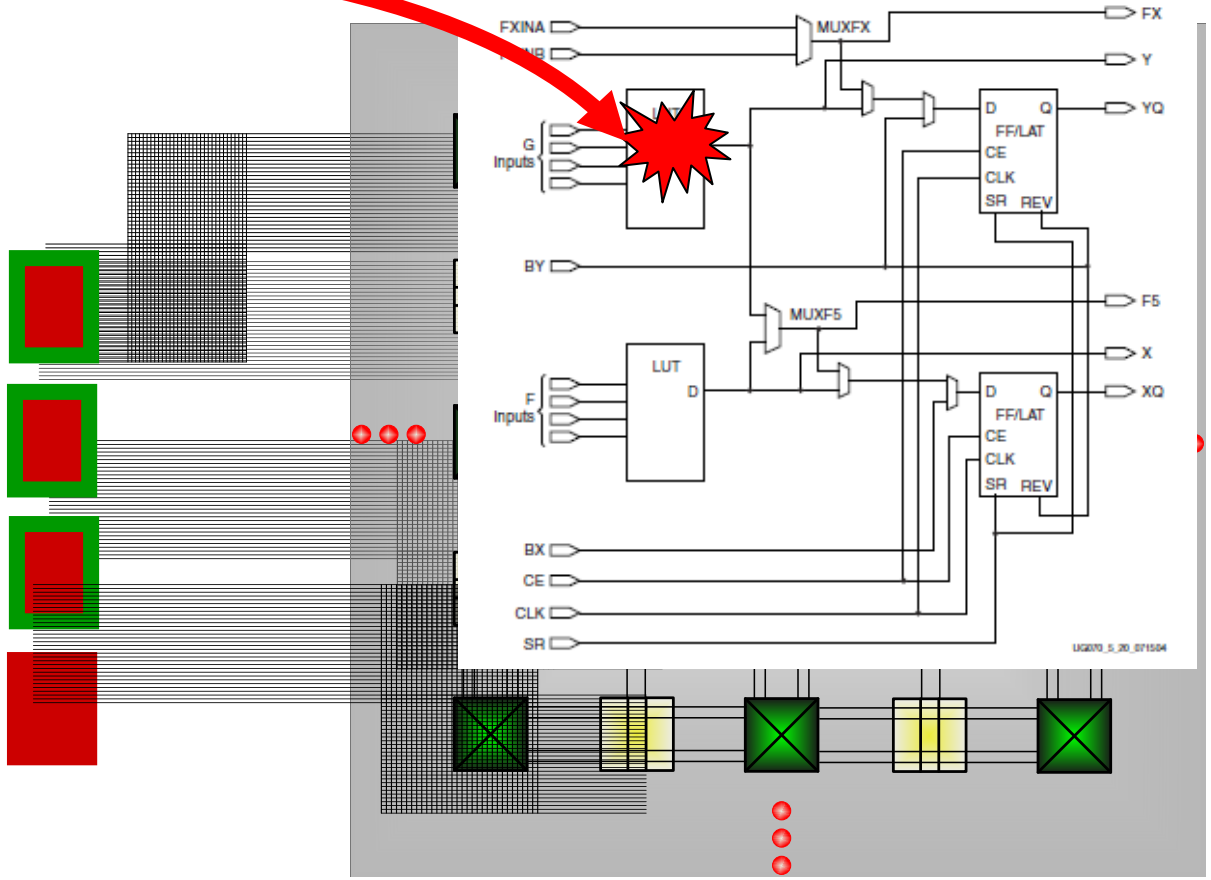


For SRAM-Based FPGA Devices, The Configuration Cells Are The Dominant Sources of Upsets

FPGA Configuration Memory SEU and Functional Upsets

An affected used configuration bit can instantaneously cause an unexpected functional effect



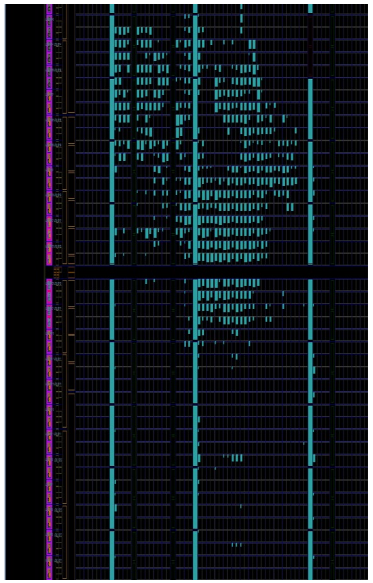


- Direct connections from configuration to user logic.

No Read-Write cycle required!

SRAM-Base FPGAs and SEU Cross-Sections

For SRAM-Based FPGAs, Configuration bits are the dominant mechanisms of failure.



We first obtain configuration-bit cross-sections

We perform a linear transformation:
(#essential_bits × configuration cross-section)

We use the linear transformation as a bounding cross-section (error rate)

$$\sigma(LET)_{configuration\_Device} = \frac{\#events}{\#Particles/cm^2}$$

$$\sigma(LET)_{configuration\_bit} = \frac{\#events}{\left(\#\frac{Particles}{cm^2}\right) * (\#unmaskedconfigurationBits)}$$

$$\sigma(LET)_{\text{Essential}\_bit} = Essential\_bits \times \sigma(LET)_{configuration\_bit}$$ **Bound**

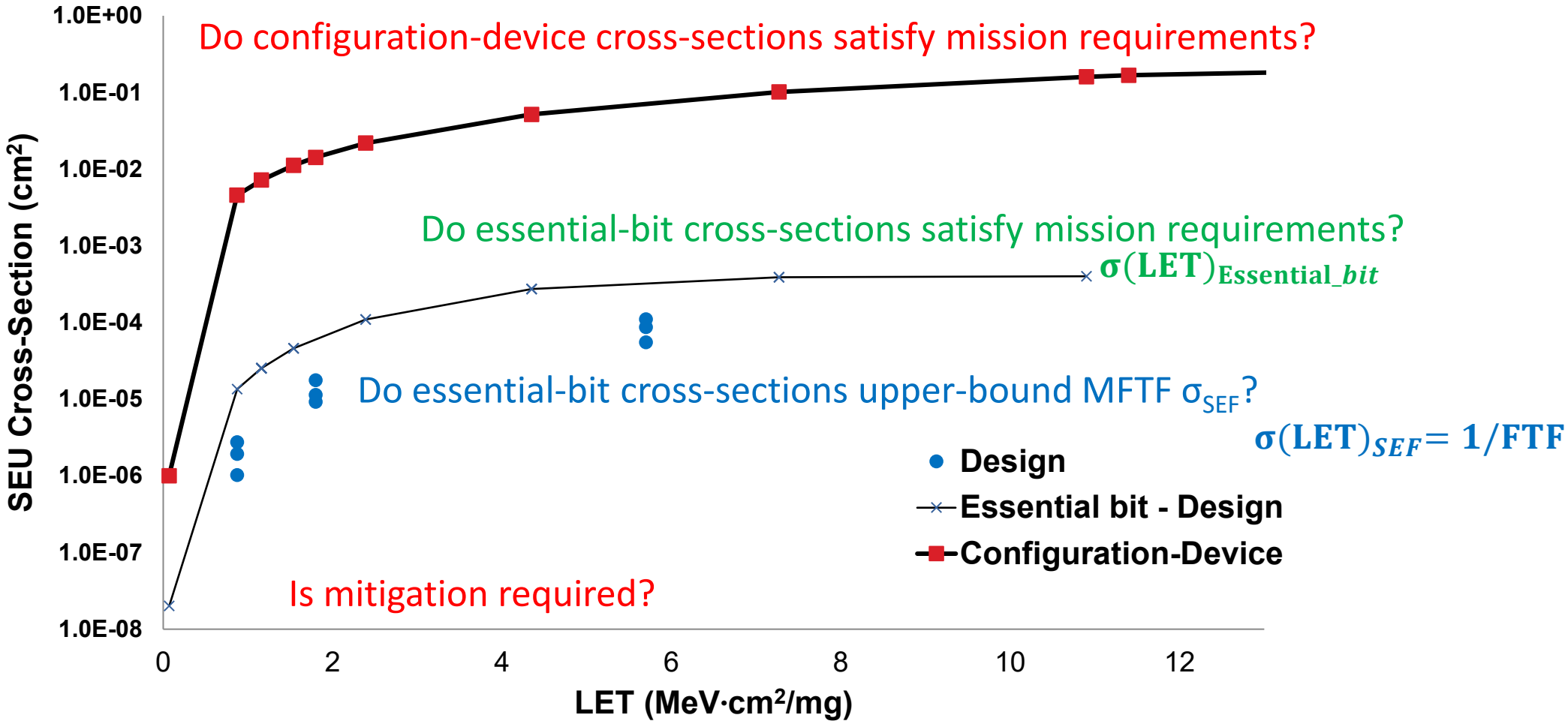
$$\sigma(LET)_{SEF} = \mathbf{1}/\text{FTF} = \mathbf{1}/((FailureTime - BeamStartTime) * \text{AverageFlux})$$

System Extrapolation

Which cross-sections do we use for failure analysis? … Must consider mission requirements.

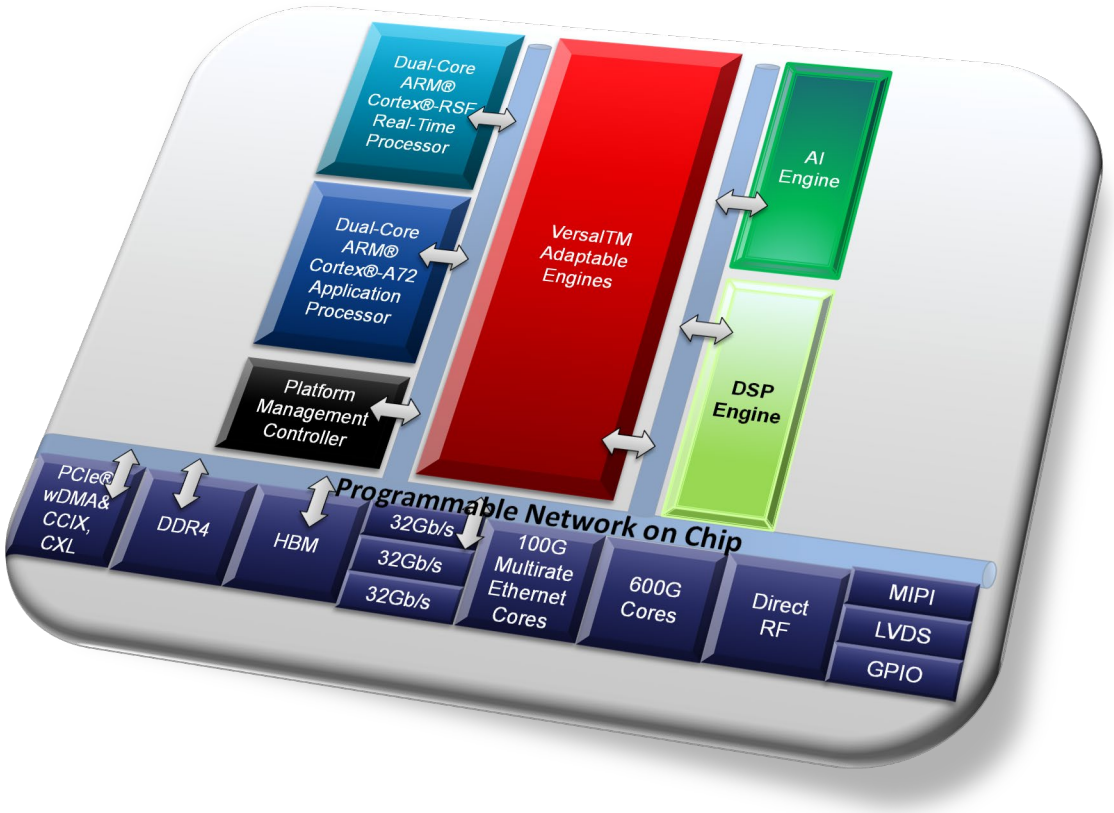
SRAM-Based FPGAs and Using Configuration Memory as An Upper-Bound

If Upper-bounds Satisfy Mission Reliability/Survivability Requirements, Then No FTF (Data Refinement) Necessary



Error Bounding is Easy… Why Not Always Use It?

- Error bounding provides extreme upper bounds without knowledge of design topology.
  - Overestimation might not meet requirements. Might need to refine SEE data by performing RMA type SEE testing.
  - Can't be used to study the efficacy of mitigation.
- When using error bounding… prove it before you use it.
  - The proof of bounding has been the missing factor; and is now necessary.
  - Why now? SoC/FPGA devices include a significant amount of hidden logic.
  - Bounding schemes for hidden logic should be based on worst case application… not on bit counts:
    - Functional blocks (or IP)
    - Protocols
    - Number of blocks/lanes
    - Redundancy



Fine-Grain Test Structures Should Not Be Used for SoC Extrapolation

- Conventional test structure: shift register.
- Shift register data (the conventional golden metric) does not provide enough information for characterization of an **SoC** application.
- Instead, test using coarse-grain structures:
  - Test operation in similar modes to flight.
  - Topology is not lost, and its effects can be studied.
  - Flight-like state-based controls, speed, and function.

Fine-grain test structure: unique topology is lost

Move from counting events of basic mechanisms

$$\sigma_{SEU} = \frac{\#events}{\#ions/cm^2} = \frac{\#events}{Fluence}$$

To obtaining the fluence until an event occurs

$$\sigma_{SEF} = \frac{1}{Fluence}$$

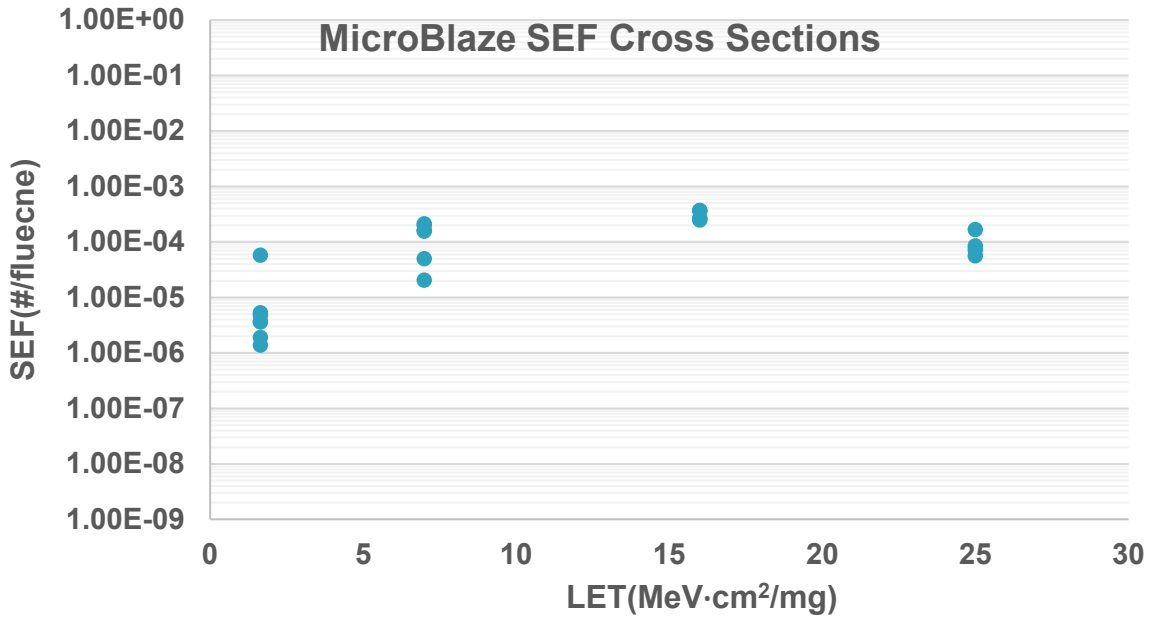
FTF: fluence-to-failure

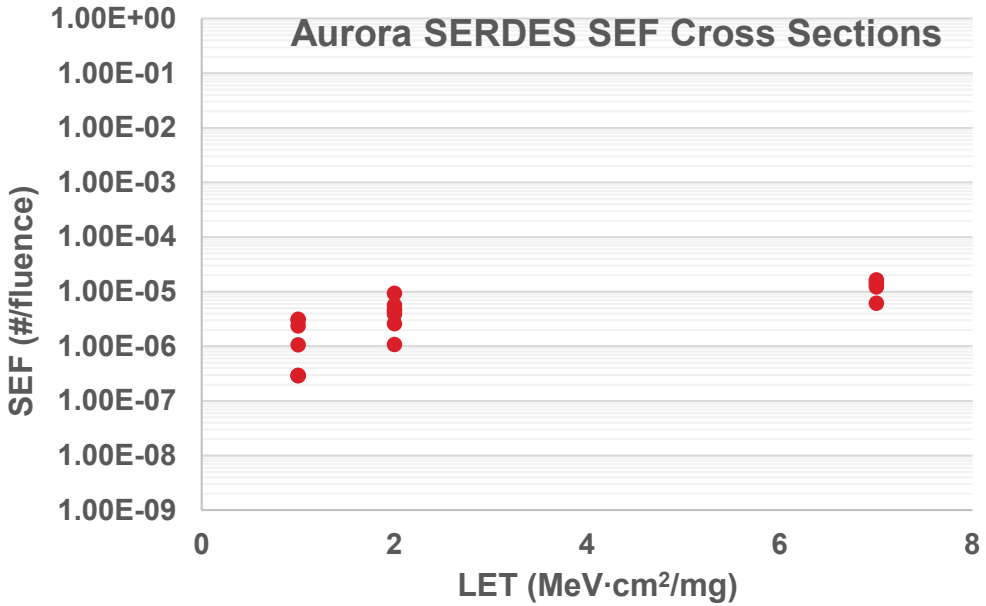
Fluence-to-Failure Experiments and The Exponential Model

Classical Reliability : transformation from the time domain to the fluence domain.

	Exponential Distribution Variables
Fluence-to-failure (FTF)	Φ_i Random Variable: per experiment-*i* for a selected LET
SEF Cross-section per experiment (rate w.r.t. fluence)	$\sigma_{SEF_i} = \frac{1}{\Phi_i}$
Sample mean (MFTF)	$\mu = \frac{1}{n}\sum_{i=i}^{T} \Phi_i$ Average of fluence-to-failure test results. **n = number of events** **T = number of experiments**
Mean SEF	$\sigma_{SEF_\mu} = \frac{1}{\mu}$ Classical Reliability: Constant per LET
Standard deviation	$\mu = MFTF$ Use of exponential population standard deviation definition
Standard error of the mean (SEM)	$\frac{\mu}{\sqrt{n}}$ Generally used for error bars
Exponential PDF Probability distribution function	$\sigma_{SEF_\mu} e^{-\sigma_{SEF_\mu}\Phi}$ or $\frac{1}{\mu} e^{-\frac{1}{\mu}\Phi}$

Xilinx/AMD Kintex-Ultrascale…FTF Data for Complex Operations





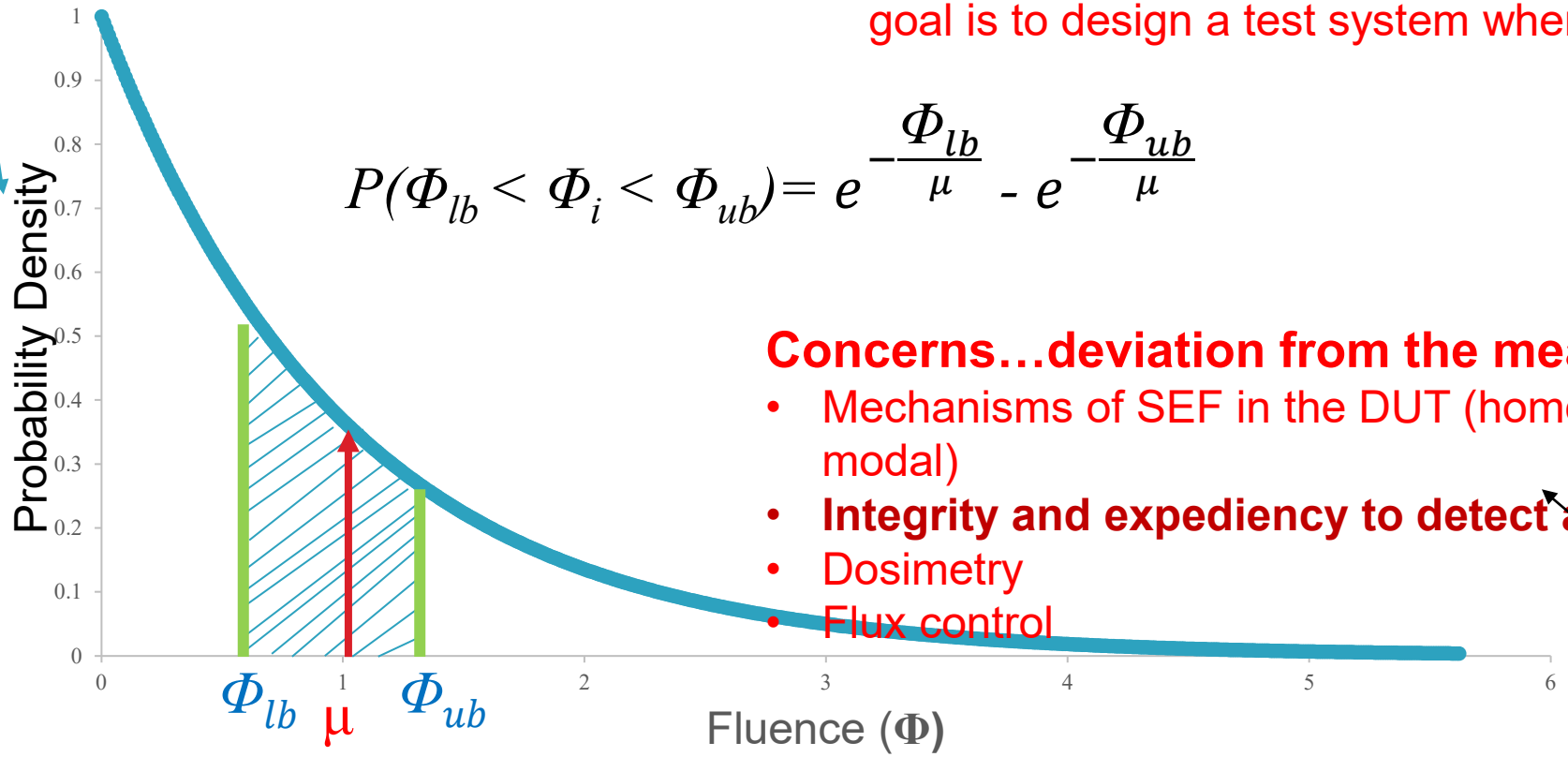
- FTF cross section data are within a decade and are sufficient for calculating SEF cross-section means
- Calculate mean per LET analyzing each experiment i :
  - No event for experiment i: n=0 and Φ_i = fluence for experiment i
  - Event for experiment i: n=1 and Φ_i = recorded fluence for event occurrence
- If n=0 for a majority of tests, increase fluence (and check your test system).

$$\mu = \frac{1}{n}\sum_{i=i}^{T} \Phi_i$$

$$\sigma_{SEF\mu} = \frac{1}{\mu}$$

FTF PDF Expected Empirical Data: How Can 5-10 Tests Be Sufficient?

$$f(\Phi) = \sigma_{SEF_\mu} e^{-\sigma_{SEF_\mu}\Phi}$$



For each experiment, most FTF data points (Φ_i) will occur near the mean, for a well-made test system. The goal is to design a test system where Φ_{lb} is close to Φ_{ub}

$$P(\Phi_{lb} < \Phi_i < \Phi_{ub}) = e^{-\frac{\Phi_{lb}}{\mu}} - e^{-\frac{\Phi_{ub}}{\mu}}$$

Concerns…deviation from the mean depends on:

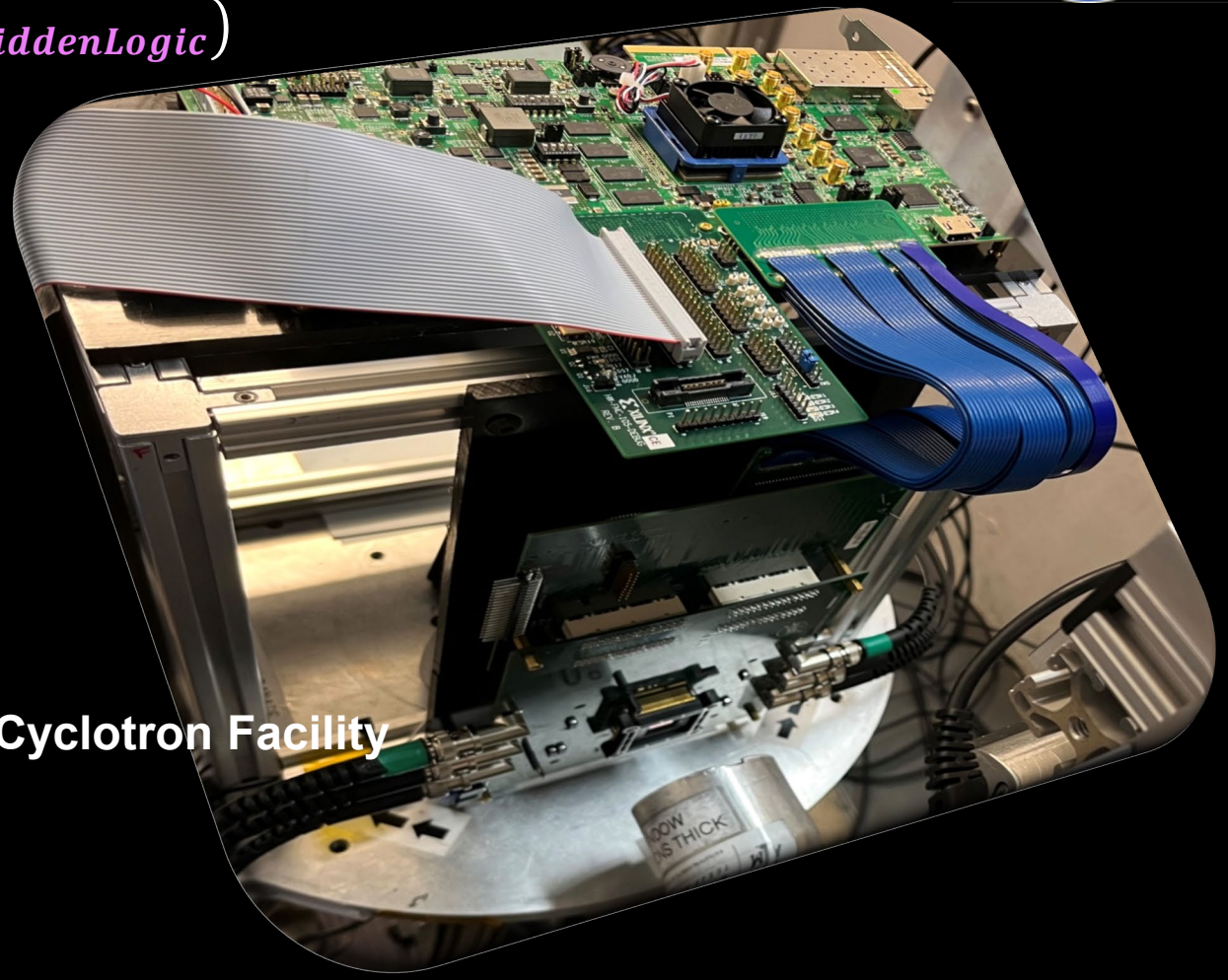
- Mechanisms of SEF in the DUT (homogeneous, multi-modal)
- **Integrity and expediency to detect and report SEF**
- Dosimetry
- Flux control

The reality is: increasing the number of tests will not bring your empirical mean closer to the actual mean if concerns are not controlled.

NASA Mission Requiring Test-As-You-Fly (FTF) Radiation Data

$$\sigma_{SEF} = f(\sigma_{configuration}, \sigma_{BRAM}, \sigma_{functionalLogic}, \sigma_{HiddenLogic})$$

- DUT: Microchip RTProASIC3 mission critical.
- Mission Requirement: work through worst week with ground intervention restricted to 0.01/day.
- DUT area constraints limit mitigation.
- **Linear bounding predicted error rates do not** meet requirements (use of shift register data).
- **Test-as-you-fly** heavy-ion testing required (**FTF data refinement**).



Texas A&M Cyclotron Facility

A robust complex system was developed:

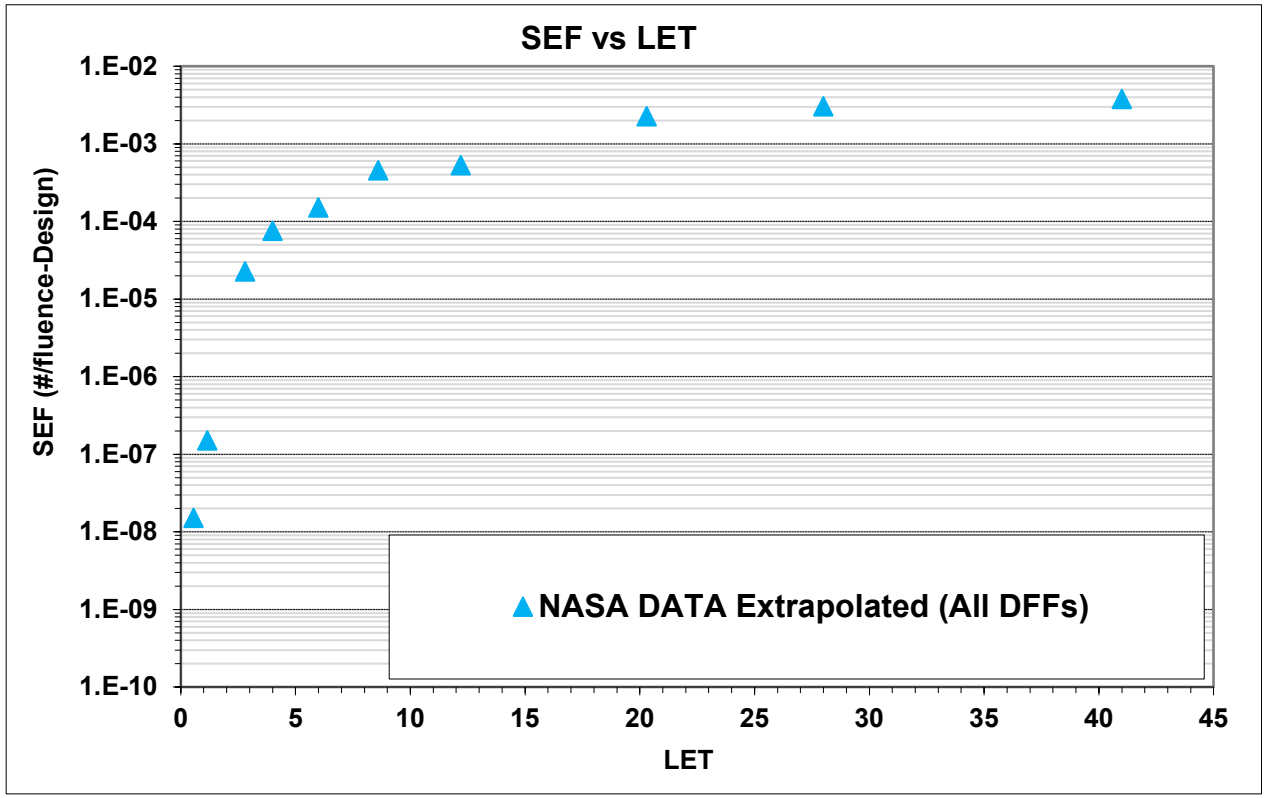
Multi-use Test Platform enabled testing the DUT with the NASA flight image. DUT was controlled and operated (at speed) as it would be in flight. FTF data were successfully obtained.

Microchip RTProASIC FTF Linear-Bounding Data

SEF: single event failure

LET: Linear energy transfer

- Linear-bounding data cannot be refined to specific function.

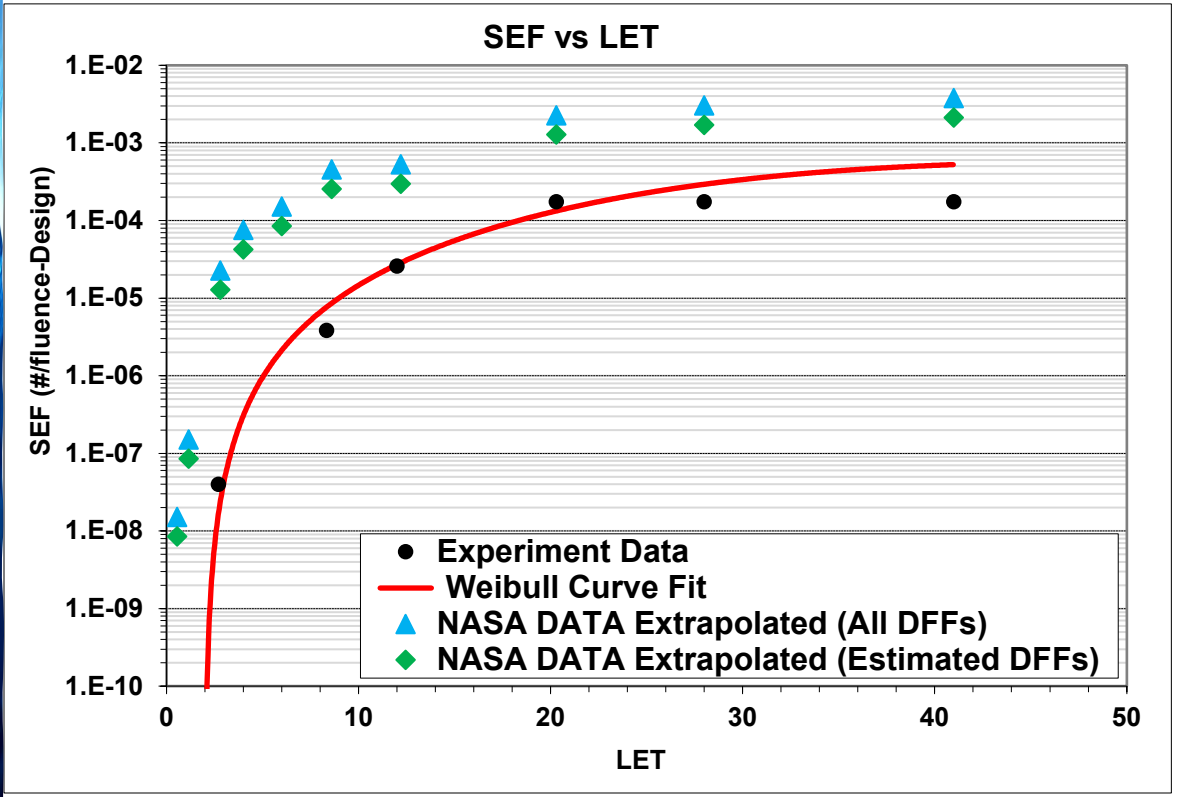


LET Range	Fluence/Day
0.1 …0.5	1.8×10^{6}
0.5 …1.0	7.6×10^{3}
1.0…5.0	1.0×10^{3}
5.0…10.0	4.2×10^{1}
10.0…20.0	8.4×10^{0}

Large number of low LET Particles per day during worst week storm conditions.

Test-As-You-Fly FTF Refined Data Meet Requirements

- FTF experiments were RMA-Test-as-you-fly.
- Linear bounding data do not meet requirements while Test-as-you-fly data do.



Weibull Parameter	Description
LET_{onset}	Onset LET
σ_{SAT}	Saturation cross-section
W	width
S	shape

Parameter	Linear Bounding	Test-As-You-Fly
LET_{onset}	0.5 MeV·cm²/mg	2.0 MeV·cm²/mg
σ_{SAT}	60 μm²	6000 μm²
W	42.58 MeV·cm²/mg	30 MeV·cm²/mg
S	2.0	2.8
Multiplier	15200	1
Error rate	2.1×10^{-1} errors/day	2.3×10^{-3} errors/day

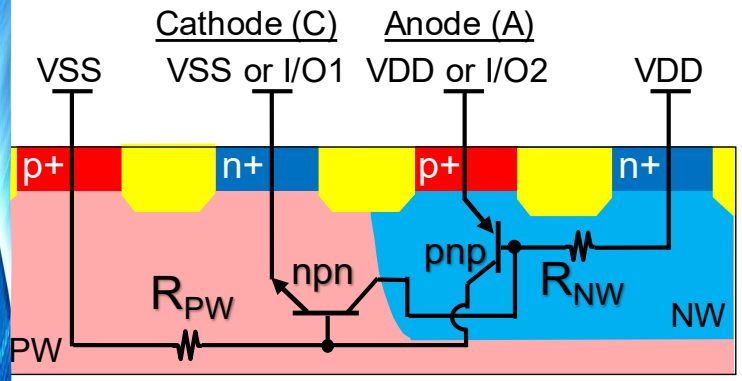
Does not meet requirements

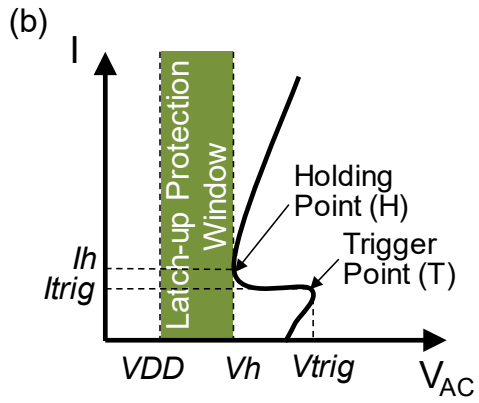
Does meet requirements

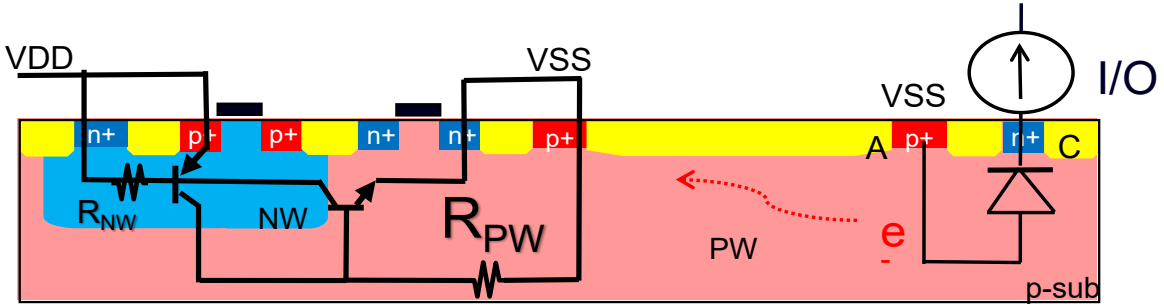
Single Event Latch-up Has Been A Problem for SoC/FPGA Devices: NEPP/SIEMENS Collaboration

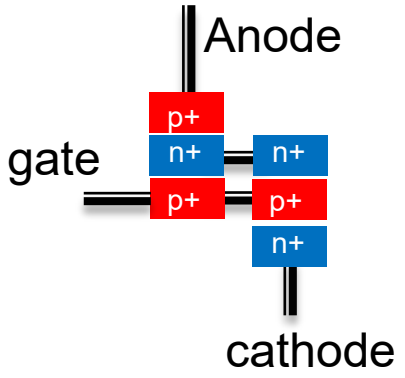
- For latch-up to occur, the voltage difference between the Anode and the Cathode (V_{AC}) must be positive and higher than the holding voltage (*Vh*) of the structure.

Karen Henderson
Abdellah Bakhali
SIEMENS Calibre® PERC™

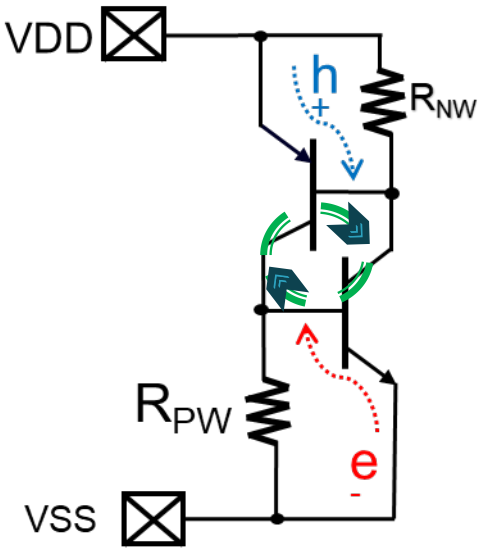




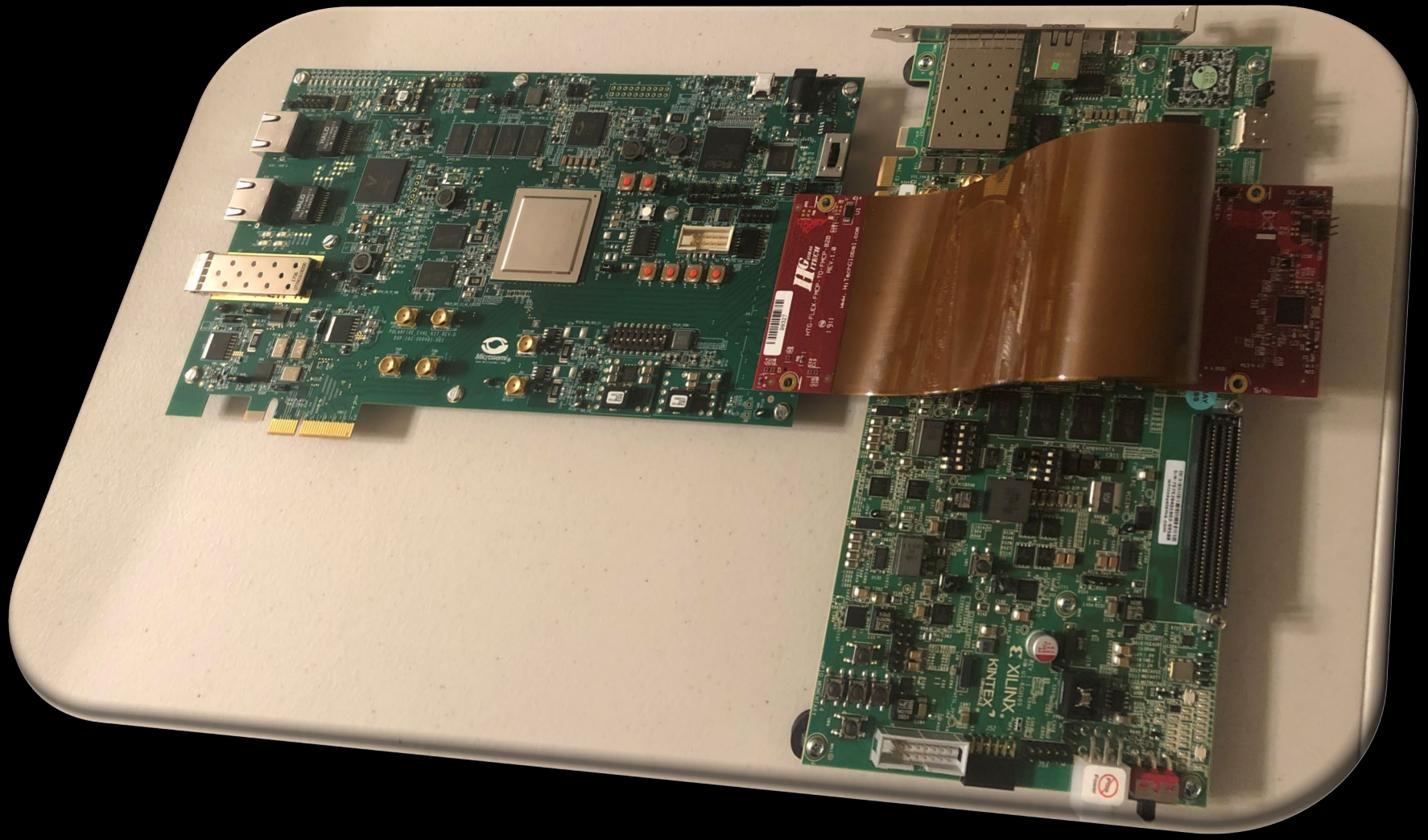




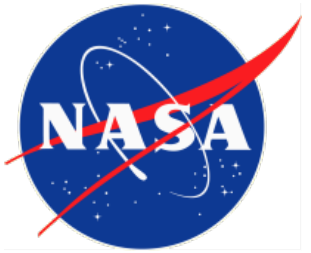
Parasitic thyristors = silicon-controlled rectifiers.



Microchip RTPolarFire Update

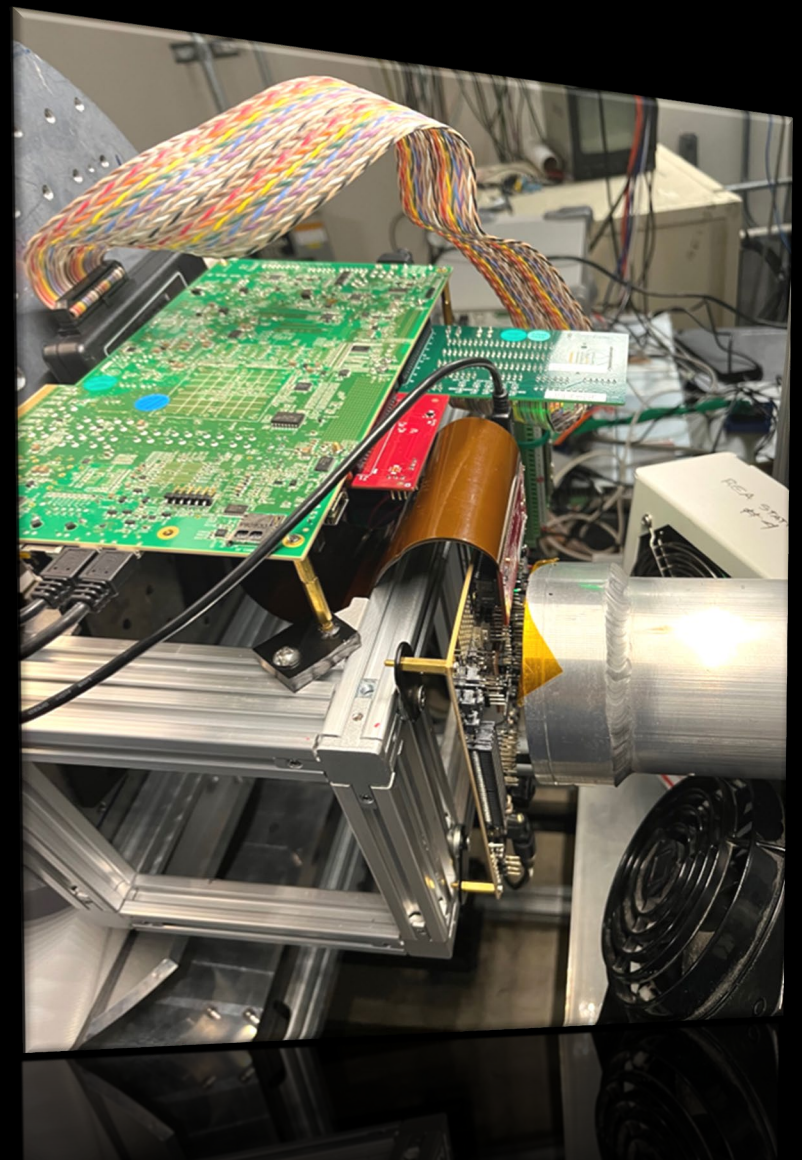


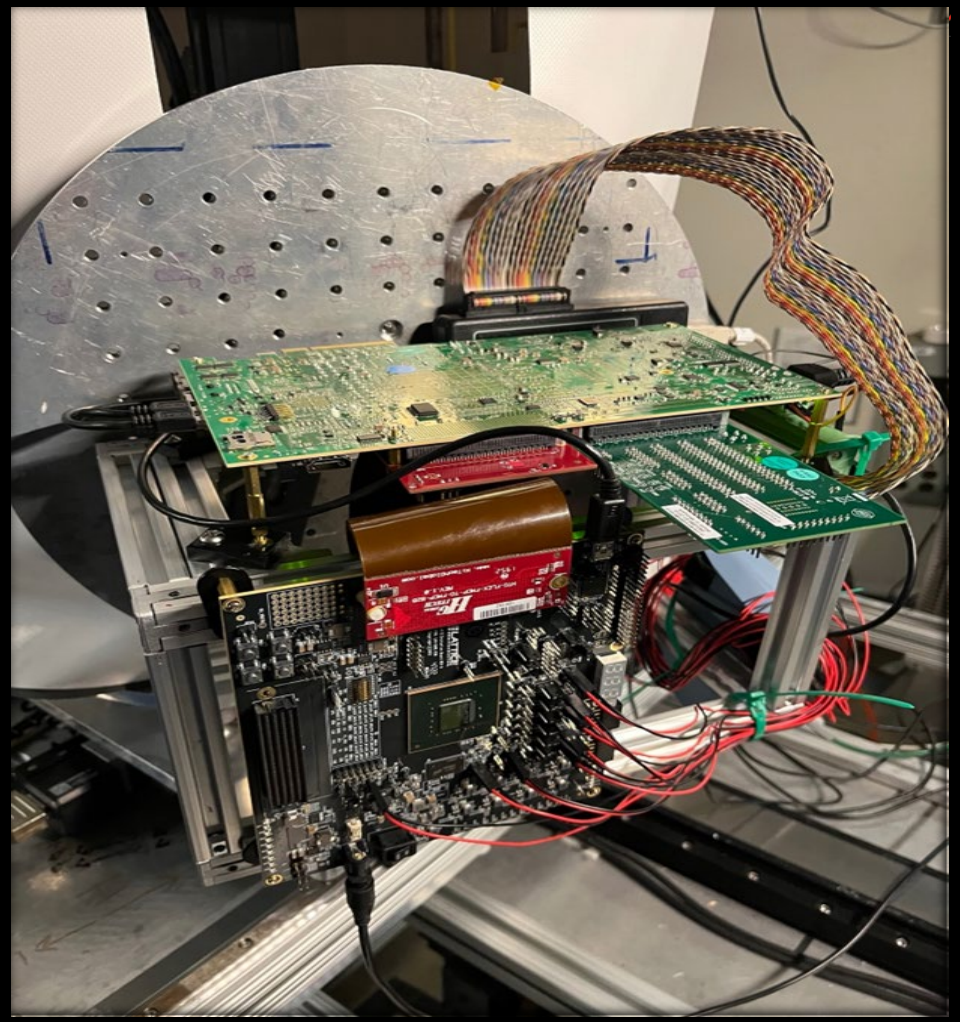
Microchip PolarFire 2023 Updates and Alerts



- 28 nm flash-based FPGA.
- No NEPP tests performed for 2022-2023 (2021 data uploaded to NEPP radhome).
- From Microchip test campaigns (2022-2023):
  - SEL found… non-destructive.
    - Microchip is re-spinning the RTdevice. Availability: 2024
    - For space applications, users are encouraged to target the respin.
    - The respin version of the device is referred to revision(Z)… SEL is expected to be fixed.
    - **Users must follow board design rules concerning capacitors. Otherwise SEL can be destructive.**
  - Turning off the system controller significantly reduces the probability of the system controller SEFI.
    - Depending on the environment (and length of the mission), system controller SEFIs are unlikely.
    - However, this may not the case for every environment/mission (e.g., space weather). Analysis is currently being performed by the manufacturer.
- Prior to assuming TMR insertion is achievable for your application:
  - Implement your TMR'd application, at speed, at the board level.
  - Do not trust static timing analysis for inserted TMR designs.

Lattice Avant SEE Campaign





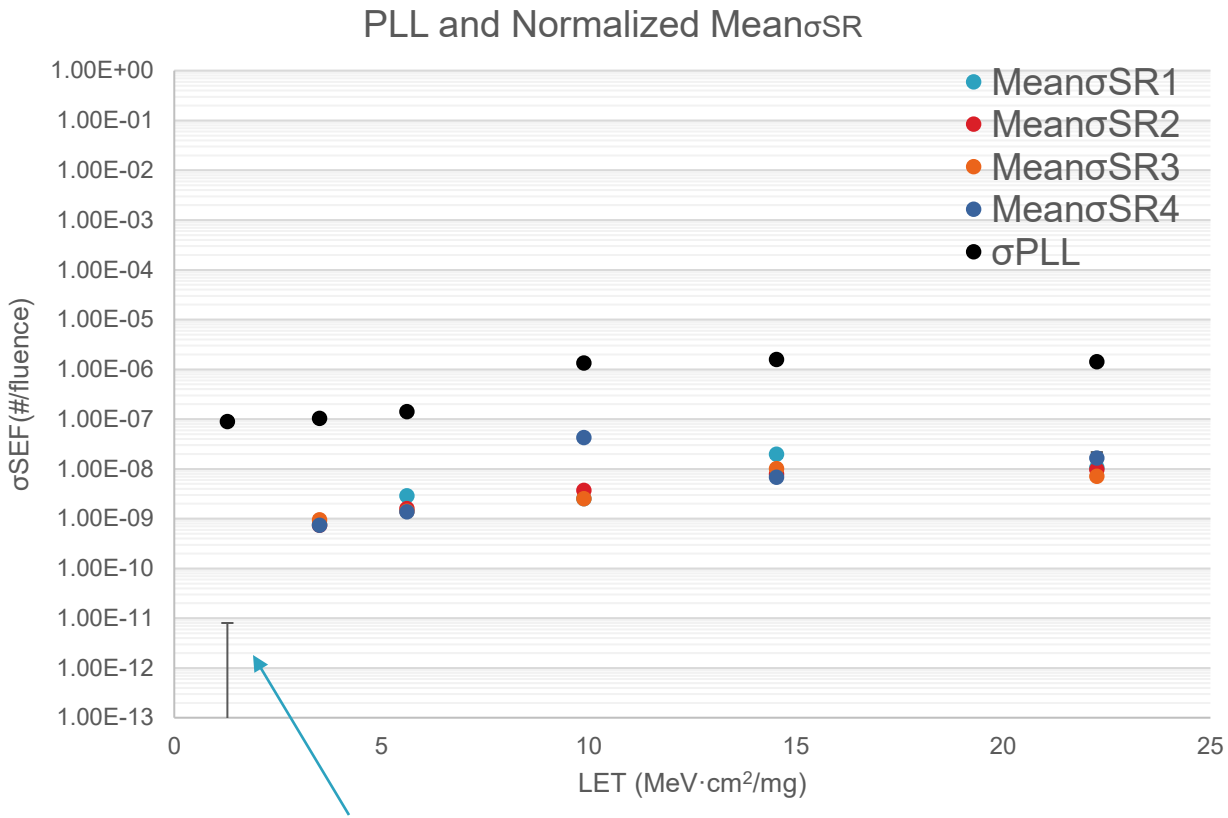
Lattice Avant Test Campaign Overview

- Device under test (DUT): Avant-E FPGA (LAV-AT-500E-3LFG1156C)
- DUT technology: **TSMC 16 nm FinFET**
- Test campaign dates: May 6th-May 7th
- Test type: first look
- Number of tests: 62
- Device thinned to 76 µm.
- Test structures: Shift registers
- Test platform: multi-use test platform
- LET range: 1.4 MeV·cm^2/mg – 58 MeV·cm^2/mg at 20 MeV
- All tests were performed at normal incidence.
- All tests were performed at room temperature.
- **No single event latch up (SEL) observed:**
  - Fluence at 58 MeV·cm^2/mg > 3.7×10^7
  - High temperature tests will be performed (test date not set).
- Early stages. Configuration is not currently able to readback. Hence, no configuration cross-sections were obtained.

Lattice Avant Shift Register (SR) Cross-Sections (σ)

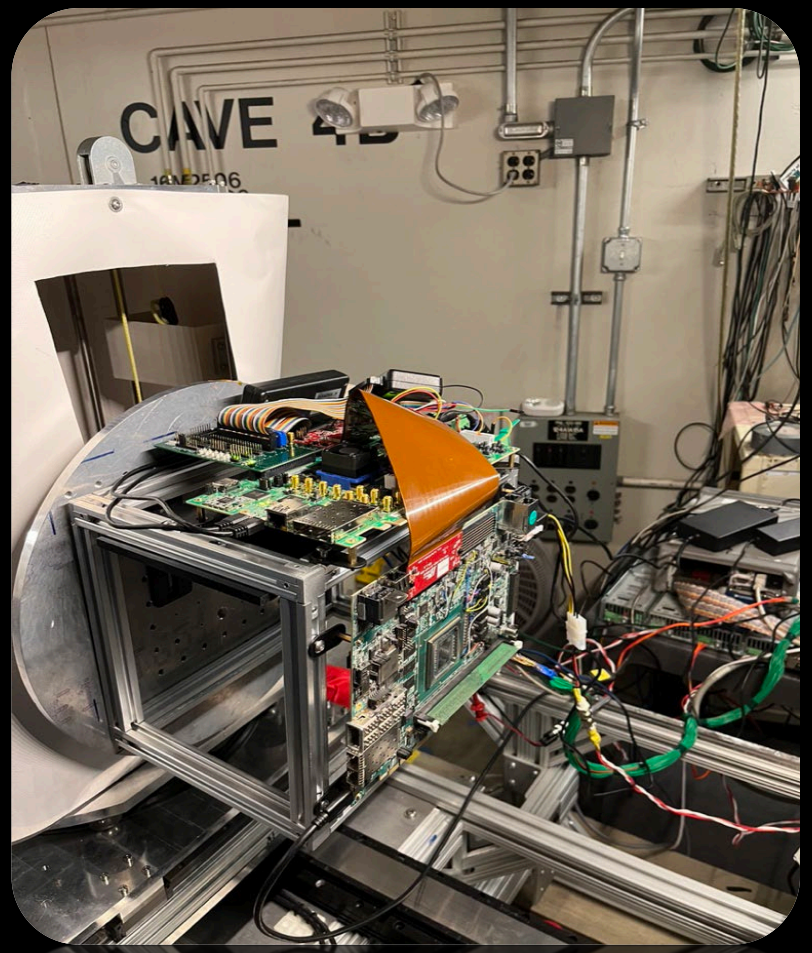
- 4 chains:
  - SR1: 2000 flip-flop stages
  - SR2: 1000 flip-flop stages
  - SR3: 100 flip-flop stages
  - SR4: 100 flip-flop stages
- σ_{SEF} : SR chains are normalized by the number of SR stages to perform comparisons.
- Normalized σ_{SEF} show that cross-sections grow linearly with the number of flip-flops for a simple shift register design.
- No frequency effects observed. Additional data will be provided in the test report.
- PLL has relative low cross-sections.
- Need angular data.
- Test report submission date: June 30th, 2023

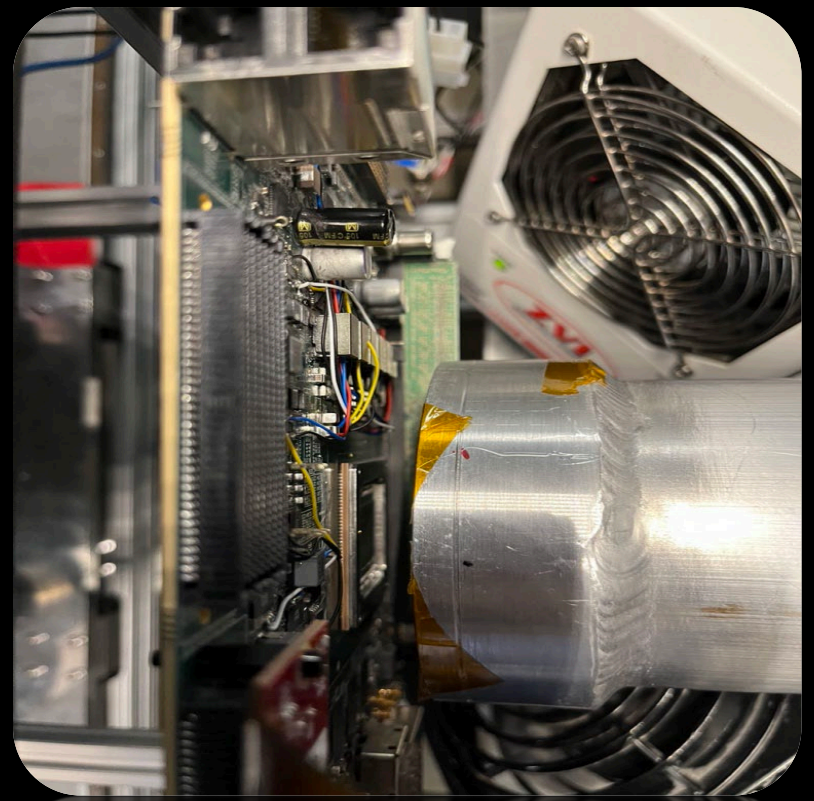
Normalized σ_{SEF}: shift register SEF cross-section = $\frac{\sigma_{SEF}}{\#stages}$



No SR SEUs observed at LET = 1.3 MeV·cm²/mg

Is It Something I Did?

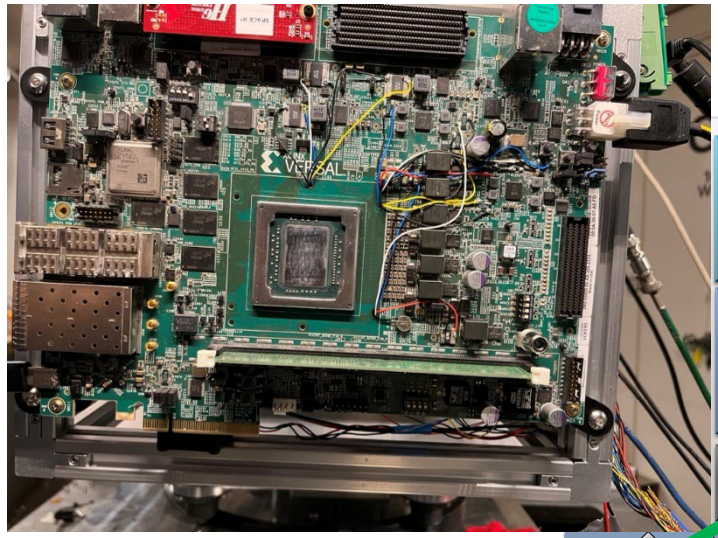


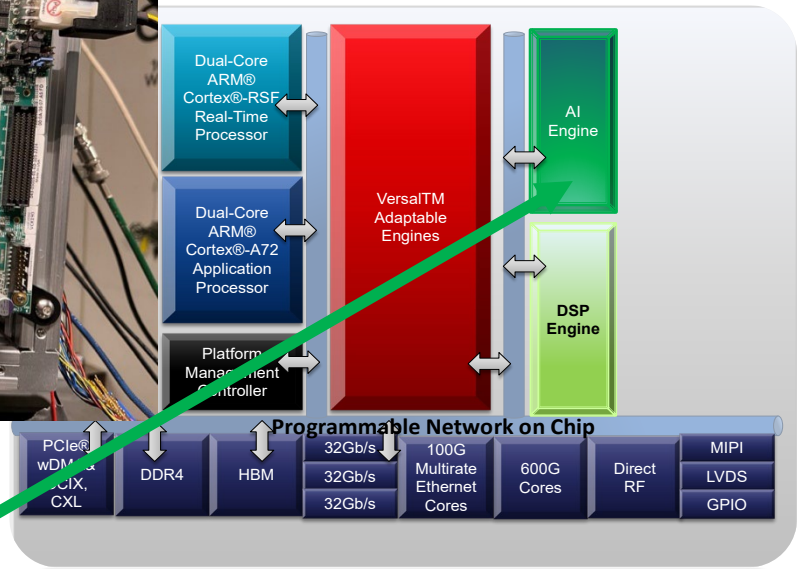


Double Check Your Results

Xilinx Versal SEE Experiments

- Test dates: May 5th- May 7th
- Test type: first look
- 4 experiments targeting the Versal AI engines were conducted.
- High current (HC) events occur at relatively high fluences at O and would be rare events.
- The HC events appear to be destructive.



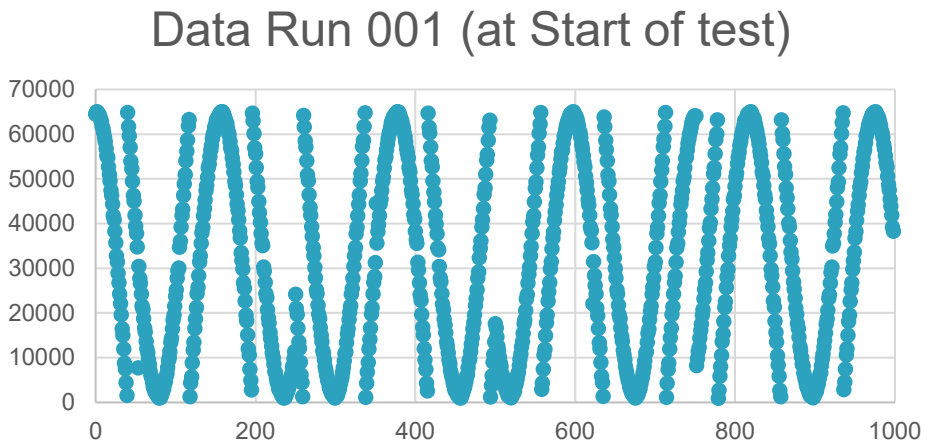


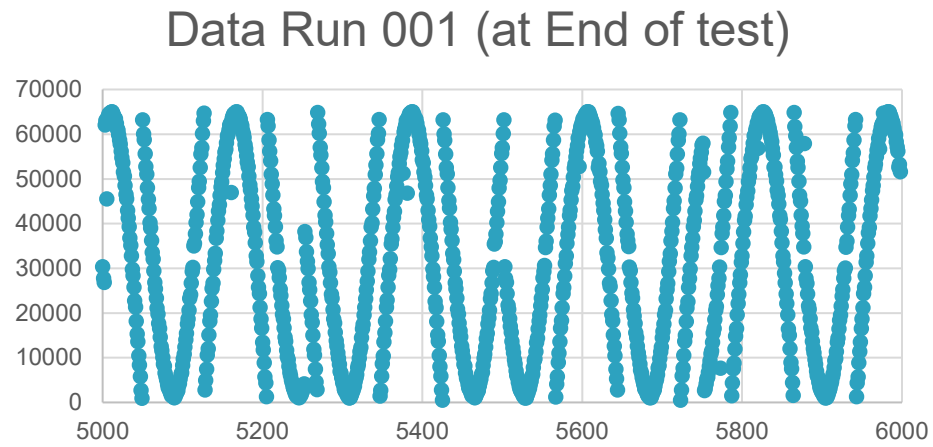
First dynamic test for programmable logic (PL) to AIE activity.

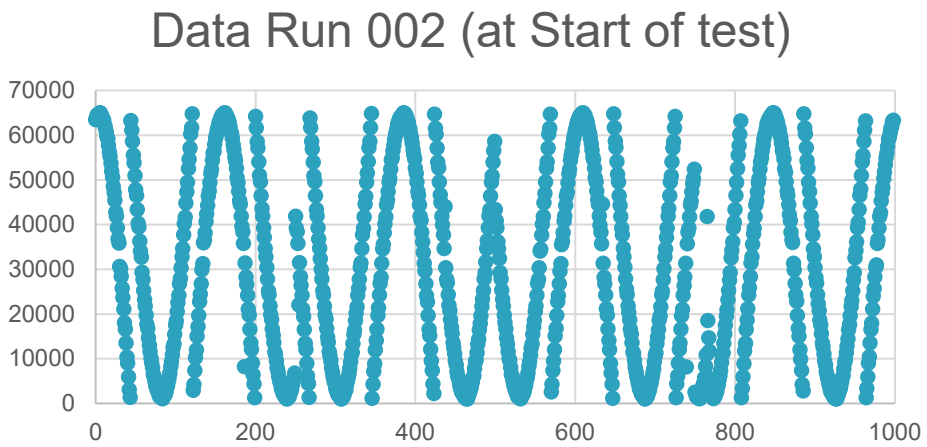
Run Log with HC Cross Sections

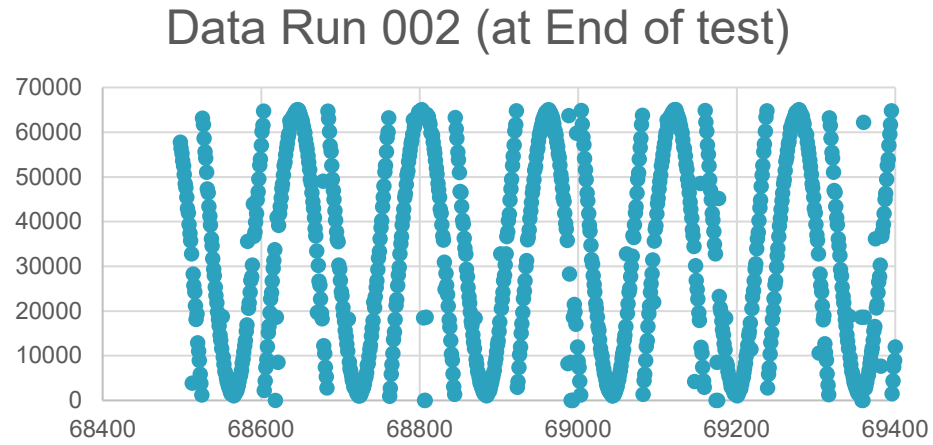
ION	Run #	LET	RunTime	Fluence	HC Cross Section	Current Event
O	1	1.28	147.00	**1.31E+07**	7.63E-08	**21 A**
O	2	1.28	892.90	1.00E+08	0.00E+00	No Event
O	3	1.28	381.40	4.00E+07	2.86E-08	17 A
Al	63	3.5	197.74	1.66E+06	6.02E-07	High current

Versal AIE Data Outputs Pre and Post Beam Exposure









Versal Experiments: Observations and Analysis

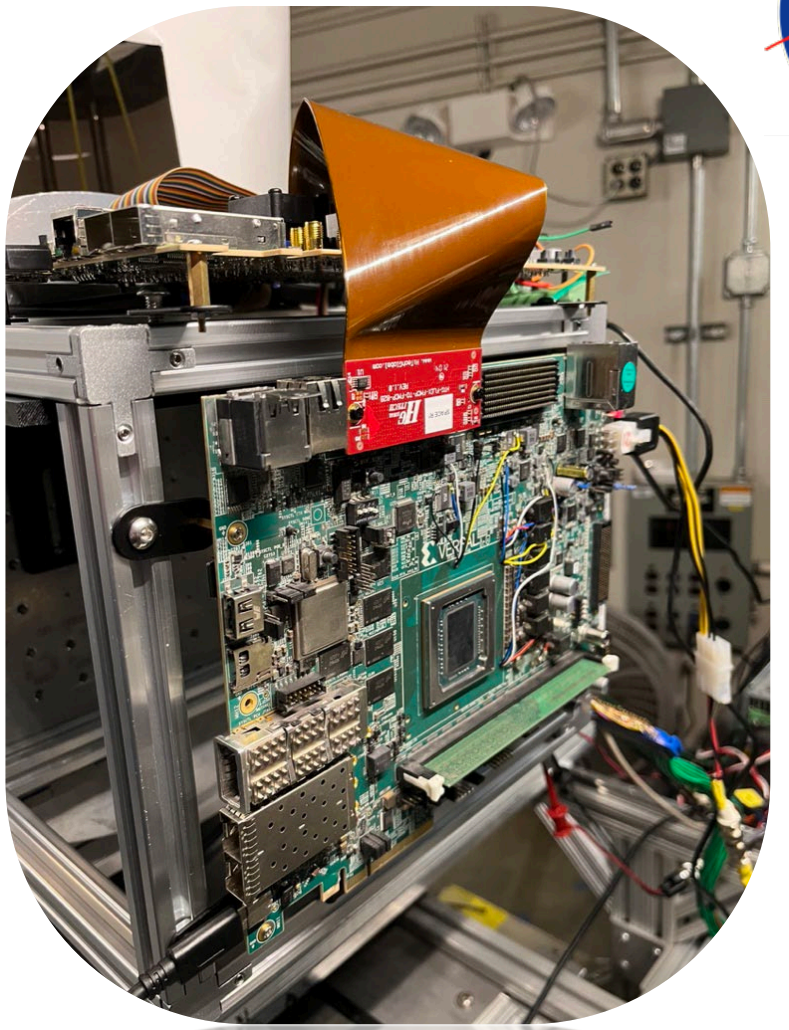
- **Observations**:
  - **Run 1:** Data start clean and SEUs are observant.
    - 5A (initial current) jumped to 21A (internal power plane).
  - **Run 2:** After power cycle, data begin erroneous (spotty errors), prior to beam.
    - Test begins in an unstable state… data are not good… curious if there will be another current jump.
    - No high current jump.
  - **Run 3:** After power cycle, unable to get good data prior to beam. Removed tester and allowed DUT to run on its own.
    - Test begins in an unstable state… data are not good… curious if there will be another current jump.
    - 5A jumped to 17 A (internal power plane).
- **Analysis**:
  - Data suggest stuck (or in hysteresis) bits occur in AIE SRAM (because data have errors during run 2 prior to starting the beam). This is only an assumption and is not definitive.
  - High current occur in Vccint power plane.

Are The Current Jumps Due To The Test System or How The Tests Were Conducted?

- **Device Processing:**
  - Could something have happened during the device thinning process?
  - We only had one device for this trip (first look).
- **Power supply Setup:**
  - Power supply settings were verified and was placed near the DUT (within 3 feet).
  - Power supply readings for manufacturer provided built in self tests (BISTs) checked out prior to conducting beam tests.
  - Current was directly monitored across on-board sense resistors… did not use I2C bus.
- **Evaluation Board Power Distribution :**
  - DUT test board is an evaluation board with voltage regulators on each power plane.
  - Vccint has 6 regulators in parallel … can this be a problem? Is this a board design problem?
- **DUT functionality without beam:**
  - DUT application had weeks of activity with no current fluctuations.
- **DUT connections:**
  - DUT was connected to the tester via an FMC connector.
  - No current jumps observed in the I/O domain… only internally (Vccint).
- **Flux: approximately 1.0×10^5** … is this too high of a flux even at a low LET (1.2? MeVcm^2/mg)?
- **Fluence:** 1.37 Particles/cm^2… is this an accumulative problem?

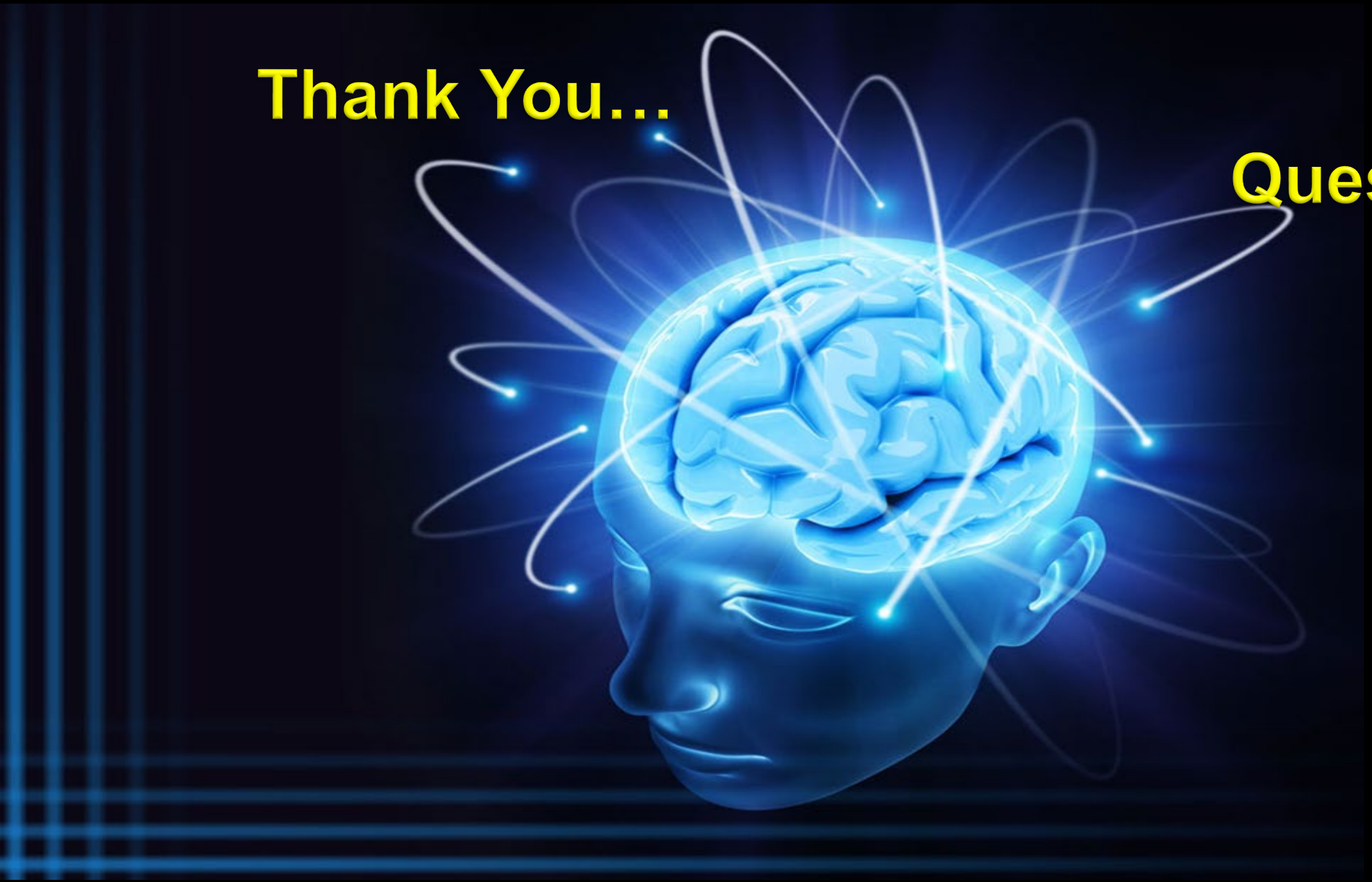
Versal Synopsis

- NEPP performed a dynamic SEE test with the PL and AIE actively processing data.
- High current event was observed at an LET=1.3 MeV·cm^2/mg.
- Additional testing will be performed to validate or debunk the high current event.
  - Procure and test different devices
  - Start at higher LET with lower flux.
  - Additional tests will be performed June 29th-30th 2023.
- Wait for further information and investigation is complete.



Personal assumption: can likely be board power distribution (Vccint: 6 regulators in parallel for one voltage domain); and hence be a lesson of what not to do for board design.

Thank You…



Questions