EXPLORE SPACE TECH
TECHNOLOGY DRIVES EXPLORATION

# *NASA's Vision for Spaceflight Avionics*

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# EXPLORE: Develop next generation high performance computing, communications, and navigation

*Developing flight computing architectures and advanced avionics to enable increased onboard intelligence and autonomy for future exploration missions in harsh environments*

| | |
|---|---|
| **Go**<br>*Rapid, Safe, & Efficient Space Transportation* | • Develop nuclear technologies enabling fast in-space transits.<br>• Develop cryogenic storage, transport, and fluid management technologies for surface and in-space applications.<br>• Develop advanced propulsion technologies that enable future science/exploration missions. |
| **Land**<br>*Expanded Access to Diverse Surface Destinations* | • Enable Lunar/Mars global access with ~20t payloads to support human missions.<br>• Enable science missions entering/transiting planetary atmospheres and landing on planetary bodies.<br>• Develop technologies to land payloads within 50 meters accuracy and avoid landing hazards. |
| **Live**<br>*Sustainable Living and Working Farther from Earth* | • Develop exploration technologies and enable a vibrant space economy with supporting utilities and commodities<br>  • Sustainable power sources and other surface utilities to enable continuous lunar and Mars surface operations.<br>  • Scalable ISRU production/utilization capabilities including sustainable commodities on the lunar & Mars surface.<br>  • Technologies that enable surviving the extreme lunar and Mars environments.<br>  • Autonomous excavation, construction & outfitting capabilities targeting landing pads/structures/habitable buildings utilizing in situ resources.<br>• Enable long duration human exploration missions with Advanced Life Support & Human Performance technologies. |
| **Explore**<br>*Transformative Missions and Discoveries* | • Develop next generation high performance computing, communications, and navigation.<br>• Develop advanced robotics and spacecraft autonomy technologies to enable and augment science/exploration missions.<br>• Develop technologies supporting emerging space industries including: Satellite Servicing & Assembly, In Space/Surface Manufacturing, and Small Spacecraft technologies.<br>• Develop vehicle platform technologies supporting new discoveries. |

Computing for:

Advanced Propulsion
Cryogenic Fluid Management(TX 1.1.3)

Entry Descent & Landing (EDL)
Real-Time Precision Landing Algorithms (TX 9.0)

Autonomous Robotic Systems (TX 7.2.3)

Environmental Control and Life Support System (ECLSS)
Autonomous Clinical Care (TX 6.3.1)

**Advanced Avionics**
**TX 2.1 Avionics Component Technologies**
**TX 2.2 Avionics Systems and Subsystems**
**TX 11.1 Software Development, Engineering, and Integrity**

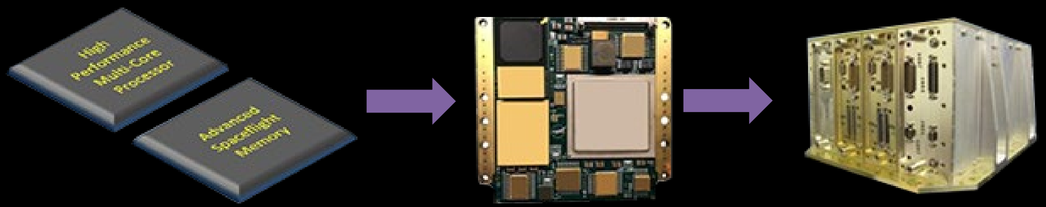
Autonomous Systems & Robotics
State Estimation, Terrain Mapping and Classification, 3D Modeling, Object Recognition, Path Planning, Fault Prognosis, Anomaly Detection, Resource Planning and Scheduling, Autonomous Navigation/Obstacle Avoidance, Autonomous Management of In Situ Activities (TX 4.0)

Rendezvous and Docking Algorithms (TX 4.5)

Sensors and Instruments
Instrument Control and Science Data Processing (TX 8.1, TX 8.3)

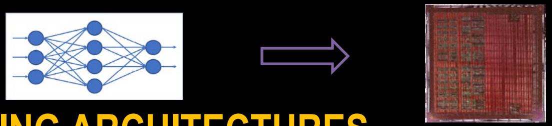
**As a "foundational technology", advanced avionics will be embedded within systems that address many of the Moon-to-Mars objectives; including most of the Infrastructure and Transportation objectives and several of the Science and Operations objectives**

# Advanced Avionics – Envisioned Future




## HIGH PERFORMANCE SPACEFLIGHT COMPUTING

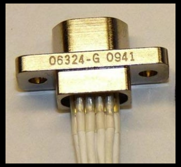
- Radiation-hardened general-purpose processor with vector processing, increased performance, and flexibility to adapt to mission specific performance, power, and fault tolerance needs
- Advanced spaceflight memory with radiation tolerance, increased capacity and improved performance
- Intelligent, efficient, multiple output Point-Of-Load (POL) power converters
- High performance Single Board Computer (SBC) incorporating high-performance general-purpose processors, advanced memory, point-of-load converters, and real-time operating system in industry standard form factors and bus architectures
- System software tools with vector support to leverage the capabilities and manage the complexity of advanced multi-core processors



## OTHER COMPUTING ARCHITECTURES

- Artificial Intelligence (AI) coprocessors to enable autonomous landing, surface navigation, robotic servicing/assembly, fault detection/mitigation, distributed systems operations, science data processing, and tip and cue for remote sensing missions
- Spaceflight quantum computers
- Low power embedded computers to support distributed robotics architectures

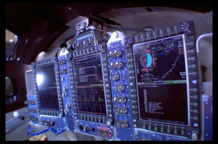
## INTERCONNECT




- Radiation-tolerant interconnects to support low latency onboard video, multi-gigabit instruments, onboard science, and enhanced autonomy applications; including end points, switches, physical layer devices, and software support
- Highly reliable, high-bandwidth deterministic wireless networks

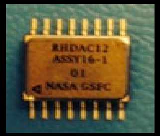
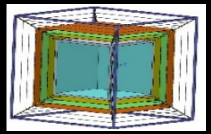
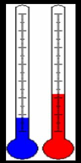
All activities depicted not currently funded or approved. Depicts "notional future" to guide technology vision.

# Advanced Avionics – Envisioned Future



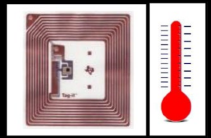
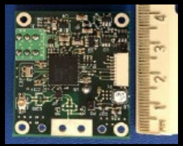
**CREW INTERFACES**

- Radiation-tolerant displays that can operate reliably for long durations mission beyond LEO
- Radiation-tolerant graphics processing that can operate reliably for long mission durations beyond LEO
- Heads Up Displays for Exploration EVA
- Crew voice and audio systems for deep space missions providing efficient compression of multiple streams, acoustic echo and noise cancellation, speech recognition and voice control, and wireless capabilities

**EXTREME ENVIRONMENT AVIONICS**

- Extreme temperature electronics capable of operating in environments with both high radiation and wide temperature ranges, including lunar/planetary surfaces or within nuclear systems
- Avionics packaging and thermal management technologies to enable avionics operation in extreme environments
- Dust tolerant connectors to enable interconnect on lunar and planetary surfaces

**DATA ACQUISITION**

- Wireless sensor networks to reduce harness mass and complexity, simplify integration and test, and improve system flexibility, serviceability, and expandability
- Low-cost, robust, high-accuracy data acquisition systems to enable distributed in situ monitoring of structures and subsystems on cost constrained missions

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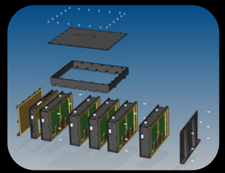
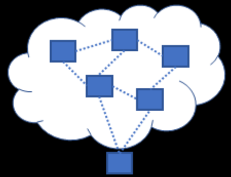
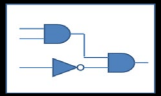
# Advanced Avionics – Envisioned Future

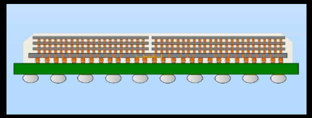




## AVIONICS ARCHITECTURES

- Interoperable avionics architectures allowing systems to be composed of standard interoperable modules from multiple vendors
- Cybersecurity tools providing defense-in-depth for spaceflight avionics
- Serviceable avionics architectures to simplify post-deployment servicing of avionics hardware
- Space cloud computing architectures allowing onboard processing to be distributed across multiple spacecraft or surface elements





## FOUNDATIONAL TECHNOLOGIES

- Advanced 2.5D/3D packaging supporting heterogeneous integration enabling miniaturization and improved performance
- Advanced semiconductor process nodes and libraries to enable next generation radiation hard devices
- Low-cost, radiation-hardened mixed-signal ASICs
- Advanced test systems accelerating radiation and reliability testing of complex COTS microelectronics devices

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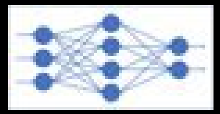
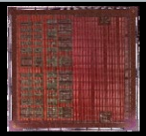
# Advanced Avionics – State of the Art


## HIGH PERFORMANCE SPACEFLIGHT COMPUTING

- Processors – Current missions either using radiation-hardened processors with limited performance, or higher performance redundant COTS-based processors limiting power efficiency
  - *Target - 3-5X performance improvement over current space processors for general purpose processing (GPP), parallel processing acceleration, and flexibility to adapt performance, power, and fault tolerance to mission needs*
- Memory – Radiation-hardened memories lack capacity and/or performance, while COTS-based memories are susceptible to radiation induced upsets
  - *Target - Radiation-hardened memory with 4-8X the capacity and/or performance of existing radiation-hardened memories*
- Point-Of-Load (POL) Power Converters – Current POL converters provide a limited number of outputs and lack embedded fault tolerance
  - *Target - Radiation-hardened, high efficiency POL converters leveraging wide-bandgap technology with at least 3 outputs, bus interface, and embedded fault tolerance*
- Single Board Computer (SBC) – Current SBCs using radiation-hardened processors have limited performance, as well as limited power and performance scaling capability
  - *Target - Radiation-hardened SBC in industry standard form factor with 5X GPP improvement, parallel processing, with ability to scale power and performance*
- HPSC Software Tools – Current system software tools do not support the complexity of the High Performance Spaceflight Computing (HPSC) multicore processor
  - *Target - System software tools with parallelism and vectorization support to allow developers to fully leverage the capabilities and flexibility of the HPSC processor*


## INTERCONNECT

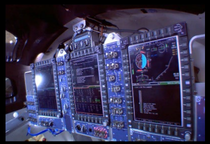
- Wired – Current onboard wired networks lack bandwidth to support increased sensor data rates of future missions
  - *Target - Wired networks with 10X bandwidth improvement*
- Wireless – Current onboard wireless networks only support low criticality needs
  - *Target - Wireless networks for critical applications in crewed and robotic missions*

## OTHER COMPUTING ARCHITECTURES

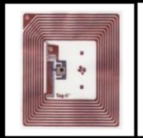
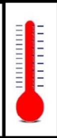
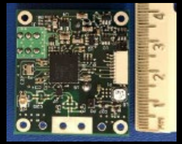
- Artificial Intelligence (AI) Coprocessors – COTS devices exist, but with unknown radiation performance and applicability to NASA onboard processing tasks
  - *Target - Radiation-tolerant AI coprocessors for NASA missions*
- Quantum Computing – Quantum computing technology is emerging, but small number of qbits limit processing capability, large infrastructure, and power requirements limit even terrestrial applications
  - *Target – Quantum computers tailored for onboard processing applications and environments*
- Low Power Embedded Computers – Current spaceflight robotics systems employ centralized architectures, which increases network bandwidth, latency, power, and system complexity
  - *Target – Low power embedded computers enabling distributed architectures*

# Advanced Avionics – State of the Art



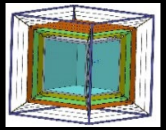
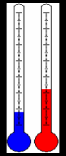
## CREW INTERFACES

- Crew Displays and Graphics Processors – Current spaceflight technologies offer limited visual performance and have uncharacterized radiation risks for long duration missions beyond LEO
  - *Target - Radiation-tolerant displays and graphics processors that can support displays with minimum of 1080p 30fps for Lunar and Mars mission durations (note - graphics processors are also applicable for other onboard processing functions)*
- Crew Voice and Audio Systems – Current systems offer limited performance and have uncharacterized radiation risks for long duration missions beyond LEO
  - *Target - Radiation-hardened system with efficient compression, speech recognition for voice control, and active noise control for Lunar and Mars mission durations*

## DATA ACQUISITION

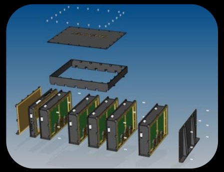
- Wireless sensor networks – Current onboard sensing requires harnessing, which incurs a mass penalty
  - *Target - Readout systems and diverse onboard wireless sensor node types*
- Data Acquisition (DAQ) Systems – Current entry descent and landing DAQ systems are too costly to deploy on wide range of missions
  - *Target - 10X cost reduction for distributed in situ monitoring of structures and subsystems on cost constrained missions*

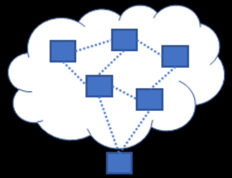




## EXTREME ENVIRONMENT AVIONICS

- Extreme Temperature/Radiation Electronics – Only limited functions have been implemented that can operate in environments with both high radiation and wide temperature ranges, including lunar/planetary surfaces and nuclear systems
  - *Target – Diverse set of circuit functions to enable systems that can operate in Lunar surface, planetary surface, and nuclear systems environments with both high radiation and wide ranges of operating temperatures*
- Packaging and Thermal Management Technologies – Current approaches limit the ability to operate at extreme cold and hot temperatures
  - *Target - Packaging and thermal management technologies that can be tailored to operate across wide temperature ranges for Lunar or planetary missions*
- Dust Tolerant Connectors – Military standard connectors offer some dust protection for terrestrial applications
  - *Target - Connectors that can protect against lunar and planetary dust while operating and surviving in extreme temperature and radiation environments*

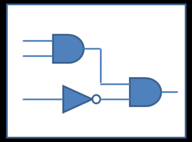
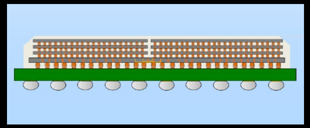
# Advanced Avionics – State of the Art





## AVIONICS ARCHITECTURES

- Interoperable Avionics – Current avionics architectures lack interoperability
  - *Target – Avionics Modular Open Systems Architectures (MOSA) allowing interoperability between a diverse set of modules*
- Avionics Cybersecurity – Current avionics lack robust defense in depth cybersecurity protection
  - *Target – Software tools providing secure boot, cybersecurity policy management, with automated detection and reaction to potential intrusions within avionics systems*
- Serviceable Avionics - Current avionics do not facilitate post-deployment robotic servicing
  - *Target – Avionics chassis and interconnect architectures that simplify crewed or robotic servicing and module level swapping*
- Space Cloud Computing - Current avionics approaches confine onboard processing within an individual spacecraft or surface element
  - *Target – Software architectures and tools that allow onboard processing applications to seamlessly utilize compute resources that are disaggregated across multiple platforms*

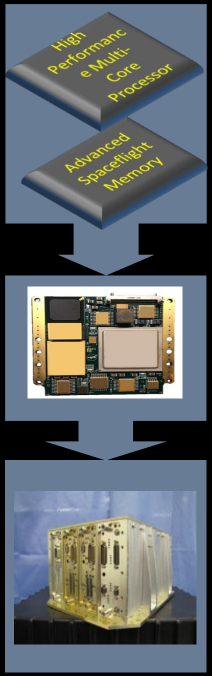
## FOUNDATIONAL TECHNOLOGIES

- Advanced 2.5D/3D Packaging and Heterogeneous Integration (HI) – These exist in industry, but lack spaceflight qualification
  - *Target - Qualified 2.5D/3D packaging and HI for NASA missions*
  - Advanced Semiconductor Process Nodes/Libraries – Existing 45nm RHBD libraries lack the density and performance needed for next generation of computing devices
  - *Target - Libraries with 2X/4X the performance/density of existing RHBD libraries*
- Low-Cost Mixed Signal ASICs – Custom mixed-signal ASIC NRE cost limits infusion
  - *Target - Radiation-hardened structured ASIC platforms to reduce NRE cost*
- Advanced COTS Microelectronics Test Systems – The cost and schedule of COTS microelectronics radiation and reliability testing is impacted by the capabilities of current test systems
  - *Target – Accelerated test preparation for radiation and reliability testing of complex microelectronics devices, thereby expediting the infusion of COTS microelectronics into avionics*

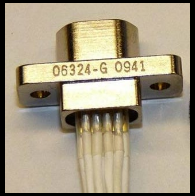
# Advanced Avionics Gap Closure Plans

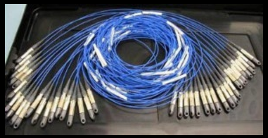
**(Green =Funded, Yellow = Partially Funded, Red = Unfunded)**

| HIGH PERFORMANCE SPACEFLIGHT COMPUTING | |
|---|---|
| Radiation-hardened general-purpose processor | Define a High Performance Spaceflight Computing (HPSC) processor concept that maximally leverages microelectronics technology advances for high reliability applications. Engage industry to develop and commercialize a radiation-hardened multi-core HPSC processor that addresses the computing needs of future NASA missions and broader markets. Leverage other government computing investments, as well as COTS developments, that are suitable for NASA use. |
| Advanced spaceflight memory | Fund the development and qualification of radiation-hardened non-volatile memory. Leverage other government agency investments in development of other radiation-hardened memory devices. Test emerging COTS memory technologies and identify devices that are suitable for NASA applications. |
| Point-Of-Load (POL) power converters | Leverage SBIR to develop intelligent, radiation-hardened multi-output POL converters that leverage industry smart power bus standards. Secure program funding for post Phase II commercialization. |
| Single Board Computer (SBC) | Define advanced avionics architectures that leverage HPSC capabilities. Develop spaceflight computer boards to demonstrate in those architectures. Engage industry to develop and commercialize spaceflight HPSC SBCs in industry standard form factors. |
| HPSC Software Tools | Port real-time operating systems, develop tools, and HPSC Middleware tools to support the full HPSC architecture. Assess existing libraries for image processing, signal processing, and machine learning, and augment as needed for HPSC architecture. |




| INTERCONNECT | |
|---|---|
| Radiation-tolerant interconnect | Leverage the HPSC concept studies and the NESC SpaceVPX Interoperability Study to select optimal interconnect standards for further development. Engage with standards organizations to ensure that evolution of selected standards meet future NASA mission needs. Assess availability of components required (i.e. endpoints, switches, physical-layer components) for a robust ecosystem for the selected standards, and leverage SBIR to develop needed components. |
| Highly reliable, high bandwidth deterministic wireless networks | Engage academic institutions to develop novel techniques that extend the capabilities of space-based wireless networks in time-sensitive and safety-critical applications. Leverage SBIR/STTR as a follow on to implement for space flight demonstration. |



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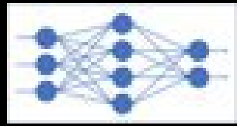
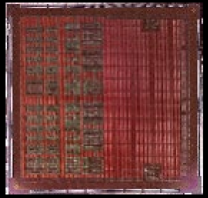
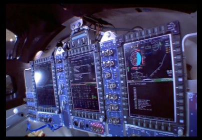
| OTHER COMPUTING ARCHITECTURES | |
|---|---|
| Artificial Intelligence (AI) coprocessor | Evaluate viability of COTS coprocessor devices and foundational technologies for NASA AI applications within the RadNeuro and the NEPP programs. Devise system-level radiation mitigation approaches to address susceptibilities in COTS devices. Demonstrate coprocessors and mitigation approaches via ground radiation testing and flight demonstrations. Study the optimal mapping of onboard (AI) applications to candidate processing architectures and devices. Develop radiation tolerant machine learning inference processor. |
| Quantum Computing | Explore candidate use cases for onboard quantum computing and compare performance with other computing technologies. Assess radiation susceptibilities of quantum computing and potential mitigations. Define concept for spaceflight quantum computer and develop prototype. |
| Low power embedded computers | Develop distributed avionics architecture to enable modular, interoperable, and reusable robotic systems. Define low power embedded computer concepts that are consistent with that architecture and can meet SWaP and extreme environmental requirements. Perform NASA development of proof-of-concept low power embedded computer, and then engage small business for further development and commercialization. |

| CREW INTERFACES | |
|---|---|
| Radiation-tolerant displays | Under ESDMD Polaris project, characterize the radiation performance of candidate display pixel technologies and support circuitry. Transfer knowledge from Polaris project to industry for development and commercialization of radiation-tolerant displays for future NASA exploration missions. |
| Radiation-tolerant graphics processing | Engage small business to characterize radiation performance of COTS Graphics Processor Units (GPUs) and develop system-level radiation mitigation approaches suitable for use in future NASA exploration missions. Specifically, develop system-level mitigation approaches for transient errors due to single event effect (SEE). |
| Heads Up Display (HUD) Optics | Advance development of Heads Up Display (HUD) optics under ESDMD Polaris project to advance xEMU displays. Continue development efforts for xEMU partnering with academia and industry. |
| Crew voice and audio systems | Engage, current NASA programs, industry partners, and small business to develop systems that can meet future mission environments and incorporate speech recognition capabilities. |







# Advanced Avionics Gap Closure Plans

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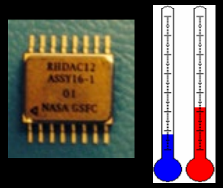
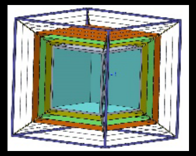
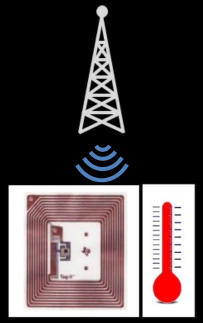
| EXTREME ENVIRONMENT ELECTRONICS | |
|---|---|
| Extreme temperature/radiation electronics | Under the SMD ColdTech and HOTTech programs along with STMD LSII and LuSTR programs, develop and characterize radiation-hardened extreme temperature design libraries in SiGe and SiC for implementation in digital and mixed-signal devices for infusion into NASA missions. Assess extreme temperature electronics from other industries for potential NASA use. |
| Avionics packaging and thermal management for extreme environments | Under the STMD PALETTE project, develop set of packaging and thermal management technologies so that avionics developers can utilize to implement passively controlled packaging for widely ranging mission environments. Infuse PALETTE technologies into lunar and planetary instruments and subsystems. |
| Dust Tolerant Connectors | Test existing spaceflight qualified connectors in relevant environments. Engage industry to enhance connector designs and materials to address issues uncovered during testing. |





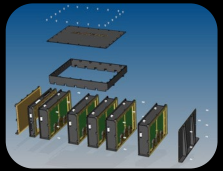
| DATA ACQUISITION | |
|---|---|
| Wireless sensor networks | Develop and demonstrate enhanced wireless sensor nodes with an implementation path for hardware that can operate reliably in harsh environments. Demonstrate in testing, support, and flight applications as needed. Specific solutions for crewed missions may be compatible with the Radio-frequency identification (RFID) Enabled Autonomous Logistics Management (REALM) system, leveraging additive manufacturing technology to provide miniaturization. |
| Low-cost, robust, high-accuracy data acquisition systems | Leverage SBIR to develop a radiation-tolerant low-cost data acquisition system technology. Secure program funding for post Phase II commercialization. |

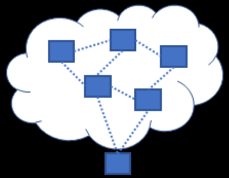


# Advanced Avionics Gap Closure Plans

**(Green =Funded, Yellow = Partially Funded, Red = Unfunded)**

| AVIONICS ARCHITECTURES | |
|---|---|
| Interoperable Avionics | Engage with industry, other government agencies, and relevant standards organizations in revising the VITA-78 (SpaceVPX) standard to ensure module interoperability. Engage with industry to develop interoperable SpaceVPX modules. |
| Avionics Cybersecurity | Leverage SBIR to develop tools for modeling avionics cybersecurity vulnerabilities. Leverage SBIR to develop onboard tools for sensing and reacting to potential intrusions within avionics. Secure program funding for post Phase II commercialization. |
| Serviceable Avionics | Assess robotic servicing options and constraints for harnessing mating and de-mating, as well as avionics module removal and insertion. Prototype and evaluate serviceable avionics implementation options. Engage industry and other agencies to develop serviceable avionics standards. |
| Space Cloud Computing | Explore candidate use cases for space cloud computing and model their performance on cloud computing architectural options. Engage industry to develop software tools implementing optimal cloud computing architectures. |

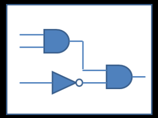


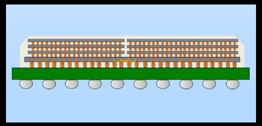


# Advanced Avionics Gap Closure Plans

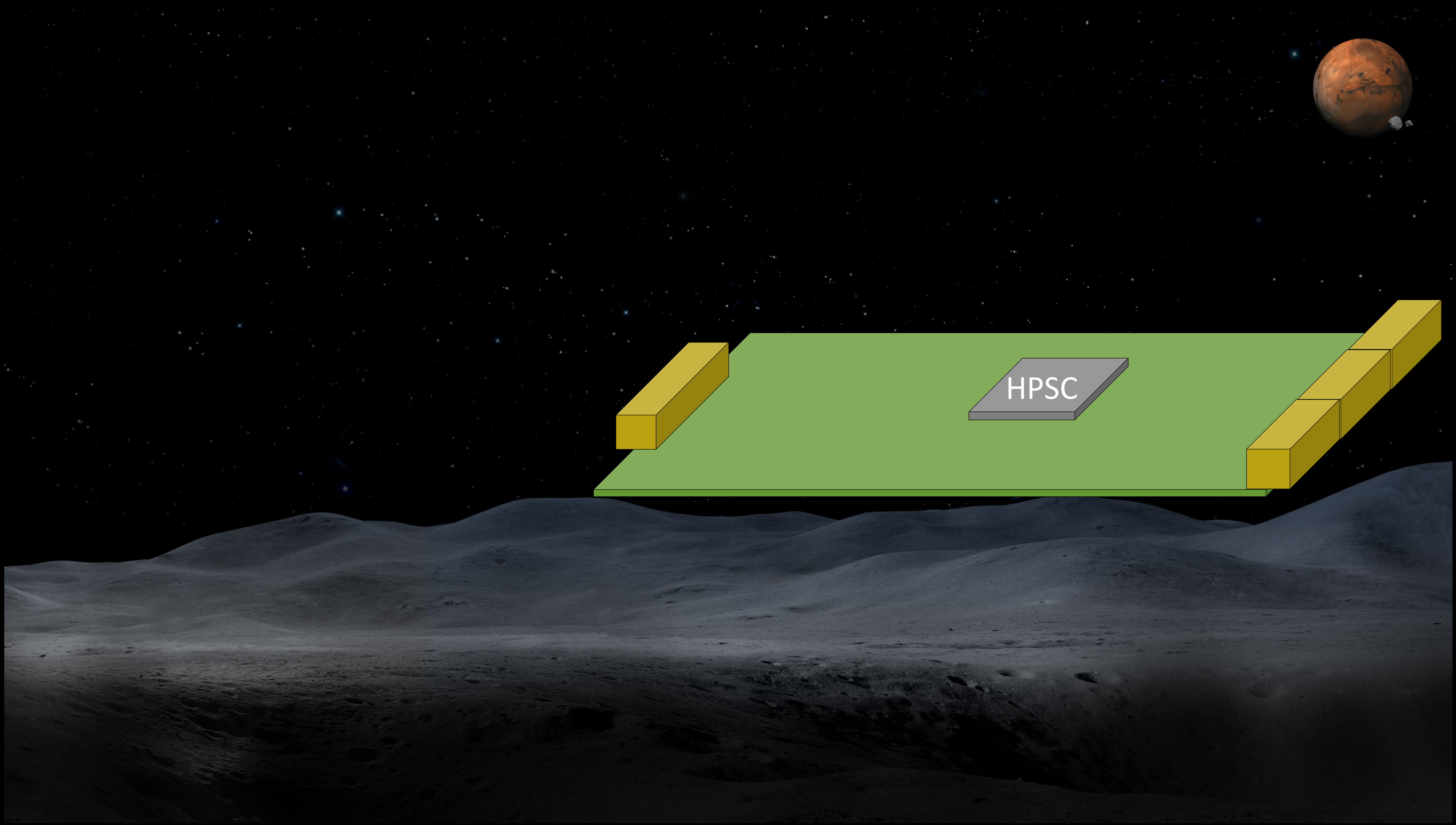
**(Green =Funded, Yellow = Partially Funded, Red = Unfunded)**

| FOUNDATIONAL TECHNOLOGIES | |
|---|---|
| Advanced 2.5D/3D packaging and heterogeneous integration | Develop conventional and additively manufactured 2.5D and 3D packaging technologies for low production volume devices. Engage Nextflex consortium to develop qualification methods for additively manufactured spaceflight electronics, and then demonstrate on smallsat missions. Engage industry on the development of qualification methods for 3D packaging. |
| Advanced Semiconductor Process Nodes/Libraries | Under NASA STMD funding, perform radiation characterization and modelling of the Global Foundries 22FDX process and automotive grade design libraries. Leverage other government and industry efforts in radiation-hardened deep submicron processes and libraries. |
| Low-Cost Mixed Signal ASICs | Engage industry to develop radiation-hardened mixed-signal structured ASIC platform to broadly meet NASA mission needs. |
| Advanced COTS Microelectronics Test Systems | Leverage SBIR to develop advanced test systems for COTS microelectronics that provide improved insight into device behavior, accelerate the development of device-specific test configurations and execution code, and expedite radiation and reliability tests. |

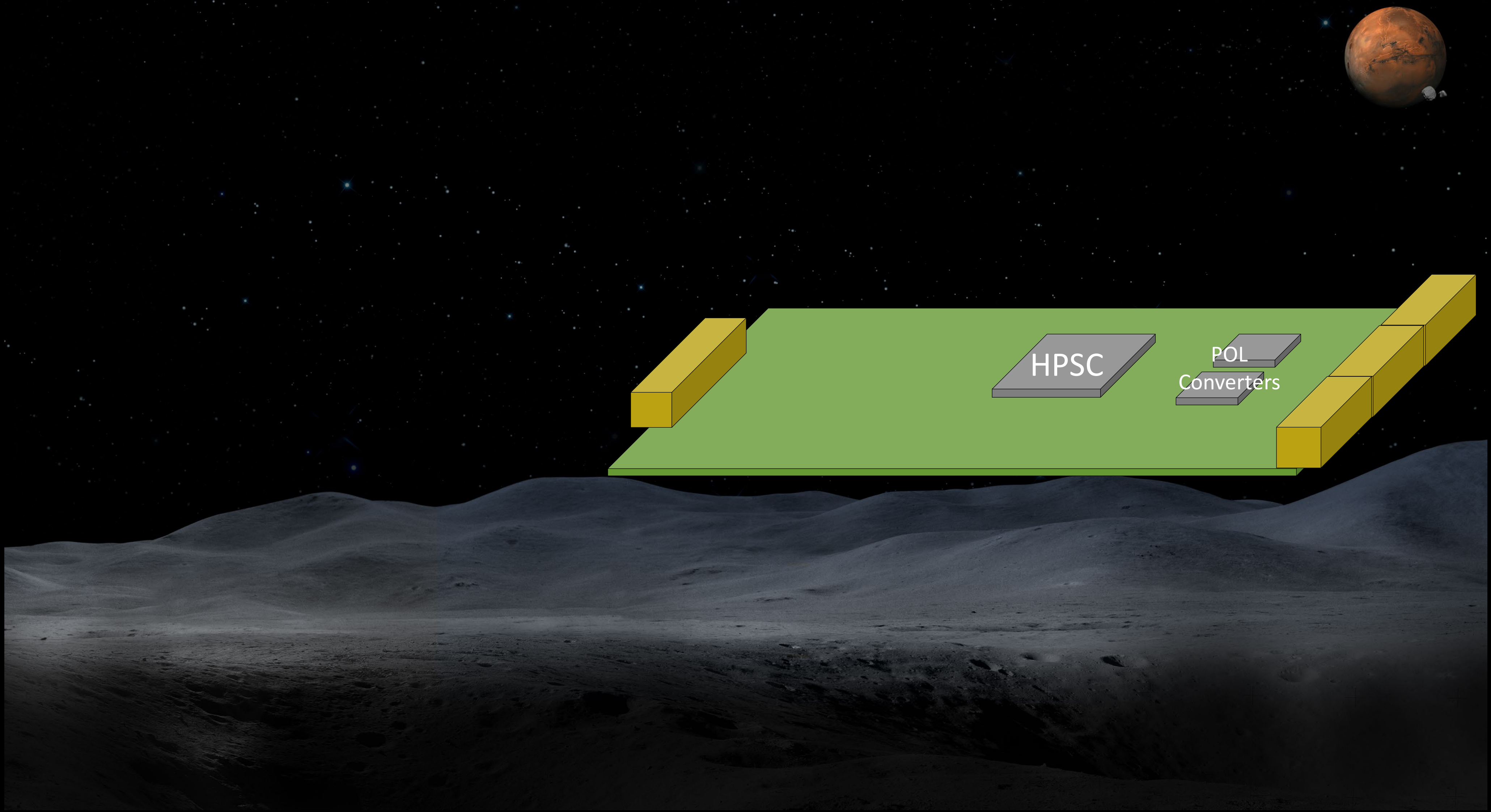




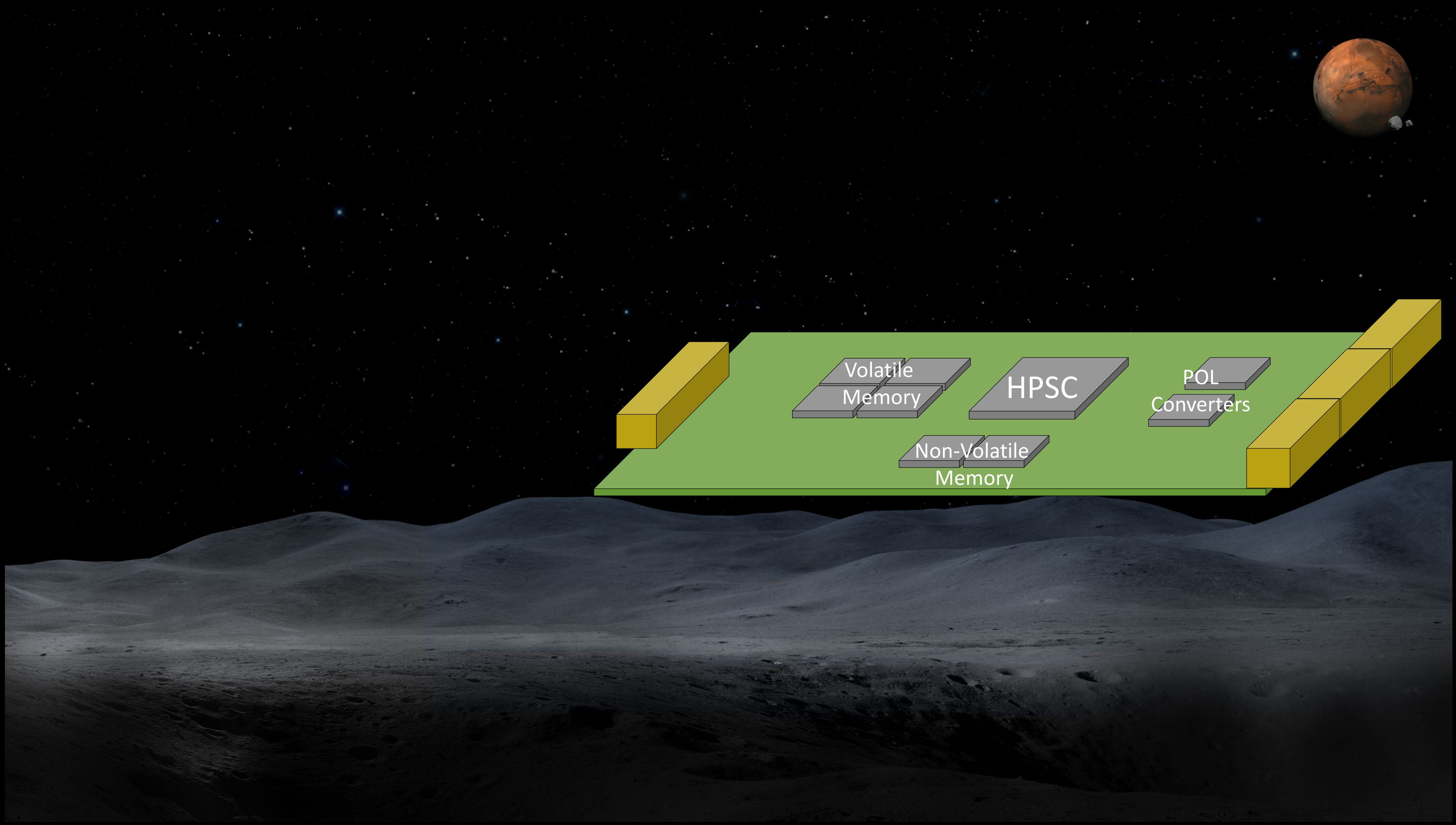
# Computing Technologies – System Context



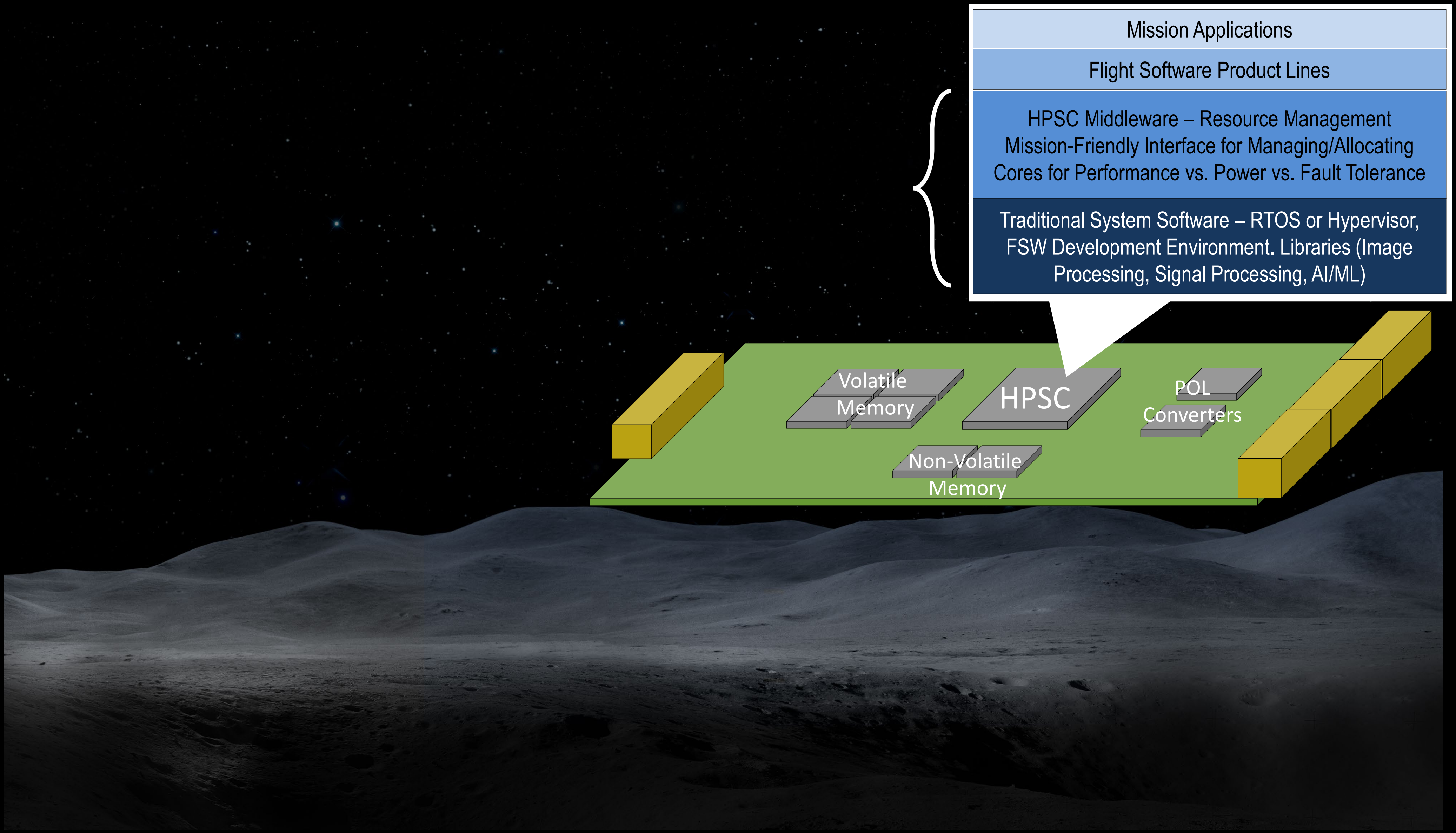
# Computing Technologies – System Context



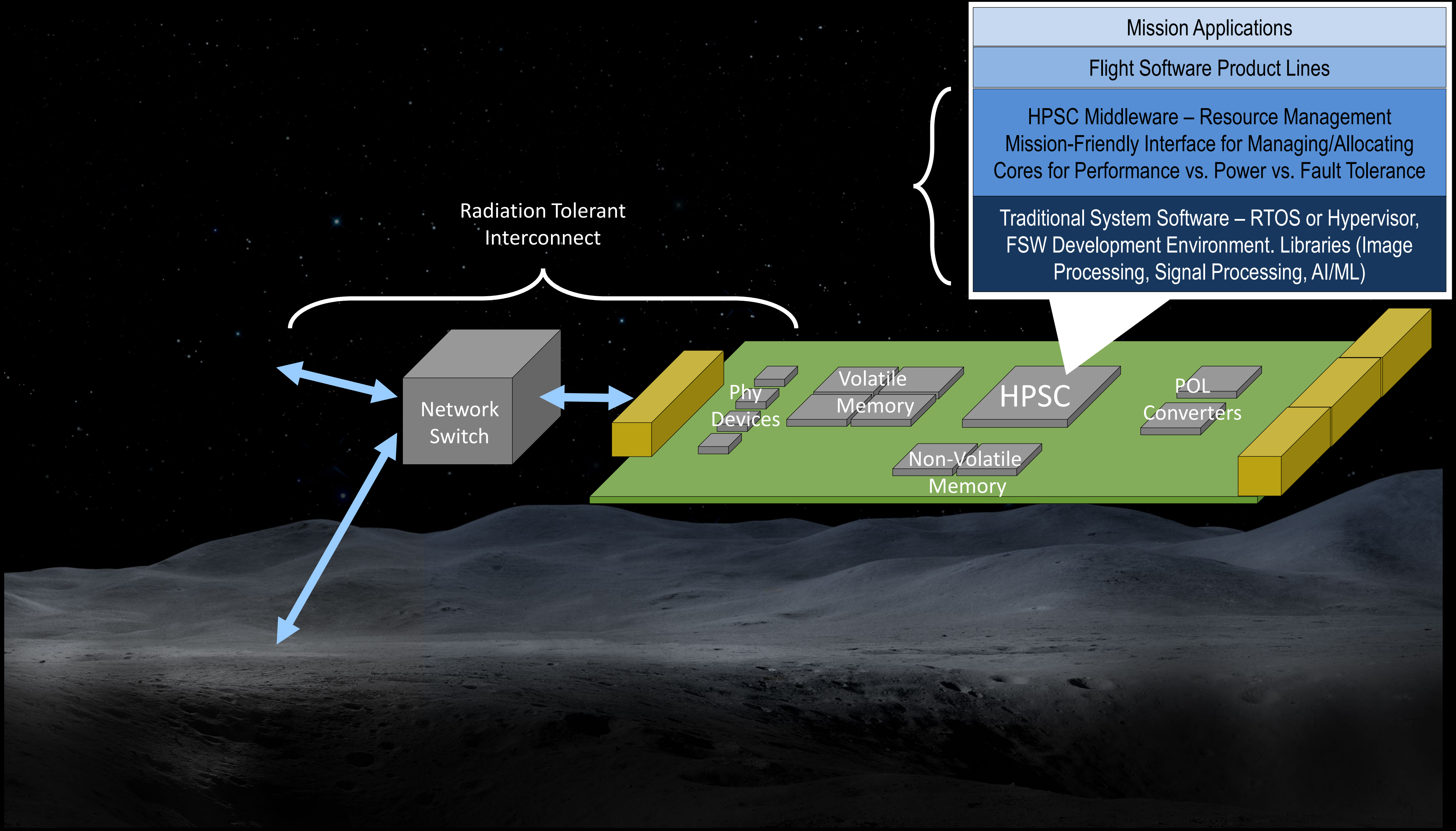
# Computing Technologies – System Context



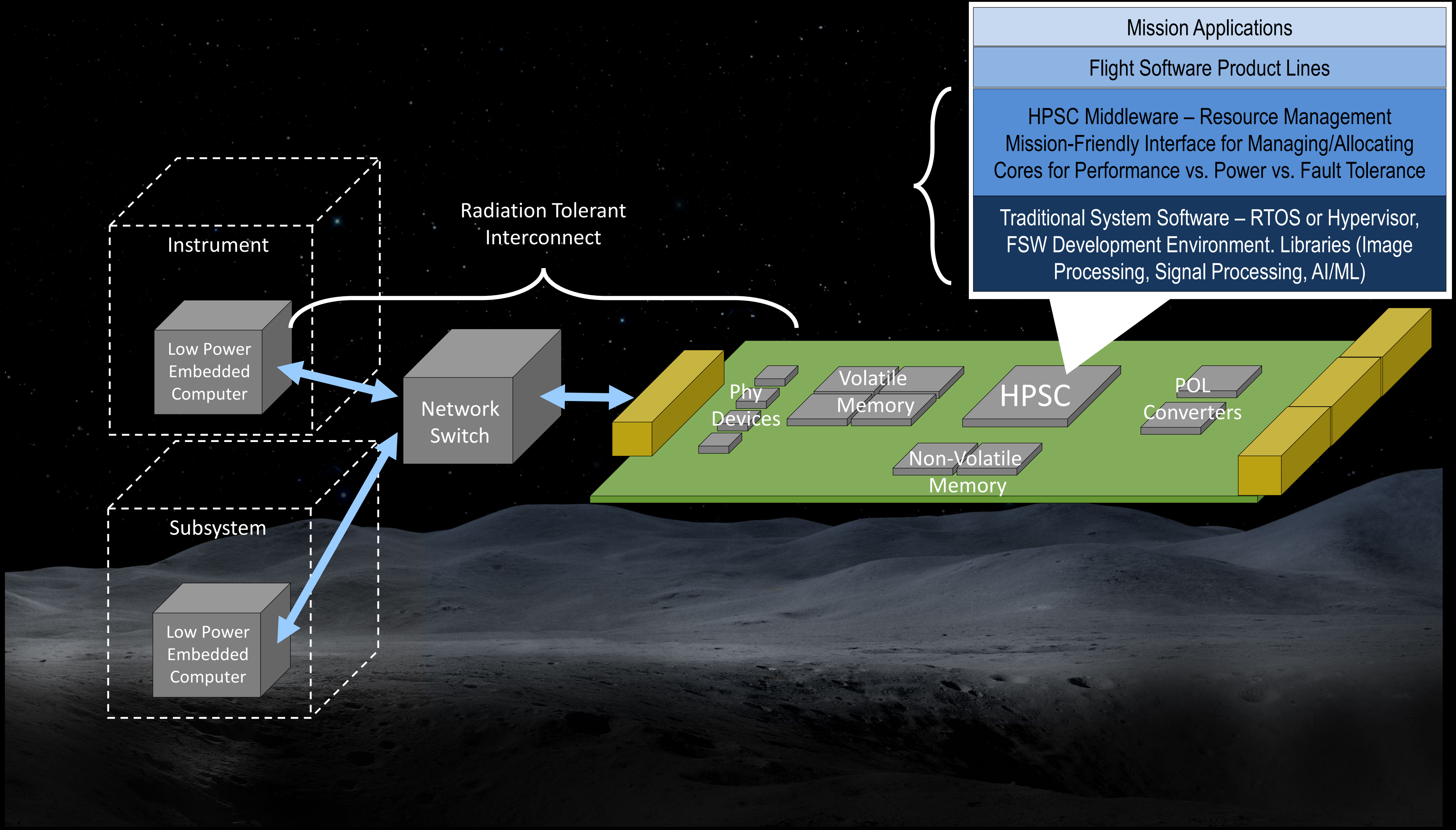
# Computing Technologies – System Context



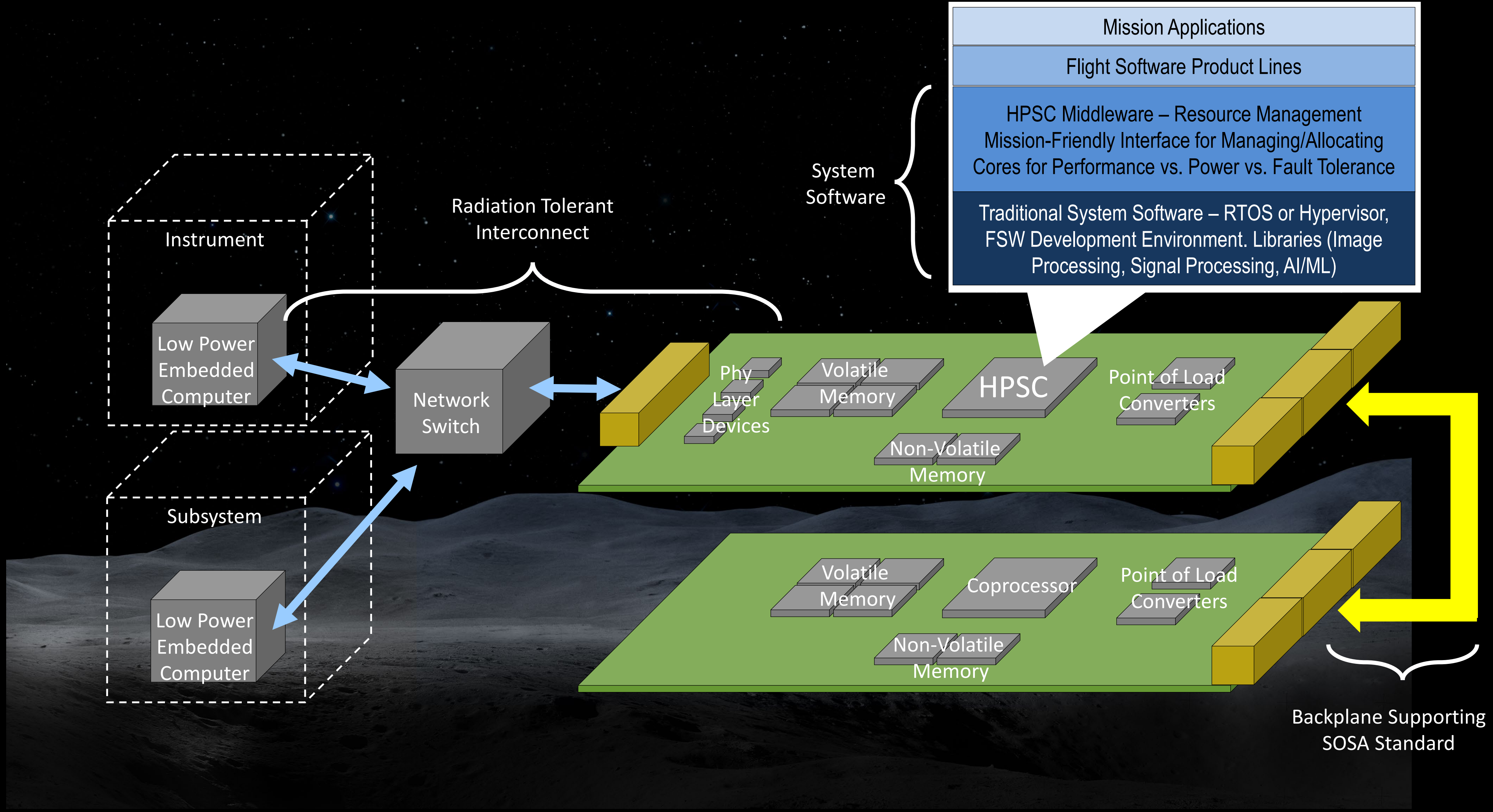
# Computing Technologies – System Context



# Computing Technologies – System Context



# Computing Technologies – System Context



# HPSC Overview

Following an HPSC concept study phase, Microchip was selected to develop the HPSC – including processors, evaluation boards, and system software

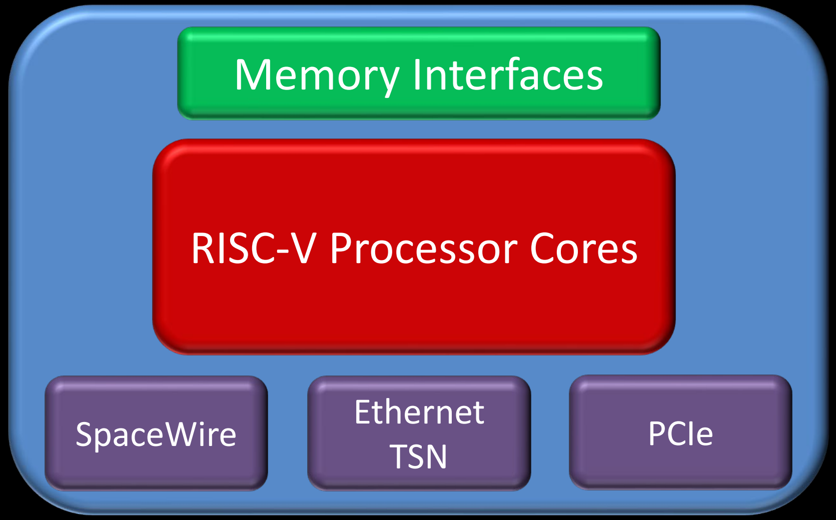
- $50 million firm-fixed-price contract was awarded
- Microchip is contributing significant research and development costs to complete the project
- Estimate prototype SoCs and evaluation boards available in 2024 and space qualified SoCs in 2025
- Target to have QML-Y qualified parts

Key HPSC features

- Based on the RISC-V ISA
- Achieves 100X scalar processing performance improvement over the existing RAD750 processor
- Provides vector processing and machine learning acceleration capabilities that are unavailable from current spaceflight processors
- Provides a wide envelop for power/performance/fault tolerance scaling

Interfaces supported

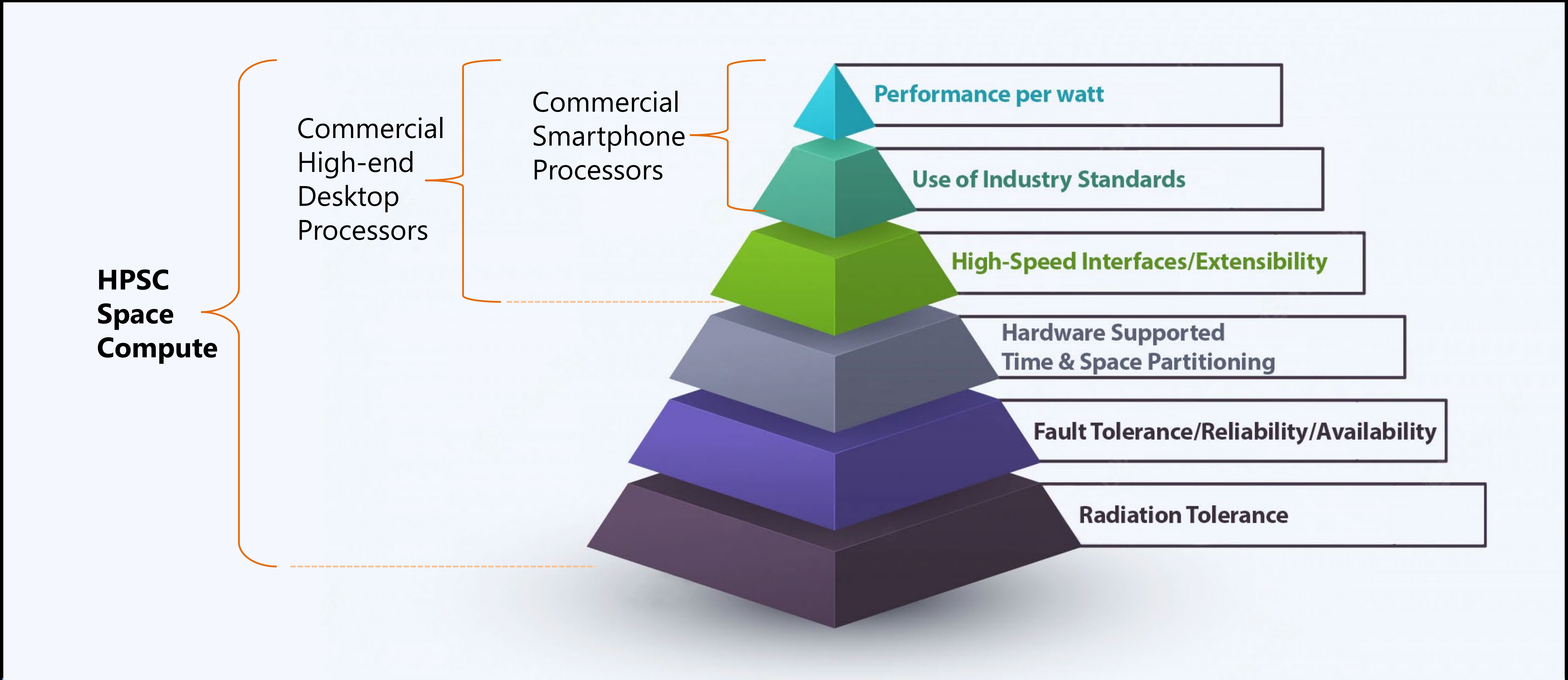
- Ethernet with Time Sensitive Networking (TSN)
- PCIe
- SpaceWire


HPSC Processor

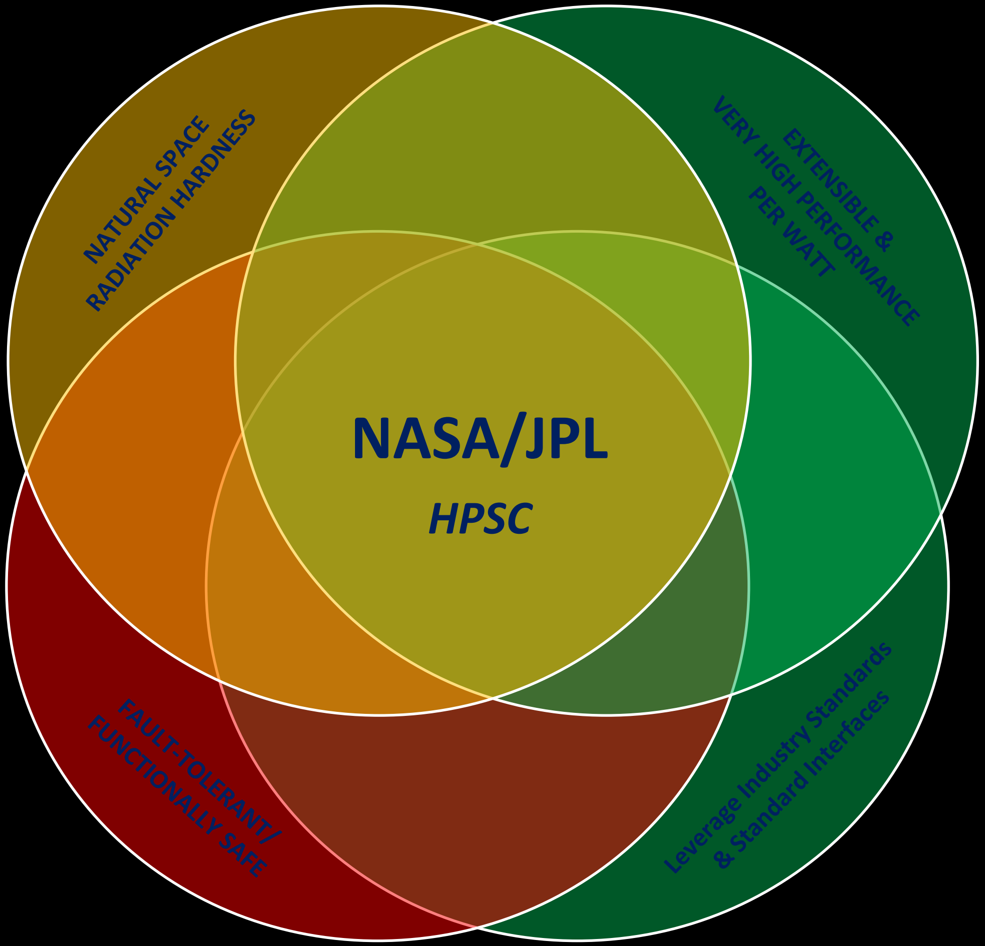
(U) UNCLASSIFIED

# Necessary Capabilities of Space Compute HW



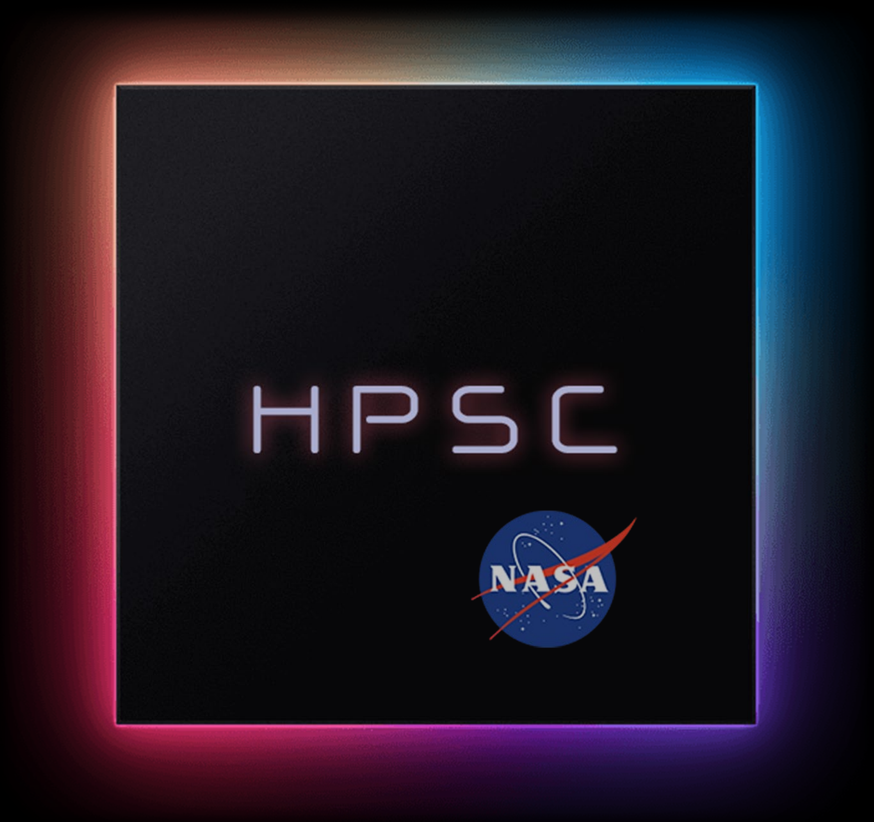

**Radiation Tolerance and Fault Tolerance Are Foundational Critical Capabilities**

# HPSC – Guiding Principles




- **HPSC Prime Directive** Deliver modern disruptive and extensible performance, performance per watt, and fault-tolerance to enable NASA & JPL to support the ever-increasing levels of mission autonomy and complexity while simultaneously reducing development cost, risk, and time.

# HPSC – What HPSC Is

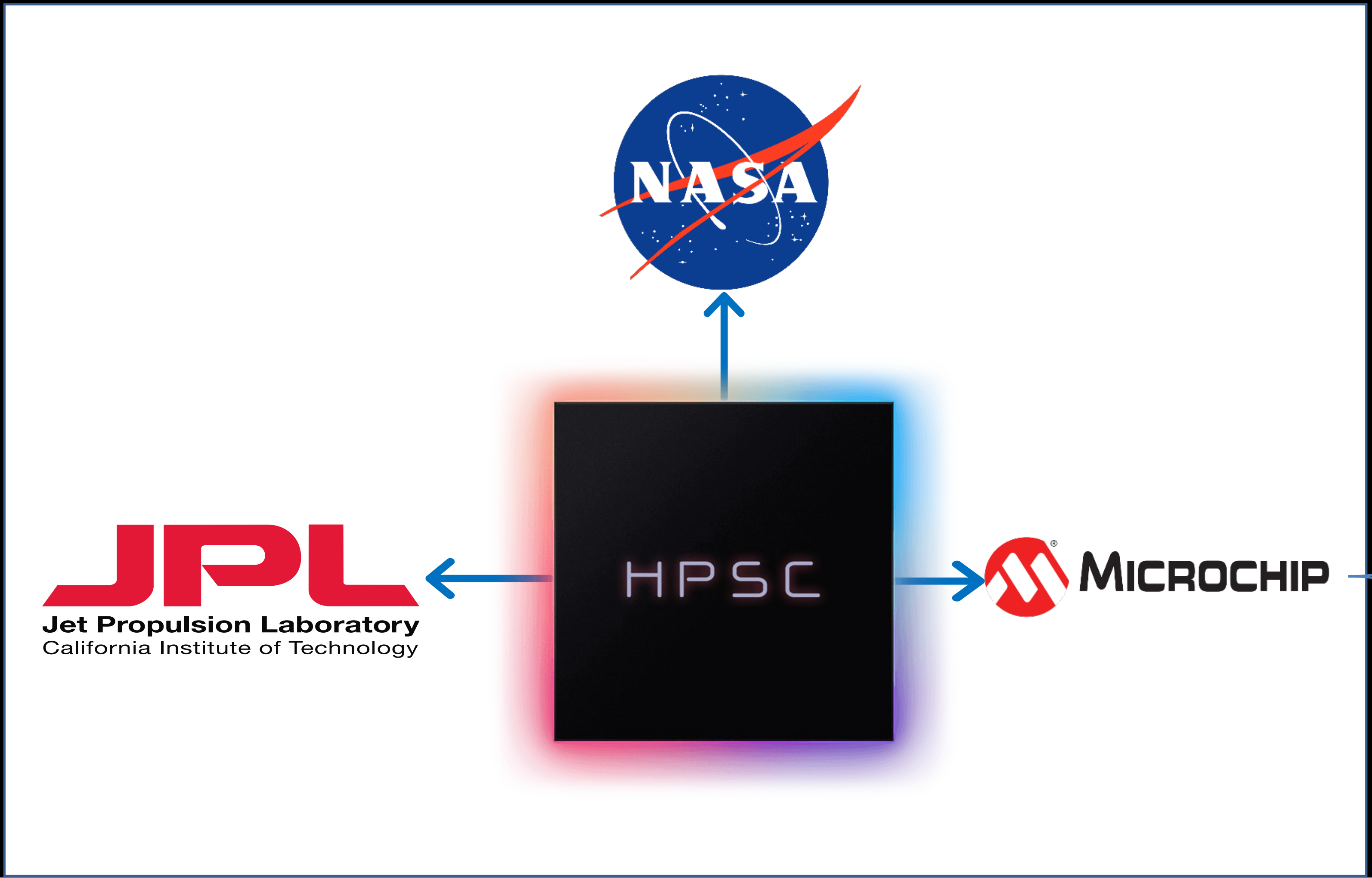



- HPSC is a multi-core RISC-V System-on-Chip (SoC)
  - **Fault-Tolerant. Functional Safety.**
  - **Software-Defined functionality.**
  - **Extensible**. Low power/single chip to Multi-chip/Asymmetrical Supercomputer class capability. AI/ML, Vector acceleration.
  - **Industry standards.** Interfaces. Software. Systems.
  - **Efficiency**. Extremely high performance per watt.
  - **Complete Platform Security.** From manufacturing to user data.

- **HPSC Project deliverables**
  - HPSC SoC
  - Evaluation Board
  - Software Stack (BSP)
  - Training, Application Notes, Reference Designs
  - HPSC Eco-System and Marketplace
  - Estimate prototype EVBs/SoCs in 2024 and full space qualified SoCs in 2025

**Disruptive Performance per watt Enables Key Mission Capabilities with Low SWaP-C**

# HPSC – Industry Markets




**Commercial Space**

Civil: Earth Observation, Weather
Commercial: TV, Mobile Voice/Data

**Commercial Aviation**

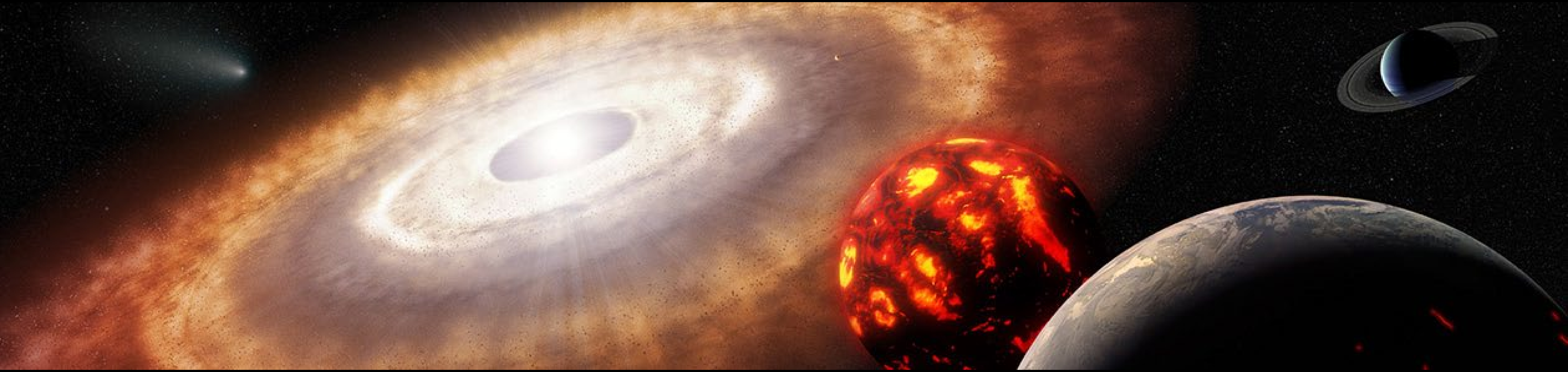
Avionics, Actuation, RF & Microwave Systems
Engine Systems & Control, Cabin Management

**Defense**

ISR
Navigation, Early Warning Systems
Launch Vehicles, Strategic Weapons
Radar/Electronic Warfare (EW)
Secure Comms, Embedded Compute

**HPSC Enables NASA and JPL's Mission Needs: Also the Commercial World**

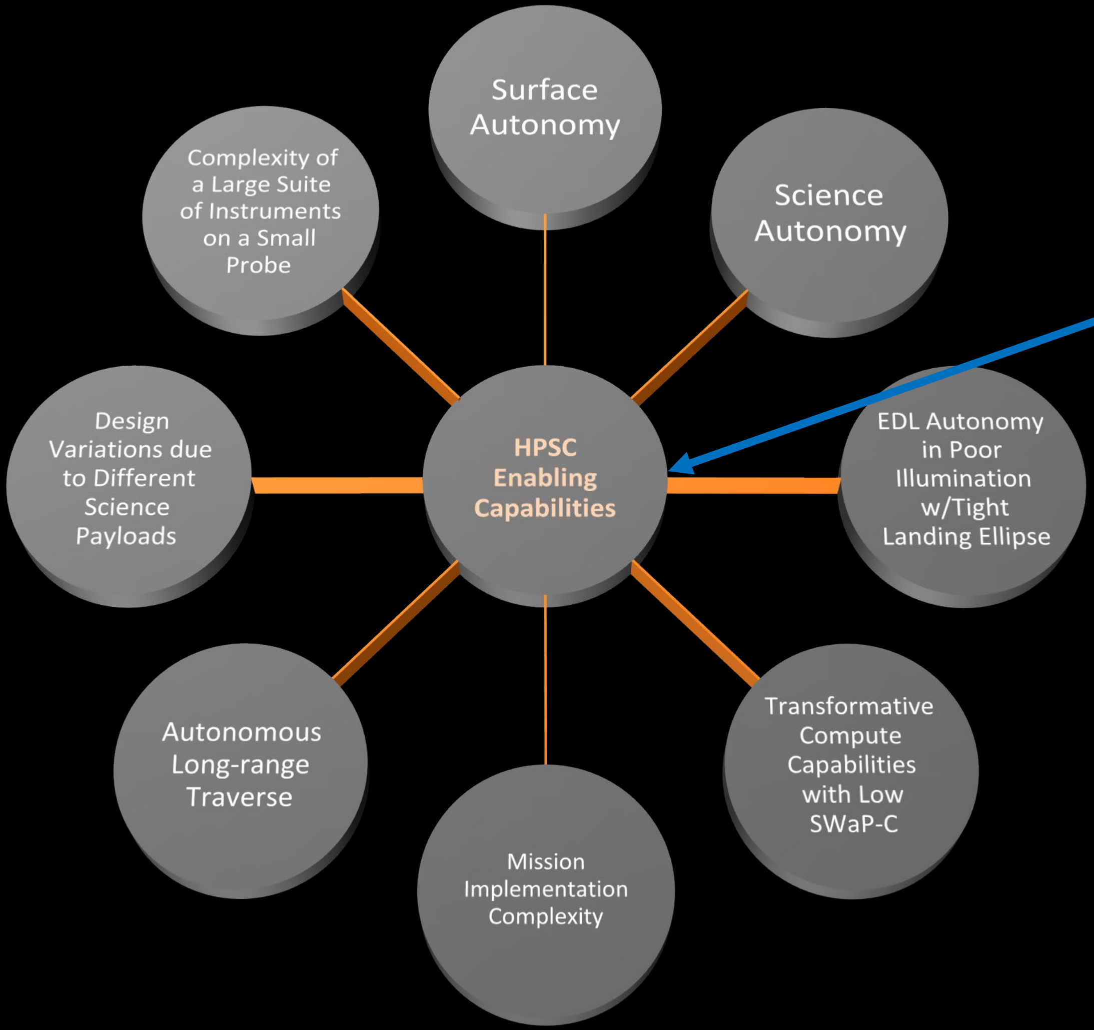
# NASA/NSF Planetary Science and Astrobiology Decadal Survey 2023-2032



The Planetary Science and Astrobiology Decadal Survey 2023-2032 assesses key scientific questions in planetary science and astrobiology, identifies priority medium- and large-class missions and other initiatives, and presents a comprehensive research strategy for the 2023-2032 timeframe.

https://www.nationalacademies.org/our-work/planetary-science-and-astrobiology-decadal-survey-2023-2032

# HPSC: Key to Realization of the Decadal 2032 Roadmap




## HPSC Enabling Capabilities

- Game-changing performance gain over current space compute with same power.
- Very high performance per SWaP-C.
- Dynamically scalable power & performance.
- Fault-tolerance and radiation tolerance.
- Extensible performance & power enabling mission customization.
- Reduced development time & cost.
- Ease of implementation variations (support of SW defined capabilities).

**HPSC Addresses a Significant Number of Key Identified Mission Obstacles**

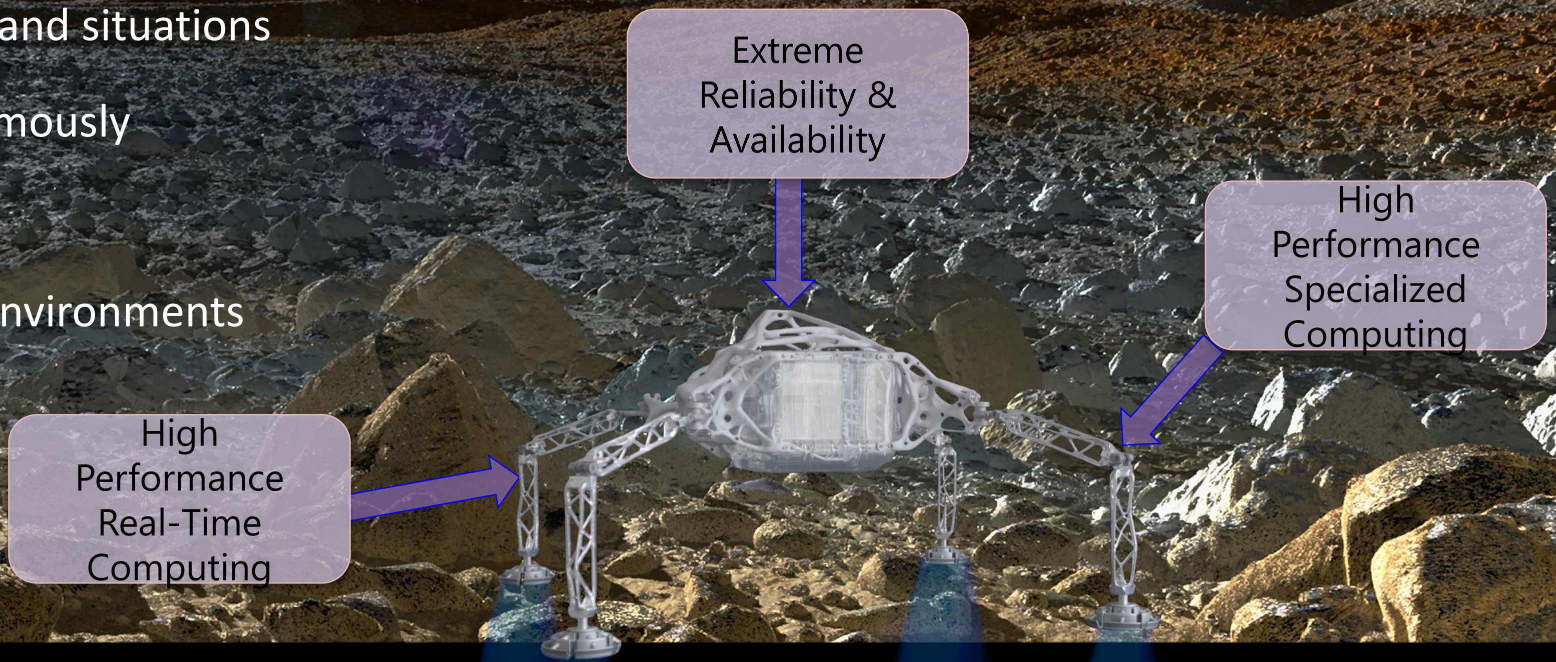
# HPSC – Why is it Critical for NASA?

- **Mission Trends – Increasing Levels of Autonomy for Future Missions**

  *Necessitating revolutionary advances in space computing*

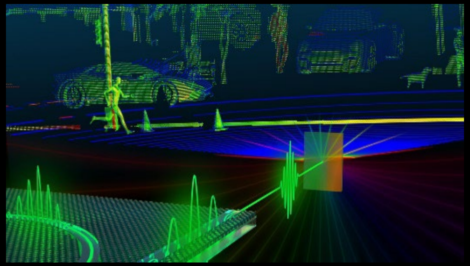
## Autonomous In-Situ Planetary Exploration

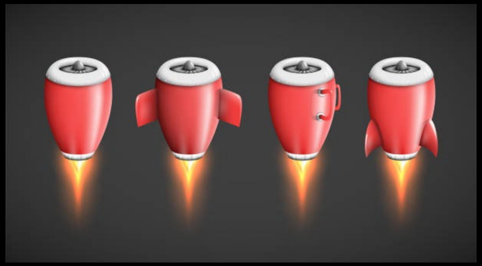
- Ability to handle unknown environments and situations
- Ability to plan and make decisions autonomously
- Carry out complex science autonomously
- Operate reliably in the harshest of space environments



# What is "Autonomy" ?

- **Enabling Complex Autonomy is Critical**



**Sense**
- Image Processing
- Remote Sensing

**Perceive**
- Image Processing
- Remote Sensing
- Orbital Orientation
- Communication

**Decide**
- Mission planning
- Orbital Orientation
- Communication

**Actuate**
- Orbital Maneuvering
- Surface Maneuvering
- Orbital Orientation
- Communication


To be presented remotely at the 2023 Space Computing Conference (SCC) Closed Session, July 21, 2023

# HPSC Architecture Highlights

Advanced
**FinFET** Process

**Machine Learning**

Multi-Core
**RISC-V**
Space Compute

Time Sensitive
**Ethernet**
Networking

**PCIe**


SWaP Optimized Heterogenous
**Fault Tolerant**
Architecture

Real-time Processing

Deterministic Latency

**Vector Engines**

Secure Enclave

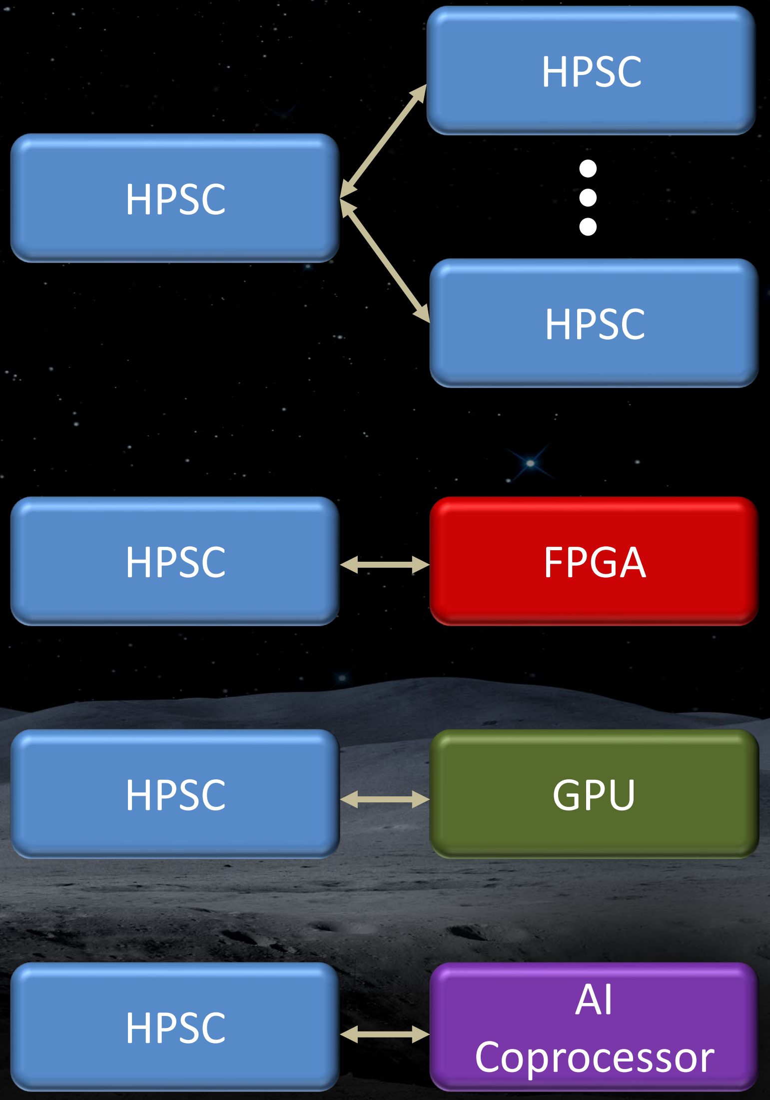
Co-processor Interfaces

Extensible Power & Performance

# HPSC Extensibility

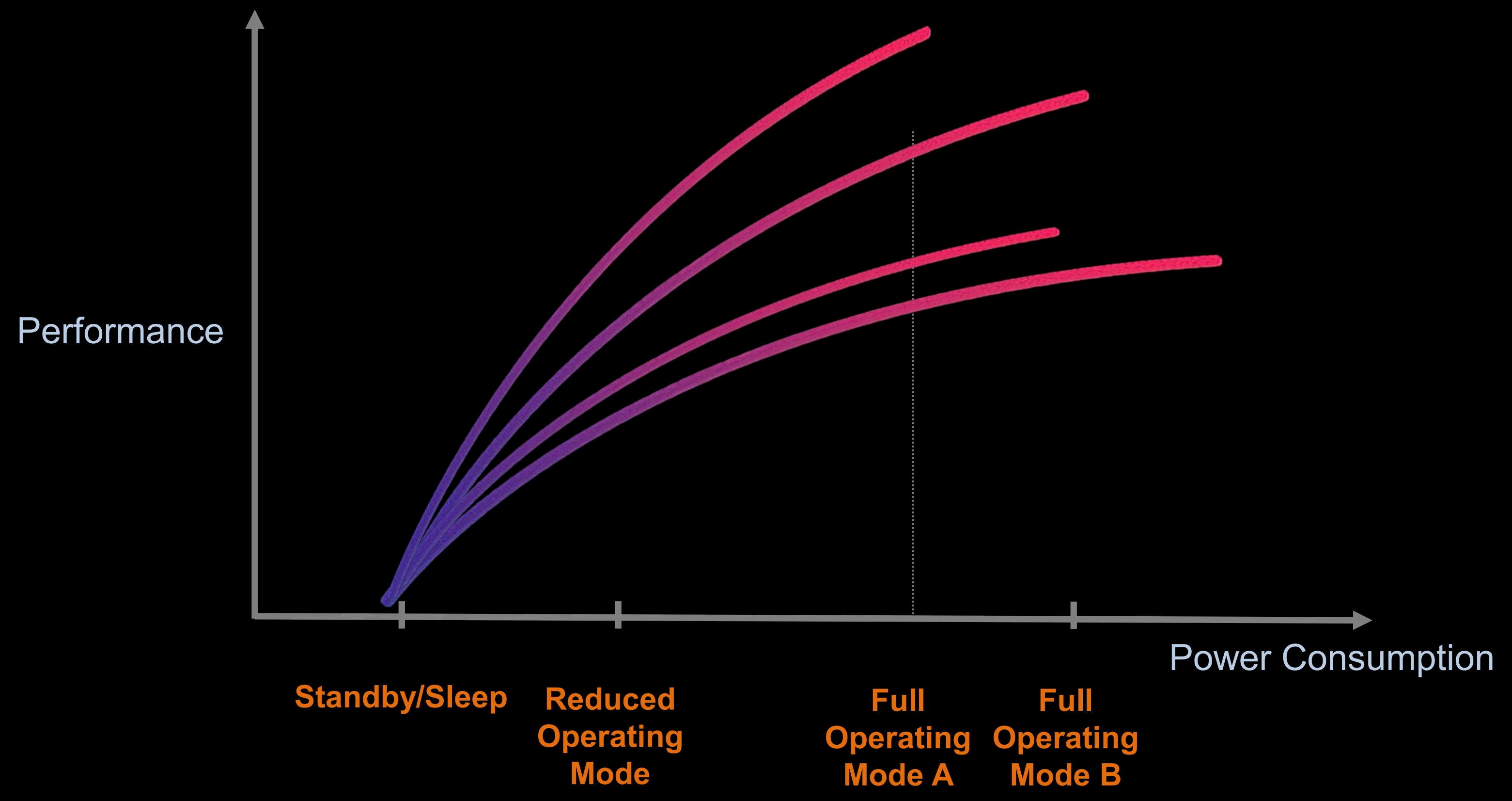
## *HPSC Embraces **Extensibility***

- Mission customizable extensibility
- Extend for :
  - Performance
  - Increased performance/watt
  - Interface Bridging
  - Mission specific functionality
  - Fault Tolerance



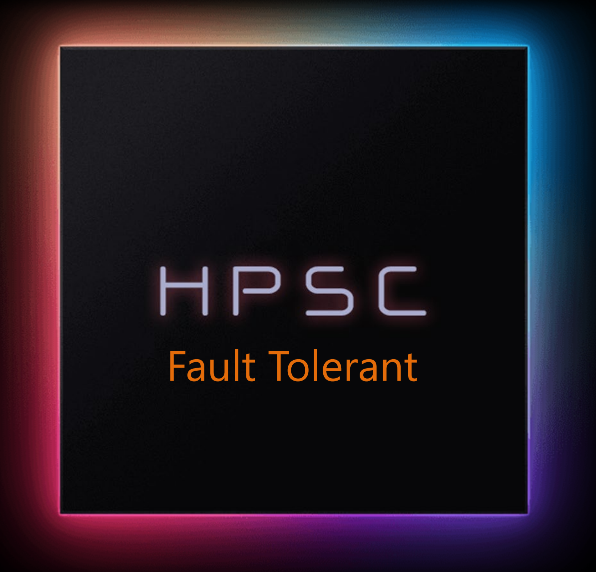
# HPSC Scalability: Small to Large

## Power, Performance, Fault Tolerance and other Functions: Scalable via Software Control




**HPSC Performance & Power are Dynamically Tunable based on Mission Needs**

# Fault Tolerance: A Layered Approach




| | | |
|---|---|---|
| Layer 6 | SW Application Layer Fault Tolerance (optional per use-case) | Application Software |
| Layer 5 | SW Managed FT, Health Monitoring of HW, SW mods to HW QoS | Middleware |
| Layer 4 | FT hooks for middleware to utilize | OS Software |
| Layer 3 | HW-based Fault Tolerance | SoC Hardware |
| Layer 2 | HW Fault Detection Boundaries/Containment Regions | SoC Hardware |
| Layer 1 | At-site Error Detection/Correction (parity checking, ECC) | SoC Hardware |
| Layer 0 | Process Technology & SEE Hardened Cells | SoC Hardware |



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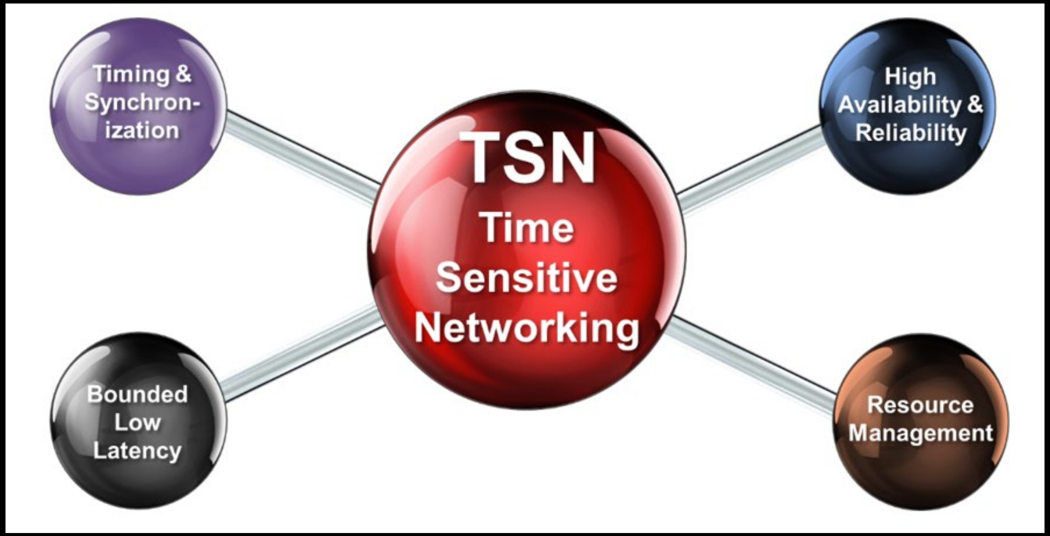
# Time-Sensitive Networking : TSN

**TSN an IEEE 802 standard** - enables us to transmit time-critical traffic over a standard ethernet physical medium, side by side with conventional ethernet traffic

**Time-Sensitive Networking (TSN) Profiles** (Selection and Use of TSN tools)

| Audio Video Bridging [802.1BA/Revision] | Fronthaul [802.1CM/de] | Industrial Automation [IEC/IEEE 60802] | Automotive In-Vehicle [P802.1DG] | Service Provider [P802.1DF] | Aerospace Onboard [IEEE P802.1DP / SAE AS6675] |
|---|---|---|---|---|---|




- **TSN Components (TSN toolset)**:
  - **Time Synchronization**
  - **Bounded Low Latency**
  - **High Availability / Ultra reliability**
  - **Resource Management & API**

Path Selection, Reservation, and Fault Tolerance

Scheduling and Traffic Shaping

Resource Management

Timing & Synchronization

**TSN 802.x spec Categories**



To be presented remotely at the 2023 Space Computing Conference (SCC) Closed Session, July 21, 2023

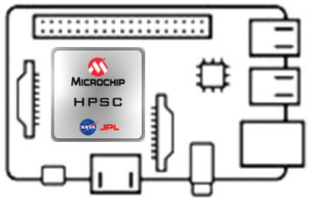
# NASA's HPSC Ecosystem Needs

## *SpaceVPX*

- Objective: Increase use of standardized COTS solutions
  - Accelerate speed of development & reduce cost
- Published SpaceVPX interoperability report to define NASA's needs
- Target 3U and 6U SpaceVPX solutions

## *Single Board Computers (SBCs)*

- Leverage flight-ready HPSC-based SpaceVPX SBCs from the industry
- Opportunity for vendors to expand HPSC-based SBCs into other form factors for broader aerospace and defense market




## *Interoperable Modules*

- Need for HPSC companion SpaceVPX modules
  - Storage, FPGA, etc.
- Aligning data plane, control plane and expansion plane interconnect to *Ethernet, SpaceWire and PCIe*

## *Commercial & Open-Source Software*

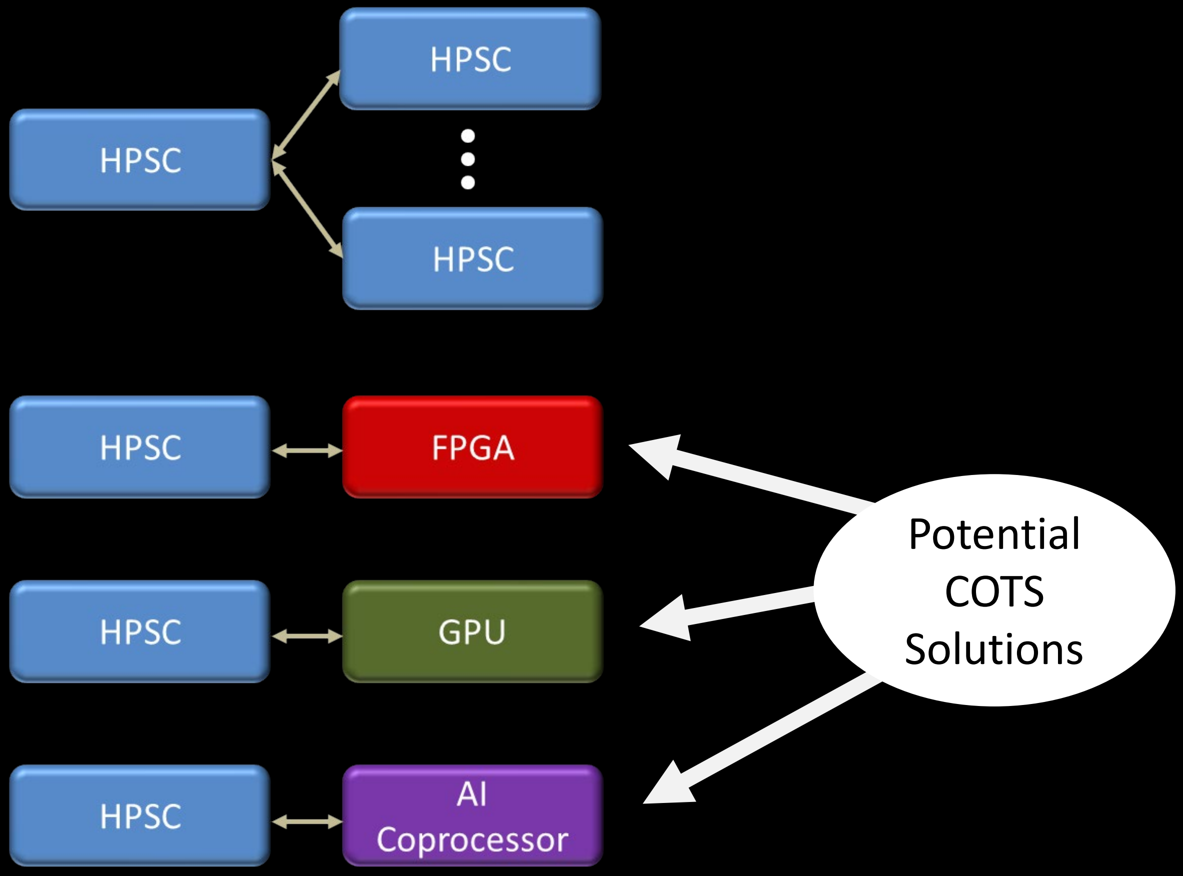
- Operating Systems
  - Open-source
  - Commercial RTOSes
- Modern Tools



To be presented remotely at the 2023 Space Computing Conference (SCC) Closed Session, July 21, 2023

# What About COTS?

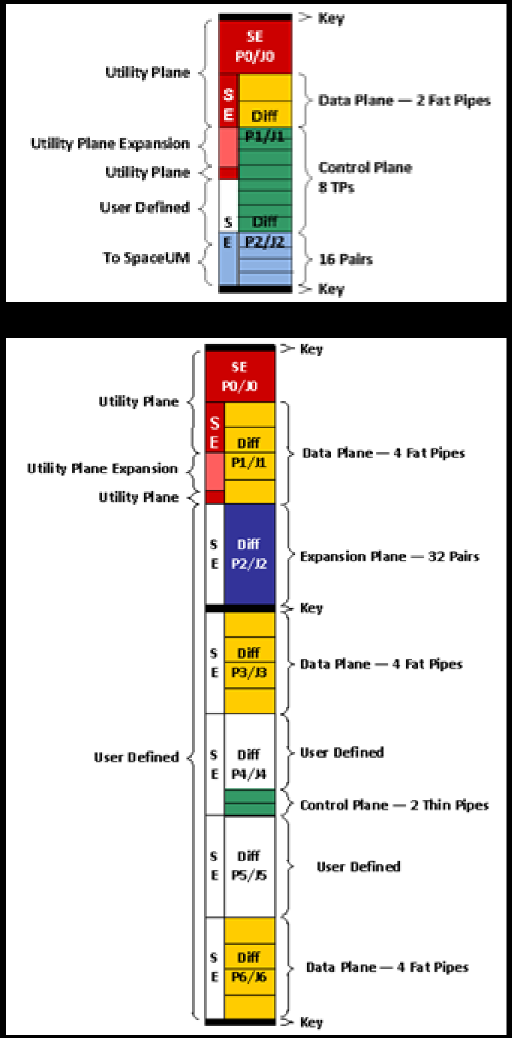
- While much of NASA's emphasis within avionics is on HPSC, there is also a role for COTS processing solutions
- Use of COTS computing technologies must be guided by Mission, mission Environment, Application, and Lifetime (MEAL) principles
- COTS parts from Industry Leading Parts Manufacturer (ILPM) are preferred
- Note that the broader HPSC ecosystem may leverage COTS coprocessors



# NASA and SpaceVPX

- As NASA missions become more frequent, interconnected, ambitious, varied and complex, the need for an ecosystem of interoperable avionics modules becomes more important due to the cost, complexity, and the need to maintain distant systems for long durations
- The previous NASA-developed and widely adopted standard for backplane-based chassis interconnect, cPCI is over 20 years old and no longer supports modern architectures. cPCI has fallen by the wayside and no other standard has risen to replace it
- Stacked-card avionics, including MUSTANG, have arisen that address applications that require limited bandwidth communication between modules
- However, no standard architecture supporting high-bandwidth, tightly coupled modules, has emerged, resulting in ad hoc, non-optimal box level avionics, with attendant impact on cost, risk, schedule

- The existing SpaceVPX industry standard, as specified in VITA-78, addresses some of the needs of the space avionics community, but falls short of an interoperability standard that would enable reuse and common sparing on long duration missions and reduce non-recurring engineering (NRE) for missions in general




3U and 6U Slot Profiles [VITA-78]

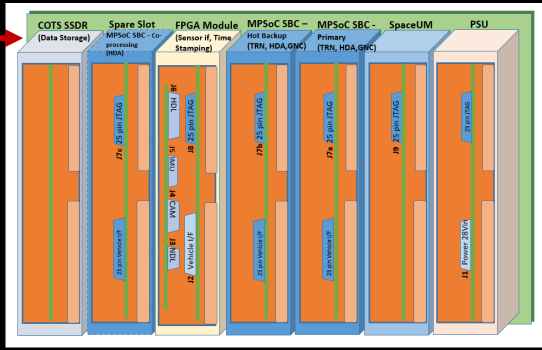
# SpaceVPX Overview

SpaceVPX is an architecture standard that defines modules, backplanes, and chassis for spaceflight avionics boxes (the SpaceVPX standard is managed by VMEbus International Trade Association (VITA) as VITA-78)

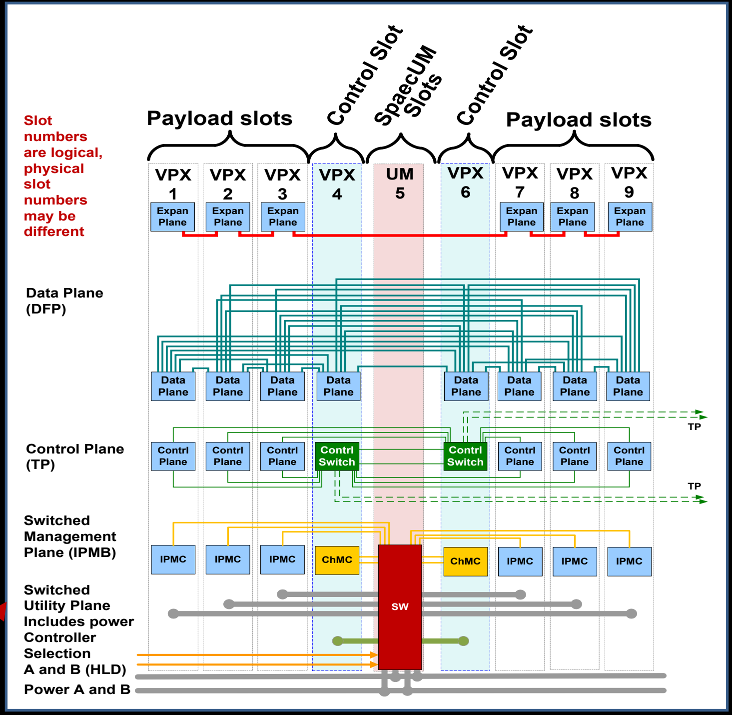
SpaceVPX adapts a Modular Open System Approach (MOSA), derived from VPX and OpenVPX (VITA-65), for space

SpaceVPX defines several general module types and how they can be interconnected, using the concept of “profiles”

- Slot Profile – A physical mapping of ports onto a slot’s backplane connectors
- Module Profile - Extends a slot profile by mapping protocols to a module’s ports and defines physical dimensions
- Backplane Profile - Defines number and types of modules supported and their interconnection topology




| Profile Name | Data Plane 4 FP | Expansion Plane P2/J2 | Control Plane 2 TP | User Defined |
|---|---|---|---|---|
| | DP01 to DP04 | | CPtp01 to CPtp02 | P3/J3, P5/J5 |
| MOD6-PAY-4F1Q2T-12.2.1-1-cc | sRIO 2.2 at 3.125 Gbaud per Section 5.2 | sRIO 2.1 at 3.125 Gbaud per Section 5.2 | SpaceWire per Section 5.2.1 | User Defined DIFF pins |



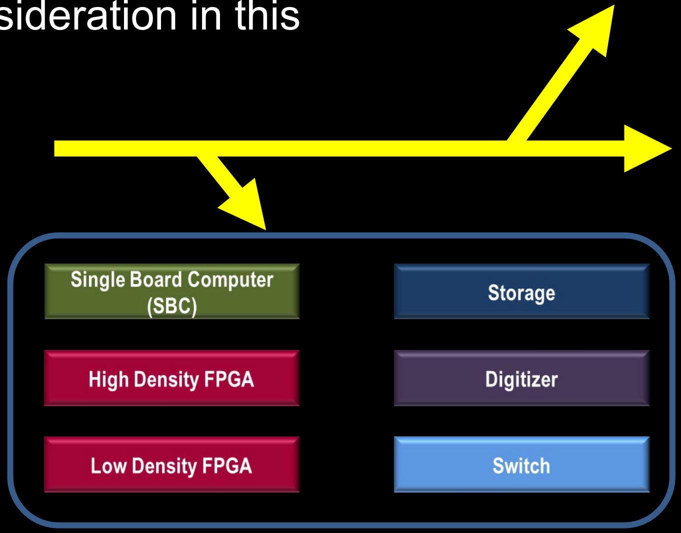

[VITA-78]

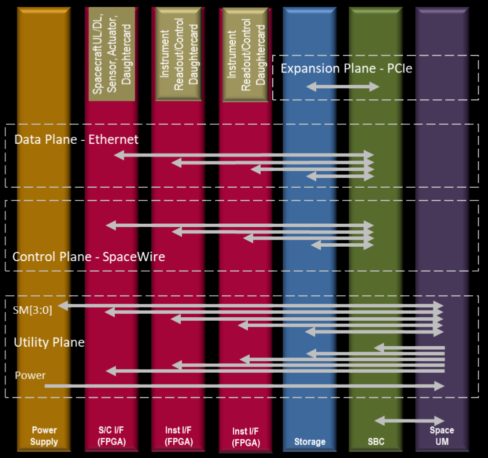
**Problem statement – There is so much flexibility within SpaceVPX that it’s possible to implement two different modules that are fully compliant with the standard yet cannot interoperate**

# NASA SpaceVPX Interoperability Study

- A NASA Engineering & Safety Center (NESC) study was conducted to address the deficiencies in the SpaceVPX standard for NASA missions and define the recommended use of the SpaceVPX standard within NASA
- The study team was comprised of subject matter experts across NASA (GSFC, JSC, LaRC, JPL)
- The future infusion of NASA's High Performance Spaceflight Computing (HPSC) processor into SpaceVPX systems was a consideration in this study
- Study results included:
  - Proposed interoperable SpaceVPX specification
  - Candidate module types
  - Example systems
- The full study report can be found at:
  - https://ntrs.nasa.gov/citations/20220013983

| | Proposed NASA Specification |
|---|---|
| RT-1 | **General**<br>Support dual redundant and single string SpaceVPX systems. |
| RT-2 | **Power distribution and management**<br>Utilize the 5-output SpaceUM (SLT3-SUM-5S1V3A1R1M3C-14.7.2) for 3U implementations with a 5V main power voltage.<br>Utilize the 8-output SpaceUM (SLT6-SUM-8S3V3A1B1R1M4C-10.8.1) for 6U implementations with +12, +5, and +3.3 main supply voltages. |
| RT-3 | **Interconnect**<br>Support the following interconnect protocols:<br>• Data Plane – Support for Ethernet 10GBASE-KR as specified in IEEE 802.3ap with support for TSN as specified in IEEE 802.1AX, CB, AS, Qbv, Qav, Qci, Qcc, and 802.1Q clauses 8.6.5.1 and 8.6.8.2<br>• Control Plane - SpaceWire as defined in ECSS-E-ST-50-12C<br>• Expansion Plane – JESD204C<br>• Expansion Plane – Support for PCIe Gen 3.1<br>• Utility Plane – IPMI and DAP as specified in VITA-78<br>• User Defined signals with the requirement that they are user programmable<br>  • SERDES - 1600mV peak-to-peak AC-coupled differential signaling; 8b/10b encoding; data rates of 1.25 Gbps, 2.5 Gbps, 3.125 Gbps, 5 Gbps, 6.25 Gbps, and 10 Gbps (note that some modules may not support all of these rates)<br>  • Single ended - 2.5V LVCMOS signaling<br>• Low-Rate Interconnect – I2C<br>• JTAG<br>• Provide pin on a front panel to disable JTAG for flight. |



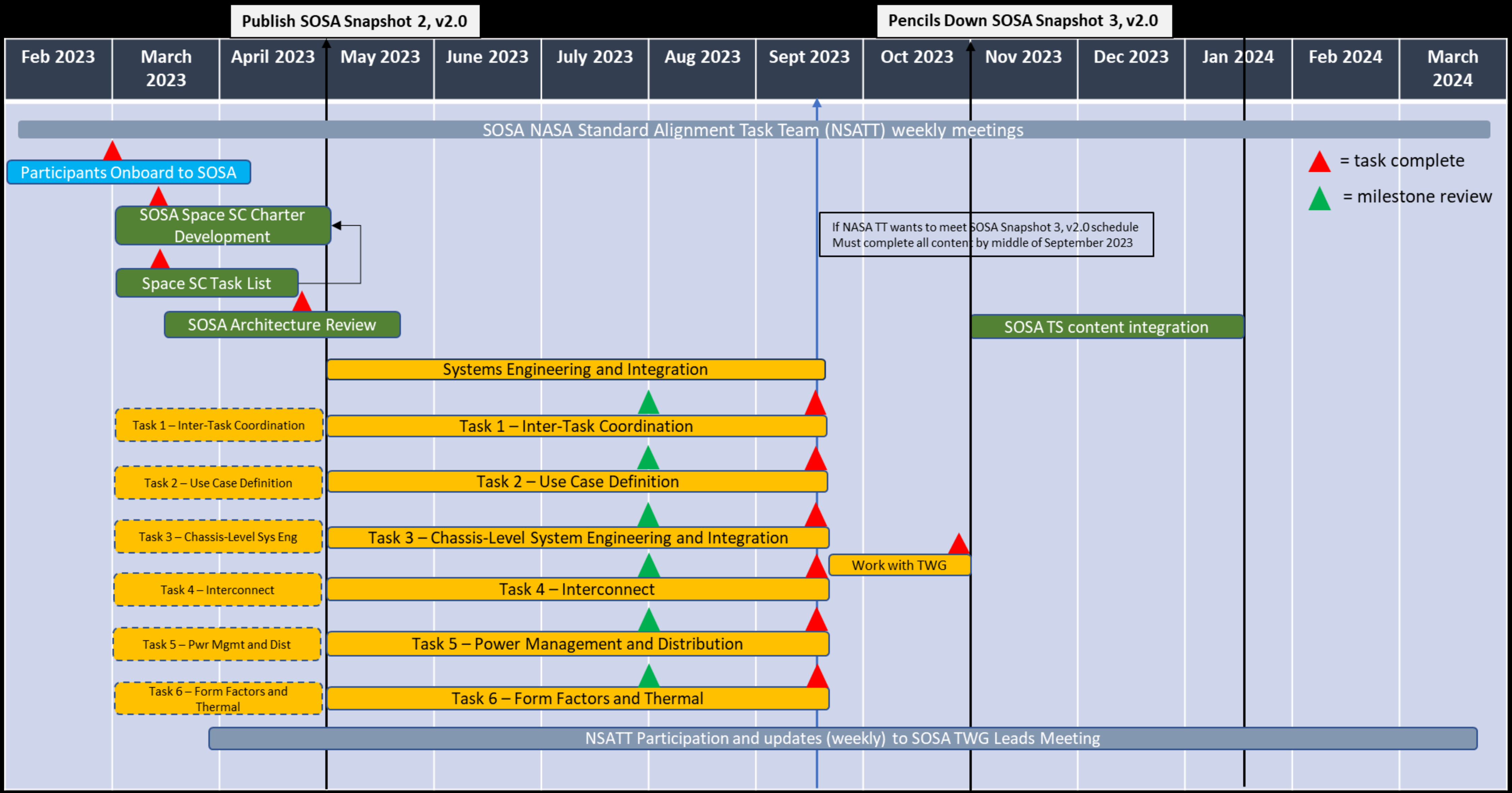




Single String 3U Smallsat Avionics

# SOSA SpaceVPX Standardization

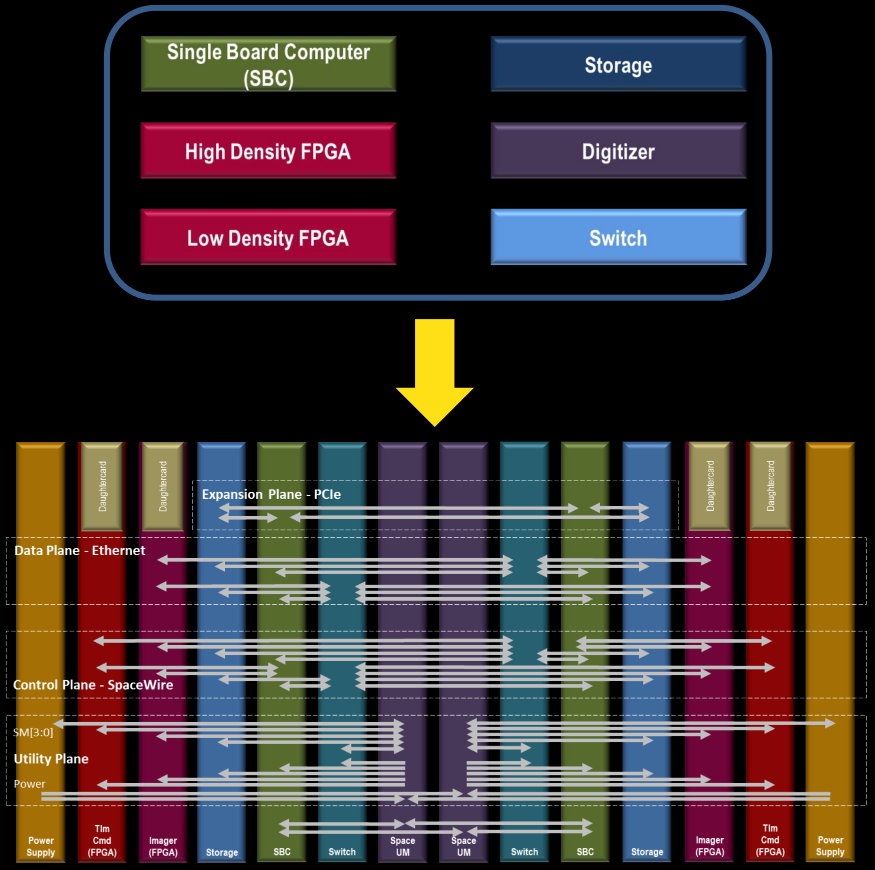
- A key recommendation of the completed NASA SpaceVPX Interoperability Assessment (R-3) states
  - NESC and STMD should engage with industry, other government agencies, and the SOSA™ Consortium on revision to VITA-78, and refine the module definition and interoperability (see Appendix B) and daughtercard use
- Consistent with this recommendation, a follow-on NESC activity has been initiated to collaborate with industry and other agencies on the development of an interoperable variant of SpaceVPX (currently specified in the VITA-78 standard) within the Sensor Open System Architecture (SOSA) standards organization
- Currently, over 25 industry and OGA participants are engaged on this effort within SOSA
- The expectation is to align content creation with existing SOSA publication schedule, with the specific goal of publishing SpaceVPX content in SOSA Snapshot 3 V2.0 in early 2024
- Content can then be integrated into the VITA-78 standard

# SOSA SpaceVPX Standardization



# Benefits of Interoperable SpaceVPX

- Once completed, an interoperable SpaceVPX standard can guide SpaceVPX development within NASA and industry to ensure interoperable avionics for future NASA missions
  - SpaceVPX provides a scalable architecture with the high-bandwidth inter-module communication and inherent fault tolerance to meet the increased onboard computing demands of future missions
  - System integrators can configure systems consisting of SpaceVPX modules from multiple vendors
  - SpaceVPX module vendors can leverage broader markets for their products, which can reduce per unit cost
  - Interoperability provides a key step toward interchangeability that would be needed for common sparing for future crewed missions
- Interoperable SpaceVPX can form the backbone of the HPSC (High Performance Spaceflight Computing) avionics ecosystem
  - SpaceVPX leverages the full capabilities of emerging flight processors




Redundant 3U System

# Conclusions

- NASA seeks engagement with industry and other government agencies in developing technologies that can address the spaceflight avionics needs of our future crewed and robotic missions

- With the development of HPSC underway, NASA is focusing on the broader HPSC ecosystem to enable mission infusion

  - DDR4 Memory
  - 10G Physical Layer (Transceivers and Connectors)
  - Point of Load Converters (POLs) and Power Management Controllers (PMCs)
  - Coprocessors
  - Software Libraries

- The development of interoperable SpaceVPX Plug-In Cards (PICs) is key to HPSC ecosystem, and the ongoing SOSA SpaceVPX standardization effort is first step toward this goal

# Acronym List

| | | | | | |
|---|---|---|---|---|---|
| AI | Artificial Intelligence | HW | Hardware | PALETTE | Planetary and Lunar Environment Thermal Toolbox Elements |
| ASIC | Application Specific Integrated Circuit | ILPM | Industry Leading Parts Manufacturer | PCIe | Peripheral Component Interconnect Express |
| BSP | Board Support Package | I/O | Intput/Output | PIC | Plug-In Card |
| cFE/cFS | Core Flight Executive/Core Flight Software | ISA | Instruction Set Architecture | POL | Point of Load |
| cPCI | Compact Peripheral Component Interconnect | ISRU | In Situ Resource Utilization | QML | Qualified Manufacturers List |
| COTS | Commercial Off the Shelf | JPL | Jet Propulsion Laboratory | REALM | RFID Enabled Autonomous Logistics |
| CPU | Central Processing Unit | JSC | Johnson Space Center | RFID | Radio-frequency Identification |
| C&DH | Command and Data Handling | LaRC | Langley Research Center | RHBD | Radiation-Hardened By Design |
| DDR | Double Data Rate | LEO | Low Earth Orbit | RISC | Reduced Instruction Set Computer |
| ECC | Error Correction Code | LLVM | Low Level Virtual Machine | RTOS | Real Time Operating System |
| ELCSS | Environmental Control and Life Support System | LPEC | Low Power Embedded Computer | SBC | Single Board Computer |
| EDL | Entry Descent and Landing | LSII | Lunar Surface Innovation Initiative | SBIR | Small Business Innovation Research |
| ESDMD | Exploration Systems Development Mission Directorate | LuSTR | Lunar Surface Technology Research | SC | Subcommittee |
| EVA | Extra-Vehicular Activity | MEAL | Mission, mission Environment, Application, and Lifetime | SCC | Space Computing Conference |
| FET | Field Effect Transistor | ML | Machine Learning | SEE | Single Event Effect |
| FPGA | Field Programmable Gate Array | MOSA | Modular Open Systems Architecture | SMD | Science Mission Directorate |
| fps | Frames per Second | MUSTANG | Modular Unified Space Technology Avionics for Next Generation missions | SOC | System-On-a-Chip |
| FSW | Flight Software | NASA | National Aeronautics and Space Administration | SOSA | Sensor Open Systems Architecture |
| FT | Fault Tolerance | NEPP | NASA Electronics Parts and Packaging Program | STMD | Space Technology Mission Directorate |
| GB | Gigabyte | NESC | NASA Engineering & Safety Center | STTR | Small Business Technology Transfer |
| Gbps | Gigabits Per Second | NRE | Non-Recurring Engineering | SW | Software |
| GCC | Gnu Compiler Collection | NumPy | Numerical Python | SWaP-C | Size Weight and Power, and Cost |
| GPP | General Purpose Processing | Open BLAS | Open Basic Linear Algebra Subprograms | TSN | Time-Sensitive Networking |
| GPU | Graphics Processing Unit | OpenCL | Open Computing Language | TX | Taxonomy |
| GSFC | Goddard Space Flight Center | OpenCV | Open Source Computer Vision | TWG | Technical Working Group |
| IEEE | Institute of Electrical and Electronics Engineers | OpenGL | Open Graphics Library | VITA | VMEbus (Versa Module Eurocard Bus) International Trade Association |
| HI | Heterogeneous Integration | OpenMP | Open Multiprocessing | xEMU | eXploration Extravehicular Mobility Unit |
| HPSC | High Performance Spaceflight Computing | OS | Operating System | | |
| HUD | Heads Up Display | OSAM | Peripheral Component Interconnect Express | | |