High Temperature Devices For Aerospace Applications

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Sorrento, Italy

Administrative Notices Regarding This Presentation

Links to source material and additional resources are provided on many slides for you to further your learning and understanding well beyond the limited information contained in this tutorial.

Any reference to a particular vendor's hardware, software, and/or media is strictly for illustrative/example informational purposes **that should NOT be considered an endorsement of any kind by NASA or the United States Government.**

This work was funded by The NASA John H. Glenn Research Center in Cleveland, OH USA with funding from the NASA Science Mission Directorate under the High Operating Temperature Technology (HOTTech) and Long-Lived In-Situ Solar System Explorer (LLISSE) projects.

Outline

Part 1: High Temperature *Aerospace* Applications (Why?)

- Missions, Benefits, Requirements
- Aeronautics and Space

Part 2: High Temperature *Electronics* Technologies (How?)

- Semiconductor Technologies
- NASA Glenn SiC JFET-R Approach

Sensors & Electronics Benefit "Non-Electronic" Applications

The incorporation of "conventional temperature" silicon IC electronics capabilities into traditionally "non-electronic" systems has enabled critical performance improvements to:

Automobiles and Aircraft (Combustion Engine)
- Sensors & controls for improved fuel efficiency and lower pollution

Energy Production Drilling (Oil, Gas, Geothermal)
- Telemetry for lower-cost and faster drilling

Space Exploration
- Enabled by ICs in launch vehicles and spacecraft

High temperatures are inherent to important applications
Silicon ICs engineered to perform in high-T applications, often with drawbacks
- Specialized silicon ICs (e.g., silicon on insulator) for T < 250 °C
- Remotely located ICs with wiring and/or environmental shielding
- Limited operating lifetime or other special operating limitations

Impact of High Temperature Electronics

Slide presented by D. Shaddock of
GE Research at 2023 IMAPS International
High Temperature Electronics Conference

DISTRIBUTED CONTROLS

- Smart Sensors & Actuators
- Power Conversion
- Hypersonic Sensing & Controls
- Hypersonic Navigation

DOWNHOLE SENSING & ACTUATION

- High Temperature downhole tools
- High Temperature communication
- Geothermal monitoring

SPACE

- Exploration Modules
- UV Imaging
- Planetary Science

Solving the world's toughest challenges

GRCTHINK

GE Research (beginning in 1900)

Slide presented by D. Shaddock of
GE Research at 2023 IMAPS International
High Temperature Electronics Conference

CREATING THE FUTURE

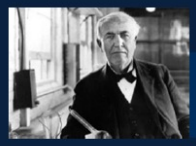
2025
Hypersonics

2026
Bioelectric Medicine

2027
RISE Engine

2027
Superconduct-ing Wind

2027
Direct Air Capture



INNOVATION LEGACY

1879
Electric lamp

1896
X-ray machine

1941
US jet engine

2014
62%+ efficy. gas turbine

2019
Most powerful wind turbine

SCALING IMPACT ACROSS GE

7,000+
Gas turbines

~4M
Imaging, mobile diagnostic & monitoring units

~70,000
Aircraft engines

~50,000
Wind turbines

- Powering 2/3 of commercial departures
- Generating 1/3 of world's electricity
- Providing health professionals 16,000+ scans every minute

Power and High Temperature are characteristics across product

IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. IE-29, NO. 2, MAY 1982

High-Temperature Electronic Requirements in Aeropropulsion Systems

WILLIAM C. NIEBERDING AND J. ANTHONY POWELL, MEMBER, IEEE

Abstract—**This paper discusses the needs for high-temperature electronic and electrooptic devices as they would be used on aircraft engines in either research and development applications, or operational applications. The conclusion reached is that the temperature at which the devices must be able to function is in the neighborhood of 500° to 600°C either for R&D or for operational applications. In R&D applications, the devices must function in this temperature range when in the engine but only for a moderate period of time. On an operational engine, the reliability requirements dictate that the devices be able to be burned-in at temperatures significantly higher than those at which they will function on the engine. The major point made is that semiconductor technology must be pushed well beyond the level at which silicon will be able to function.**

I. INTRODUCTION

THE PURPOSE of this paper is to describe the needs for high-temperature electronics in the aircraft engine field.

During this process many prototypes are
development purposes. These prototypes,
engine components, are operated repeat
facilities. For each of these test runs the e
is instrumented with the maximum numbe
so that as much of the desired informati
tained from each facility run. Even after
for flight, problems arise in its operation
of improving its operational characteristi
so that this testing process continues well
of an engine model. An example of this
gram conducted by NASA to modify engi
DC9 and the Boeing 727 to reduce the
model engine had been in service for many
sures generated by environmental concer
to go back and redesign parts of it for rad

CONCLUSION: "We cannot help but feel that high-temperature electronics will indeed have wide application not only to the areas discussed at this conference but also to far more important areas which we just do not have the vision to predict."

Sources: https://doi.org/10.1109/TIE.1982.356644 & https://www1.grc.nasa.gov/glenn-history/hall-of-fame/biographies/j-anthony-powell/

Potential Benefits of High Temperature Electronics Has Been Recognized for Decades

First International
High Temperature Electronics Conference

Albuquerque Marriott Hotel
Albuquerque, New Mexico USA

June 16 - 20, 1991

1991

HiTEC

CONTENTS

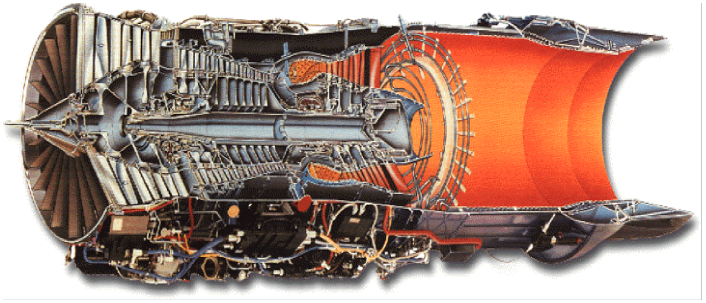
SESSION I: Users and Needs

Conference Organizers: Sandia National Laboratory (US Dept. of Energy) and US Air Force Research Laboratory

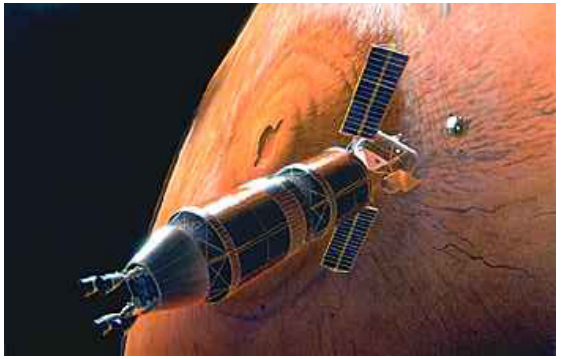
High Temperature Electronics Benefits to NASA Missions

(Electronics thermal limits impacts most missions, even in cold places)

Intelligent Propulsion Systems

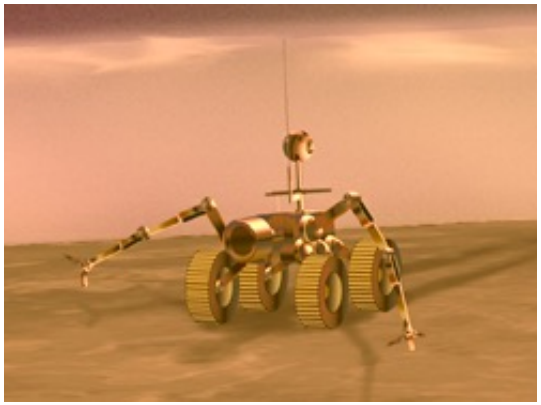


Space Exploration PMAD



More Electric + Distributed Control Aircraft

Venus Exploration



Extreme Environment Application Drivers

- Thermoacoustic instabilities
- Active combustion control
- Exhaust noise emission

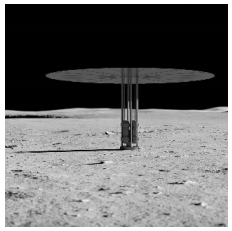
Turbine Engines

- Combustion instabilities
- Mode Transition Unstart

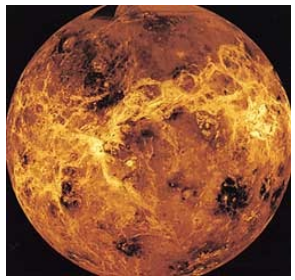
X-43A Scramjet with supersonic Combustion ramjet engine

Pressure pulse/shock quantification

Pulse detonation engine

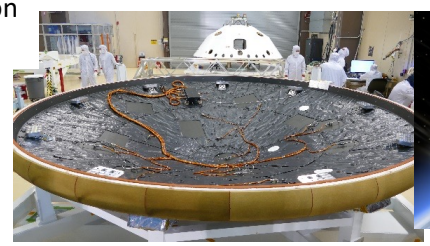


Instrumentation for Advanced Micro Nuclear Reactors



Venus

- 460 °C
- Aggressive chemistry
- Atmospheric pressure (93 Earth atm.)

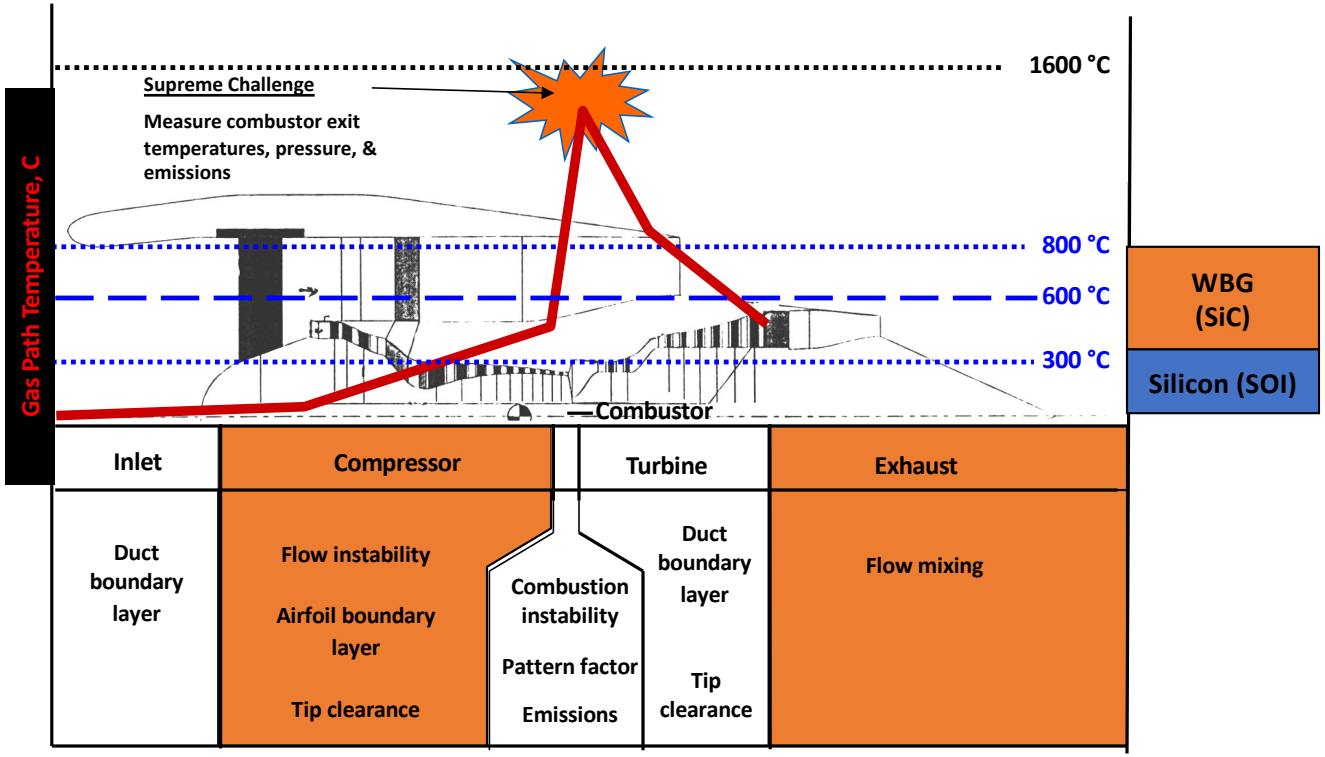


Recession sensors for Thermal Protection Systems

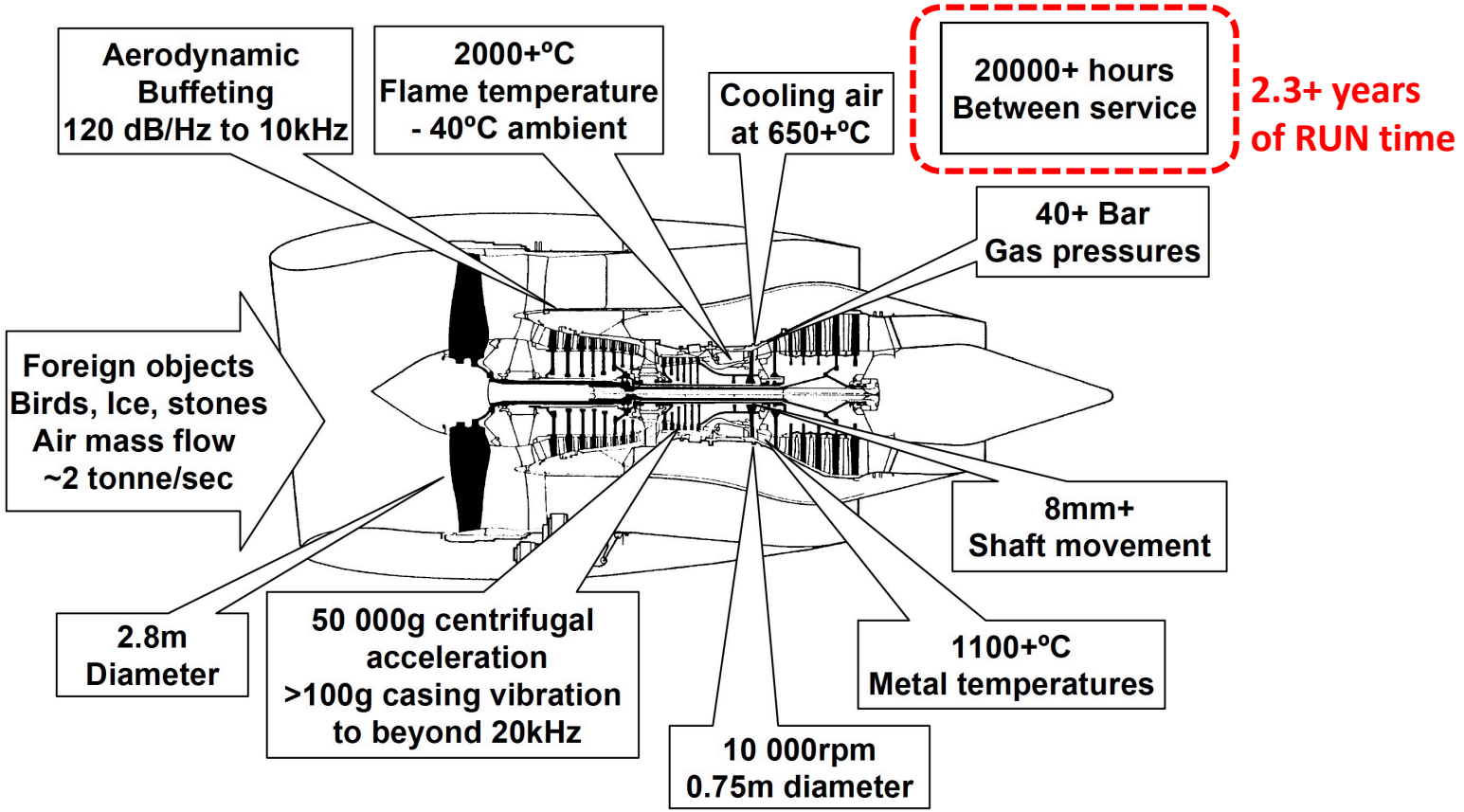
Source: R. Okojie, NASA Glenn Research Center
https://ntrs.nasa.gov/citations/20230001416

Intelligence included throughout the engine requires the development of High Temperature Electronics capable of prolonged operation

Key compressor and exhaust regions beyond realm of silicon



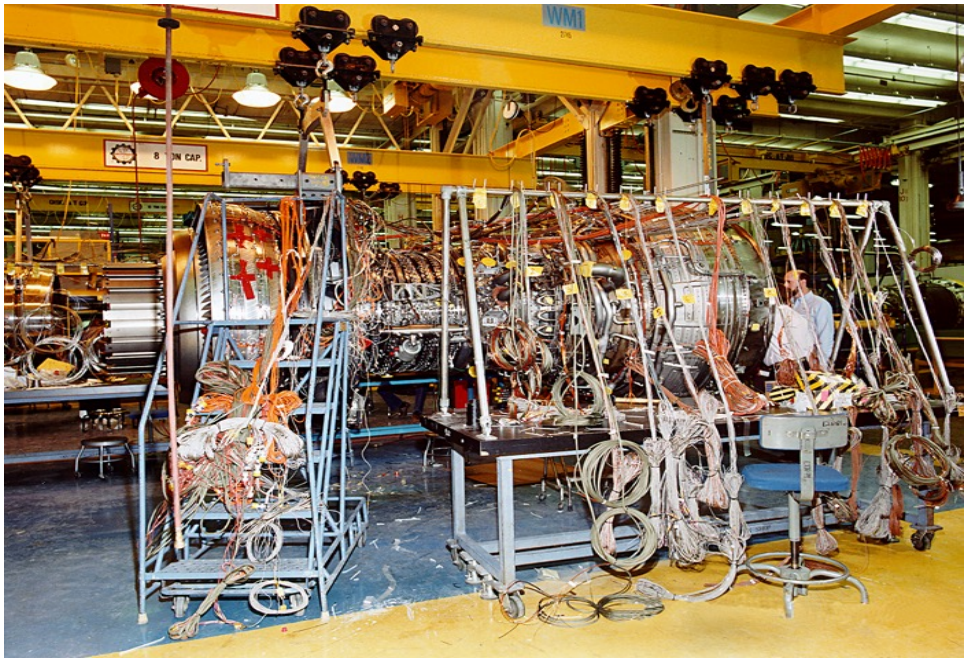
Environment Within Aircraft Gas Turbine Engine



Source: S. Garg et al., https://ntrs.nasa.gov/citations/20100029602

Shorter Term Application: Turbine Engine Ground Test Instrumentation

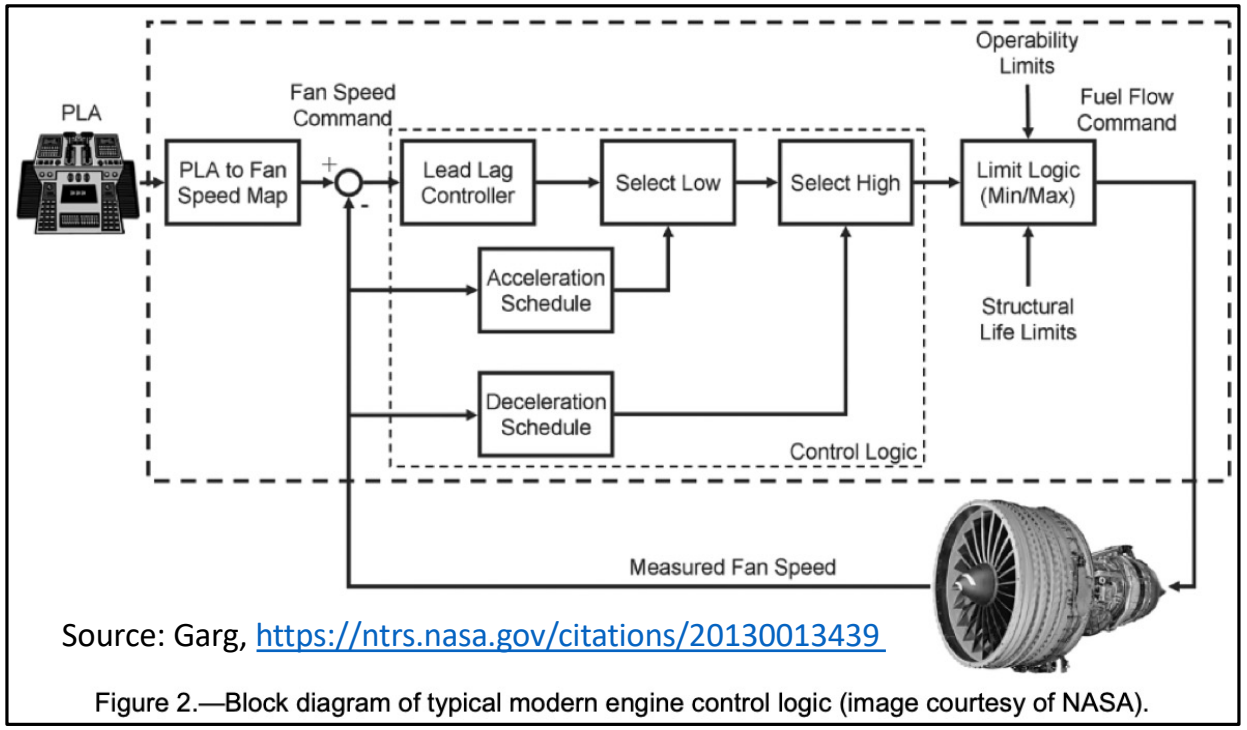
(~ 1000 hours duration)



Typical - 1300 wires for sensor data communication. Multiplexing, amplification, signal conditioning, and wireless data transmission functionality at point of sensing in high temperature regions would enable greatly improved test instrumentation capability while simultaneously reducing wires & connectors.

What is a FADEC, and what does it do?

Full
Authority
Digital
Engine
Control



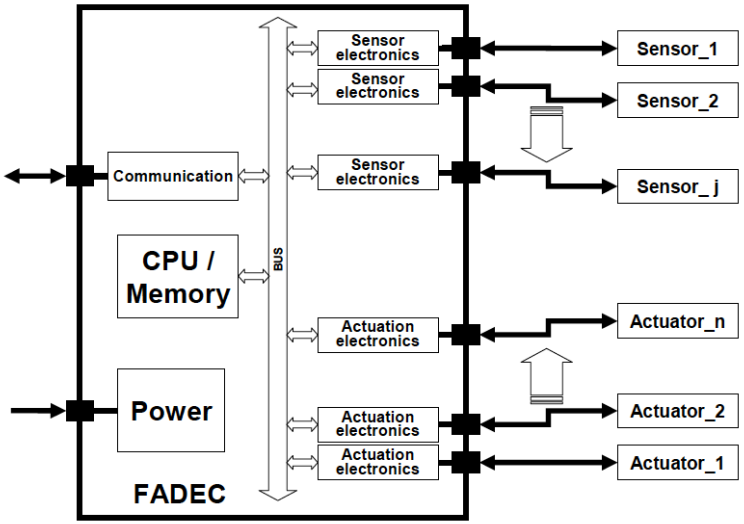
Source: Garg, https://ntrs.nasa.gov/citations/20130013439

Figure 2.—Block diagram of typical modern engine control logic (image courtesy of NASA).

Video: https://www.baesystems.com/en-us/productfamily/electronic-engine-controls

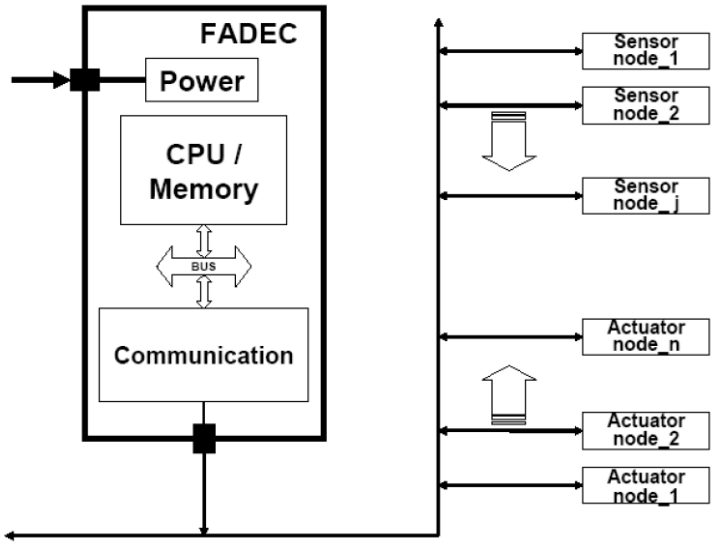
Jet Engine Control Architectures

Centralized Architecture
(Present Practice)



FADEC=Full Authority Digital Engine Controller

Distributed Architecture
(Future – WITH PEFORMANCE BENEFITS)



Distributed "smart nodes" (some High-T) enable improved combustion control with far less wiring.

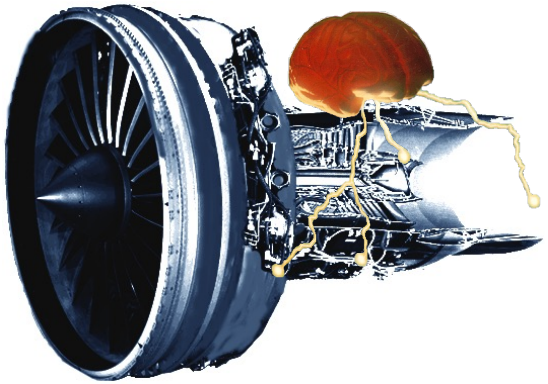
Source: S. Garg et al., https://ntrs.nasa.gov/citations/20100029602

Additional Info: https://www.decwg.org

Longer Term Application: On-Engine Electronics, MEMS, Actuators

Add capability without adding connectors, cables, plumbing need for
Ultimate goal: “Lick and Stick” high temperature self-powered wireless nodes.

Active Control
for enhanced performance and reliability, and reduced emissions
- active control of combustor, compressor, vibration etc.
- MEMS based control applications



Advanced Health Management for self diagnostic and prognostic propulsion system
- Life usage monitoring and prediction
- Data fusion from multiple sensors and model based information

Distributed, Fault-Tolerant Engine Control for enhanced reliability, reduced weight and optimal performance with system deterioration
- Smart sensors and actuators
- Robust, adaptive control

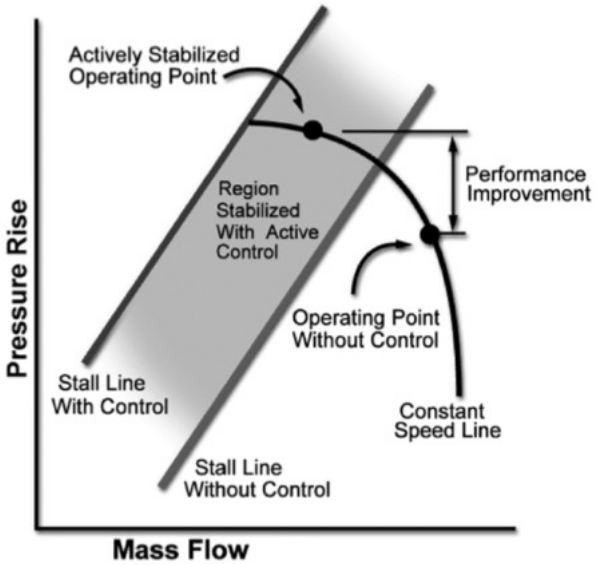
Multifold increase in propulsion system affordability, reliability, performance, capability and safety

Longer Term Application: MEMS Jet Engine Compressor Surge/Stall Control

Jet engine with array of MEMS highly sensitive pressure sensors, smart processing electronics, and microactuators/micro bleed valves located on the shroud surrounding the compressor rotor.

Sensors and smart electronics would register pressure instabilities indicating imminent onset of compressor stall, open microbleed valves to alter flow in time to prevent compressor stall.

Would enable significant reduction of compressor over-design (excess stages) and improve engine reliability.

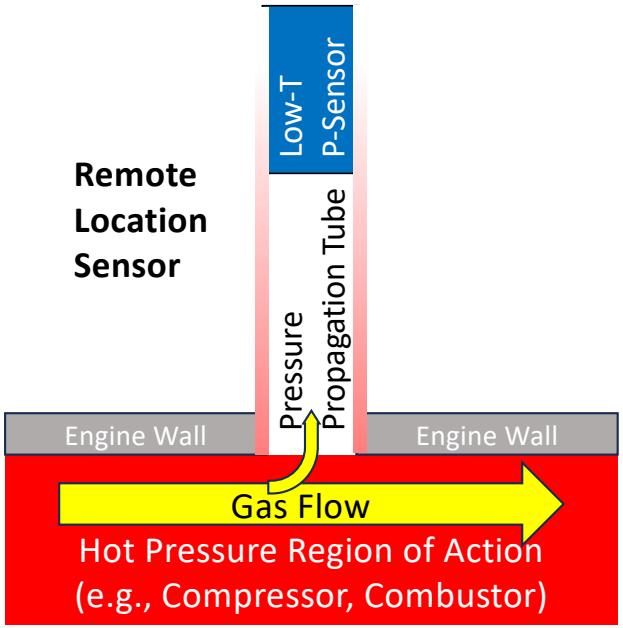


Operating Requirements:
Pressure: Up to 200 PSI
Pressure Resolution: 0.02 PSI
Temperature: Up to 500 °C
Microactuator motion: up to 0.7 mm

Source: S. Garg et al., https://ntrs.nasa.gov/citations/20100029602 and https://ntrs.nasa.gov/citations/20130013439

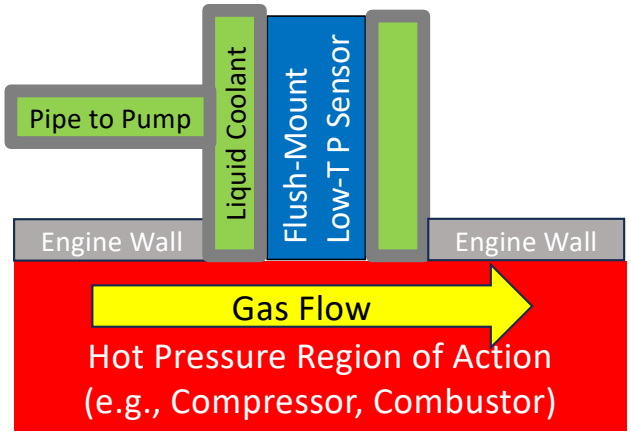
Pressure Sensor Approaches for Enabling Active Jet-Engine Control

(Simplified Cross-Section of **Pressure Sensor** Mounted on **Jet Engine Outer Wall**)



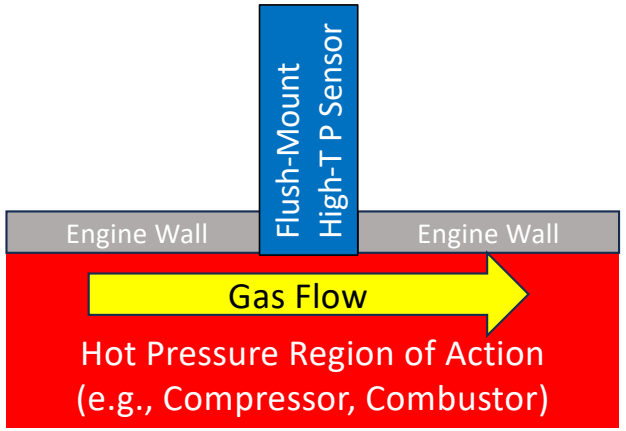
Major Drawback: Tube loss of high-f pressure behavior impedes timely detection of flow instability.

Liquid Cooled Sensor



Major Drawbacks: Adverse overhead of cooling system (weight & reliability), and coolant-flow crosstalk.

High-T Sensor

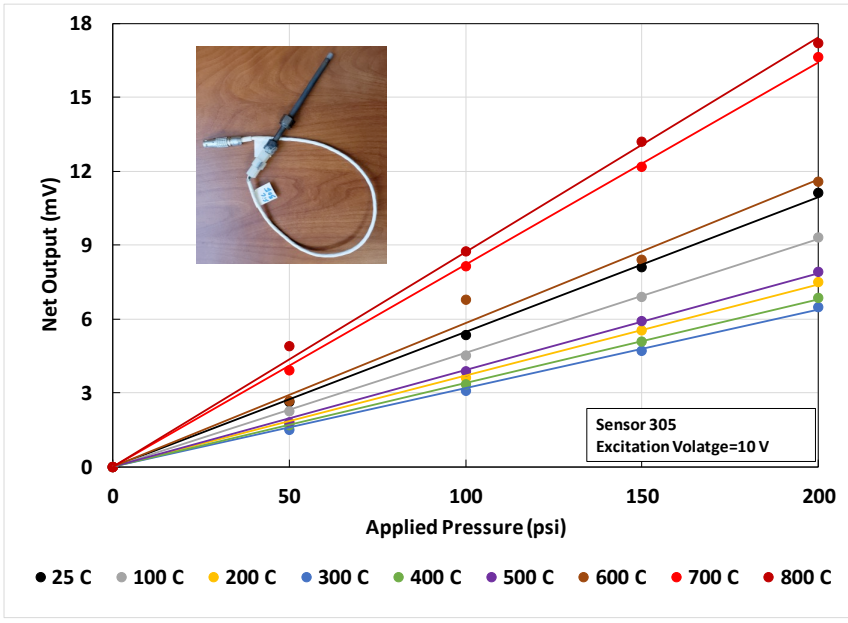


If long-term durable & stable response, advanced stall and combustion control approaches are enabled!

For more info see: Jang & Lee https://doi.org/10.1016/j.csite.2022.102184

High Temperature SiC Pressure Sensors at NASA Glenn

R. Okojie, NASA Glenn Research Center



Single-chip of 4H-SiC piezoresistors etched over thinned diaphragm region.

Packaged in tube/header for flush-mount insertion into small hole in wall of jet engine (is very challenging!!).

Enables direct sensing of hot-zone high-frequency pressure signals without active cooling.

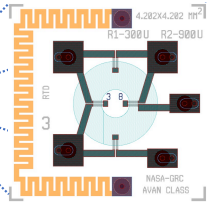
HIGH-T ELECTRONICS TO AMPLIFY SMALL SENSOR SIGNALS FOR TRANSMISSION OUT OF HOT ZONE IS ALSO VITAL!

Integrated Pressure/Temperature Sensor for 800 ºC Operation

Integrated Pressure/Temp Sensors at 800 °C without Cooling

Accurate Pressure/Temp Relationship, Real-time Temperature Compensation and Voltage-Pressure Conversion.

Full-bandwidth Capture of Pressure Transient due to Direct Interaction with Flow-Field at High Temperature.



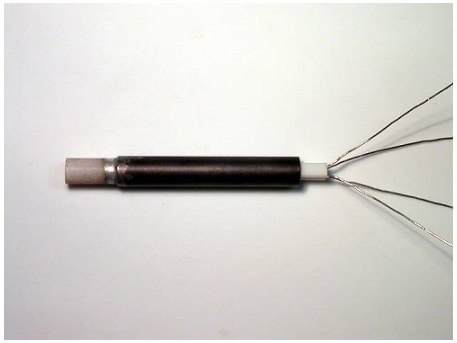
Sensor chip inside

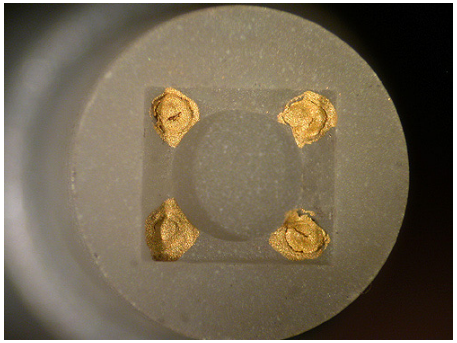
Source: R. Okojie
NASA Glenn

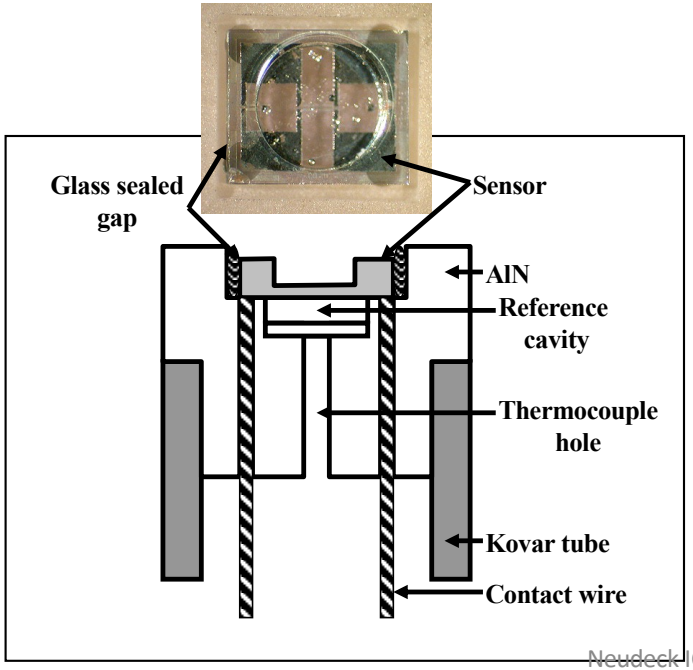
Unique Characteristic: No wire bond Direct Chip Attach

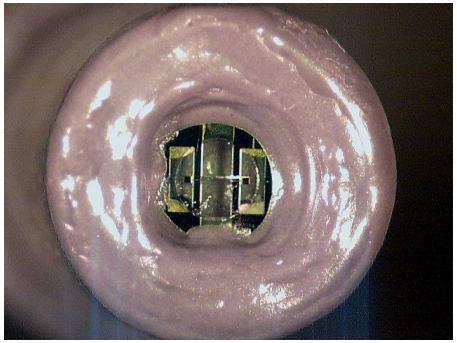
Reliability by Design-Matching Critical Components

Source: R. Okojie
NASA Glenn









Glass CTE ~4.1 ppm/°C
SiC CTE =3.7 ppm/°C
AlN CTE = 4.1 ppm/°C
Kovar CTE = 5.13-6.15 ppm/°C
SS Steel Housing CTE = 10 – 15 ppm/°C

US Pat. # 5,845,664 Issued Jan 25, 2005

The Case for High Temperature Electronics in Aircraft Power Systems

(Conventional combustion jet engine propulsion aircraft)

Growth of electrical systems/power demand on commercial and military aircraft has continued unabated for decades.

- Performance-driven, providing both commercial competitive and tactical military advantages
- Mechanical/pneumatic actuation replacement with electric motor actuation
- Communications, radar, information/entertainment displays, electronic warfare, safety & redundant systems

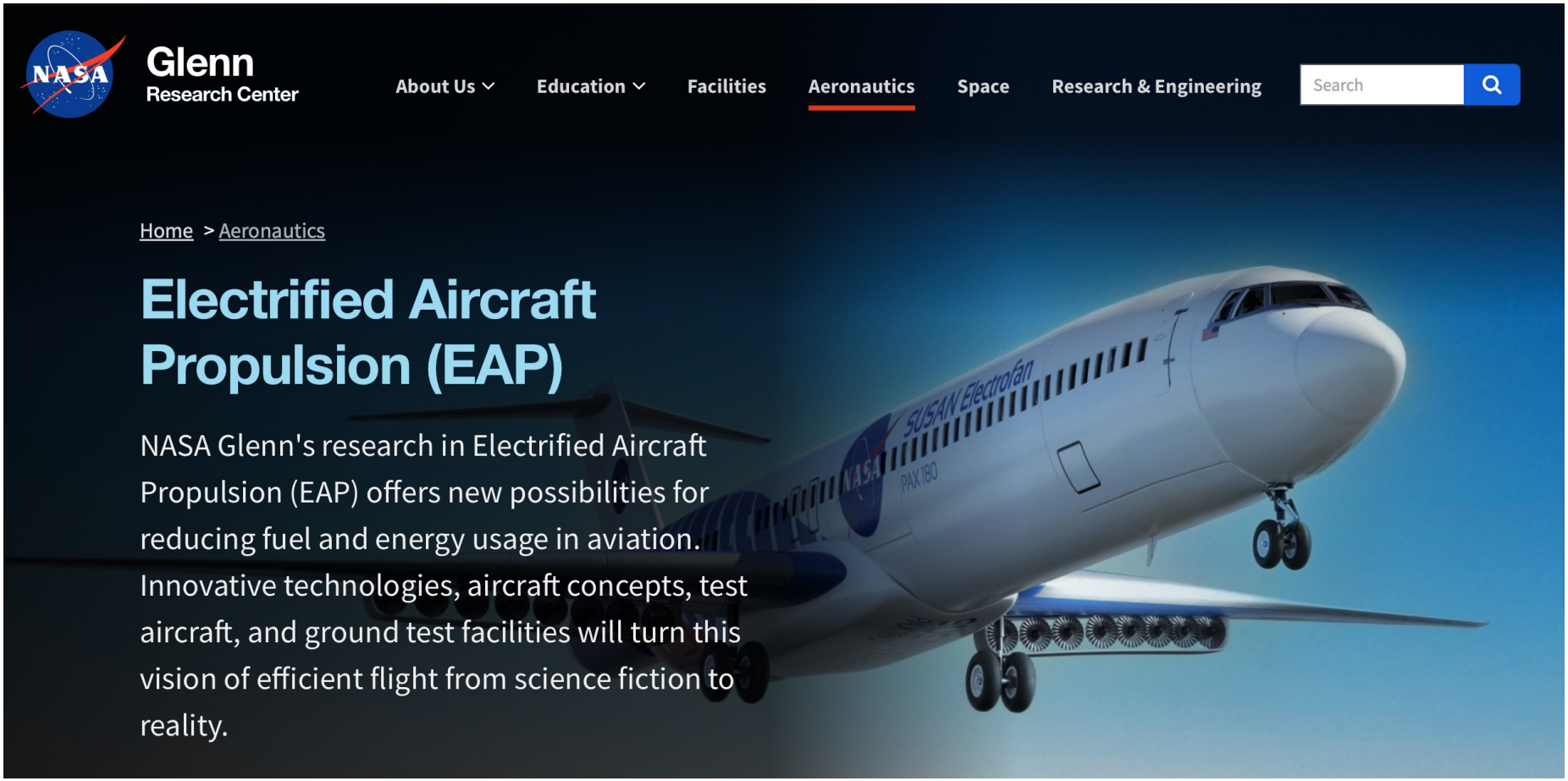
The power management and distribution hardware must:

- Have highest efficiency (wasted electrical energy turns into unwanted heat energy)
- Lowest mass and smallest size possible (size and weight are vital to aircraft capability)

Environmental and design challenges for power electronics thermal management in aircraft

- Thermal management system overhead (liquid cooling, fan cooling) INCUDING ELECTRICAL POWER!
- Numerous heat sources, often within confined aircraft spaces (jet engines, skin heating, electronics heating).

R. Brewer, Lockheed-Martin Corp. Fellow at 2023 IMAPS Int. High Temperature Electronics Conference:
"Increased power loads and temperatures drive to self-defeating demand for more cooling system power"
Unsustainable **"POWER THERMAL DEATH SPIRAL"** is at hand with conventional-T (silicon or SiC) power devices



Source: https://www1.grc.nasa.gov/aeronautics/eap/

Variety of Approaches to Electrifying Aircraft Propulsion

(Reducing carbon emissions of passenger aviation)

All-Electric Concept Aircraft

Battery or hydrogen fuel-cell electrical power
- Many small electric motors along wing
- Enhance airfoil lift and reduce drag
- Smaller range, smaller aircraft
- Substantial energy storage weight

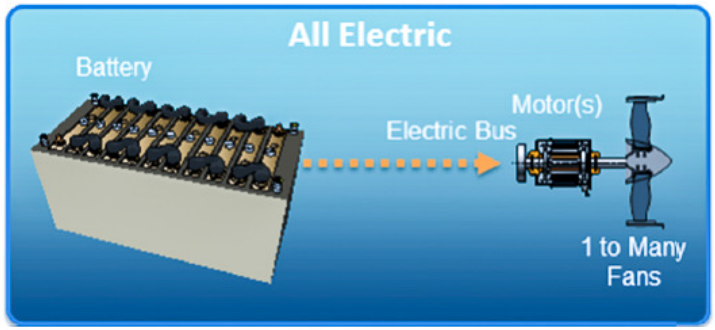
Hybrid Turbo-Electric Concept Aircraft

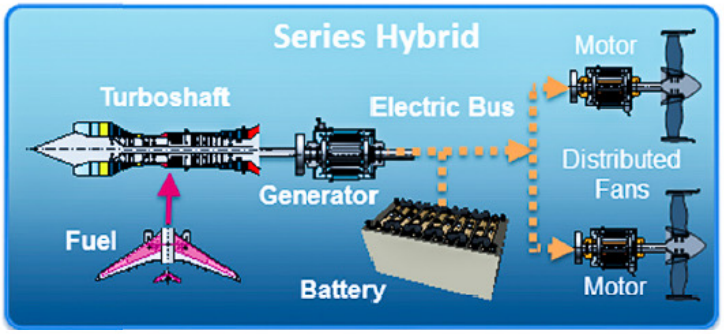
Combustion power (jet-fuel or hydrogen)
- Jet-engine driven generators power tail electric motor fan
- Significantly reduced aerodynamic drag
- Reduced fuel and emissions
- Longer range, larger aircraft

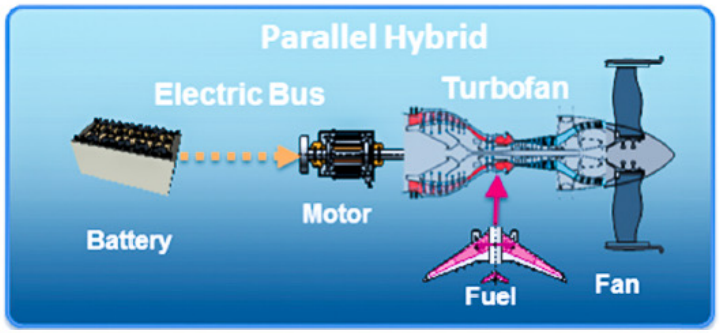
More info: https://www1.grc.nasa.gov/aeronautics/eap/ and Fard et al., https://doi.org/10.1109/TTE.2022.3197332

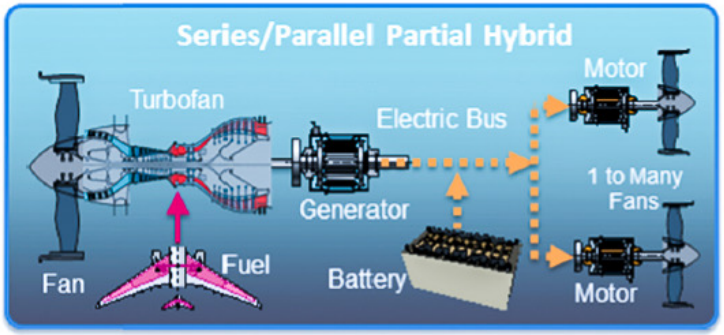
Variety of Approaches to Electrifying Aircraft Propulsion

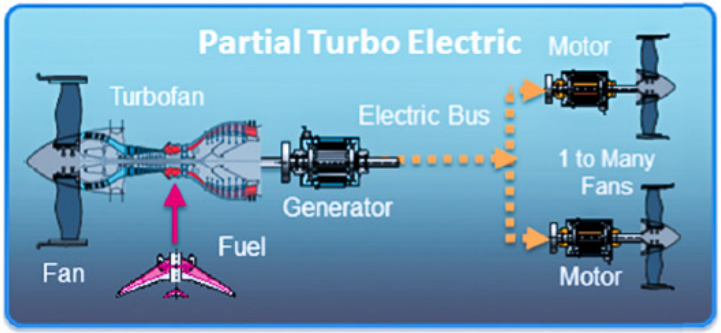
Source: https://www1.grc.nasa.gov/aeronautics/eap/airplane-concepts/aircraft-configurations/

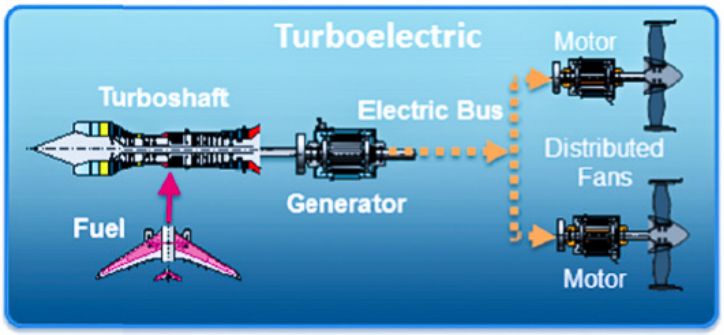












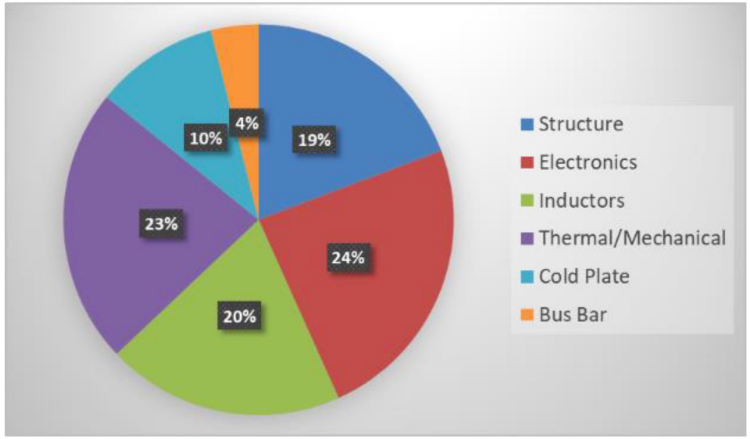
Design of a High Power Density, High Efficiency, Low THD 250kW Converter for Electric Aircraft

(Granger et al., NASA Glenn Research Center, 2021, https://doi.org/10.2514/6.2021-3332)

Thermal management required to keep all electrical components < 140 °C is 33% of converter mass.
HOWEVER, mass of cooling system supplying cooled liquid to the Cold Plate is NOT included!

Component	Mass [kg]	Percent [%]
Structure	4.9	19
Electronics	6.1	24
Inductors	5.0	20
Thermal/Support	5.8	23
Cold Plate	2.6	10
Bus Bar	1.0	4
SUM	**25.4**	**100**

(a)



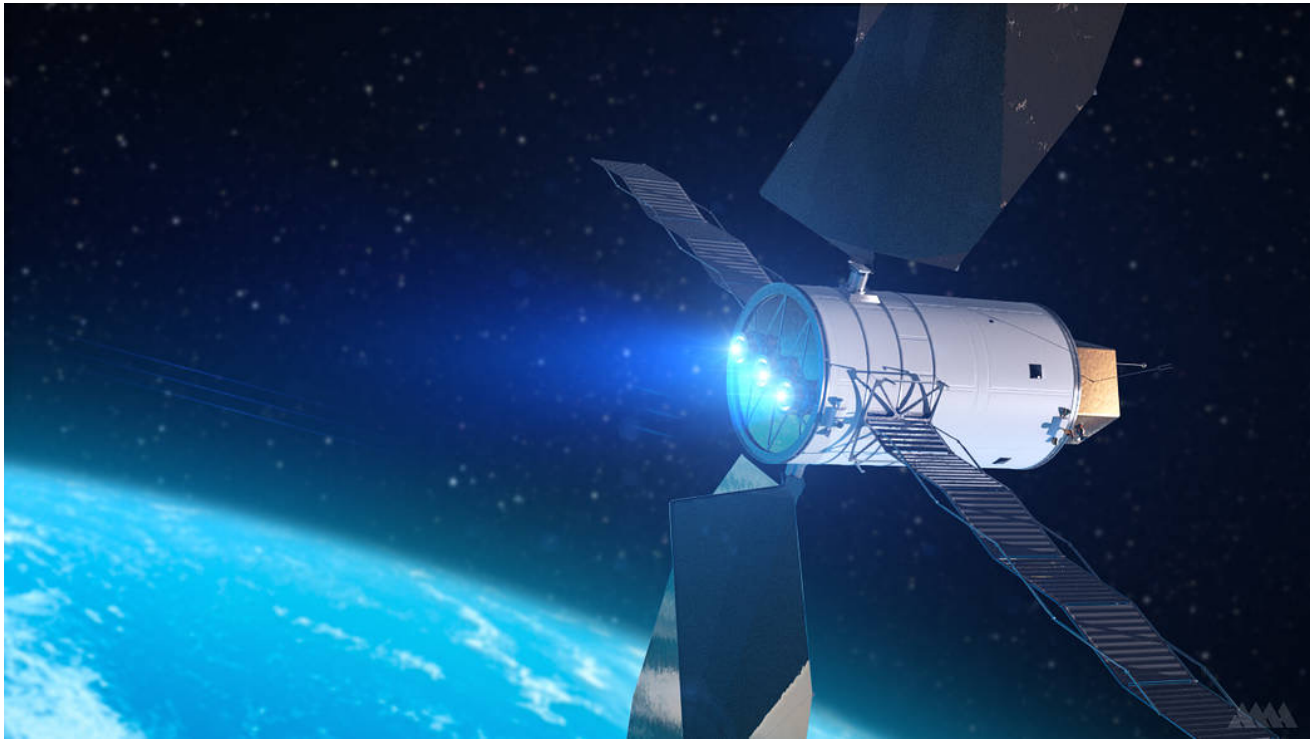
(b)

Fig. 9 Mass breakdown of preliminary converter design, (a) table and (b) pie chart.

SiC power devices operating above 200 °C offer thermal cooling system mass reductions to electric aircraft and spacecraft power converters (degree of improvement is mission-specific).

Electric Energy In-Space Propulsion

(Solar power source or nuclear power source)



- Electrically accelerated propellant velocity >> Chemically accelerated propellant velocity
- Small thrust for long duration provides larger change in momentum using far less propellant

Source: https://www1.grc.nasa.gov/space/sep/

Why Nuclear Thermal Propulsion?

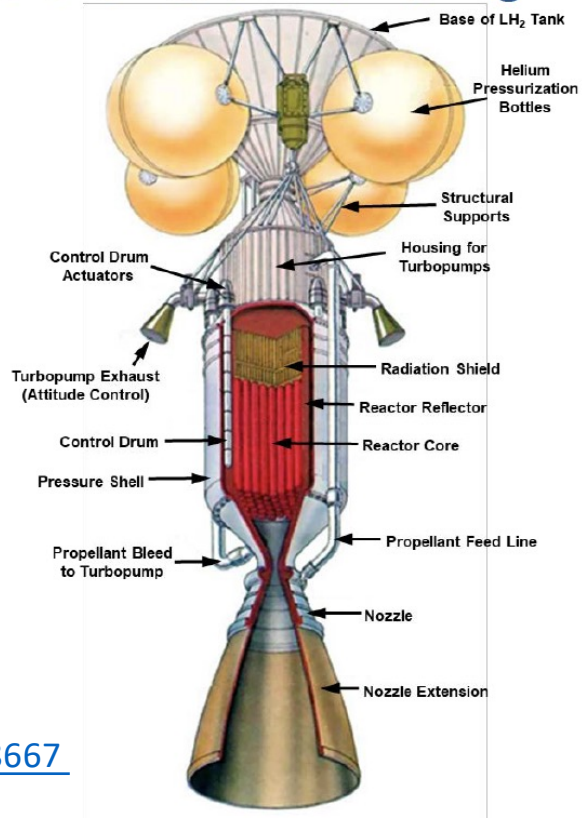
- For human Mars missions, first generation NTP can reduce crew time away from earth from >900 days to <500 days while still allowing ample time for surface exploration
  - Reduce crew exposure to space radiation, microgravity, other hazards
- First generation NTP can enable abort modes not available with other architectures
  - Potential to return to earth anytime within 3 months of earth departure burn, also to return immediately upon arrival at Mars
- First generation NTP is a stepping stone to fission power systems and highly advanced nuclear propulsion systems that could further improve crew safety and architectural robustness

Source: King & Houts https://ntrs.nasa.gov/citations/20180008667

Sensor Needs for Engine System Design

Instrumentation is needed for engine control and health monitoring:

- High thermal temperatures and vibration levels
- Nuclear radiation composed of neutron fluxes and gamma rays
- Non-invasive sensor designs for:
  - Neutron flux (outside reactor)
  - Chamber temperature
  - Operating pressure
  - LH2 propellant flow rates



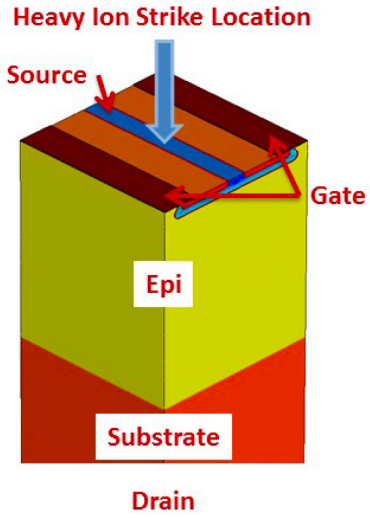
Source: King & Houts, https://ntrs.nasa.gov/citations/20180008667

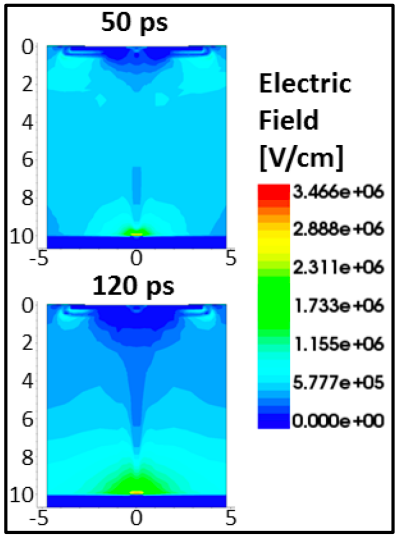
Heavy Ion Strike Single-Event Burnout of SiC Power Devices

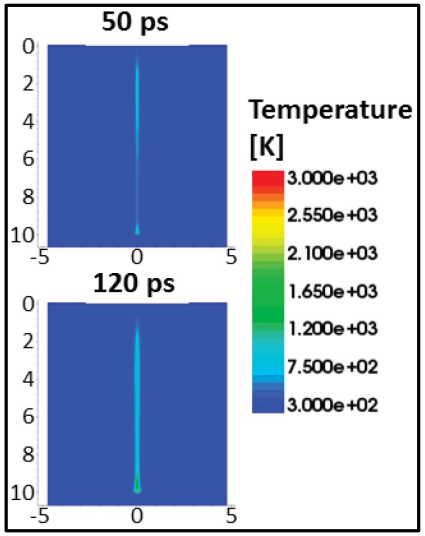
Catastrophic failure that forces HUGE de-rating of SiC power devices for aerospace missions!

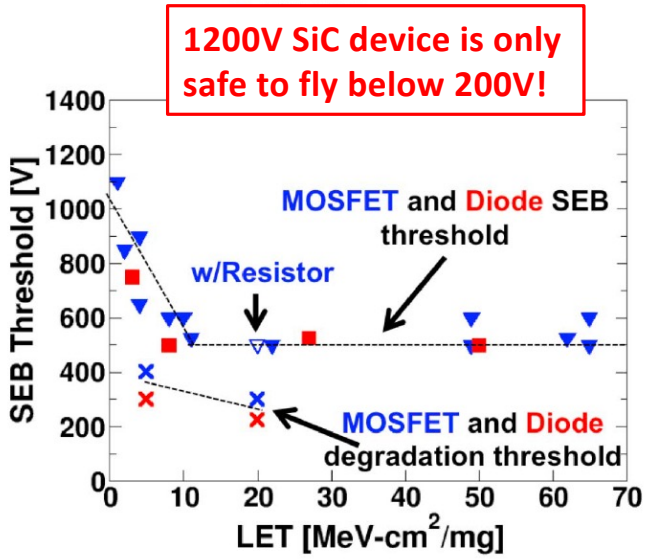
McPherson et al: https://ntrs.nasa.gov/citations/20190033217

Ball et al: https://doi.org/10.1109/TNS.2019.2955922







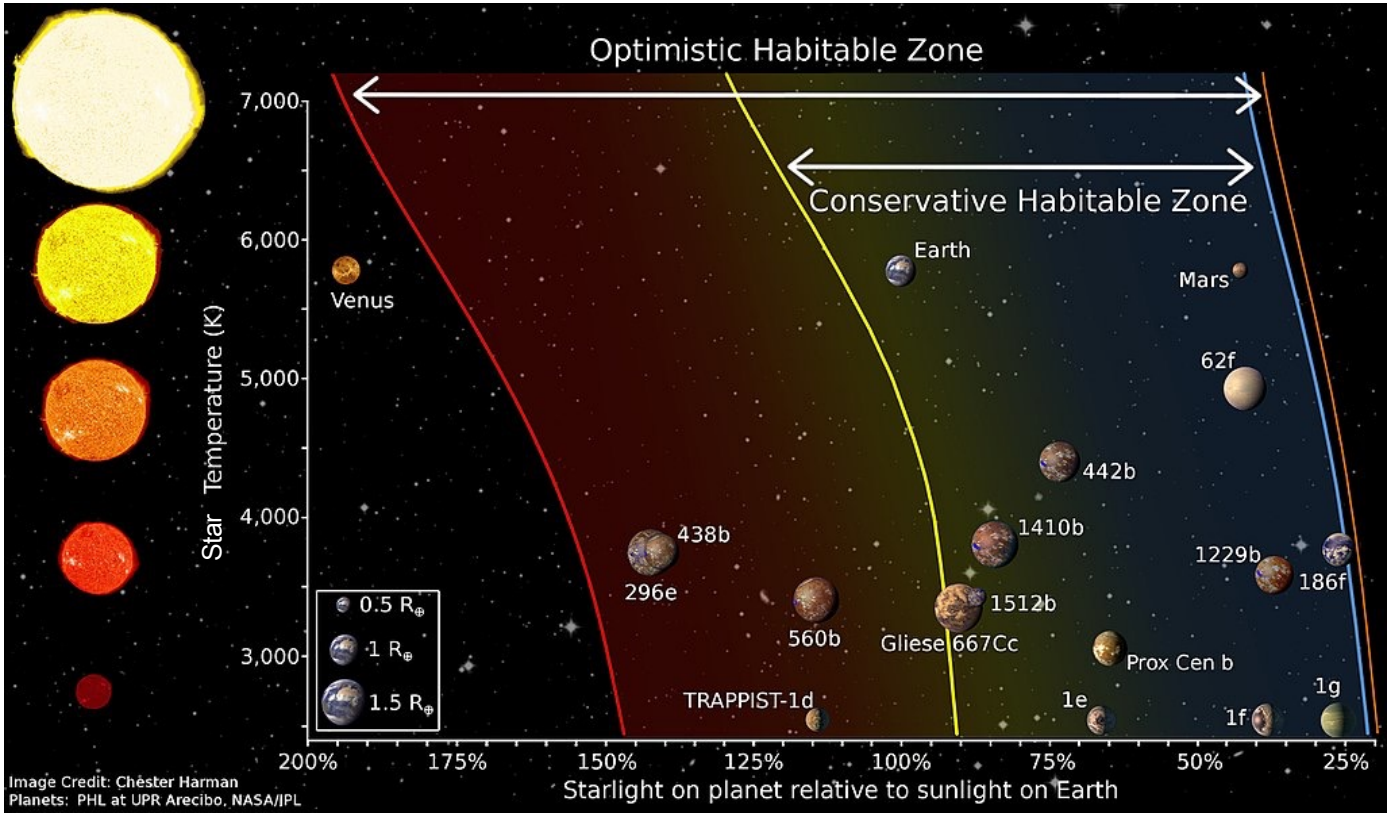


This issue has been a major impediment to actual flight deployment of SiC power device benefits!

- Aerospace devices and systems MUST demonstrate immunity to space radiation (including jet aircraft)
- Amount of de-rating necessary drastically cuts otherwise large SiC performance benefit to power systems
- Progress on reducing amount of de-rating is being made, but more is needed to enable full SiC benefits

Interesting Circumstellar Habitable Zone Exoplanets

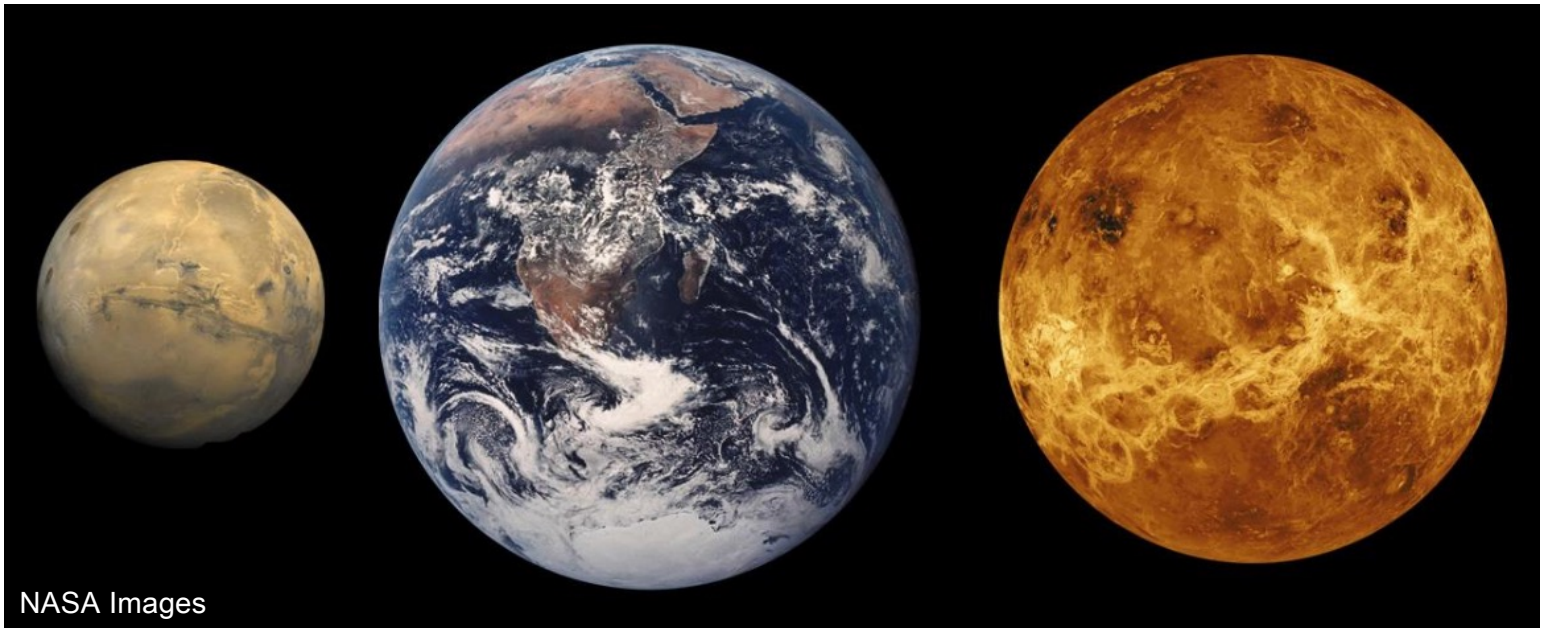
(Out of 5000+ planets detected & confirmed, majority by NASA Kepler ST transit observations)



https://commons.wikimedia.org/wiki/File:Diagram_of_different_habitable_zone_regions_by_Chester_Harman.jpg

More info: https://exoplanetarchive.ipac.caltech.edu

Which Planet is Earth's Closest Planetary Neighbor?

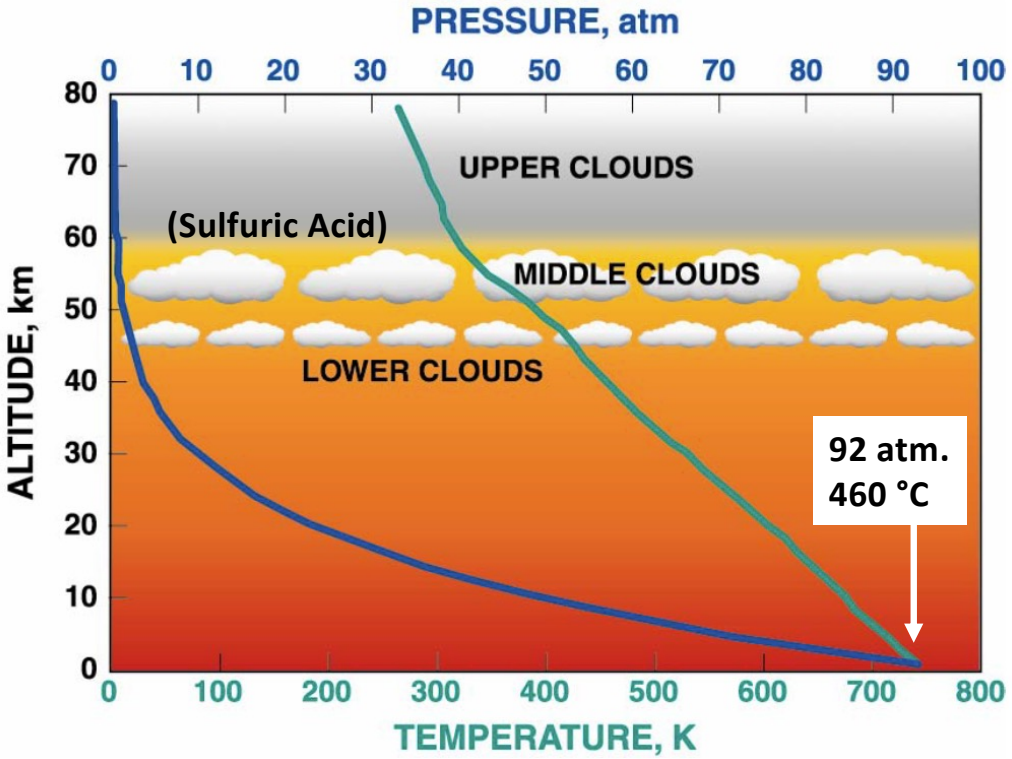


Mars
Mass: 10% Earth
Orbit: 150% Earth
T (surface): -143 °C to +35 °C
Lander Missions: Years of data

Venus (Radar Image)
Mass: 82% Earth
Orbit: 72% Earth
T (surface): +460 °C
Lander Missions: Hours of data

Surface of Venus: Toughest Place In Solar System

Combination of Temperature, Pressure, and Reactive Gas Extremes



Gas Composition at Surface of Venus

Gas	Ratio
CO_2	0.965
N_2	0.035
SO_2	18.0×10^{-5}
OCS	5.10×10^{-5}
H_2O	3.00×10^{-5}
CO	1.20×10^{-5}
H_2S	0.20×10^{-5}
HCl	5.00×10^{-7}
HF	2.50×10^{-9}

Figure modified from E. Kowala et al., Extreme Environment Technologies for Future Space Science Missions, NASA Jet Propulsion Laboratory, Pasadena, CA, USA, 2007, Report JPL D-32832. p. 49.

Past Missions:

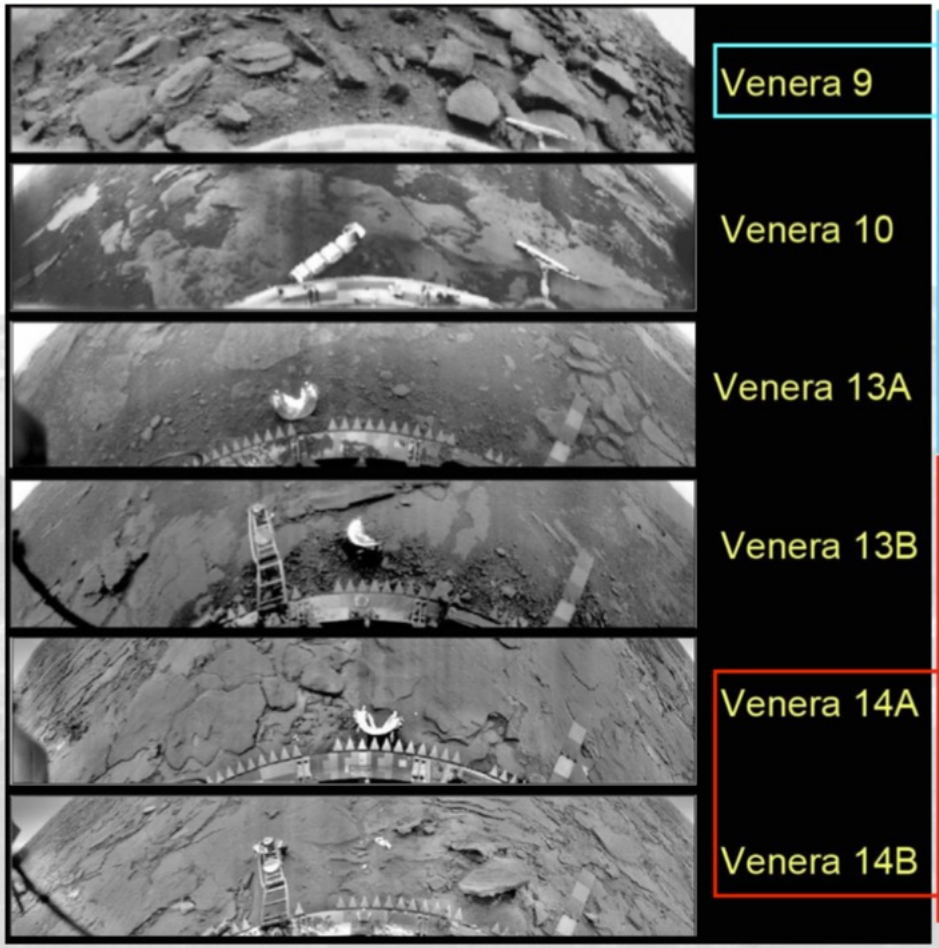
Russian Venus Lander Missions (1965-1981)

Source: https://www.lpi.usra.edu/vexag/chapman_conf/presentations/ocampo_for_saunders.pdf

	Year	Type / Method	Comment	Method EDL
Venus				
Venera 3 *FAILED*	1965	Venus Lander	Impacted Venus, Contact Lost	Parachute
Venera 4 FAILED	1967	Venus Probe	Failed at altitude 24.96 km	Parachute ~ 380 kg, Capsule Crushed
Venera 5 FAILED	1969	Venus Probe	During parachute descent data was transmitted from the atmosphere for 53 minutes before failure	Parachute ~ 380 kg, Capsule Crushed
Venera 6 FAILED	1969	Venus Probe	During parachute descent data was transmitted from the atmosphere for 51 minutes before failure	Parachute ~ 380 kg, Capsule Crushed
Venera 7 *PARTIAL FAILURE*	1970	Venus Lander	35 minutes of data during descent, 23 min. weak signal from the surface (1st man made object to return data after landing on another planet)	Aerobraking then parachute ~ 500 kg
Venera 8	1972	Venus Lander	Data during descent, plus 50 minutes after landing	Aerobraking/ D2.5m parachute at 60km ~ 500 kg
Venera 9	1975	Venus Orbiter and Lander	Operated for 53 minutes after landing	Protective hemispherical shell/ three parachutes/ disk shaped drag brake/ metal, compressible doughnut-shaped landing cushion
Venera 10	1975	Venus Orbiter and Lander	Operated for 65 minutes after landing	See Venera 9 ~ 660 kg
Venera 11	1978	Venus Lander	Transmitted data after touchdown for 95 minutes, until it moved out of range with Earth.	Aerodynamic ~/ parachute ~/ atmospheric braking/ soft landing
Venera 12	1978	Venus Lander	Worked until out of range , transmitted from the surface for 110 minutes.	See Venera 11
Venera 13	1981	Venus Lander	The lander survived for 117 minutes.	Parachute/ at 47km parachute released/ aerobraking
Venera 14	1981	Venus Lander	The lander survived for 57 minutes	See Venera 13

The longest surface mission survived for almost 2 hours

Past Missions:
Close-up Surface Features on Venus (USSR)



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Source: https://www.lpi.usra.edu/vexag/chapman_conf/presentations/ocampo_for_saunders.pdf

National Aeronautics and Space Administration

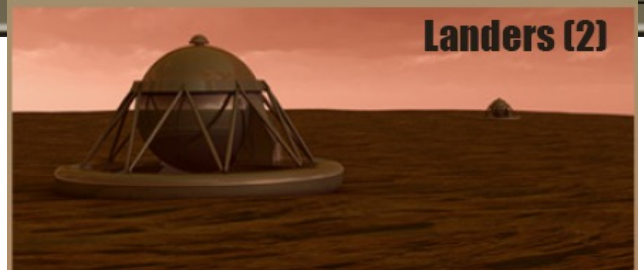
NASA's Flagship Mission to Venus

A Future Mission Concept

Venus Flagship Science Themes and Objectives

Science Theme	Science Objective
What does the Venus greenhouse tell us about climate change?	Understand radiation balance in the atmosphere and the cloud and chemical cycles that affect it
	Understand how superrotation and the general circulation work
	Look for evidence of climate change at the surface
How active is Venus?	Identify evidence of current geologic activity and understand the geologic history
	Understand how surface/atmosphere interactions affect rock chemistry and climate
	Place constraints on the structure and dynamics of the interior
When and where did the water go?	Determine how the early atmosphere evolved
	Identify chemical and isotopic signs of a past ocean
	Understand crustal composition differences and look for evidence of continent-like crust

Mass (CBE + Cont.)
686 kg; Payload mass: 106.2 kg
Lander Design
0.9-m diameter titanium shell (1-cm wall thickness); Rotating pressure vessel; Drill to 10-cm (2 samples)
Thermal Design
Passive thermal management: Lithium nitrate phase change material (PCM); Silica insulation: 5-cm external; 1-cm internal; Carbon dioxide backfilled pressure vessel
Power
Llithium-thionyl chloride primary batteries (the same cells used on the balloons), (6 kWh, 12.6 kg)
Telecom
S-band LGA to Orbiter with Electra (backup to flyby s/c)
Functions
Descent science for ~1 hour; Surface science for 5 hours



Despite ~ 30-year technology update:

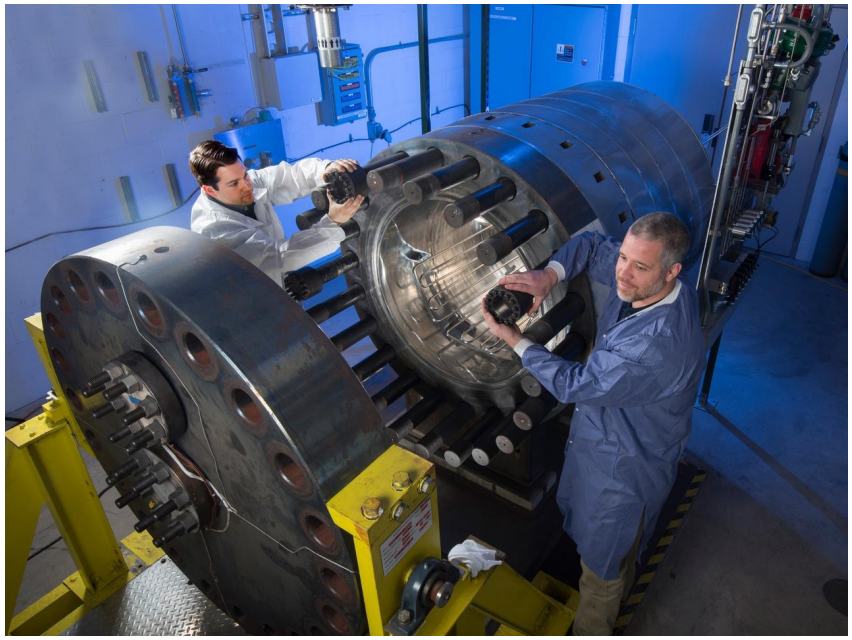
- Electronics is environmentally shielded
- Heavy lander mass (686 kg)
- 5 hours of science on surface

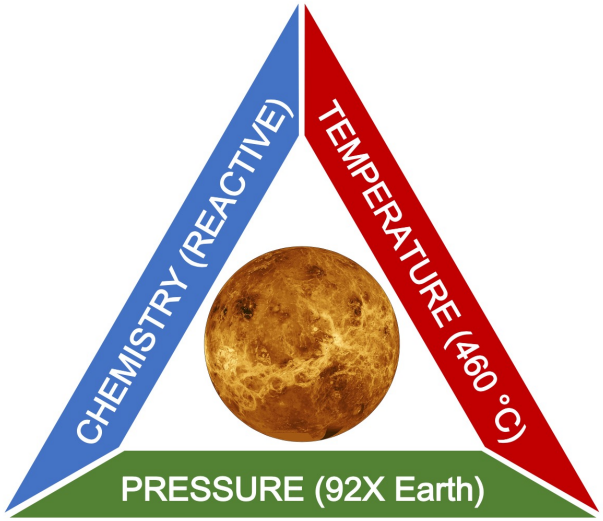
Source: https://www.lpi.usra.edu/science/kiefer/Publications/venusSTDT2009_finalreport.pdf

NASA Glenn Extreme Environment Rig (GEER)

https://www1.grc.nasa.gov/space/geer/

800-liter test chamber for high-fidelity simulation of Venus surface environment

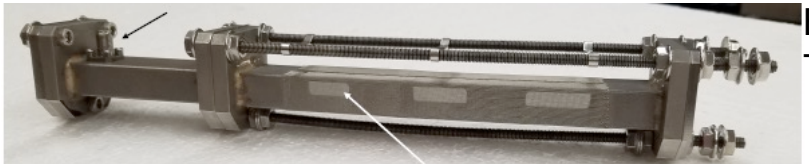




- **First 10 chemical constituents of Venus atmosphere**
- 460 °C (860 °F), 1350 psia (~ 92 Earth atmospheres)
- Long duration (months) test runs

NASA Glenn GEER Testing Experience

Full surface conditions (including gas composition to small concentrations) is relevant!
Many commonly-used elements react badly. Sufidization instead of oxidation.
Encapsulation/passivation of parts against Venus surface atmosphere is problematic.



Before Test

After Test

Large sulfide crystals formed on metal-alloy waveguide exposed to Venus surface conditions for 60 days in GEER.

Venus Atmosphere

Gas	Ratio
CO_2	0.965
N_2	0.035
SO_2	18.0×10^{-5}
OCS	5.10×10^{-5}
H_2O	3.00×10^{-5}
CO	1.20×10^{-5}
H_2S	0.20×10^{-5}
HCl	5.00×10^{-7}
HF	2.50×10^{-9}

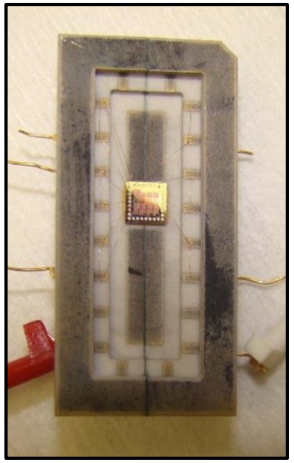
60 Day SiC Integrated Circuit Venus Test (in GEER)[1]

Two NASA Glenn SiC IC Gen. 10 circuits passed 60 days of stable electrical operation **directly exposed to the Venus surface environment** (no package lid).

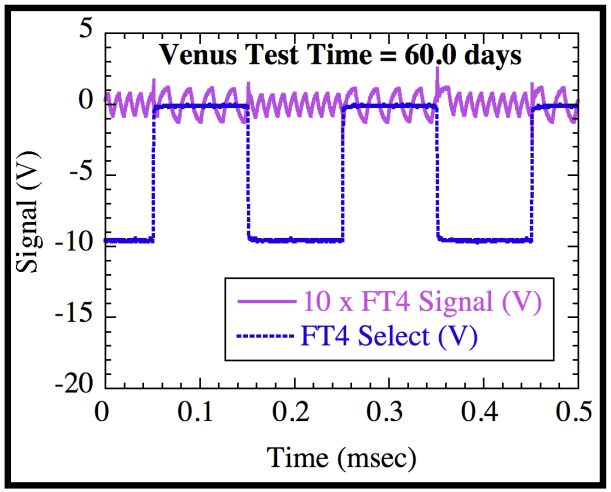
User-selectable ÷2/÷4 clock oscillator demonstration IC (175 transistors).

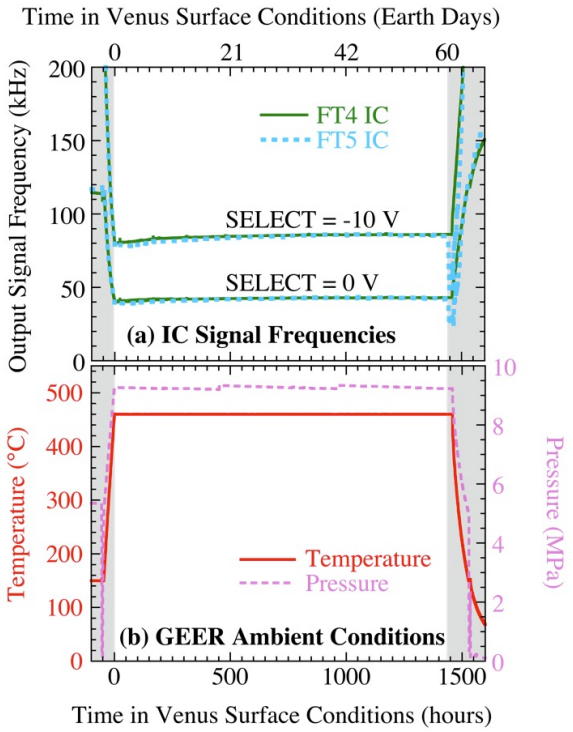
Before GEER

60 days GEER



Input and Output IC Waveforms

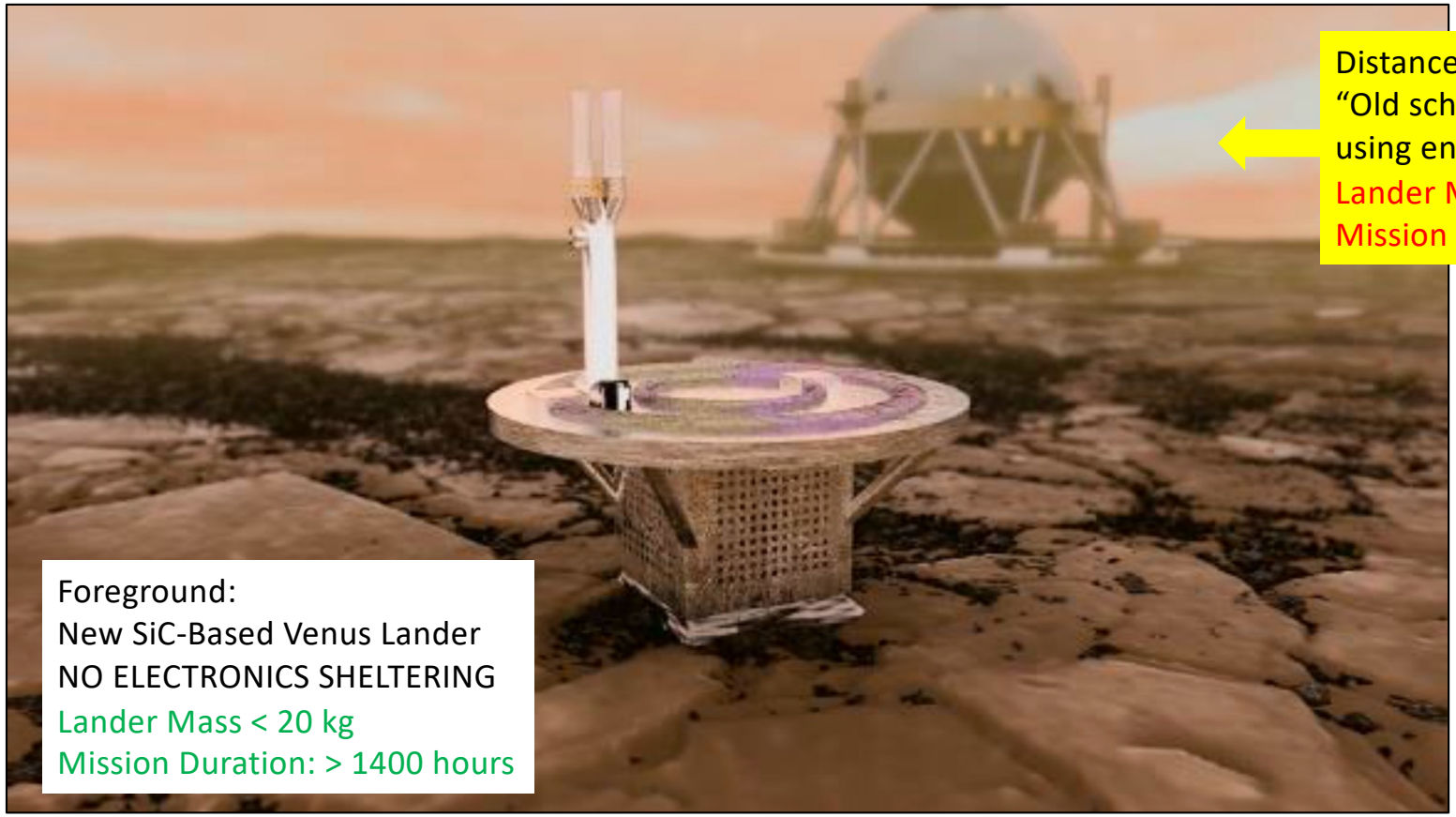




Source: Neudeck et al., https://doi.org/10.1109/JEDS.2018.2882693

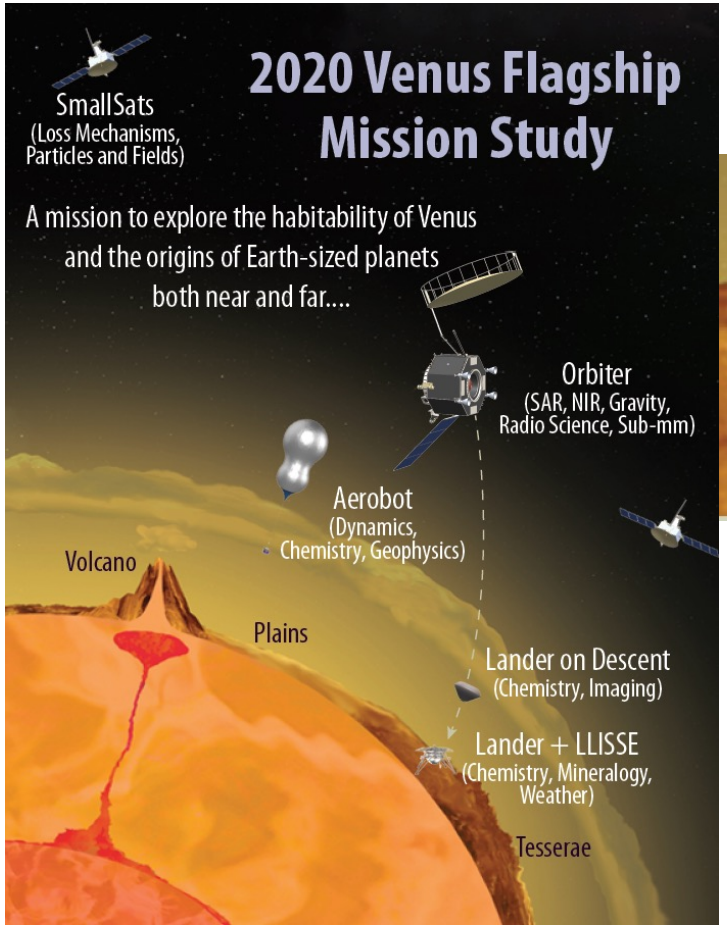
Impact of Venus Durable SiC Electronics

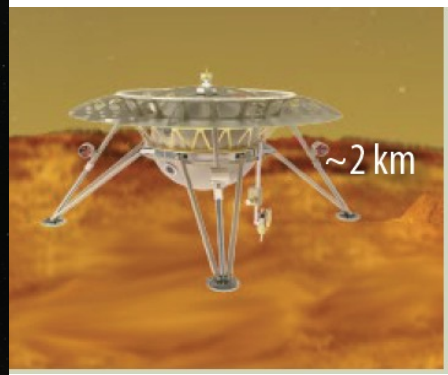
Completely new engineering approach enabled by SiC!



Source: T. Kremic & G. W. Hunter, https://doi.org/10.3847/25c2cfeb.cb6775e1

2020 Venus Flagship Mission Update





Lander	
Mass (MEV)	2002 kg
Power	9 Internal batteries (200 Ah)
Telecom	S-band to orbiter (80 mins), SmallSats (lander lifetime)
Lander Design	Ti pressure vessel, MLI insulation blankets, n-Eicosane phase change material, high vacuum environment
Functions	1 hr descent science, 7 hrs surface science, carry long lived surface meteorological package (60 days)

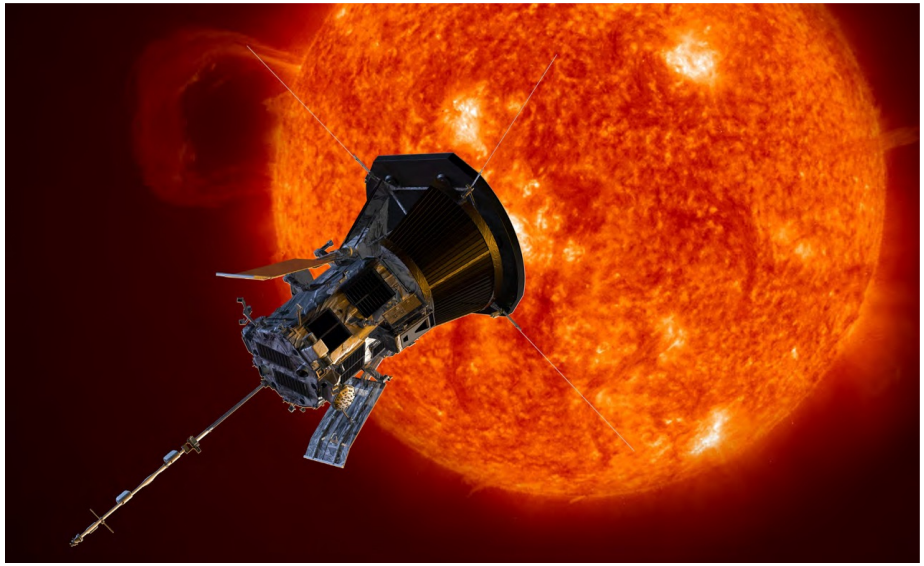
Small and independent all-SiC “LLISSE” lander would deploy along with heavy “old-school” Venus lander.

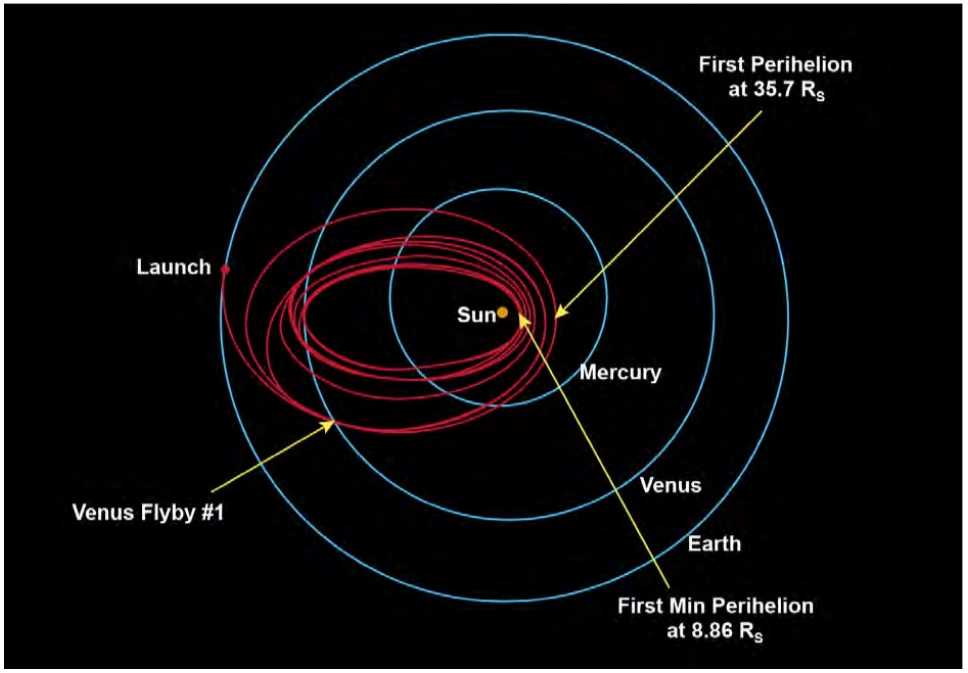
Technology demonstration proofs needed to justify full future transition to all-SiC Venus lander approach.

Source: https://science.nasa.gov/science-red/s3fs-public/atoms/files/Venus%20Flagship%20Mission.pdf

Parker Solar Probe Mission

Mission to study the Sun, including a series of the closest flybys ever attempted

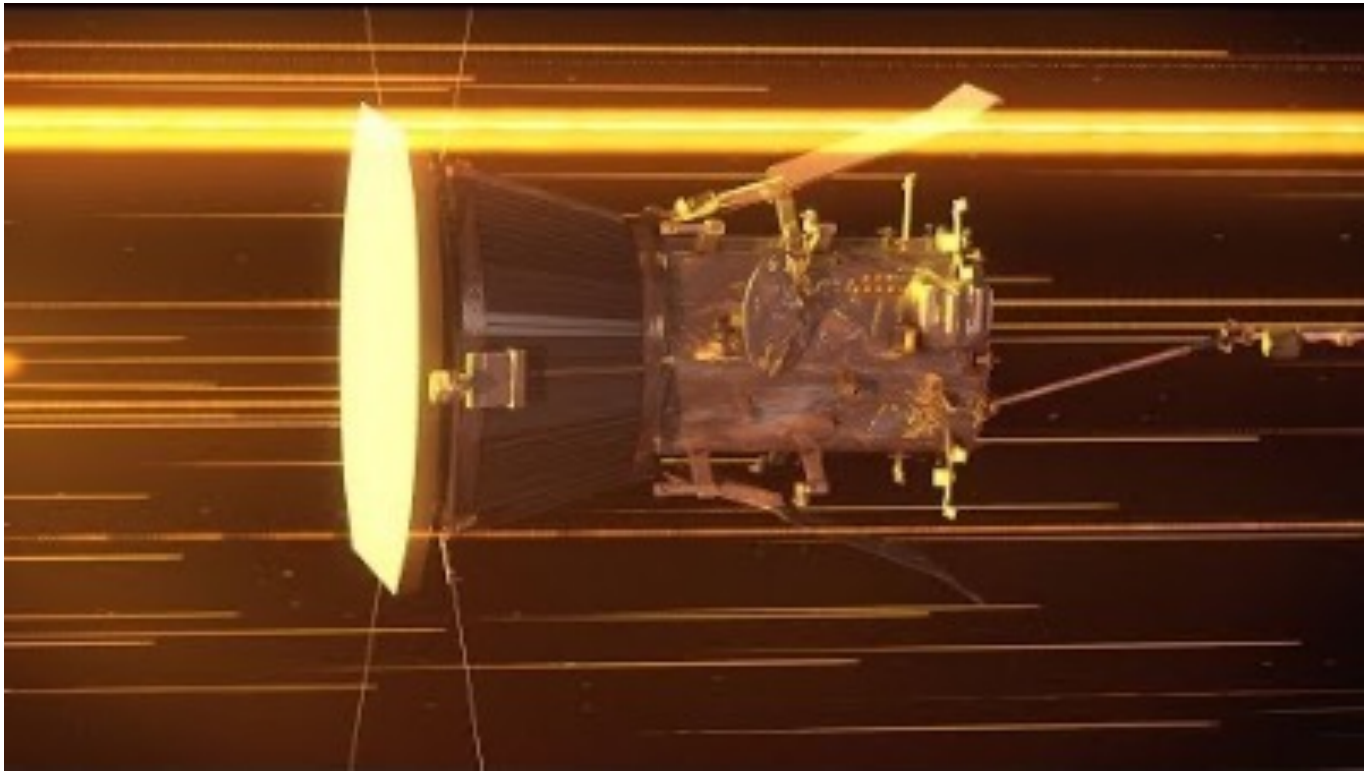




The Parker mission relies heat shield and cooling,
NOT high temperature electronics!

Source: https://www.nasa.gov/content/goddard/parker-solar-probe

Why Doesn't Parker Solar Probe Need High-T Electronics?



Source: https://www.nasa.gov/feature/goddard/2018/traveling-to-the-sun-why-won-t-parker-solar-probe-melt

It's The Capability, NOT The Technology

While the High Temperature Electronics (HTE) consumer market size is relatively small compared to conventional-temperature electronics market, competitive advantages HTE offers to crucial competitive performance advantages to very high-value aerospace systems.

New aerospace missions and new systems are enabled by High Temperature Electronics capability, but only if:

1. HTE is accessible for beneficial infusion and use = commercially manufactured & affordable & customizable
2. HTE is reliable, durable, predictable, *including the packaging and electrical connections to the system*

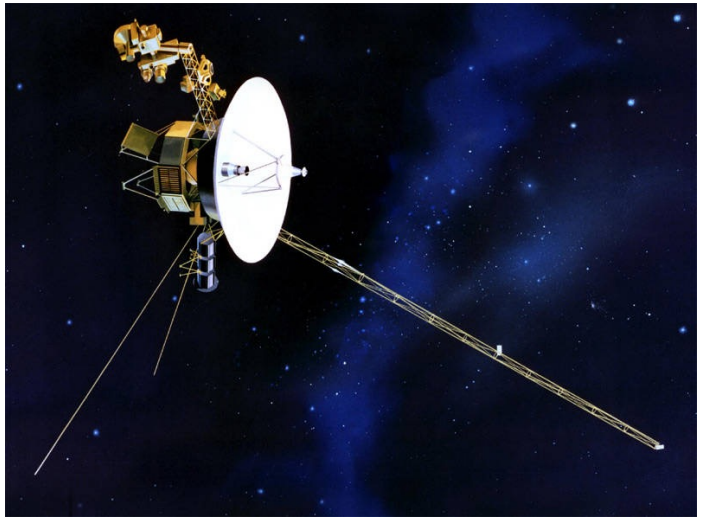
The aircraft system designer will not care which semiconductor is sitting inside avionics bays, so long as they are reliably helping aircraft performance at lowest cost.

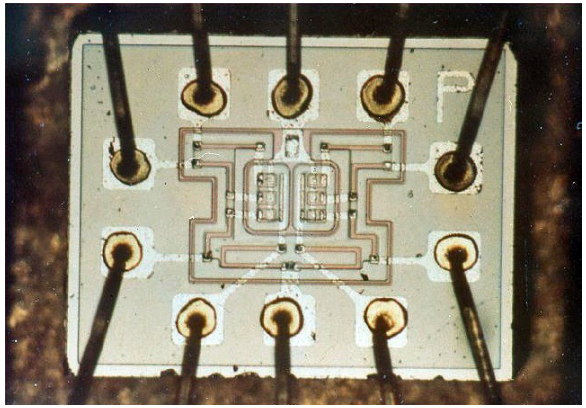
Use HTE to do the most necessary (highest system impact) functions in the harsh environment

- Never intended to completely supplant conventional-temperature aerospace electronics

“Simple” ICs Explored The Solar System

(NASA Images)





Apollo flew using 6 transistors per chip ICs.

Voyager spanned the solar system using few thousand transistors/chip ICs.

500 °C durable SiC ICs are already reaching a useful level of complexity.

Outline

Part 1: High Temperature *Aerospace* Applications (Why?)

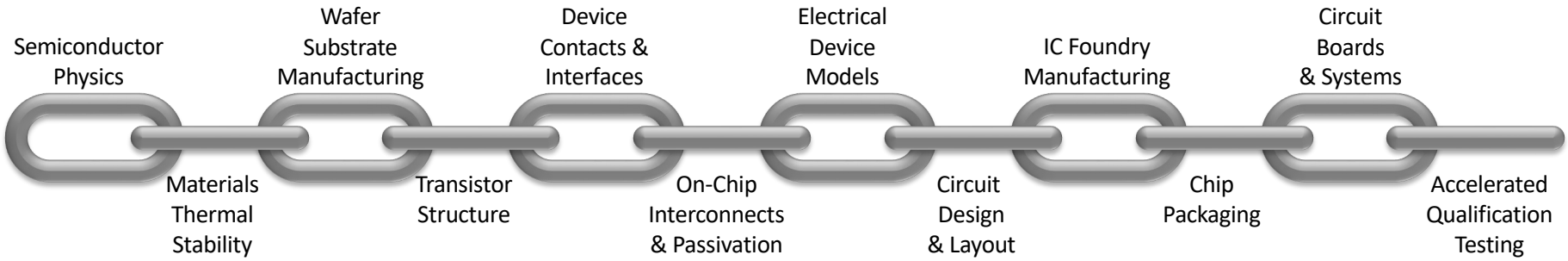
- Missions, Benefits, Requirements
- Aeronautics and Space

Part 2: High Temperature *Electronics* Technologies (How?)

- Semiconductors
- Packaging
- NASA Glenn SiC JFET-R Approach

IC Electronics Technology Chain

Chain that is taken for granted at conventional temperatures **is far from trivial to expand to temperature extremes.**



Any single weak link will prevent practical infusion and deployment of electronics.

IN THE DESIRED APPLICATION ENVIRONMENT, ALL LINKS MUST

1. FUNCTION INTEGRATED TOGETHER
2. BE PROVEN LONG-TERM DURABLE/STABLE - WITH MARGIN!

High-Temperature Electronics—A Role for Wide Bandgap Semiconductors?

PHILIP G. NEUDECK, SENIOR MEMBER, IEEE, ROBERT S. OKOJIE, MEMBER, IEEE, AND LIANG-YU CHEN

https://doi.org/10.1109/JPROC.2002.1021571

Invited Paper

High Temperature Electronics Application	Peak Ambient	Chip Power	Current Technology	Future Technology
Automotive				
Engine Control Electronics	150 °C	< 1 kW	BS & SOI	BS & SOI
On-cylinder & Exhaust Pipe	600 °C	< 1 kW	NA	WBG
Electric Suspension & Brakes	250 °C	> 10 kW	BS	WBG
Electric/Hybrid Vehicle PMAD	150 °C	> 10 kW	BS	WBG
Turbine Engine				
Sensors, Telemetry, Control	300 °C	< 1 kW	BS & SOI	SOI & WBG
	600 °C	< 1 kW	NA	WBG
Electric Actuation	150 °C	> 10 kW	BS & SOI	WBG
	600 °C	> 10 kW	NA	WBG
Spacecraft				
Power Management	150 °C	> 1 kW	BS & SOI	WBG
	300 °C	> 10 kW	NA	WBG
Venus & Mercury Exploration	550 °C	~ 1 kW	NA	WBG
Industrial				
High Temperature Processing	300 °C	< 1 kW	SOI	SOI
	600 °C	< 1 kW	NA	WBG
Deep-Well Drilling Telemetry				
Oil and Gas	300 °C	< 1 kW	SOI	SOI & WBG
Geothermal	600 °C	< 1 kW	NA	WBG

There are many definitions and flavors of the term, "High Temperature Electronics"

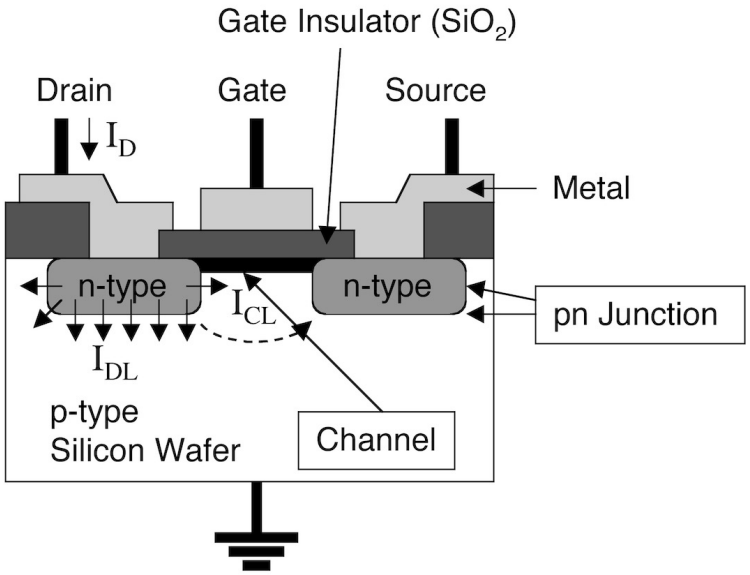
Atmospheric-temperature?
Device-temperature?
Package-temperature?
Constant-temperature?
Peak-temperature?
Transient-temperature?

Typically, T > 125 °C

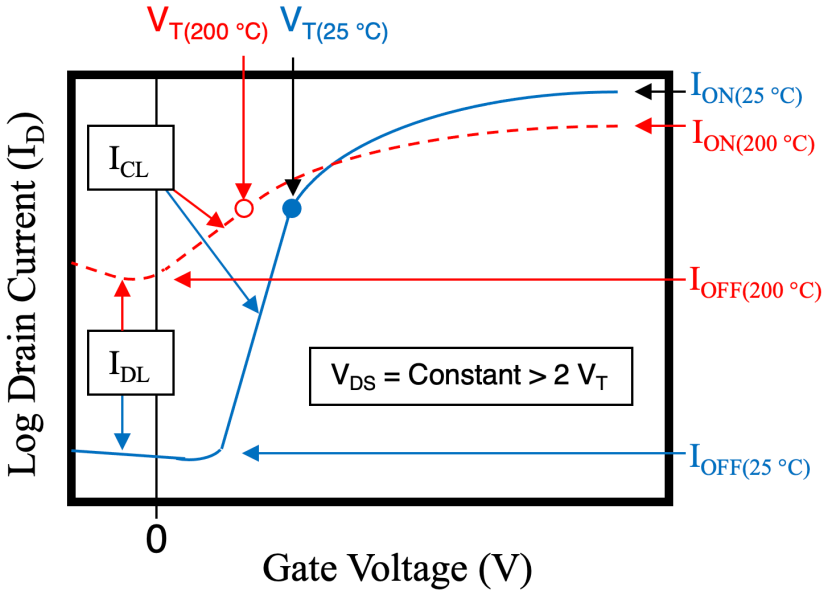
Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

How does device operation change when temperature is increased?

MOSFET Cross-Sectional Structure



MOSFET Turn-Off I-V Characteristics



Reverse bias leakage current of drain pn junction I_{DL} dictates MOSFET off-state current floor I_{OFF}

At temperature goes up, the conventional MOSFET:

- **Loses gain and on-state current (I_{ON})**
- **Loses its ability to turn off ($I_{OFF} \approx I_{DL}$ current floor)**

Source Neudeck, Okojie, & Chen: https://doi.org/10.1109/JPROC.2002.1021571

High-Temperature Electronics—A Role for Wide Bandgap Semiconductors?

PHILIP G. NEUDECK, SENIOR MEMBER, IEEE, ROBERT S. OKOJIE, MEMBER, IEEE, AND LIANG-YU CHEN

https://doi.org/10.1109/JPROC.2002.1021571

Invited Paper

Approximation formula for reverse-biased pn junction leakage:

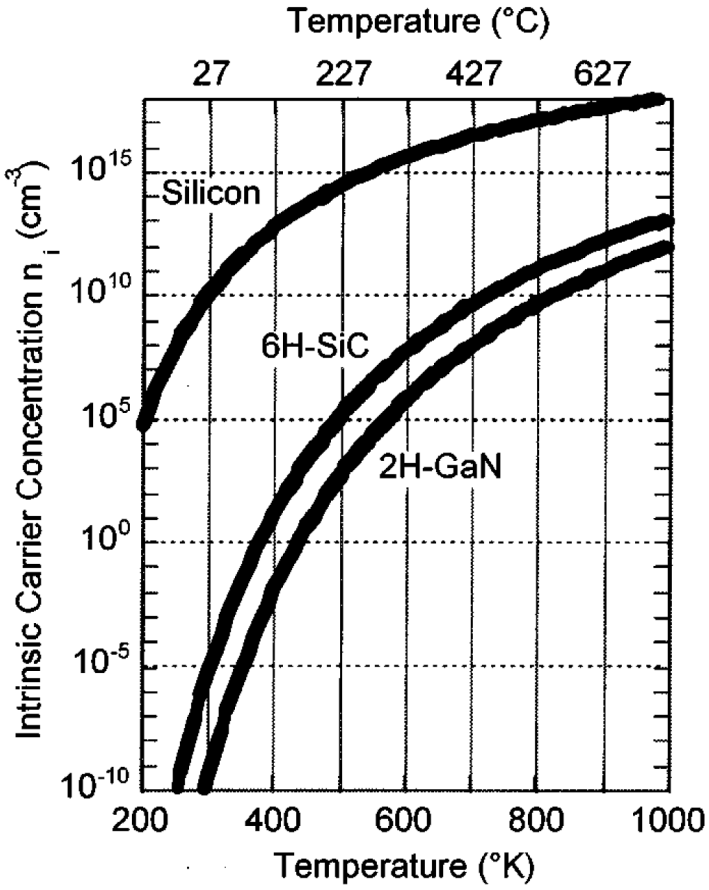
$$I \cong -qAn_i \left[\frac{n_i}{N_D} \sqrt{\frac{D_P}{\tau}} + \frac{W}{2\tau} \right]$$

Strongest temperature dependence is n_i the intrinsic carrier concentration:

$$n_i = \sqrt{N_C N_V}\, e^{-E_G/2kT}$$

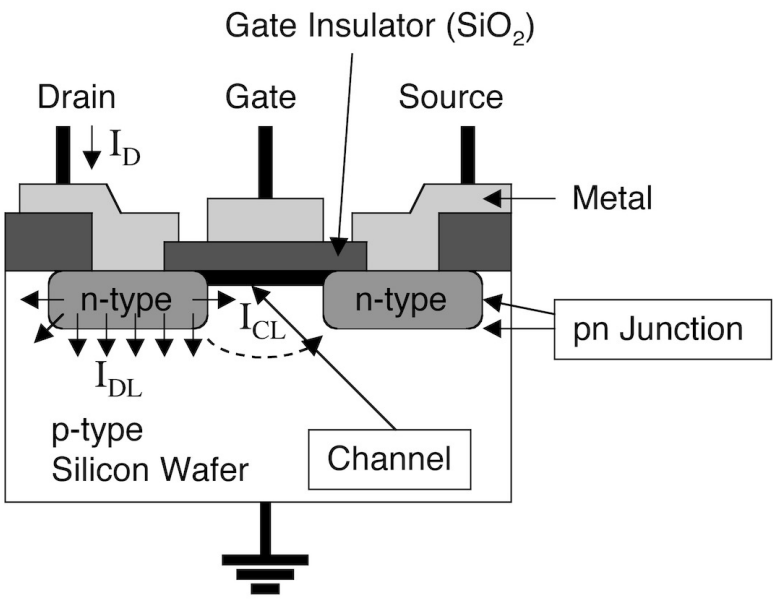
which has exponential dependence on semiconductor bandgap E_G and temperature T.

Leakage current is often the factor limiting device/circuit high temperature functionality instead of intrinsic carrier conduction

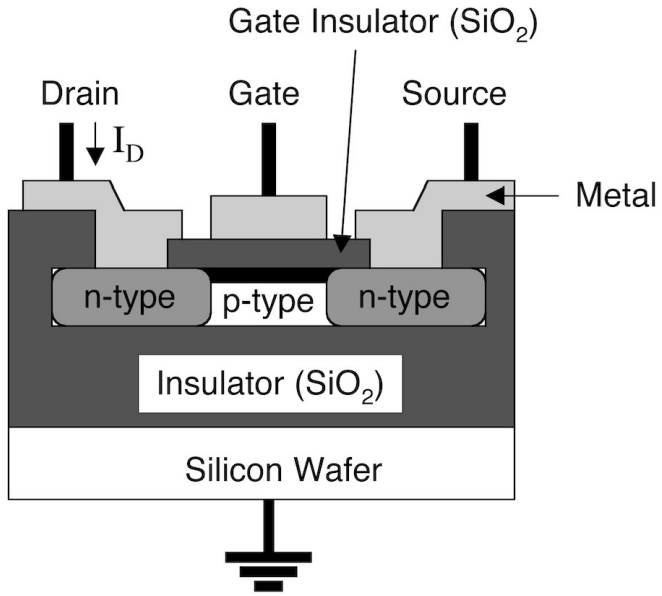


Silicon-On-Insulator (SOI) MOSFET

Conventional MOSFET Cross-Section



SOI MOSFET Cross-Section



By decreasing pn junction leakage area, leakage current is lowered permitting operation at higher temperature.

- Amount of leakage, highest temperature are circuit and application-specific!
- For example, “Signal integrity” criteria will be different for digital vs. analog circuits.

Source Neudeck, Okojie, & Chen: https://doi.org/10.1109/JPROC.2002.1021571

High Temperature Semiconductor Device Development

Prototype T > 450 °C operation has been reported for decades.

- Multiple research groups (industrial, academic, and governmental)
- Multiple semiconductor materials (SiC, III-N, silicon-on-insulator)
- Multiple transistor approaches (JFET, MESFET, MOSFET/CMOS, and Bipolar)

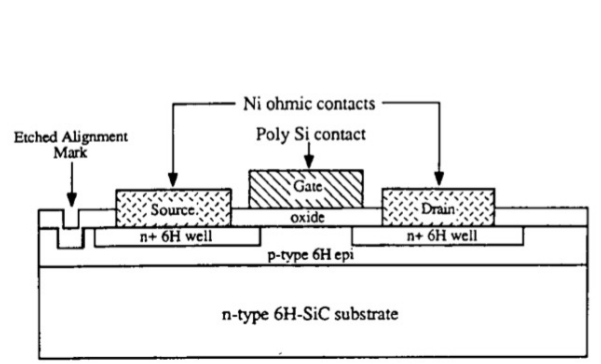
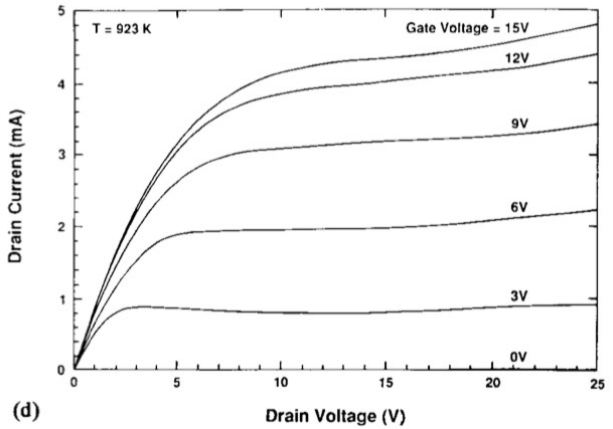


Fig. 19. Material structure of a 6H-SiC MOSFET fabricated at Cree Research, Inc.



Davis et al., Proc. IEEE, vol. 79, no. 5 pp. 677-701 (1991).

Missing from majority of reports: Long term operational stability at T > 450 °C

- In most cases, only brief (~ 1 hour) heated probe-station testing

Demonstrations insufficient for serious consideration by aerospace systems designers

NASA Glenn SiC IC Technology Development Goals

Greatly expand the application-viable IC operating temperature envelope

Bring initial IC electronics capability reliably to previously unthinkable places
- **Enable new approaches to systems dealing with harsh environments**

- At least 500 °C operation for long duration
  - More than 200 °C above silicon-on-insulator practical limit

- At least 2000 hours of stable electrical operation at 500 °C
  - Jet engine ground test, Venus surface missions

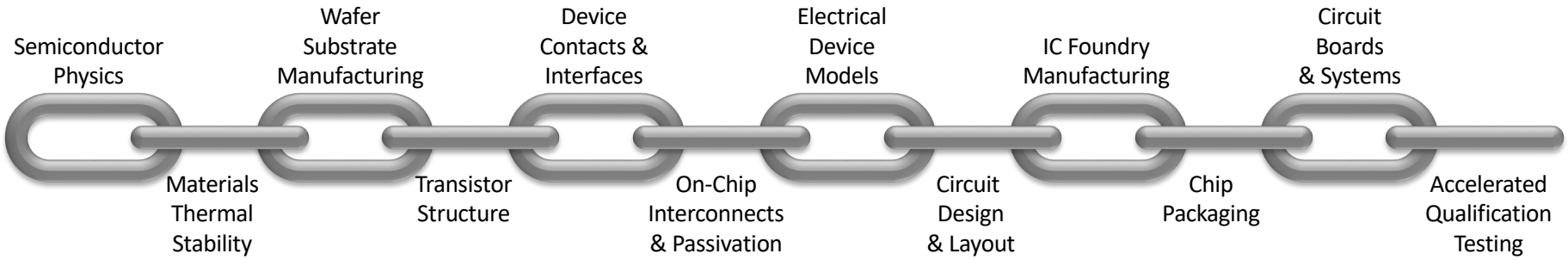
- At least 2 levels of 500 °C durable on-chip interconnect
  - Enable more complex, higher density ICs

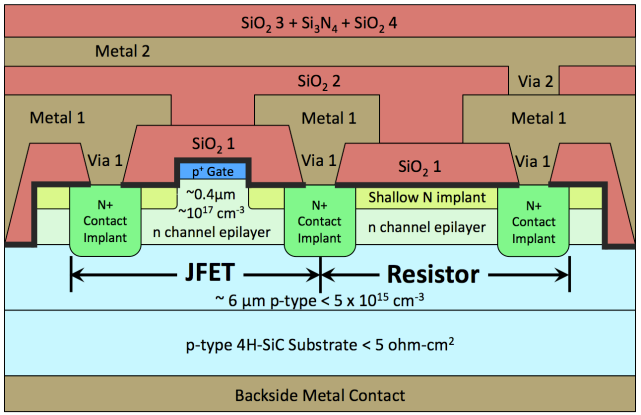
- Chip packaging and multi-chip circuit boards for 500 °C operation
  - Integration with sensors, wireless communications, subsystems

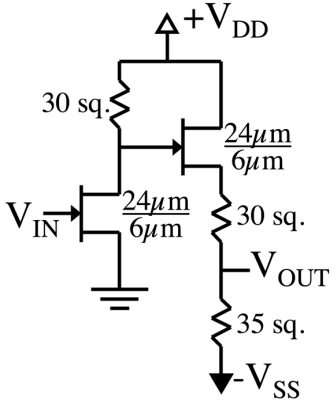
- Infusion of beneficial 500 °C ICs into missions and systems

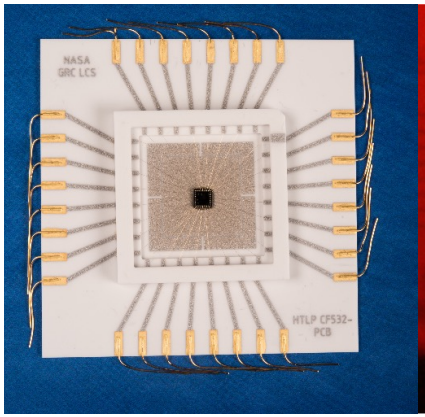
High Temperature Electronics Technology Chain

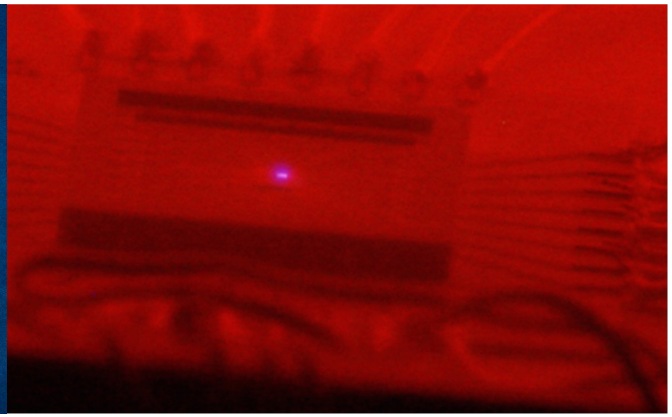
Chain that is taken for granted at conventional temperatures **is far from trivial to expand to temperature extremes.**











"Learn by Doing" Prototype SiC Design, Fab, Package, & Test Workflow

NASA Glenn SiC IC Development Philosophy

"Over-design" every aspect to make high temperature durable ICs

- De-prioritize other device metrics (such as power & frequency)
- Seek compatibility IC manufacturing materials, tools, and techniques

Device Foundation

- SiC epilayer PN homojunction transistor (not metal-semiconductor or MOS gate)
- Stable ohmic contacts

On-chip Integration

- Stable interconnect
- High circuit density (2-level interconnect, small devices & isolation)
- Temperature and process tolerant circuit design

Ceramic packaging and circuit boards

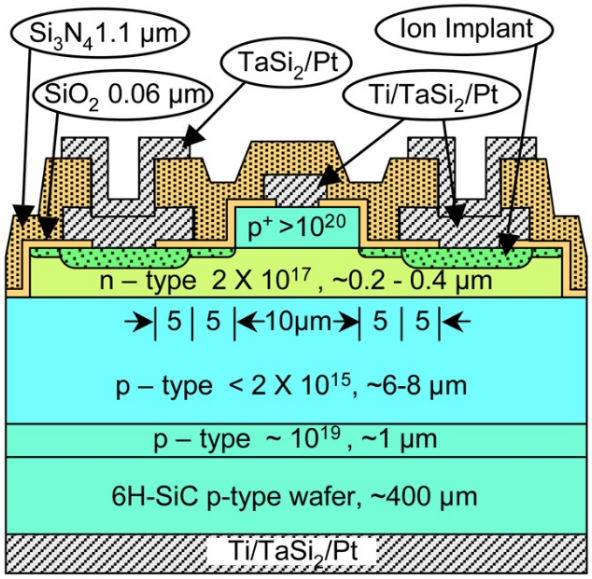
Demonstrate initial 500 °C durable IC capability, infuse and improve in parallel

"LEARN BY DOING" OVER SUCCESSIVE GENERATIONS (CYCLES) OF PROTOTYPE IC FABRICATION AND CHARACTERIZATION.

Transistor Device Approach

Epitaxial SiC n-JFETs developed as the most straightforward foundational transistor for achieving long-term device stability at T ≥ 500 °C

2007 NASA 6H-SiC JFET [1]



SiC is the most stable/inert semiconductor crystal
- Low impurity diffusion, low reactivity

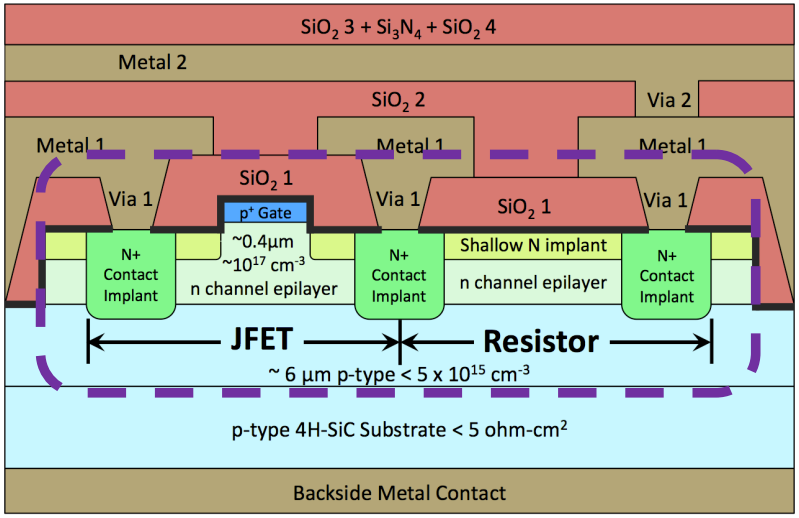
Inherent JFET High-T Stability Advantages
- Majority carrier device
- Low-leakage epilayer PN homojunctions
- Minimal sensitivity to p-type (gate) contact
- N-type ohmic contacts/implants

Other transistor types more challenging to render stable/durable at T > 450 °C.
- Bipolar transistors: n-type AND p-type contact AND minority carrier sensitivity
- MOSFETs/CMOS: MOS junction sensitivity
- MESFETs: Rectifying metal-semiconductor junction leakage & sensitivity
- III-N HFETs & Ga_2O_3: Heterojunction sensitivity, more reactive than SiC

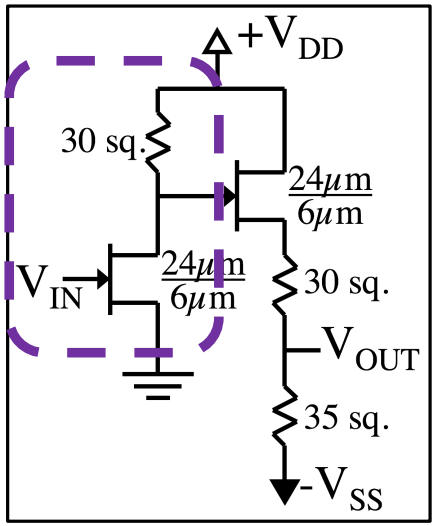
[1] Neudeck et al., IEEE Electron Device Lett. vol. 25, no. 5, pp 456-459 (2008) https://doi.org/10.1109/LED.2008.919787

Basic Device & Circuit Approach[1,2]

JFET and Resistor (JFET-R) Device Cross-Sections



NOT Logic Gate Schematic



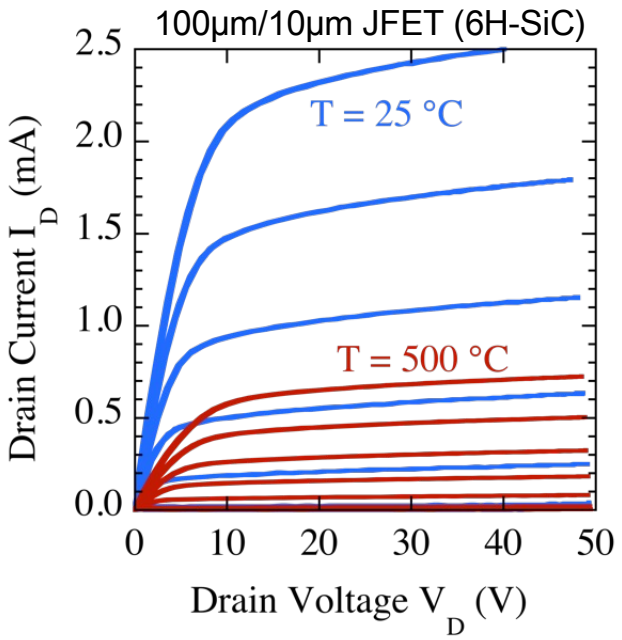
- **Resistors made with same epi as JFET → well-matched T dependence**
- Layout ratio-based circuit design (not absolute component values)
- Negative threshold voltage V_T → negative signal voltages (roughly -1V to -10V logic)
- Typical V_{DD} = +25 V, V_{SS} = -25V Chip backside is biased at V_{SS}

[1]M. J. Krasowski, US Patent 7,688,117 (2010) https://image-ppubs.uspto.gov/dirsearch-public/print/downloadPdf/7688117
[2]Neudeck, Spry, Chen: https://ntrs.nasa.gov/citations/20160014886

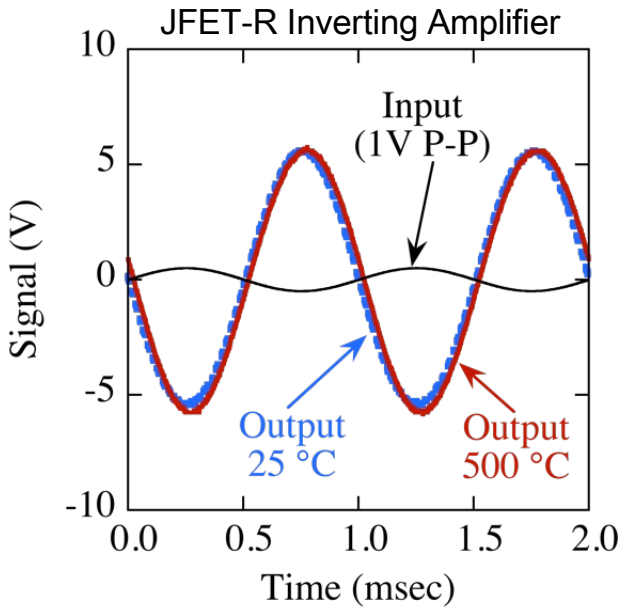
SiC JFET-R Temperature Performance

Source: https://ntrs.nasa.gov/citations/20130000502

Transistor Characteristics



Circuit Characteristics



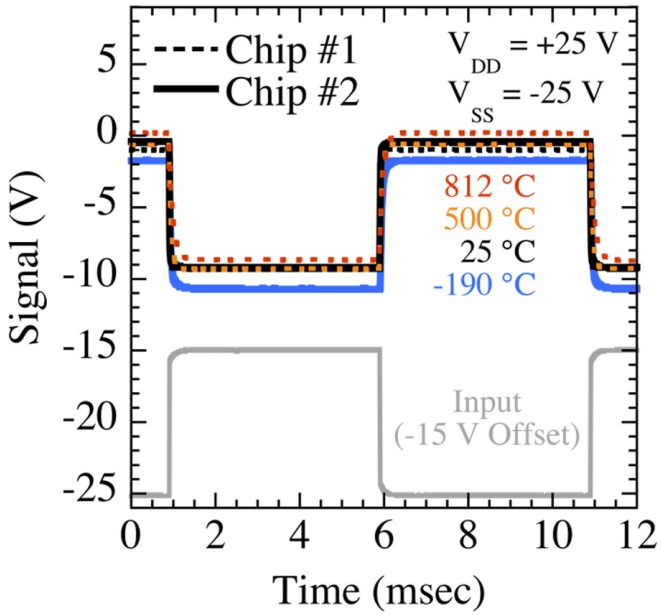
Despite large (> 3X) change in JFET characteristics…

→

…nearly temperature-independent circuit operation can be achieved!

-190 °C to +812 °C "Go Anywhere" Functionality

(Generation 10.1 NOT Gate Testing)

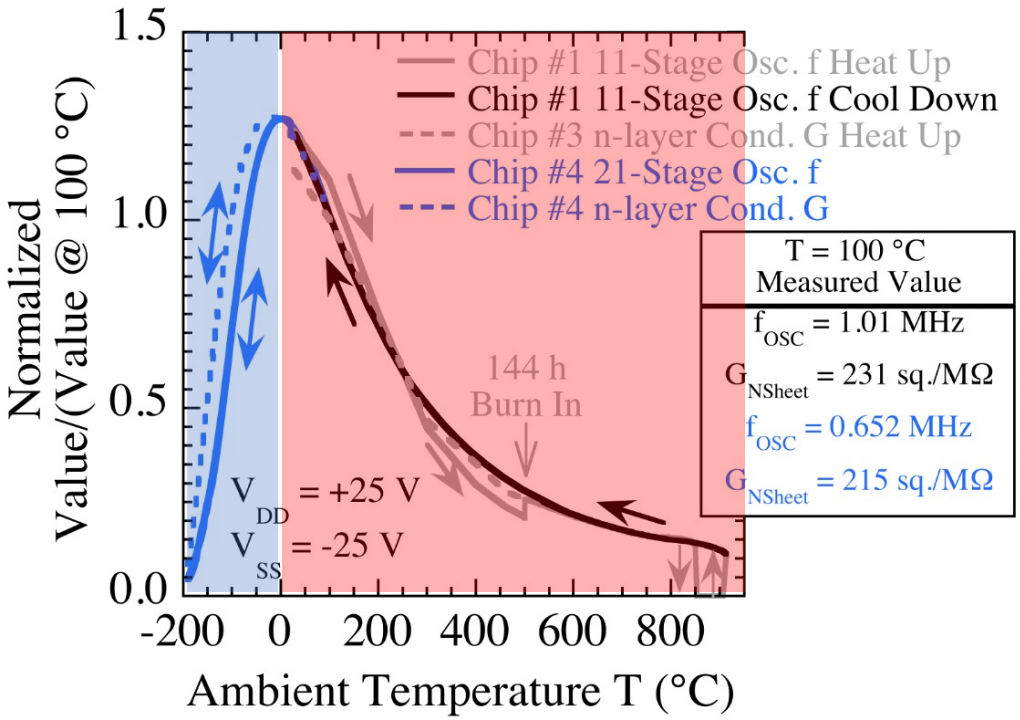


- 1000 °C temperature span WITHOUT changing signal/supply input voltages!
- *SiC JFET ICs function in cold environments WITHOUT "cold start" issues.*
- Temperature-accelerated 800 °C lifetime testing for long-duration 500 °C missions.
- Straightforward functional yield screening at 25 °C (on-wafer probe test).

Source: Neudeck, et al: https://ntrs.nasa.gov/citations/20190027358

Sheet Conductance & Ring Oscillator Frequency vs. Temperature

Circuit frequency & power track 4H-SiC n-layer conductivity change



Low Temperature (T < 0 °C):

Incomplete ionization "freezeout effect" dominates 4H- SiC n-layer conductivity

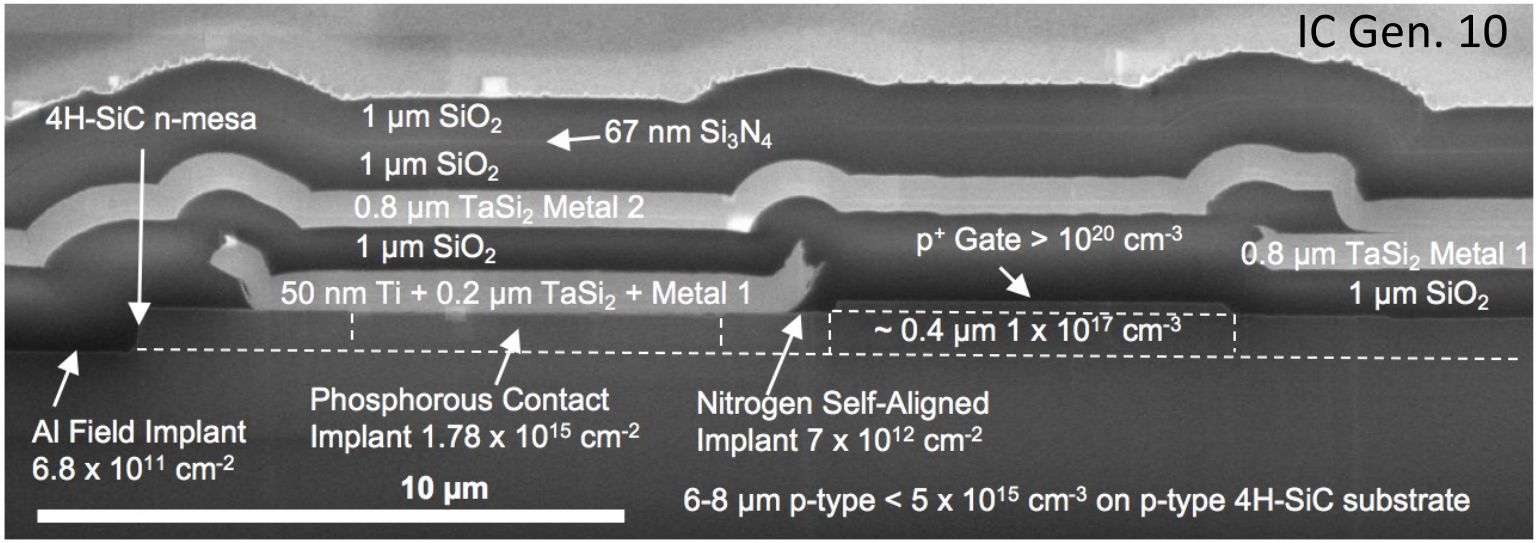
High Temperature (T > 0 °C):

Carrier mobility reduction due from thermal phonon scattering dominates 4H-SiC n-layer conductivity.

Circuit frequency and power are highest near 0 °C, decrease by roughly factor of 4-5 as temperature increased to 500 °C.

Neudeck, et al., https://ntrs.nasa.gov/citations/20190027358

500 °C Stable Two Levels Interconnect[1]

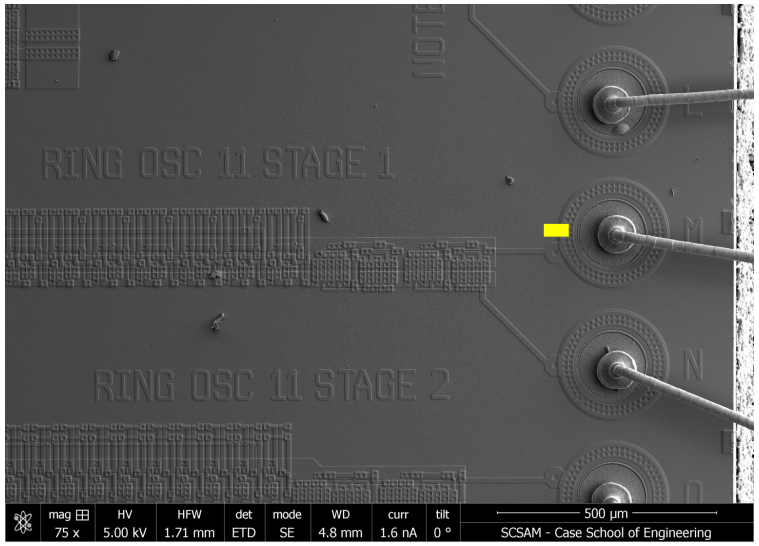


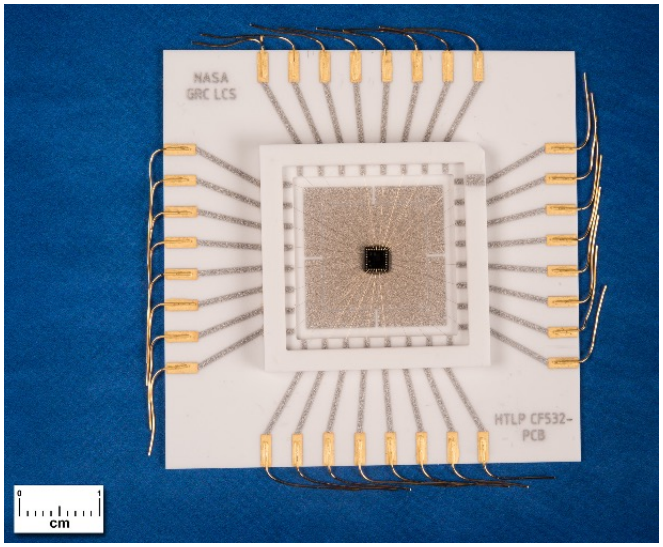
IC processing and materials compatible with SiC power device tools & manufacturing

- Close-proximity sputtering of $TaSi_2$ (21mm target to substrate spacing)
- LPCVD tetraethyl orthosilicate (TEOS) and Si_3N_4 layers deposited at 720 °C
- **All interconnect completely buried/passivated beneath dielectric.**

[1]P. G. Neudeck, et al., 2018 IMAPS High Temperature Electronics Conf. pp. 71-78
https://ntrs.nasa.gov/citations/20180003391

500 °C Stable Bond Pads and Packaging[1,2]



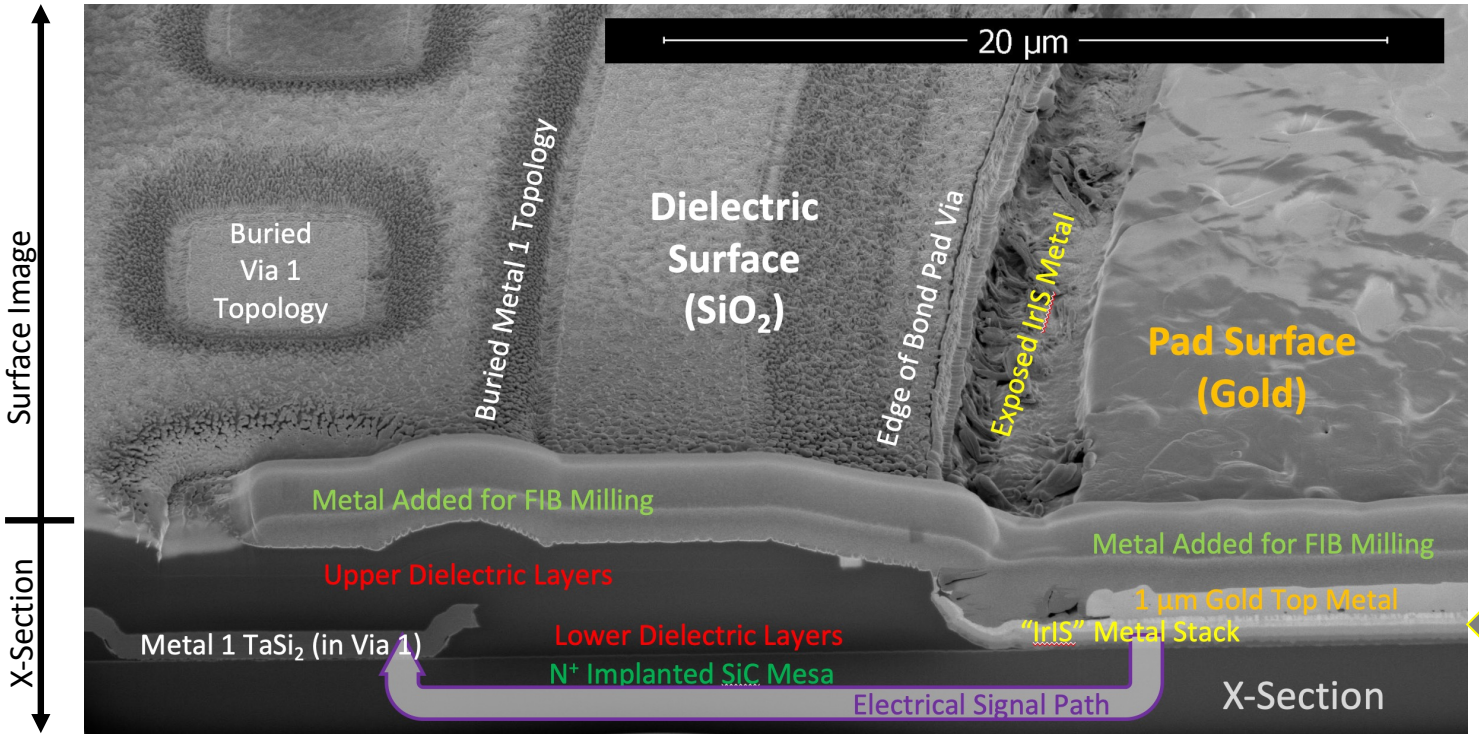


- "IrIS" bond pad metal stack anchored directly to SiC[1]
- Pt thick-film traces, Au/Pt pads, Au die attach (600 °C), and Au ball bonding[2].

[1]D. Spry & D. Lukco, J. Electronic Materials 41 p. 915 (2012)
[2]L. Chen, et al., Proc. 2016 IMAPS High Temperature Electronics Conf. pp. 66-72
https://ntrs.nasa.gov/citations/20160014867

500 °C Durable "Iridium Interfacial Stack" (IrIS) Bond Pad[1]

(FESEM FIB Cross-Section)

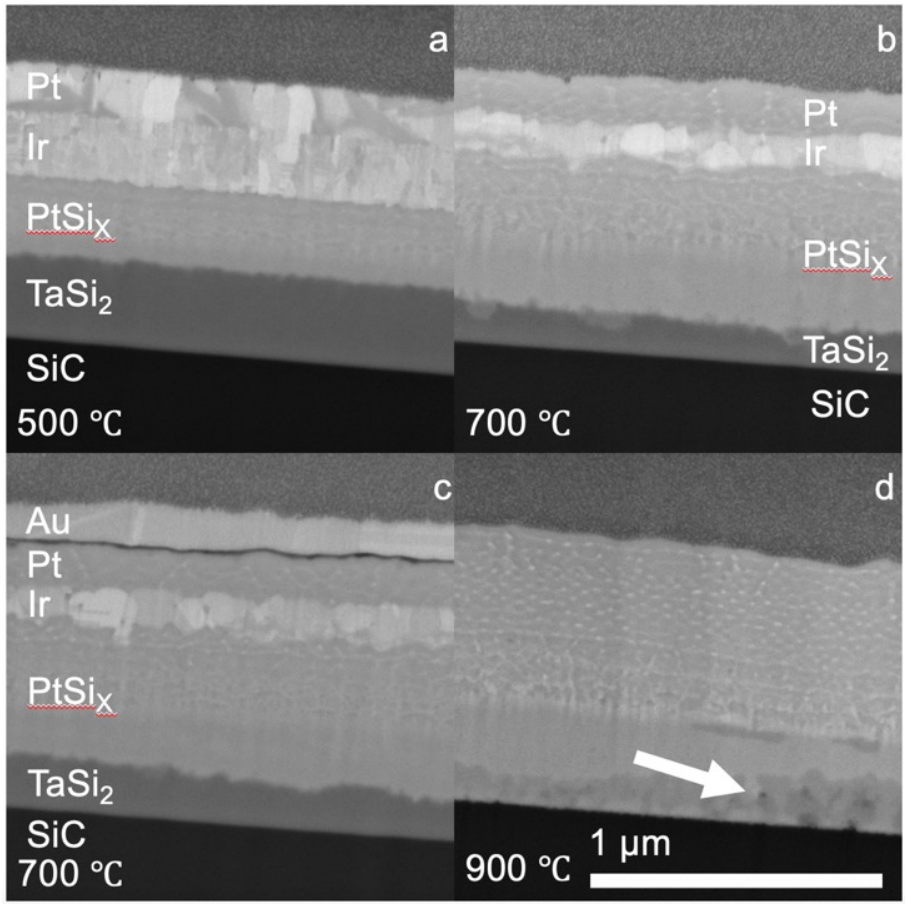


"IrIS" Stack[1]
0.2 µm Pt (Top)
0.3 µm Ir
0.2 µm Pt
0.4 µm $TaSi_2$ (Bottom)

Large-area "IrIS" metal bond pad stack is anchored directly to hard SiC crystal foundation.
Interconnect Metals 1 & 2 are 100% buried in dielectric and DO NOT TOUCH "IrIS" metal.
- N+ Implanted SiC connects "IrIS" with Metal 1 (~ 100 Ω series resistance).

[1]Spry et al., J. Electronic Materials 41(5) p. 915 (2012).

Annealing Study of Thermal Limits of "IrIS" Bondpads



The first clear structural temperature limit is just above 700 °C.

Image **a** after 500 °C anneal the IrIS stack has segregated into its planed layers of $TaSi_2$ that contacts the underlying SiC, $PtSi_X$, Ir, Pt.

Image **b** post 700 °C image of bond pad without Au cap reveals a thickened $PtSi_X$ zone that comes closer to SiC interface, the contact remains a smooth and abrupt interface between $TaSi_2$ and SiC.

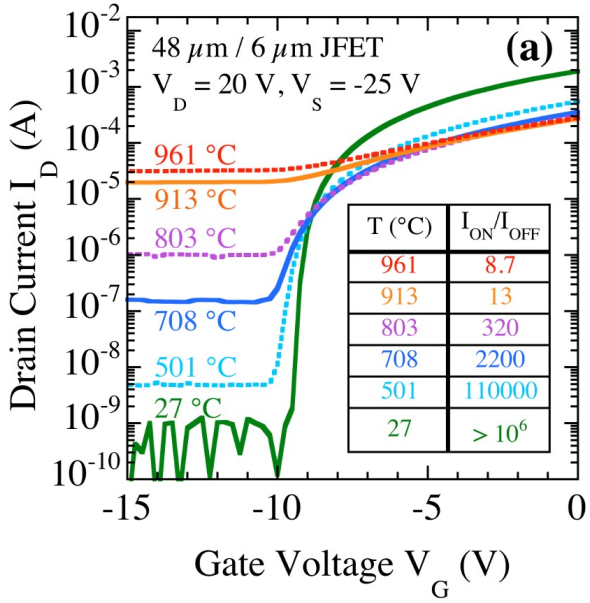
However, image **c** of 700 °C anneal IrIS stack with Au cap shows evidence of oxygen accumulation at the Au/Pt interface which could become a bonding failure point if the Au ball bond attached during chip packaging is not thick enough to prevent oxygen penetration.

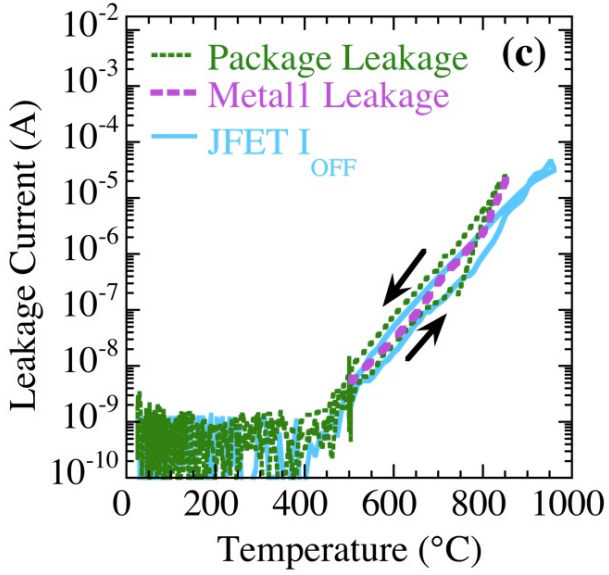
Image **d** at 900 °C, the Fig. 2d image shows Pt has reached the SiC interface along with evidence of voiding (white arrow).

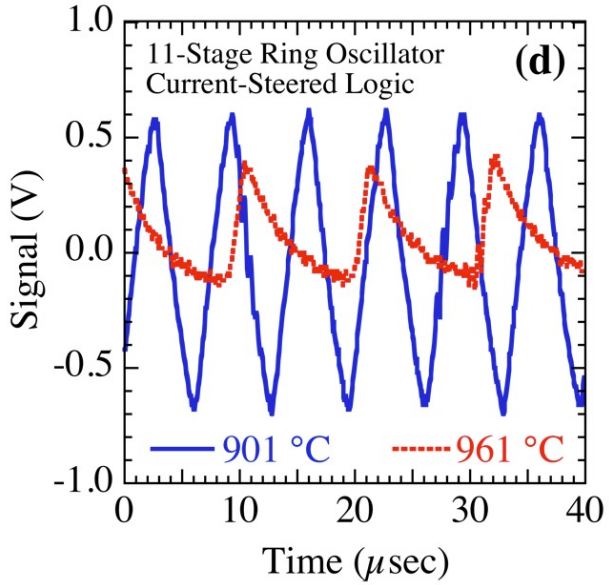
D. Spry & P. Neudeck, http://csmantech.org/wp-content/uploads/Digest/Digests-2021/4.3.2021-CSMantechReportSpryF1.pdf

Short-Term Operation Demonstrated Above 900 °C[1]

Enables temperature-accelerated lifetime qualification testing for 500 °C applications.





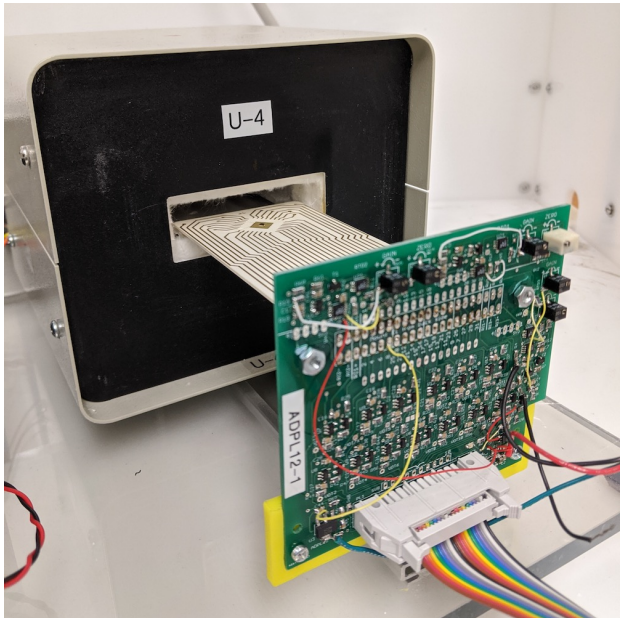


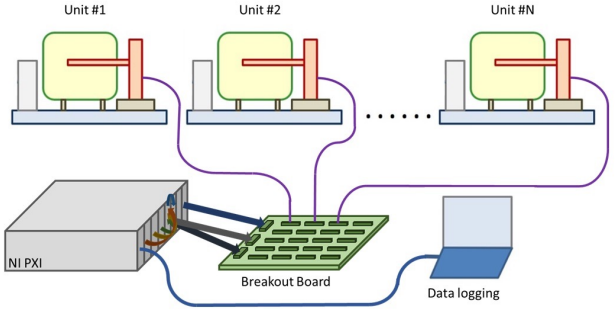
(Note: Waveforms are probe-loaded)

- Packaging leakage was limiting experimental factor, package was designed for 500 °C.
- **"Intrinsic" JFET-R IC high-temperature limit remains to be ascertained.**

[1]P. Neudeck, et al., IEEE Electron Device Lett. 38 (2016) 1082-1085 https://doi.org/10.1109/LED.2016.2544700

Electronics Qualification for Long-Term 500 °C Operation





Aerospace & automotive electronics qualification processes practiced for decades need to be extended/adapted to cover much higher temperature

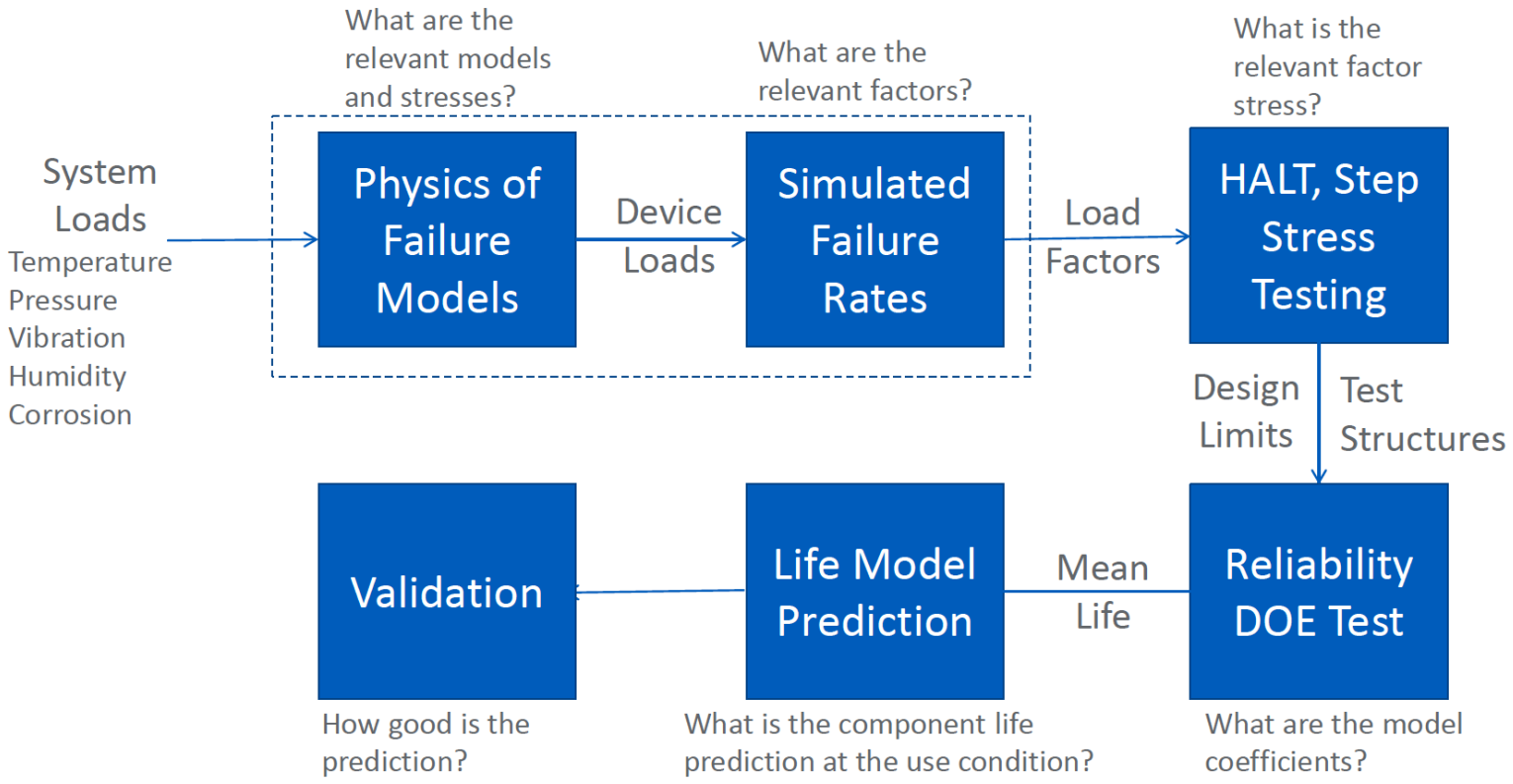
- Testing statistics (parallel testing)
- Chips, packages, and multi-chip circuit boards
- Temperature acceleration, voltage/current acceleration
- Repeated thermal cycling and shock testing
- Vibration testing at high temperature
- **Failure mechanism documentation & understanding across the intended application environment**

NASA Glenn expansion of parallel testing capacity using “small pizza oven” concept[1]
- Chip (+package) on ceramic board inserted into oven slit.
- Goal is 50+ parallel IC tests with rapid thermal cycling.

Source: Izadnegahdar et al., https://ntrs.nasa.gov/citations/20210011676

Reliability Testing Approach (QALT)

Slide presented by D. Shaddock of GE Research at 2023 IMAPS International High Temperature Electronics Conference



" Let the parts do the talking and the engineers do the guessing" – former Motorola trainer

IC Gen. 10 Primary Durability Limitation

Sudden and unpredictable "open-circuit" failures occur due to dielectric crack formation[1,2].

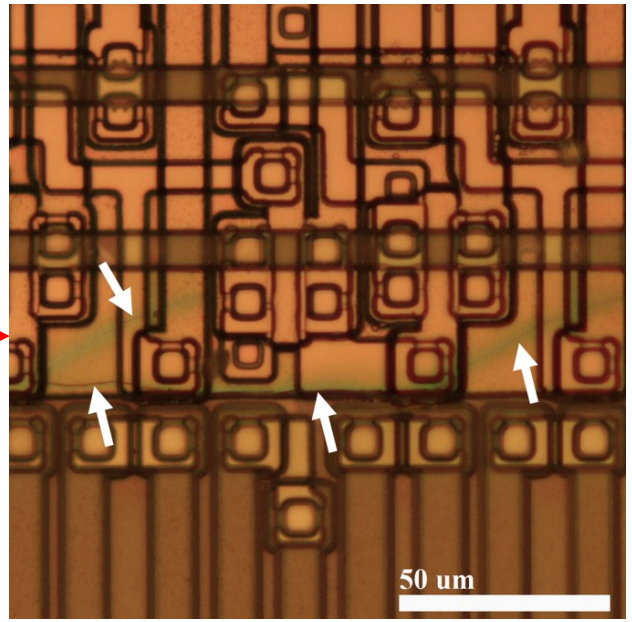
- Unacceptable random failure risk for missions

Table I. 500 °C JFET IC Test Summary

Packaged IC Sample	*r* (mm)	500 °C Time	Test Status
RAM #1	13.4	63 days	Suspended
RAM #2	6.7	420 days	Running
Clock #1	24.2	19 days	Failed
Clock #2	15.3	437 days	Running
Clock #3A	12.4	403 days	Running
Clock #3B	12.4	403 days	Running
Clock #3C	13.4	87 days	Failed

Above table is the total oven-test data set for complicated Gen. 10 ICs.

- Much larger quantities of oven-tests needed to meet standard practices/statistics for aerospace-mission qualification of ICs.



White arrows denote examples of dielectric cracks and metal trace discoloration/oxidation are observed in the oven-failed Clock #1 IC.

[1]D. J. Spry, et al., Proc. IMAPS High Temperature Electronics Conf., 2016, pp. 249-256 https://ntrs.nasa.gov/citations/20160014879

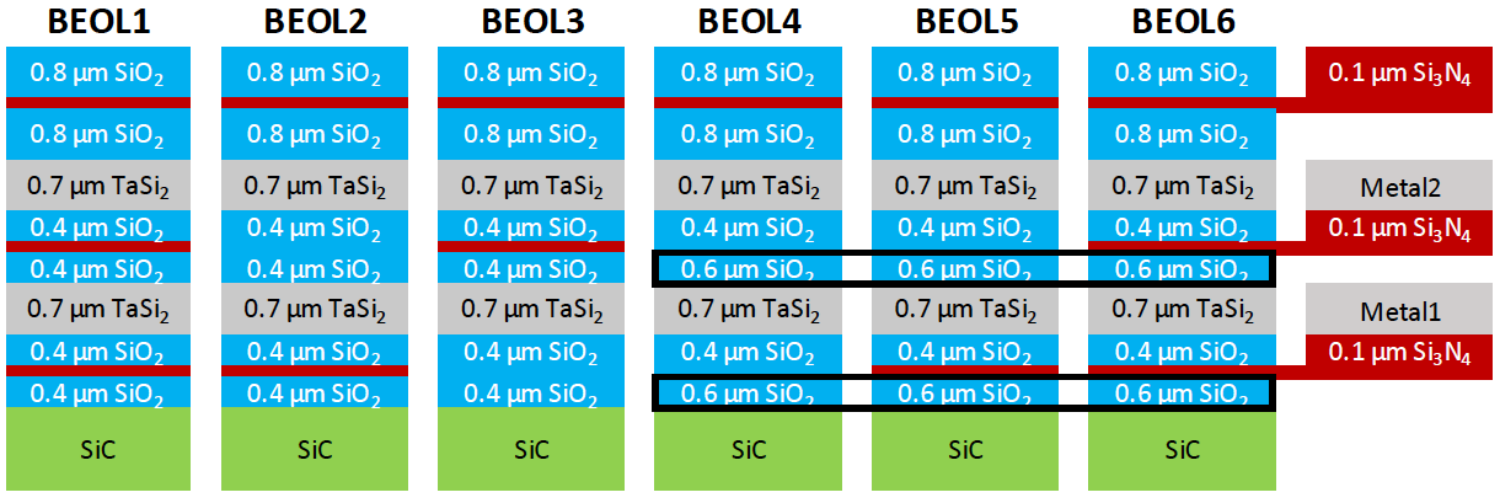
[2]P. G. Neudeck, et al., Proc. IMAPS High Temperature Electronics Conf., 2018, pp. 71-78. https://ntrs.nasa.gov/citations/20180003391

Back End Of Line (BEOL) Interconnect Process Experiments

Source: https://ntrs.nasa.gov/citations/20230002648

Experimental "test flights" of six different BEOL interconnect stack structures on SiC wafers

- Full interconnect trial fabrication run (from dummy SiC wafers through 500 °C oven-testing)
- Realistic SiC epilayers, mesas, ion implants, bond pads, and mask layouts found on IC Gen. 12
- Ascertain interconnect process of lowest dielectric crack density and highest electrical yield
- Deliver SiC resistor test chips of identical bond pad layout as IC Gen. 12 for verification of packaging, multi-chip boards, and high temperature testing (by NASA and external partners)



Back End Of Line (BEOL) Interconnect Process Experiments

Experimental Results: BEOL6 is best process

- Fewest observed cracks, all confined to wafer edge
- Highest electrical probe-test yield

Quarter-wafer region maps showing optically counted number of cracks observed on each 5 mm x 5 mm die

BEOL1

0	1	1	0				
1	0	0	0	1			
0	2	0	0	2	4		
0	0	0	0	0	0	0	
0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

BEOL2

0	0	0	0				
2	2	0	0	0			
2	1	0	0	0	0		
0	0	2	1	0	0	0	
0	1	2	1	1	0	0	0
0	0	0	0	2	0	0	0
10	5	2	3	1	0	3	0
0	7	4	3	2	0	5	0

BEOL3

2	0	0	0				
0	0	0	0	0			
1	1	1	0	0	0		
1	1	1	1	1	0	0	
1	1	1	1	1	0	0	0
0	0	0	1	0	1	0	0
0	1	0	0	1	0	0	0
0	0	0	0	0	0	0	0

BEOL4

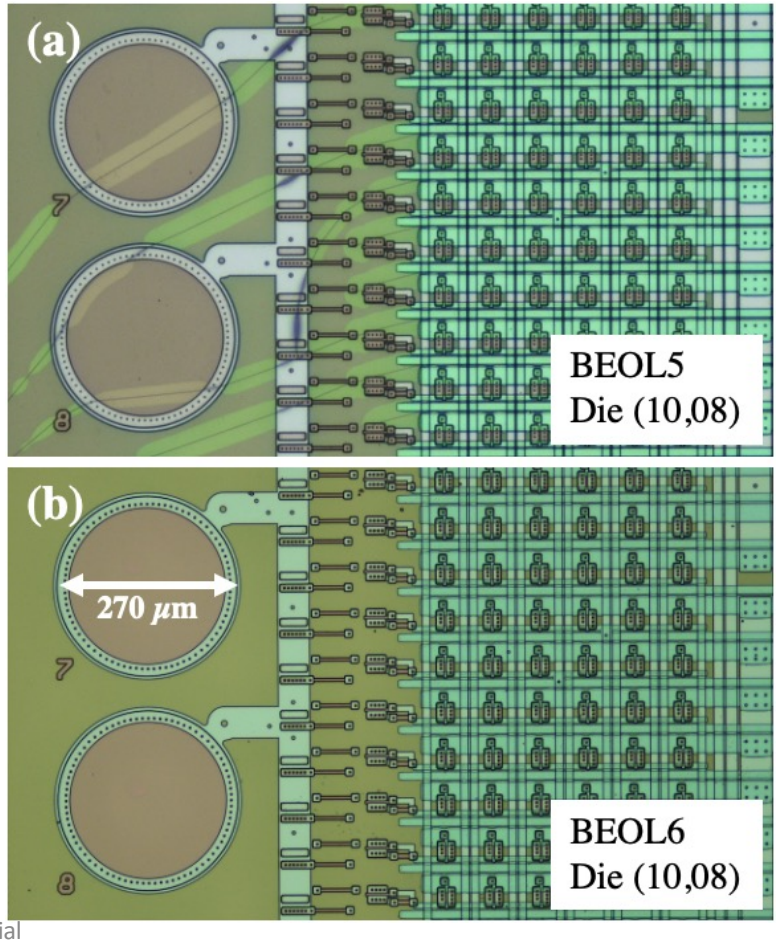
0	1	1	0				
0	0	0	0	0			
0	0	0	0	0	0		
0	0	0	2	0	0	0	
4	2	3	6	2	0	0	0
5	3	9	3	0	0	0	2
0	2	0	1	1	3	0	0
1	0	0	2	0	0	0	0

BEOL5

1	0	0	0				
1	0	0	0	0			
0	0	1	0	2	2		
0	0	0	0	0	2	0	
5	5	1	0	4	0	0	0
0	0	0	0	0	0	1	0
0	0	0	0	1	0	2	1
2	0	0	4	1	1	0	1

BEOL6

0	0	0	0				
0	0	0	0	0			
0	0	0	0	0	0		
0	0	0	0	0	1	1	
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0



Dicing, packaging & oven testing remains to be conducted

Source: https://ntrs.nasa.gov/citations/20230002648

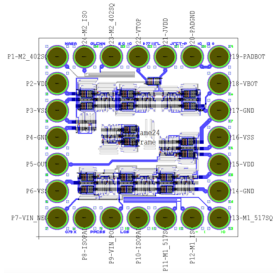
IC Gen. 12 Chipset Overview

50 Application Specific Integrate Circuit (ASIC) chip designs are being fabricated in IC Gen. 12

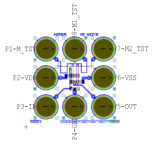
Including:

- Microprocessor dual-chip (assembly language)
- 8-bit analog to digital (serial output), digital to analog
- 2-kbit mask-programmed ROM, 248-bit RAM
- Venus lander control and analog-to-digital conversion
    - 4-channel 6-bit “Tech Demo”
    - 16-channel 8-bit “Exploration Mission”
    - Microseconds to hours clock/timer
- Venus imager array signal processing
- 12 customized analog sensor amps (op-amp based)
    - Wind, pressure, temperature, gas, & battery
- Power JFET chips for paralleling in power module
- External customer Space Act Agreement chips
    - Makel Engineering (NASA/MEI designed chip)
    - Ozark IC (Ozark IC designed chip)
    - Draper Labs (Draper designed half-chip)
- Miscellaneous logic (gates, flip flops, multiplexors, tri-states), analog (op-amp), and process test chips

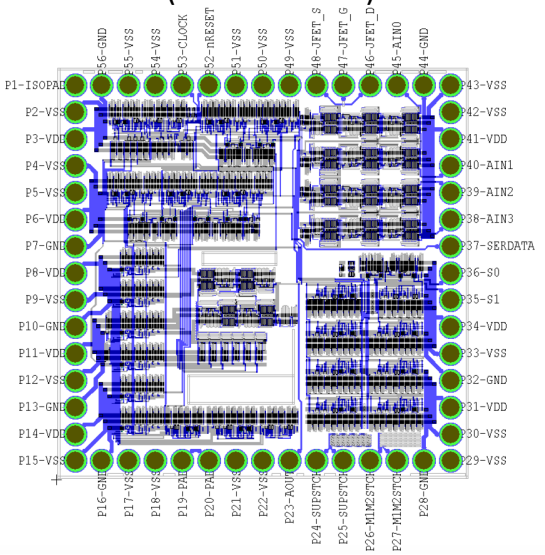
Pressure Sensor ASIC
(2.5 mm x 2.5 mm)



NOT Gate Chip
(1.3 mm x 1.3 mm)



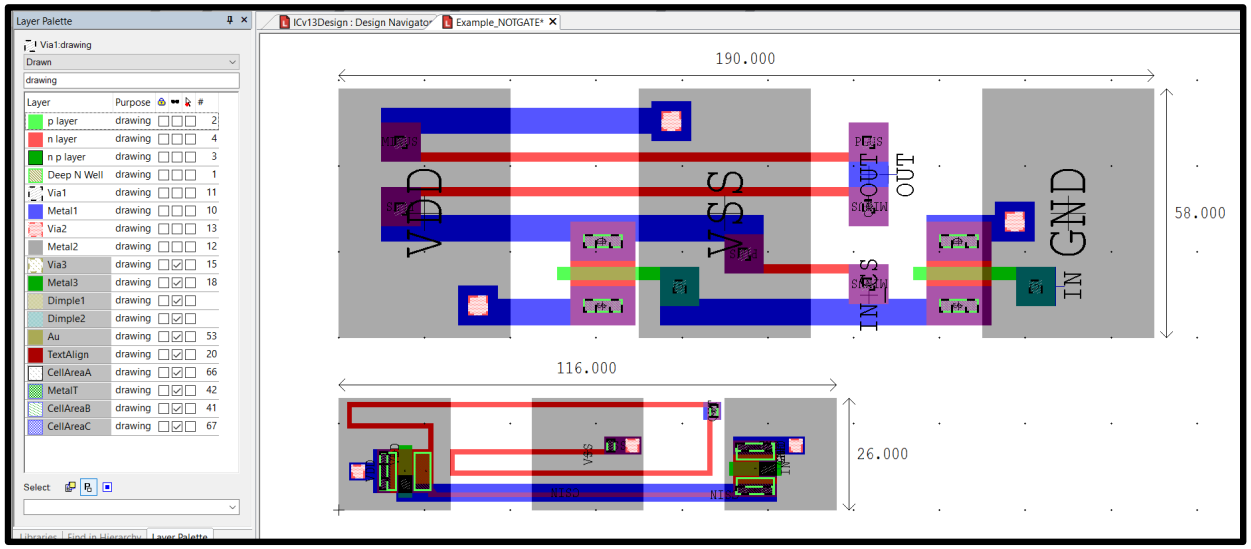
Venus Lander Control ASIC
(5 mm x 5 mm)



Source: https://ntrs.nasa.gov/citations/20230002648

Online SiC JFET IC Design Guide

https://go.nasa.gov/jfetic



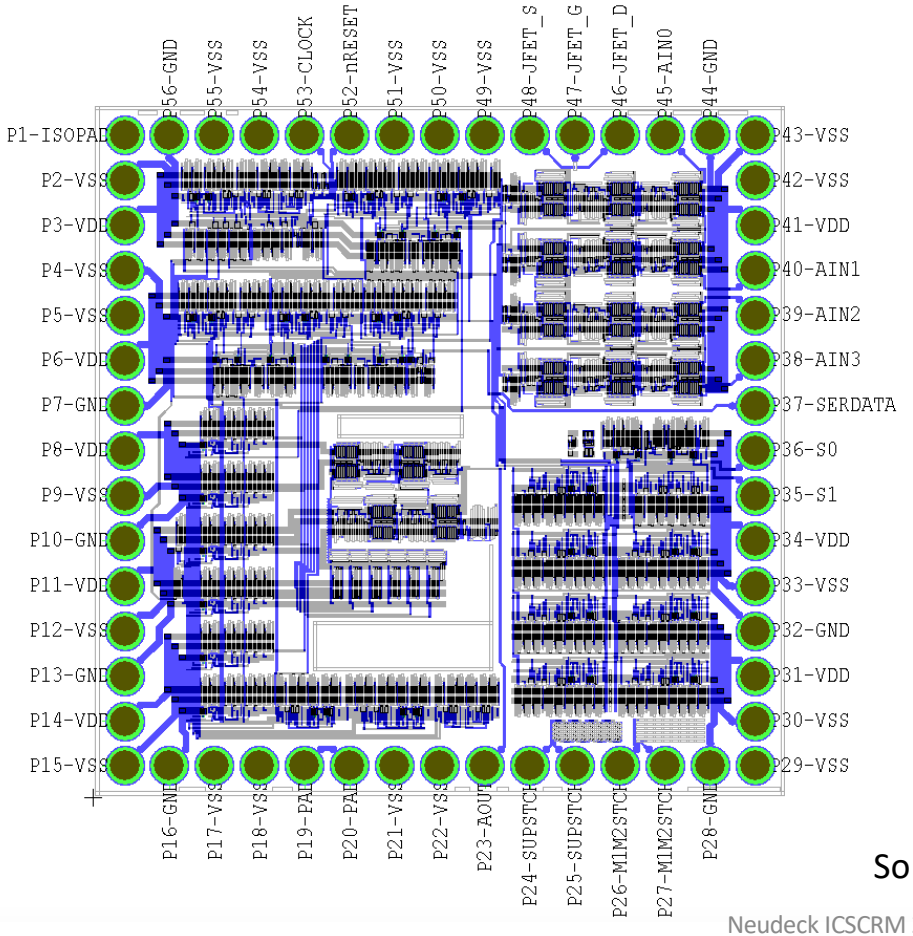
Gen. 12
NOT Gate Area
11021 µm^2

Gen. 13
NOT Gate Area
3016 µm^2

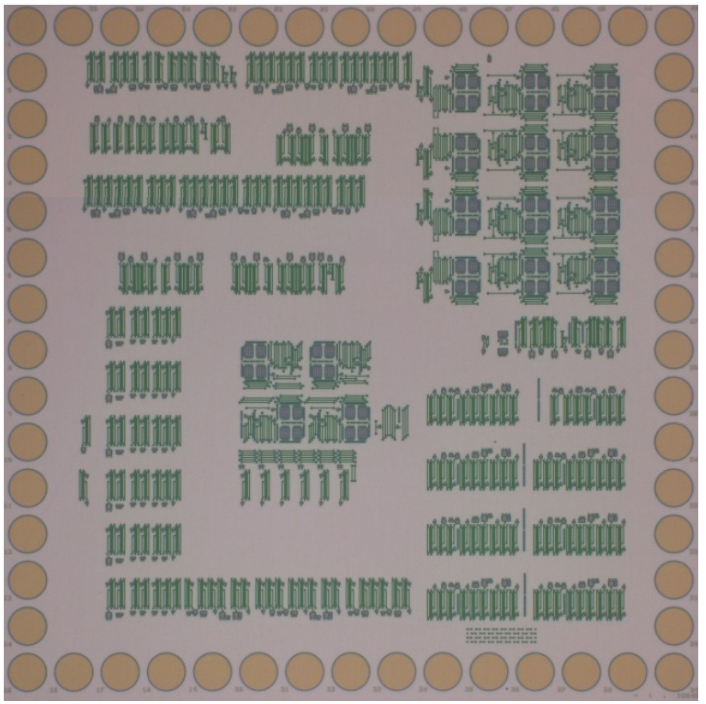
- SPICE models for circuit design and mask layout rules (Gen. 12 and Gen. 13)
- External partner IC designs are in Gen. 12 fabrication run (Space Act Agreements)
- Commercial SiC JFET-R IC design services available (https://www.ozarkic.com)

IC Gen 12 LLISSE-TD Chip

Low-power simple state-machine control chip for Venus lander technology demonstration mission



Chip after transistor processing, ready for interconnect processing

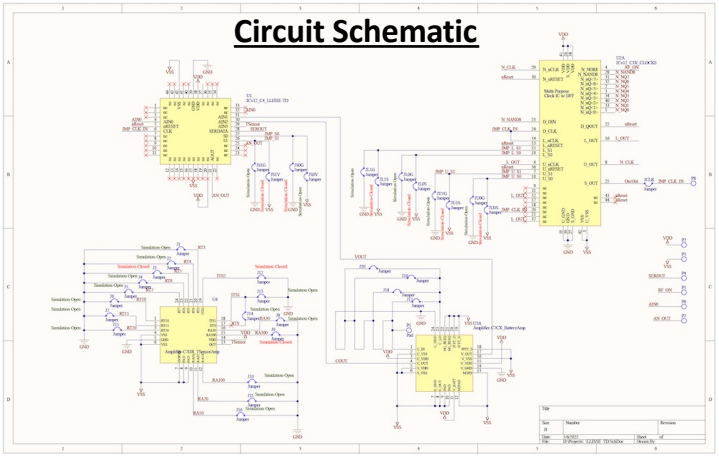


Source: https://ntrs.nasa.gov/citations/20230002648

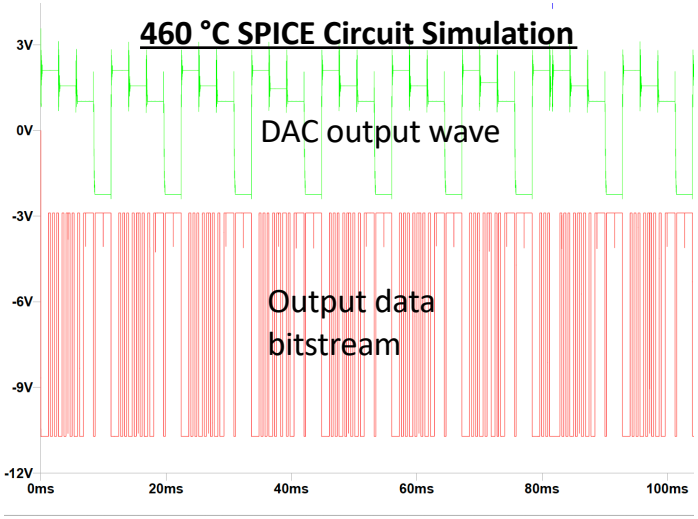
LLISSE Tech Demo Control Demonstration Board

Accomplishes timing, control, and digitization for Venus lander technology demonstration mission

Circuit Schematic

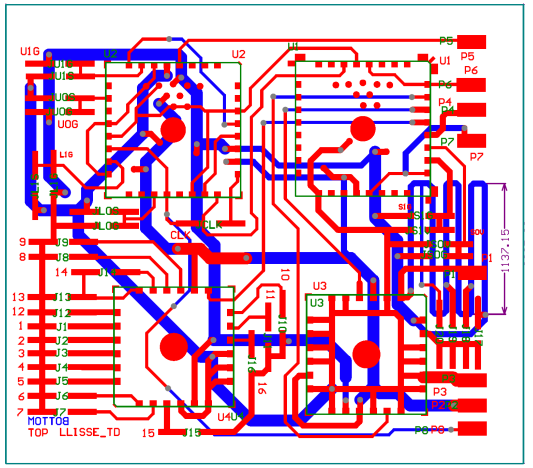


460 °C SPICE Circuit Simulation



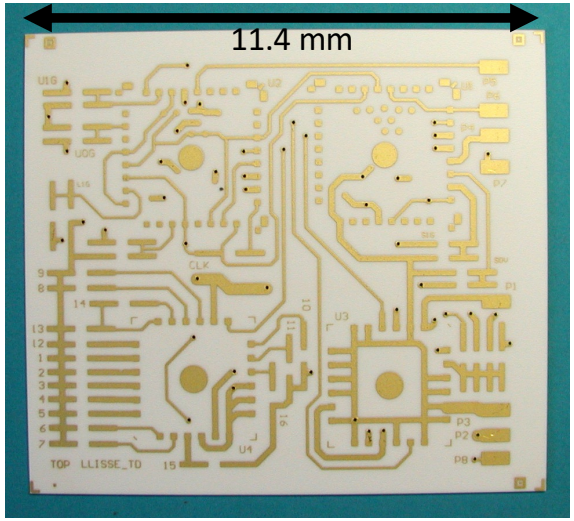
Circuit Board Layout

2-sided with through vias
4 chips
11.4 cm x 10.1 cm



Circuit Board

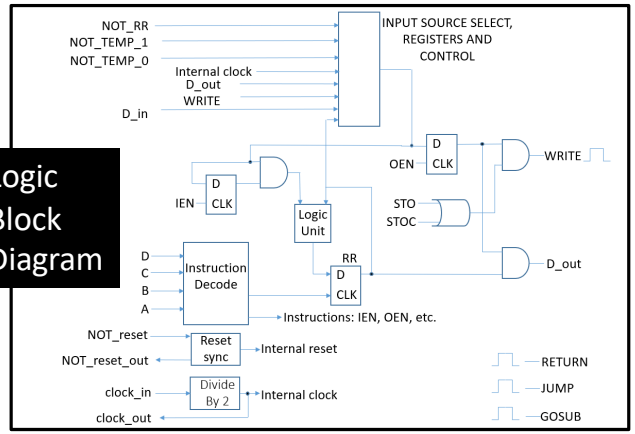
Manufactured by Thick Film Technology, Inc., to be populated with packaged IC Gen. 12 chips



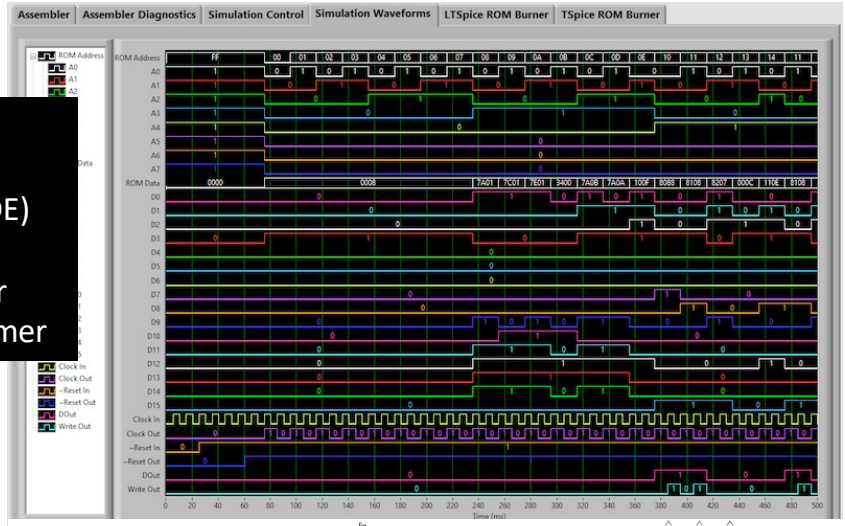
NASA Glenn SiC IC Gen. 12 SiC Microprocessor

Extreme Environment Programmed Operations

Logic Block Diagram



Integrated Development Environment (IDE)
- Assembler
- Logic Simulator
- ROM Programmer

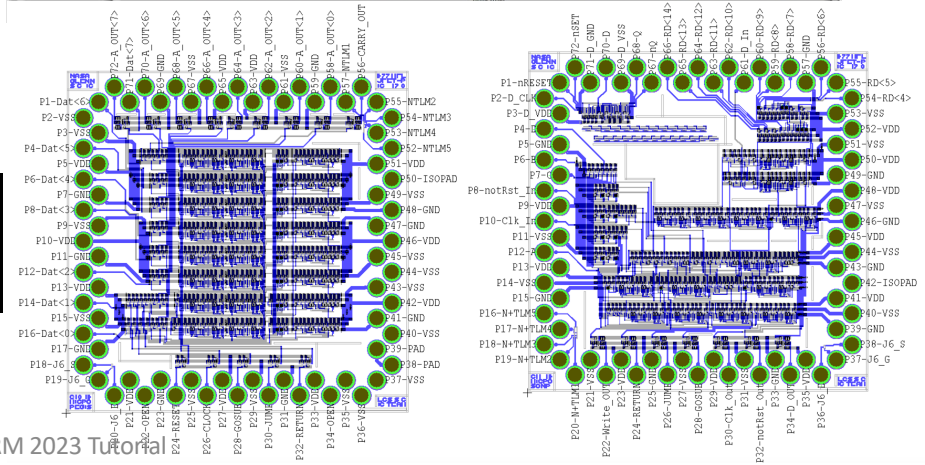


Transport Triggered Architecture

Instruction Set

OP CODE (DCBA)	OPERAND	OPERATION
0000	XOR	If **RR** ≠ **D_in**, then, **RR** → 1
0001	XNOR	If **RR** = **D_in**, then, **RR** → 1
0010	AND	**RR** · **D_in** → **RR**
0011	NAND	$\overline{RR \cdot D\_in}$ → **RR**
0100	OR	**RR** + **D_in** → **RR**
0101	NOR	$\overline{RR + D\_in}$ → **RR**
0110	LD	**D_in** → **RR**
0111	LDC	$\overline{D\_in}$ → **RR**
1000	STO	**RR** → **D_out**, **WRITE** → Π
1001	STOC	$\overline{RR}$ → **D_out**, **WRITE** → Π
1010	IEN	**D_in** → **IEN**
1011	OEN	**D_in** → **OEN**
1100	SKZ	Skip next instruction IF **RR** = 0
1101	RTN	**RETURN** Flag → Π, skip next instruction
1110	JMP	**JUMP** Flag → Π
1111	GOSUB	**GOSUB** Flag → Π

2-Chip Layout Design



1.3 W @ 460 °C
(SPICE Simulation)

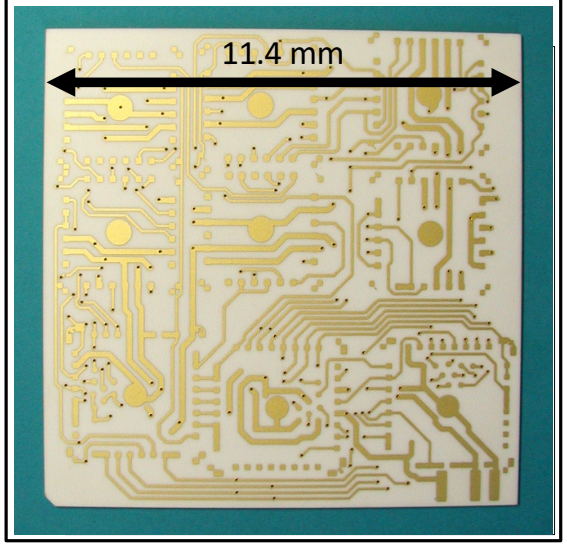
Microprocessor-Based Motor Control Demo Board

2-stepper-motor robot can follow line on floor using left, right, and front optical sensors

IC Gen 12 chip list & 2-sided circuit board

Bill Of Materials

Line #	Designator	Comment	Quantity
1	48EdgeConnector	z48pinEdgeConnector_Simulation	1
2	U1	ICv12_C11_MicroSeq	1
3	U2	ICv12_C10_MicroReg	1
4	U3, U6	ICv12_C13AY_Quad 2-1 Mux	2
5	U4	ICv12_C13C_1:8 Mux	1
6	U5, U8	ICv12_C13BY D Flip Flop Bank	2
7	U7, U10	8:1 Mux with NAND	2
8	U9	ICv12_C1X_ROM_LINE_FOLLOWER	1



Portion of assembly program compiled & built into IC Gen. 12 ROM chip

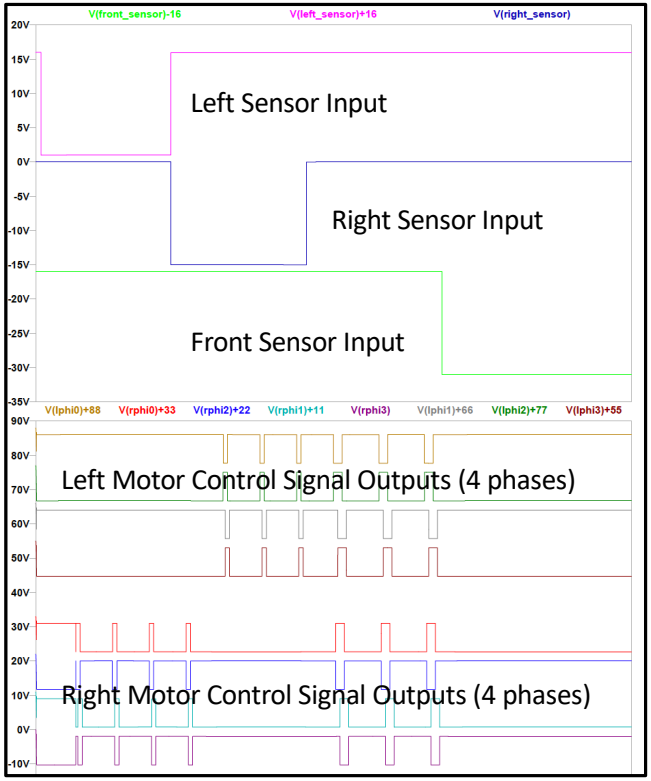
```
; Valentino Braitenberg vehicle program
; Robot follows a black tape on a shiny floor, or vice versa.

%ORG $00 ;address of first line of code is $00
%LEFT EQU $00 ;source address of LEFT eye
%RIGHT EQU $01 ;source address of RIGHT eye
%FRONT EQU $02 ;source address of FRONT eye
%RIGHTMOTOR EQU $01 ;address of LEFTMOTOR stepper
%LEFTMOTOR EQU $02 ;address of RIGHTMOTOR stepper

;main program
;
Start: nxor RR,RR ;make a 1
ien RR ;also use it to enable inputs
oen RR ;use it to enable outputs
top: ldc_e RR,(FRONT) ;Read /FRONT eye
skz ;If result is 1 (no obstacle) then skip loopback
and continue
jmp top ;loopback

FORWARD: stoc_e (LEFTMOTOR),RR ;RR contains a 1
sto_e (RIGHTMOTOR),RR
stoc_e (LEFTMOTOR),RR
sto_e (RIGHTMOTOR),RR
stoc_e (LEFTMOTOR),RR
sto_e (RIGHTMOTOR),RR
stoc_e (LEFTMOTOR),RR
sto_e (RIGHTMOTOR),RR
jmp top
```

SPICE circuit simulation of stepper motors controlled by sensor inputs



SiC high temperature power modules needed to switch each stepper motor phase on/off

Notable 500 °C Durable Electronics Technology Gaps

SiC JFET-R is confined to relatively low operating frequency (few MHz at most)
- Other technologies (e.g., SiC BJT) needed for ≥ 100 MHz (e.g., RF transmitter)

SiC JFET-R is “normally on” device poorly suited for power switching & management
- Other technologies (e.g., SiC BJT) needed for “normally off” high power switching
- High-voltage (kV) high-current (10-100A) 500 °C durable chip packaging not demonstrated

SiC JFET-R logic requires more than 10-fold higher power than complementary (CMOS) logic

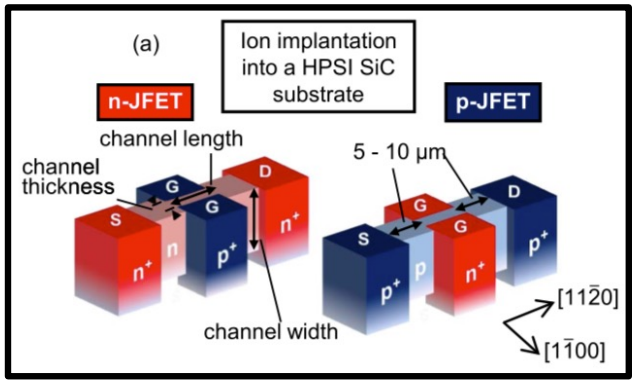
500 °C durable memory is primitive compared to modern room-temperature memories
- Less than 1 kbit/chip, mW/bit RAM storage power, mask-programmed ROM
- Electronically burnable 500 °C durable non-volatile memory/FPGA yet to be demonstrated

500 °C durable “quartz crystal” like timing reference clock has yet to be demonstrated
- SiC JFET-R ring oscillators are non-precise, though stable to within 10%

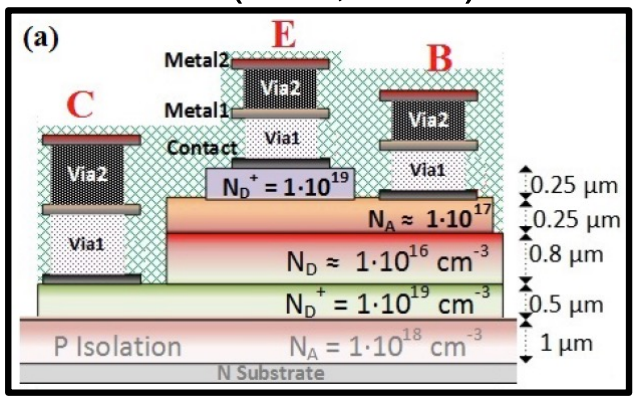
Alternative Device Approaches

- **Worthwhile benefits IF/WHEN prolonged and stable 500 °C operation achieved**
- Challenging integration with durable interconnect & packaging?

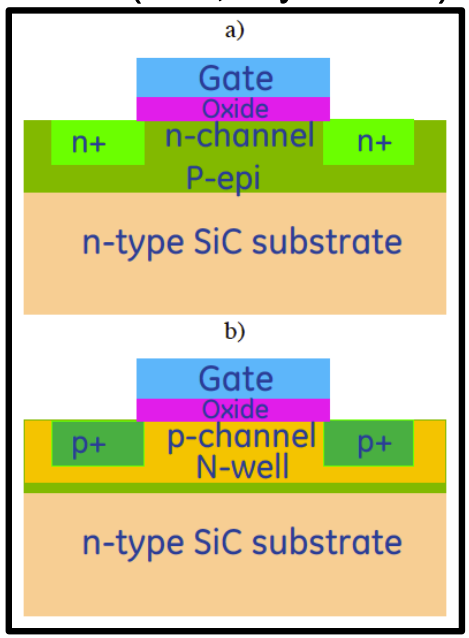
Implanted JFET (Kyoto U.[1], United SiC)



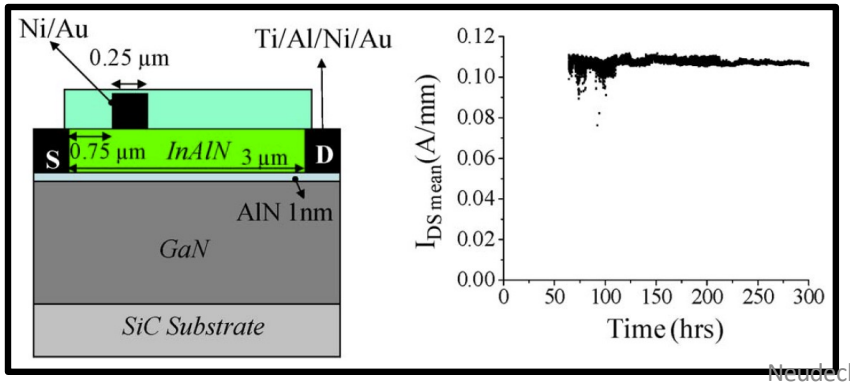
BJT (KTH[3], Purdue)



CMOS (GE[2], Raytheon UK)



III-N FETs[4], Ga_2O_3, Other Wide Bandgaps



[1] Nakajima et al, IEEE Electron Dev. Lett., **40**, 866 (2019).
[2] Chen et al., 2014 IMAPS Int. Conf. High Temp. Electronics, p. 72.
[3] Shakir et al., Electronics. 8, 496 (2019).
[4] Maier et al., IEEE Trans. Device and Mat. Rel., **4**, 427 (2010).

IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. IE-29, NO. 2, MAY 1982

High-Temperature Electronic Requirements in Aeropropulsion Systems

WILLIAM C. NIEBERDING AND J. ANTHONY POWELL, MEMBER, IEEE

Abstract—**This paper discusses the needs for high-temperature electronic and electrooptic devices as they would be used on aircraft engines in either research and development applications, or operational applications. The conclusion reached is that the temperature at which the devices must be able to function is in the neighborhood of 500° to 600°C either for R&D or for operational applications. In R&D applications, the devices must function in this temperature range when in the engine but only for a moderate period of time. On an operational engine, the reliability requirements dictate that the devices be able to be burned-in at temperatures significantly higher than those at which they will function on the engine. The major point made is that semiconductor technology must be pushed well beyond the level at which silicon will be able to function.**

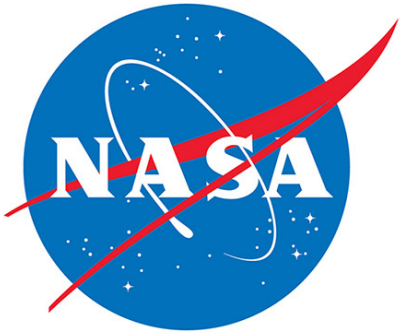
I. INTRODUCTION

THE PURPOSE of this paper is to describe the needs for high-temperature electronics in the aircraft engine field.

During this process many prototypes are
development purposes. These prototypes,
engine components, are operated repeat
facilities. For each of these test runs the e
is instrumented with the maximum numbe
so that as much of the desired informati
tained from each facility run. Even after
for flight, problems arise in its operation
of improving its operational characteristi
so that this testing process continues well
of an engine model. An example of this
gram conducted by NASA to modify engi
DC9 and the Boeing 727 to reduce the
model engine had been in service for many
sures generated by environmental concer
to go back and redesign parts of it for rad

CONCLUSION: "We cannot help but feel that high-temperature electronics will indeed have wide application not only to the areas discussed at this conference but also to far more important areas which we just do not have the vision to predict."

Sources: https://doi.org/10.1109/TIE.1982.356644 & https://www1.grc.nasa.gov/glenn-history/hall-of-fame/biographies/j-anthony-powell/



NASA Glenn SiC Team Website: https://go.nasa.gov/sic
NASA Glenn SiC JFET IC Technology Guide: https://go.nasa.gov/jfetic
NASA Glenn Microsystems Fabrication Lab: https://www1.grc.nasa.gov/facilities/microfab/