Single-Event Effects Response of 96- and 176-Layer 3D NAND Flash Memories

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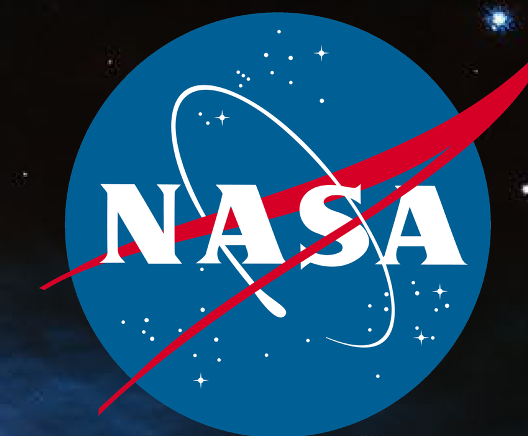


National Aeronautics and Space Administration

Devices Tested

Three state-of-the-art NAND flash devices have been characterized for single-event effects (SEE) response. These devices are all based upon different 512 Gb triple-level cell (TLC) dice. Two are manufactured by Micron on their 96- and 176-layer processes, and the third is manufactured by SK Hynix on a 176-layer process. The two Micron devices are 16-die stacks totaling 8 Tb of memory.

TABLE I. RELEVANT SPECIFICATIONS OF FLASH DEVICES TESTED

Part Number	MT29F8T08EWLGEM5	MT29F8T08EWLKEM5	H25G9TC18CX488
Manufacturer	Micron	Micron	SK Hynix
3D NAND Technology	96 Layers, SLC/TLC Floating Gate (B27C)	176 Layers, SLC/TLC Replacement Gate (B47T)	176 Layers, SLC/TLC Charge Trap (V7)
Advertised Die Capacity	512 Gb TLC	512 Gb TLC	512 Gb TLC
Total Capacity	8 Tb TLC (16 die)	8 Tb TLC (16 die)	512 Gb TLC (1 die)
LDC	IYG22	2PK22	212T
Tested Voltage	V_{CC}: 2.5 V – 3.3 V V_{CCQ}: 1.25 V	V_{CC}: 2.5 V – 3.3 V V_{CCQ}: 1.25 V	V_{CC}: 3.3 V V_{CCQ}: 1.25 V
Package	132 LBGA	132 LBGA	152 BGA

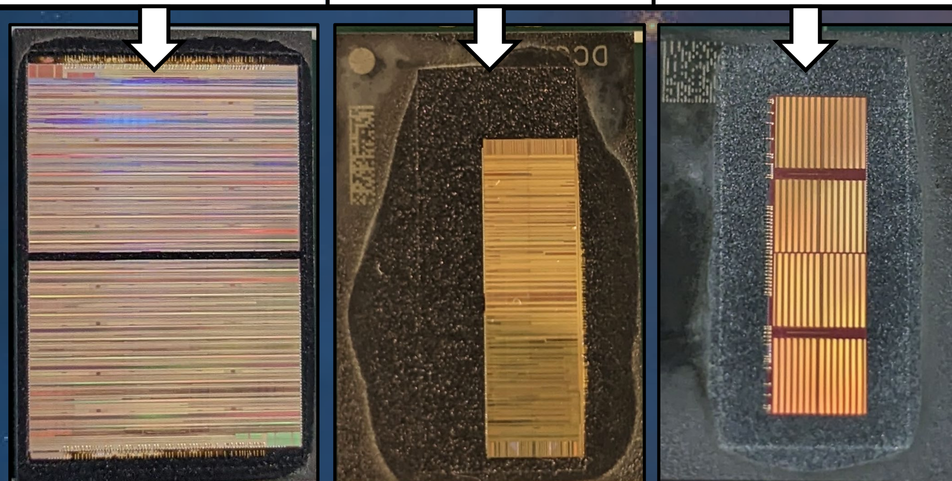


Fig. 1. Die photographs of all three devices as-tested

Test Configurations

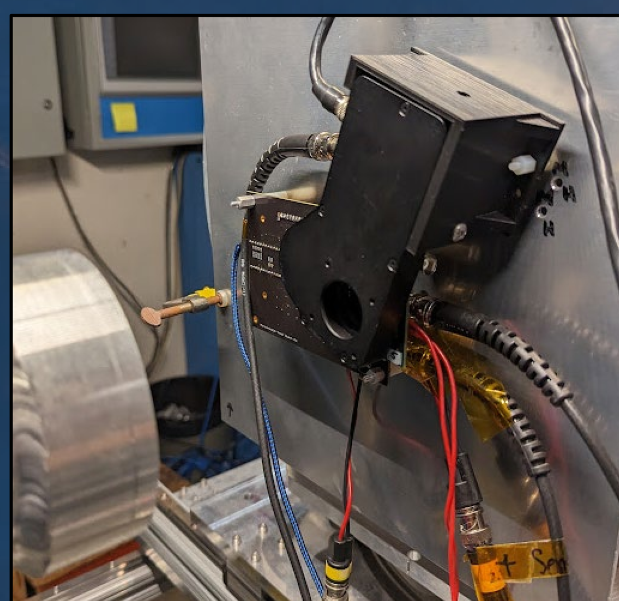


Fig. 2. Flash devices under heavy-ion irradiation with external shutter in place (top) and removed (bottom)

Hardware - Parts were tested with an ARM-Cortex M7 microcontroller running at 600 MHz and customized NAND flash control software. Testing was completed at the Lawrence Berkeley National Laboratory and the Massachusetts General Hospital.

SEU Characterizations – Performed by irradiating the flash in a powered-off condition, at room temperature, and measured at nominal operating voltages. Multiple data patterns were explored, with a pseudorandom pattern typical.

SEFI Characterizations – Performed by irradiating while actively erasing, programming, and reading the memory *or* while repeatedly querying the device for correct device identification code.

SEL Detection – Devices were operated at maximum nominal voltage at 85°C. A surface LET of 79 MeV·cm²/mg was used and the device in some cases was actively erased/programmed to exercise internal circuitry and enable all internal voltages.

Heavy Ion SEU Results

Typical SEU test results are presented as a single cross-section vs LET curve (as in Fig. 4, left, for the 96-layer Micron devices).

Some devices offer a user-mode programmable read offset level to adjust the voltage threshold used to discriminate between erased ('1') and programmed ('0') states within individual transistors (see Fig. 5 for effects on SEU response).

Because NAND flash single-event upsets result in programmed ('0') cells turning into erased ('1') cells, it follows that adjusting the read offset setting towards the erased state might increase the resistance to SEU, especially at lower LET where deposited charge is insufficient to fully shift a cell from 0 to 1. See Fig. 3 for an illustration of this effect. Other tradeoffs (e.g., long-term data retention) are possible.

As in past generations[2], operation in triple-level cell (TLC) mode[1] provides significantly less margin between logical states, resulting in more susceptibility to all forms of data corruption[3], including SEU. NASA NAND flash testing primarily addresses SLC response.

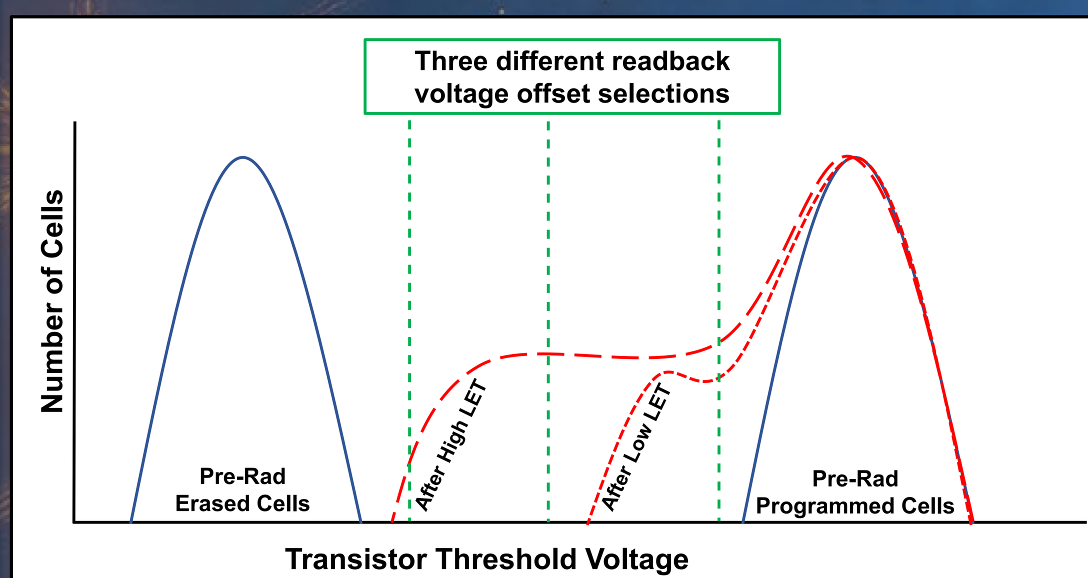
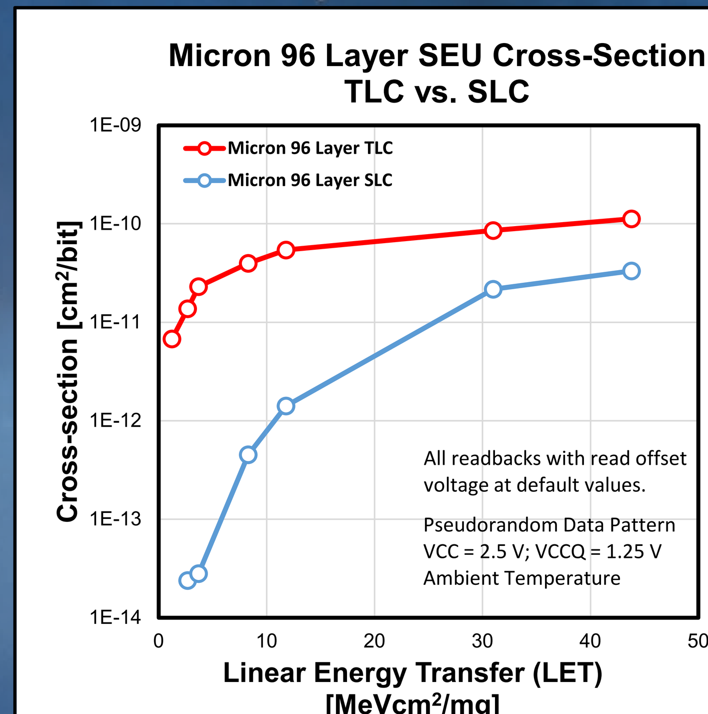


Fig. 3. Generic illustration of effect of changing read offset voltage on pre-rad and post-rad cells for two arbitrary LET values.



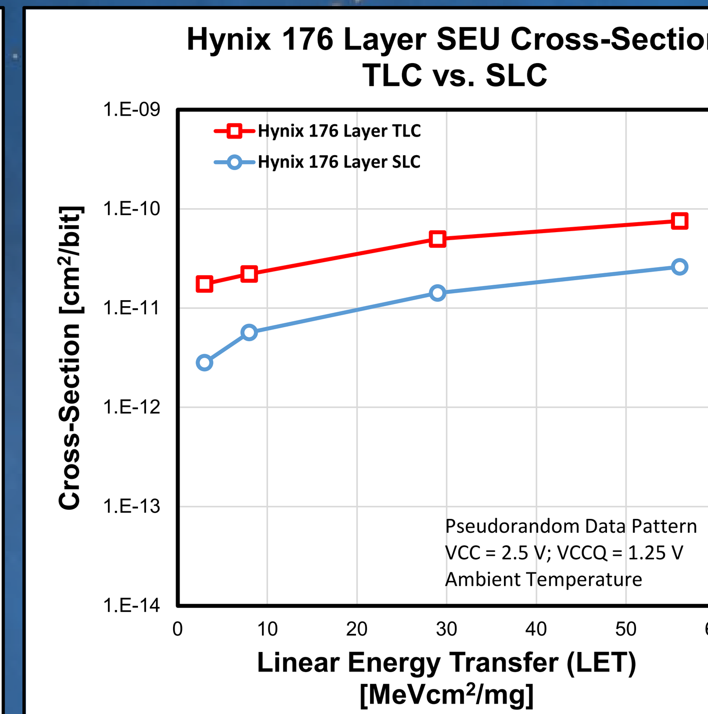
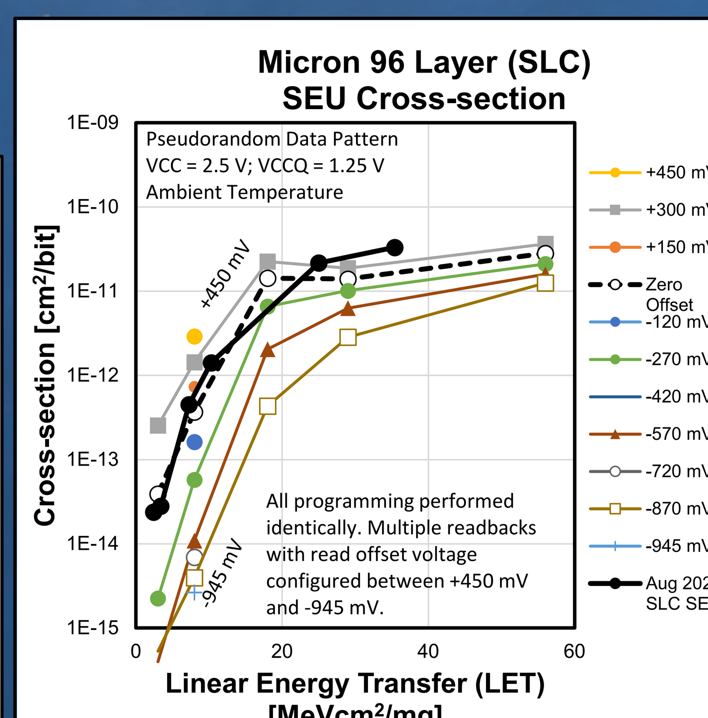


Fig. 4. SEU test data for all three devices tested, with TLC and SLC comparison



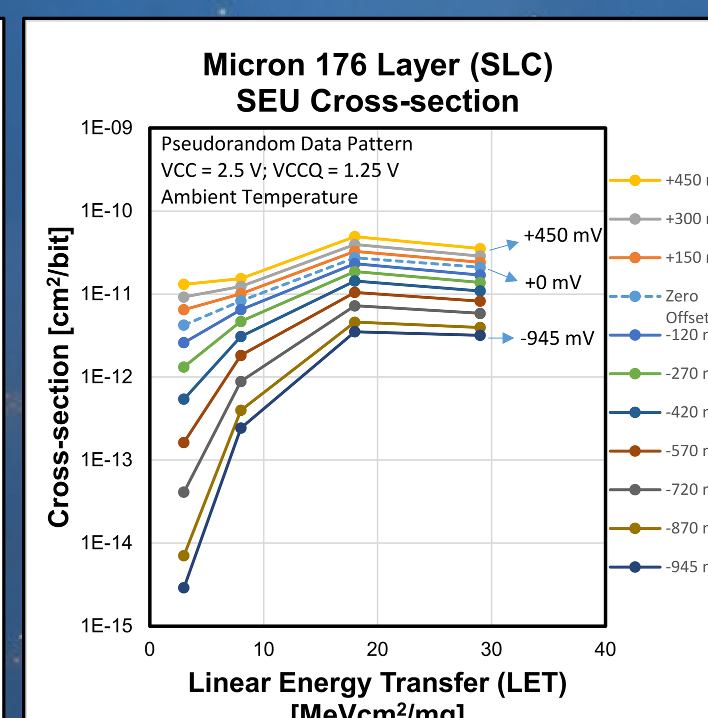


Fig. 5. SEU test data exploring the effects of read offset voltage changes.

Heavy Ion SEL Results

Testing with 16 MeV/amu Xe (incident LET 56.0 MeV·cm²/mg) revealed no SEL in any of the devices tested when irradiated at 85°C to a fluence of 1x10⁷/cm² at V_{CC} of 3.3 V.

When irradiated at 45° angle (effective LET of 79.2 MeV·cm²/mg at die surface) no SEL was observed in the two Micron devices. The Hynix 176-layer device had an anomalous high-current condition that reached power supply compliance and required a power cycle. This may be single-event latchup. Functionality was successfully recovered on-site, but further evaluation for latent damage has not been performed.

The control circuitry for these devices is implemented under the flash memory stack (on the order of 10-20 um below die surface). Beams used for this experiment had sufficient range to reach these circuits before the Bragg peak. Precise estimation of tested LET requires construction analyses.

Acknowledgements and Further References

Authors acknowledge the support of Mike Wojtczak, Jeff Cassidy, and MEMKOR; the NASA GSFC Radiation Effects and Analysis Group (REAG); the Lawrence Berkeley National Laboratory; and Ethan Cascio of the Massachusetts General Hospital. Testing was funded by the NASA Electronic Parts and Packaging (NEPP) program. Background image courtesy NASA/JWST.

[1] M. Bagatin et al., "Single Event Effects in 3-D NAND Flash Memory Cells With Replacement Gate Technology," in IEEE Transactions on Nuclear Science, vol. 70, no. 4, pp. 308-313, April 2023

[2] E. P. Wilcox et al., "A TID and SEE Characterization of Multi-Terabit COTS 3D NAND Flash," 2019 IEEE REDW, San Antonio, TX, USA, 2019

[3] F. Irom et al., "Evaluation of Mechanisms in TID Degradation and SEE Susceptibility of Single- and Multi-Level High Density NAND Flash Memories," in IEEE Transactions on Nuclear Science, vol. 58, no. 5, pp. 2477-2482, Oct. 2011

DUT: Device Under Test
LET: Linear Energy Transfer
SEFI: Single-Event Functional Interrupt
SEL: Single-Event Latchup
SEU: Single-Event Upset
SLC: Single-Level Cell
TLC: Triple-Level Cell

Heavy Ion SEFI Results

SEFI testing evaluated the individual susceptibilities during specific modes of operation (Fig. 6 and Table II) by blocking the beam during other phases of an erase-program-read cycle. In the event of a block SEFI (failure to erase, program, or read one or more NAND blocks), both the time of detection and the time of occurrence can be relatively well identified and correlated to specific device activities.

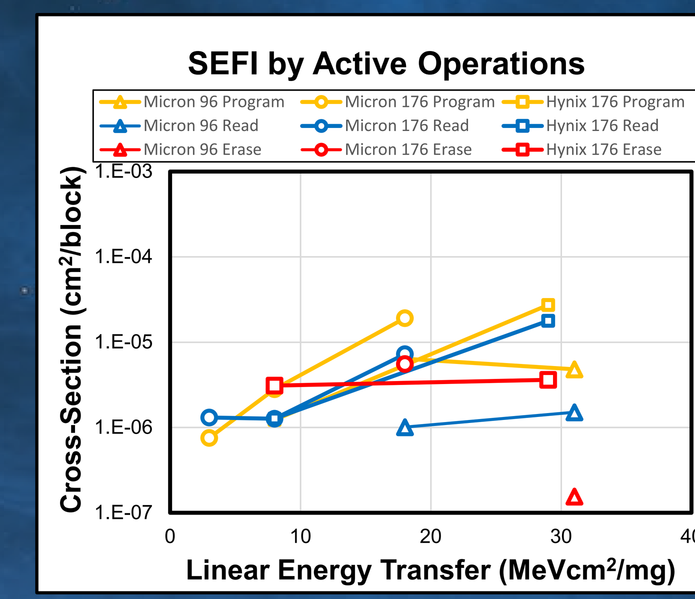


Fig. 6. SEFI susceptibilities by operational mode

TABLE II. ACTIVE ERASE/PROGRAM/READ SEFI TESTING OF HYNIX 176-LAYER FLASH. EACH TEST COVERED 100 BLOCKS AT A TIME, AUTOMATICALLY RECOVERING FROM EACH WITH A POWER CYCLE.

LET	Fluence	Operational State While Irradiating	Count of block SEFI detected as a failure to:		
MeVcm²/mg	/cm²		ERASE	PROGRAM	READ
8.0	2.23 x 10⁵	ERASE	390	1	385
8.0	6.58 x 10⁵	PROGRAM	39	1	81
8.0	2.74 x 10⁵	READ	25	0	35
29.0	1.05 x 10⁵	ERASE	49	3	38
29.0	1.21 x 10⁵	PROGRAM	167	66	331
29.0	6.58 x 10⁵	READ	200	113	144

Recoverability from the most severe SEFI (complete lack of communication) was attempted automatically when a loss of functionality was observed (Tables III-V). Here a RESET and HARD RESET are specific NAND flash commands; a power cycle was remotely initiated by the test setup only when RESET or HARD RESET were insufficient to recover.

TABLE III. SEFI RECOVERY TESTING OF MICRON 96 LAYER FLASH

LET	Fluence	Count (and %) of READID SEFI resettable by		
MeVcm²/mg	/cm²	RESET	HARD RESET	Power Cycle
18.0	2.01 x 10⁶	10 (77%)	3 (23%)	0 (0%)
29.0	2.61 x 10⁶	10 (71%)	1 (7%)	3 (21%)
56.0	8.58 x 10⁶	89 (77%)	20 (17%)	6 (5)
79.2	1.05 x 10⁷	132 (70%)	40 (21%)	16 (9%)

TABLE IV. SEFI RECOVERY TESTING OF MICRON 176 LAYER FLASH

LET	Fluence	Count (and %) of READID SEFI resettable by		
MeVcm²/mg	/cm²	RESET	HARD RESET	Power Cycle
3.0	5.00 x 10⁶	3	0	0
8.0	2.01 x 10⁶	2	0	0
18.0	1.01 x 10⁶	2	0	0
29.0	1.00 x 10⁶	6	0	0

TABLE V. SEFI RECOVERY TESTING OF HYNIX 176 LAYER FLASH

LET	Fluence	Count of READID SEFI resettable by		
MeVcm²/mg	/cm²	RESET	HARD RESET	Power Cycle
8.0	1.15 x 10⁶	0	0	0
29.0	1.0 x 10⁶	0	1	0

Proton SEU and SEFI Results

All three devices were tested briefly at the Francis H. Burr Proton Therapy Center (MGH). Two beams of 125- and 200-MeV protons were available. SEU data vs. energy in SLC mode (Fig. 8), SEU for each die in the 16-die package (Fig. 9), and limited SEFI characterization data (Table VI) were measured.

For these tests, the DUT was separated from the test hardware by a 12" cable to reduce the likelihood of secondary effects on the microcontroller or support hardware.

TABLE VI. HIGH-ENERGY PROTON SEFI TEST RESULTS

Energy (MeV)	Device	Total Fluence (/cm²)	Observed SEFI	Cross-section (cm²)	Recovery
200	SKHynix 176	1x10¹¹	0	0	
200	Micron 96	4x10¹¹	2	5.0x10⁻¹²	Both recovered with RESET
	Micron 176	Not tested			

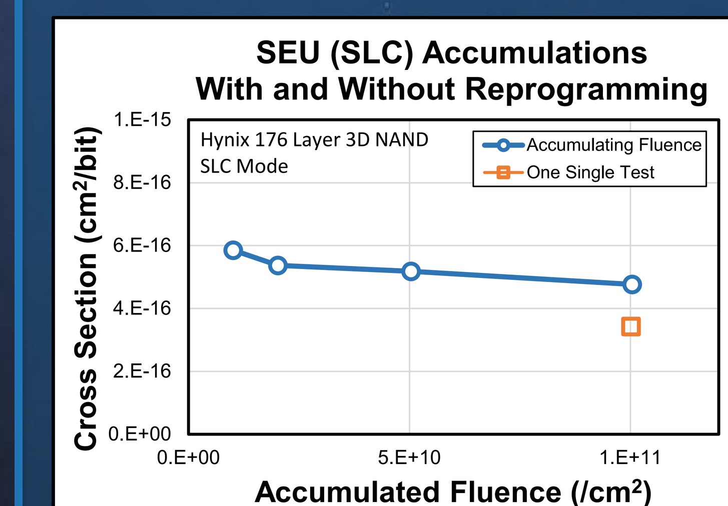


Fig. 7. Comparison of SEU count when irradiating directly to target vs. taking intermediate steps

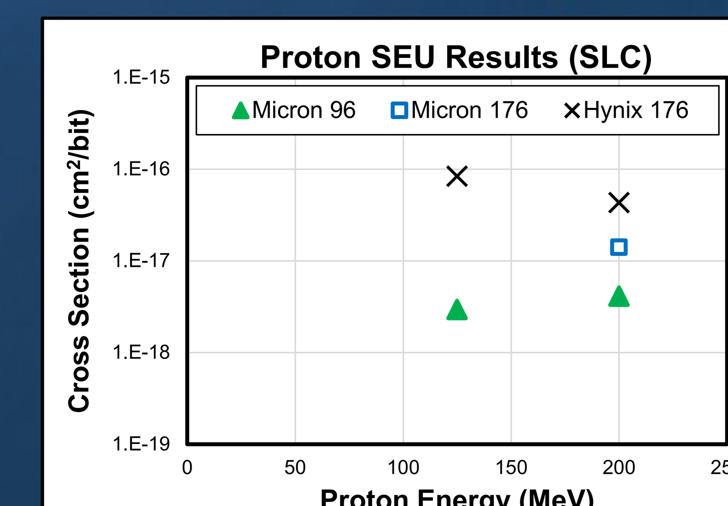


Fig. 8. Proton-induced SEU for all three devices at two energies tested

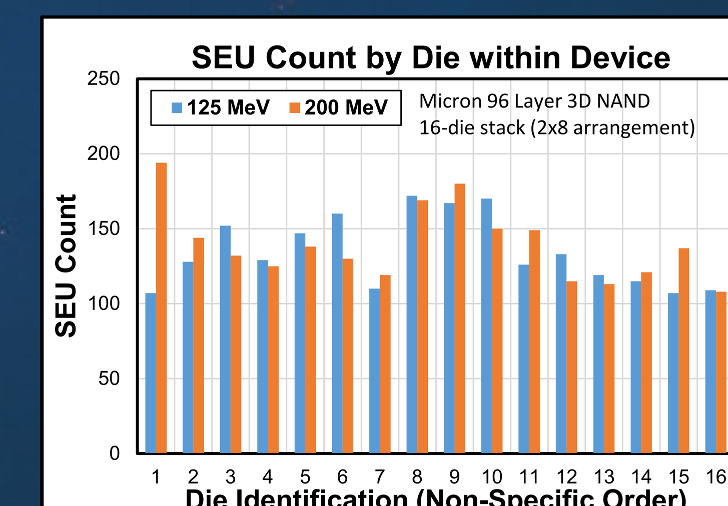


Fig. 9. Proton-induced SEU throughout a 16-die stack of 96-layer 3D NAND.