Single-Event Effects Response of 96- and 176-Layer 3D NAND Flash Memories

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***Abstract*—Single-event effects testing (heavy-ion and proton) is presented for 96- and 176-layer commercially-available 3D NAND flash memory, with emphasis on SEFI detection and recovery.**

***Index Terms*—Flash memory, proton, heavy ion, single-event upset, three-dimensional NAND, single-event functional interrupt**

I. Introduction

STATE-OF-THE-ART 3D NAND flash memories [1], [2] are characterized for single-event effects (SEE) response, including single-event upset (SEU), single-event latchup (SEL), and single-event functional interrupt (SEFI). With limited options for high-density radiation-hardened-by-design (RHBD) memories available, commercial parts are likely candidates for use in space, whether as-is or with significant aftermarket vendor screening and/or repackaging. These devices have well-known susceptibilities to multiple single-event effects phenomena [3]–[6]. In this work, the SEE responses of three off-the-shelf devices are characterized and compared with heavy-ion and proton [7] irradiation, along with some exploration of the necessary mitigation steps to recover from complex error modes.

II. Devices Under Test

The three commercial off-the-shelf (COTS) NAND flash devices tested are Micron 96- and 176-layer 3D NAND flash, and SK Hynix 176-layer 3D NAND flash, further described in Table I. Throughout this document they are generally referred to based on the manufacturer and number of layers for convenience, e.g., Micron 96-layer flash. All are nominally triple-level cell (TLC) memories with the capability to operate in a classical single-level cell (SLC) mode for improved performance and endurance. Each device was prepared for heavy-ion testing by laser-chemical decapsulation to expose a single die as shown in Fig. 1, Fig. 2, and Fig. 3. For proton testing, no decapsulation was performed.

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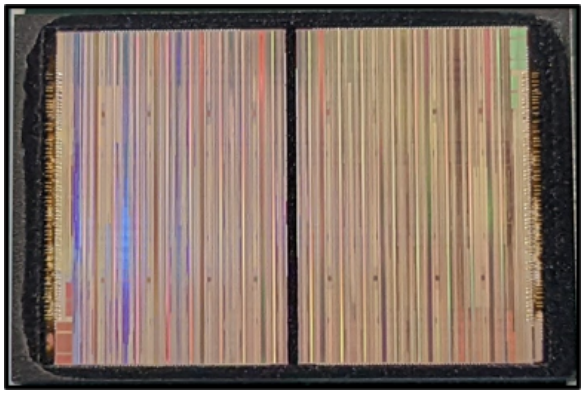

Fig. 1. Decapsulated Micron 96-layer flash memory

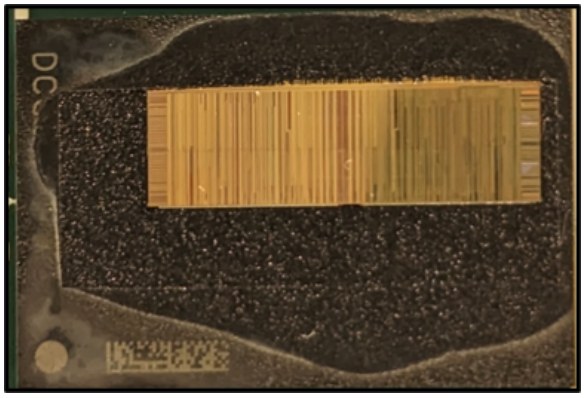

Fig. 2. Decapsulated Micron 176-layer flash memory

III. Testing Description

All three devices were tested under heavy-ion irradiation at the Lawrence Berkeley National Laboratory's (LBNL) 88" Cyclotron [8]; the Micron 96-layer device in August of 2022, and all three devices in November 2022. Testing was performed with the 16 MeV/amu cyclotron tune using ions with incident linear energy transfer (LET) of approximately 1.2 to 56 MeV·cm^2/mg. All testing was performed in air. Testing at elevated temperature, where indicated, used resistive heating elements adhered to the printed circuit board; temperature was monitored by use of integrated on-chip temperature sensors within the NAND devices.

High-energy proton testing was subsequently performed at the Massachusetts General Hospital's Francis H. Burr Proton Therapy Center [9] in December 2022. All three devices were characterized in varying degree to SEU and SEFI with 125- and 200-MeV protons. Some limited multi-die test results are

TABLE I
DEVICES UNDER TEST

Part Number	MT29F8T08EWLGEM5	MT29F8T08EWLKEM5	H25G9TC18CX488
Manufacturer	Micron	Micron	SK Hynix
3D NAND Technology	96 Layers, SLC/TLC Floating Gate (B27C)	176 Layers, SLC/TLC Replacement Gate (B47T)	176 Layers, SLC/TLC Charge Trap (V7)
Advertised Die Capacity	512 Gb TLC	512 Gb TLC	512 Gb TLC
Total Capacity	8 Tb TLC (16 die)	8 Tb TLC (16 die)	512 Gb TLC (1 die)
Lot Date Code	IYG22	2PK22	212T
Tested Voltage	VCC: 2.5 V - 3.3 V VCCQ: 1.25 V	VCC: 2.5 V - 3.3 V VCCQ: 1.25 V	VCC: 2.5 V - 3.3 V VCCQ: 1.25 V
Package	132 LBGA	132 LBGA	152 BGA

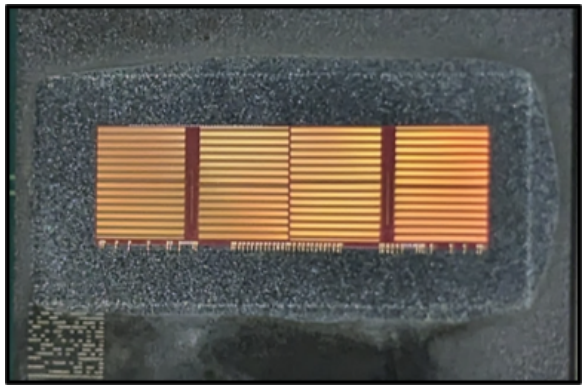

Fig. 3. Decapsulated SK Hynix 176-layer flash memory

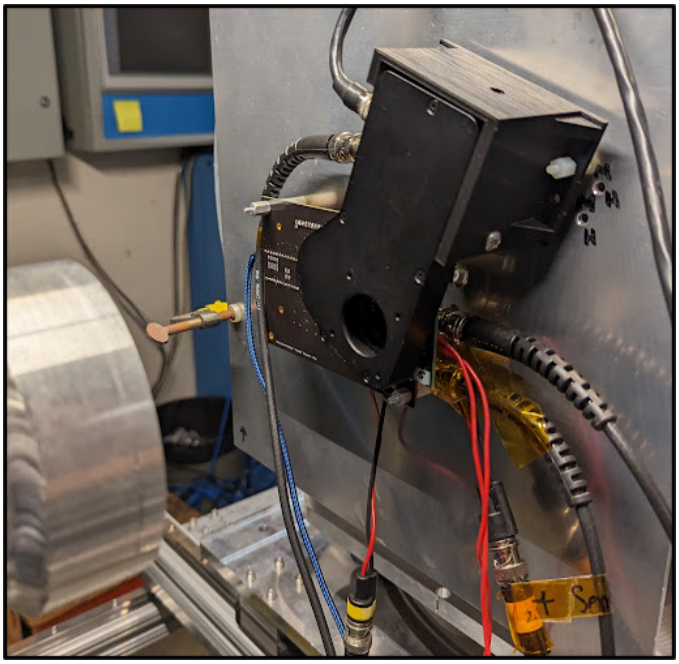

Fig. 4. External shutter inserted in between facility and DUT

presented for the high-energy proton testing, but in general, testing was still based on a single die at a time. The airgap was 81 cm and aperture size 3.5 cm at 200 MeV, and the airgap 51 cm and aperature size 2.5 cm at 125 MeV. A radiochromic film verified that the proton beam spot covered the flash memory device.

Practical considerations of available beam time and test infrastructure generally preclude the complete testing of multi-terabit high-density memories. Instead, a representative sample of the array is characterized and assumptions made regarding the response of the entire device. A more thorough test is certainly appropriate when a specific application is targeted. In this work, the results sections indicate the size of memory tested, and test configuration, for each condition. In the case of heavy-ion testing at LBNL, it is only possible to test the top-most device in the stack due to ion range constraints.

Heavy-ion SEFI testing included a fast (∼10ms) shutter mechanism in front of the device (Fig. 4) to ensure that beam was only applied during specific operations [11], and that it could be immediately blocked from the device when a SEFI was detected. The fully-autonomous SEFI test detects anomalous device operation (or lack of any device response) and attempts recovery by RESET command, HARD RESET command, and finally by power cycle. RESET and HARD RESET are standard NAND flash commands documented by the manufacturer and communicated by the normal parallel databus. A power cycle physically pulls all device pins (both power and data) to 0V. Larger sample sizes are possible without the need to manually reconfigure the test between each event, and a more precise fluence-to-failure estimation is achieved by eliminating any manual response time.

IV. HEAVY ION RESULTS

A. Single-Event Upsets

All SEU data were gathered with powered-off testing to isolate memory cell upsets from peripheral circuitry effects. The August 2022 heavy ion data for the 96-layer Micron flash (Fig. 7) represents four blocks (one per plane) totaling about 72 MB of single-level cell (SLC) flash, and two blocks totaling about 108 MB of triple-level cell (TLC) flash. The November heavy ion data (Fig. 5) represents ten SLC blocks.

It was observed initially that the SLC response was noticeably better than expected at low LET compared to previously-published data for flash memories of generally-similar technologies [5]. After further investigation, the parts were tested again (Fig. 5), but this time with adjustments made to the internal voltage threshold used to discriminate programmed cells (‘0’) from erased cells (‘1’) as provided in the manufacturer datasheet. Because NAND flash single-event upsets result in programmed (‘0’) cells turning into erased (‘1’) cells, it follows that adjusting the read offset setting towards the

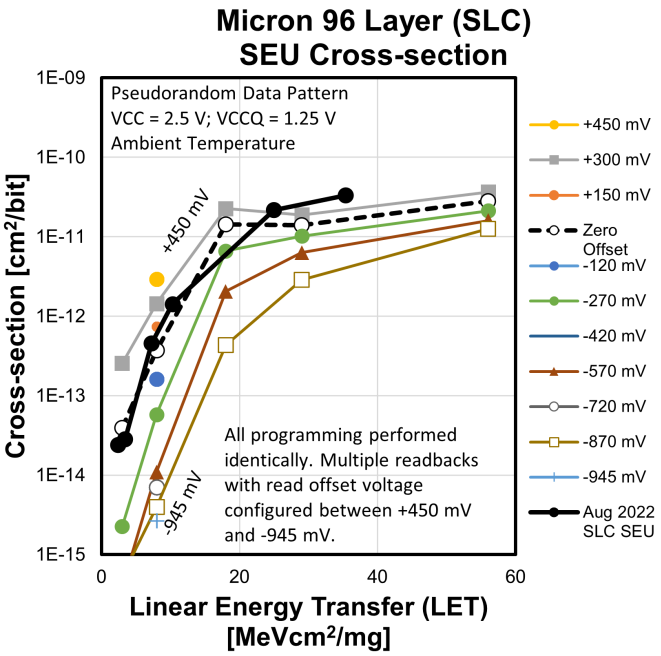

Fig. 5. Micron 96-layer flash heavy-ion SEU response

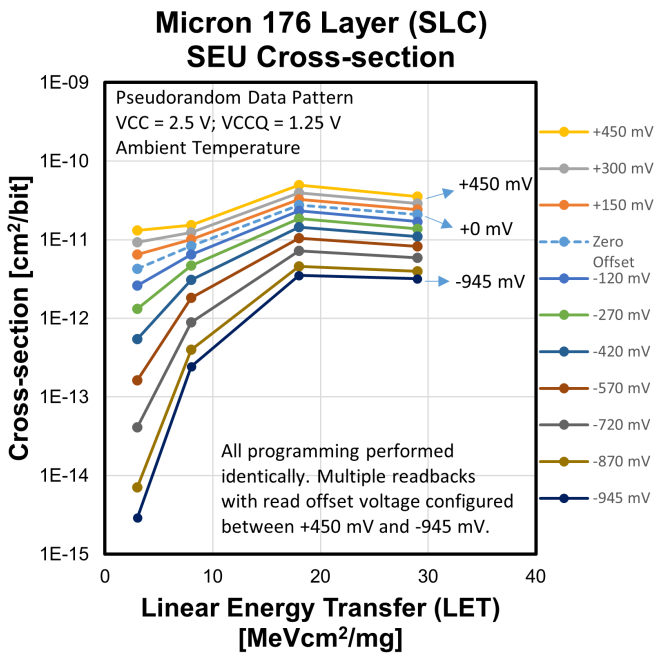

Fig. 6. Micron 176-layer flash heavy-ion SEU response

erased state might increase the resistance to SEU, especially at lower LET where deposited charge is insufficient to fully shift a cell from 0 to 1. See Fig. 9 for a generic illustration of this effect. Other tradeoffs (e.g., long-term data retention) are possible.

The black line in Fig. 5 is the original SLC data from Fig. 7 with the default threshold voltages. The dashed line is a repeat of that test with zero offset explicitly set for confirmation of prior results. A clear trend of increased SEU hardness with lowered (i.e., more negative) voltage threshold offset is present, as predicted by the effect of Fig. 9. Similar test results are available for the 176-layer Micron device in Fig. 6.

The Hynix device did not include a published mechanism to adjust the voltage threshold offsets and such testing was not performed in this study; a comparison of TLC and SLC SEU data is in Fig. 8.

B. Single-Event Functional Interrupts

Each device was tested for susceptibility to single-event functional interrupts (SEFI), which are non-destructive (recoverable) events caused by an upset in a critical element of control or peripheral circuitry that causes anomalous behavior. NAND flash SEFI are most easily grouped into those that cause a total loss of functionality requiring a power cycle, and those that cause malfunction within a portion of the memory array (e.g., block-level SEFI that prevent successful READ, ERASE, or PROGRAM operations). The SEFI that completely disrupt functionality are detected in this test by frequent polling of the device with a READID command; this can be easily automated to collect statistically-significant volumes of events with accurate fluence-to-failure recorded. Additionally, the tester autonomously recovered from each of these SEFI and recorded whether a simple RESET or HARD

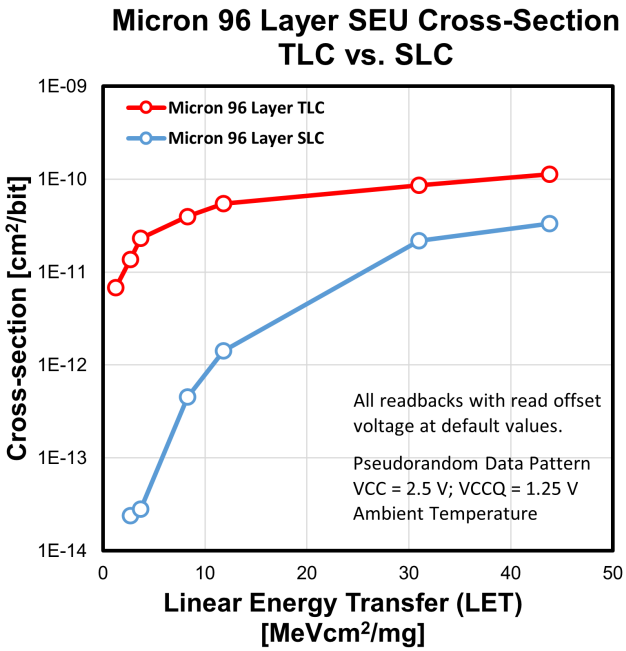

Fig. 7. Micron 96-layer flash comparison of SLC and TLC modes

RESET command was sufficient, or if the device required a power cycle to restore communications.

Necessary and sufficient recovery steps for the Micron 96-layer device are in Table II, for the Micron 176-layer flash in Table III, those for the Hynix 176-layer device are in Table IV, and breakdown of operational mode SEFI vulnerability in Table V. In Table V, a secondary shutter system was used to ensure the device was only exposed directly to the beam when the operational modes desired were active.

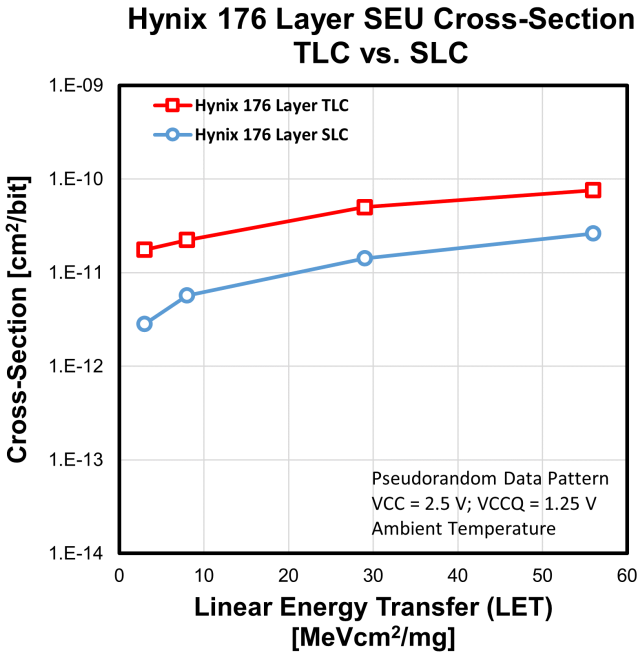

Fig. 8. SK Hynix 176-layer flash comparison of SLC and TLC modes

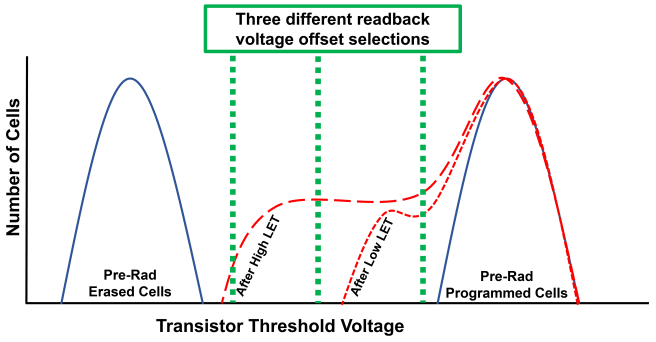

Fig. 9. Graphical diagram of the effect of varying LET on programmed flash cell threshold voltages. Green dashed lines are the programmed settings used to discriminate between programmed and erased SLC cells.

SEFI testing of individual device operational modes was performed on all three memories. However, such testing is inherently time-consuming and not all combinations of device and operational mode were extensively characterized at all LET of interest; lack of data at any given LET does not imply a zero-error result. Data available are in Fig. 10. Each device type is identified by marker shape, and each operational type during irradiation is indicated by color. Filled shapes indicate

TABLE II
SEFI RECOVERY STEPS NECESSARY FOR MICRON 96-LAYER DEVICE

LET (MeV·-cm^2/mg)	Fluence /cm^2	Count of READID SEFI resettable by RESET	HARD RESET	Pow. Cycle
18.0	$2.01 * 10^6$	10 (77%)	3 (23%)	0 (0%)
29.0	$2.61 * 10^6$	10 (71%)	1 (7%)	3 (21%)
56.0	$8.58 * 10^6$	89 (77%)	20 (17%)	6 (5%)
79.2	$1.05 * 10^7$	132 (70%)	40 (21%)	16 (9%)

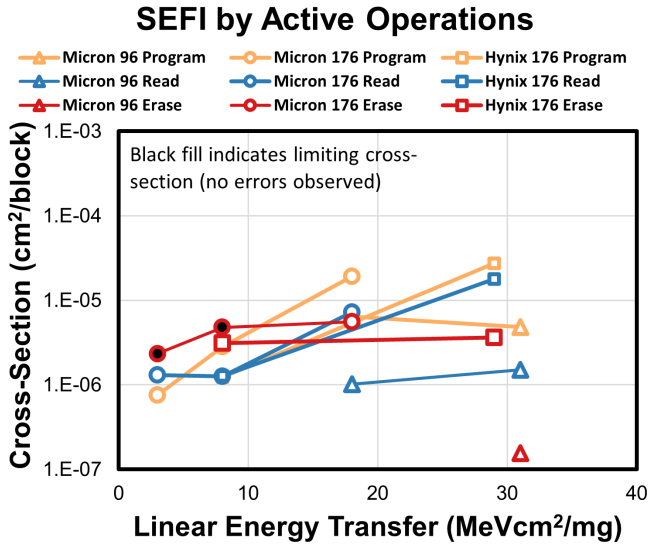

Fig. 10. Cross-section vs LET data for heavy-ion SEFI results in all three memories.

TABLE III
SEFI RECOVERY STEPS NECESSARY FOR MICRON 176-LAYER DEVICE

LET MeV·cm^2/mg	Fluence /cm^2	Count of READID SEFI resettable by RESET	HARD RESET	Power Cycle
3.0	$5.00 * 10^6$	3	0	0
8.0	$2.01 * 10^6$	2	0	0
18.0	$1.01 * 10^6$	2	0	0
29.0	$1.00 * 10^6$	7	0	0

limiting cross-sections where no errors were observed during testing, and are computed as the inverse of the total tested fluence at that LET.

SEFI operational testing was always performed with erase, program, read, and idle operations as typical of a data recorder-type application. In the case of an ERASE mode test, errors were detected in the erase or program stages by verifying the NAND status register flag was correctly set by the device indicating a successful operation after each erase or program command. Errors detected during readback were by means of an unrealistically-high error count at the block level. Following the erase-program-read-idle process, the device was reset and power cycled before restarting and re-opening the shutter.

If a SEFI was observed during the active phase (e.g., a failure to erase while under active irradiation) the beam was immediately blocked to minimize the probability of multiple events occurring during one cycle.

In the case of a PROGRAM mode test, a single operational cycle was erase-program-read-idle-erase, such that the effects of a SEFI induced while programming could be evaluated

TABLE IV
SEFI RECOVERY STEPS NECESSARY FOR HYNIX 176-LAYER DEVICE

LET MeV·cm^2/mg	Fluence /cm^2	Count of READID SEFI resettable by RESET	HARD RESET	Power Cycle
8.0	$1.15 * 10^6$	0	0	0
29.0	$1.0 * 10^6$	0	1	0

TABLE V
SEFI SUSCEPTIBILITY OF HYNIX 176-LAYER FLASH TO BLOCK-LEVEL ERASURE, PROGRAMMING, AND READBACK FAILURES

LET MeV·cm^2/mg	Fluence /cm^2	Operational State While Irradiating	Count of block SEFI detected as failure to: ERASE	PROGRAM	READ
8.0	$2.23 * 10^5$	ERASE	390	1	385
8.0	$2.23 * 10^5$	PROGRAM	39	1	81
8.0	$2.23 * 10^5$	READ	25	0	35
29.0	$2.23 * 10^5$	ERASE	49	3	38
29.0	$2.23 * 10^5$	PROGRAM	167	66	331
29.0	$2.23 * 10^5$	READ	200	113	144

during all subsequent phases. Similarly, a READ mode test is constructed of erase-program-read-idle-erase-program, with only the read portion exposed to beam; subsequent SEFI observed during erase and program were fully evaluated prior to restarting the next test.

These operational phases are similar to those described graphically and in more detail by [11].

The total number of program-erase cycles did not approach the datasheet limits for these devices in either SLC or TLC mode.

C. Single-Event Latchup

Testing with 16 MeV/amu Xe (incident LET 56.0 MeV·cm^2/mg) revealed no single-event latchup (SEL) in any of the devices tested when irradiated at 85°C to a fluence of $1*10^7$/cm^2 at V_{CC} of 3.3 V.

When irradiated at 45° angle (effective LET of 79.2 MeV·cm^2/mg at die surface) no SEL was observed in the two Micron devices to a fluence of $1.05*10^7$/cm^2. The Hynix 176-layer device had an anomalous high-current condition at this LET that reached power supply compliance and required a power cycle. This may be single-event latchup. Functionality was successfully recovered on-site, but further evaluation for latent damage has not been performed.

The control circuitry for these devices is implemented under the flash memory stack (on the order of 10-20 um below die surface). Beams used for this experiment had sufficient range to reach these circuits before the Bragg peak. However, precise estimation of tested LET requires construction analyses and will have the effect of raising the LET in the sensitive volume.

V. PROTON RESULTS

A. Single-Event Upsets

Proton testing at the Massachusetts General Hospital's Francis H. Burr Proton Therapy Center used 125- and 200-MeV proton irradiation to explore the proton sensitivity of the devices. Basic single-event upset test results are in Fig. 11 and represent test results with a 0x00 repeating data pattern. To investigate any cumulative dose-related effects, one experiment included a series of exposures with intermediate measurement points to a total fluence of $1*10^{11}$p/cm^2. In Fig. 12, four tests were performed without re-programming the memory. Then, a single test to the same fluence was performed for comparison.

Proton testing also allowed the opportunity to explore the responses of individual die within the stacked part, rather than only a top-level die as in heavy-ion testing. In Fig. 13, the

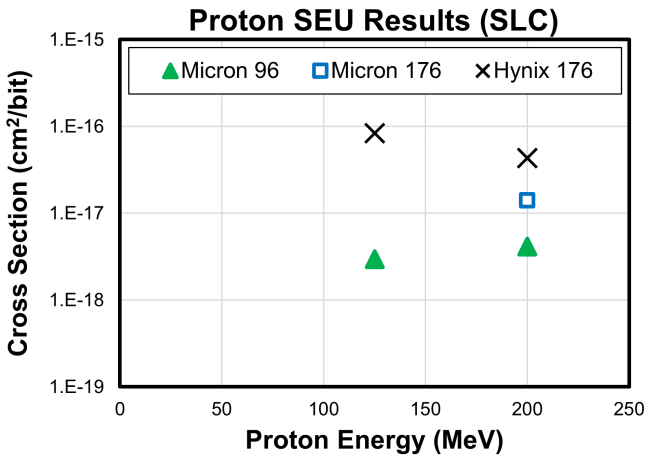

Fig. 11. SEU data for all three devices with high-energy protons.

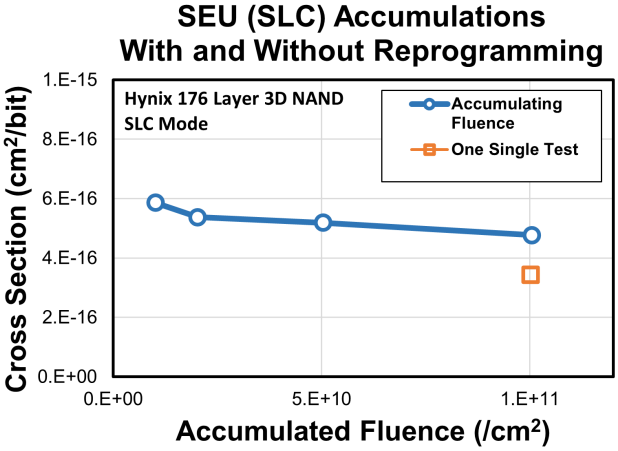

Fig. 12. Cumulative measurement of proton-induced upsets compared to a single measurement.

125- and 200-MeV proton responses of all sixteen die are compared. The fluence for each energy was $1*10^{11}$p/cm^2. The actual physical order of the sixteen die is unknown.

B. Single-Event Functional Interrupts

Some 200-MeV proton SEFI test data is also available, though the overall sensitivity to SEFI with protons was relatively low. Testing was only performed with READID-style testing, in which the device ID is rapidly polled to verify basic functionality of the device. Results are in Table VI. Block

TABLE VI
SEFI SUSCEPTIBILITY WITH 200 MEV PROTONS.

Energy (MeV)	Device	Total Fluence (/cm^2)	Observed SEFI	Cross-section (cm^2)	Recovery
200	SK Hynix 176	1*10^{11}	0	0	N/A
200	Micron 96	4*10^{11}	2	5.0*10^{-12}	Recovered with RESET
	Micron 176	Not Tested			

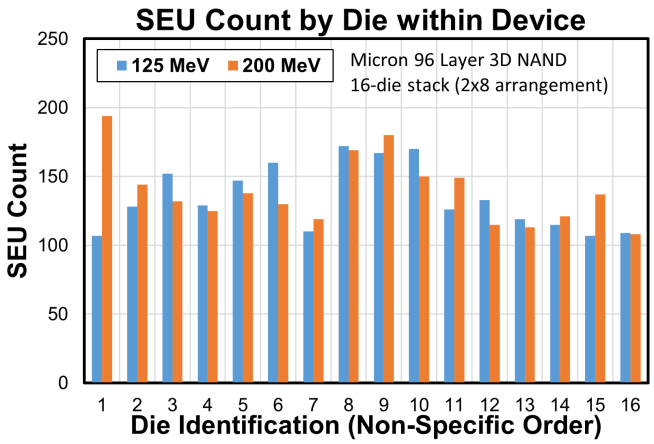

Fig. 13. Proton-induced upsets in all sixteen die of the stacked device.

SEFI events affecting memory integrity were not evaluated with protons.

While the Micron 176 layer device was not tested for SEFI with proton due to time constraints, it should be noted that this device had no READID SEFI (SEFI that resulted in loss of communications with the device) requiring more than a RESET command during heavy ion testing.

VI. ACKNOWLEDGMENTS

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