

On-chip Broadband Load Calibrators for Characterizing Transition-Edge Sensor Bolometers

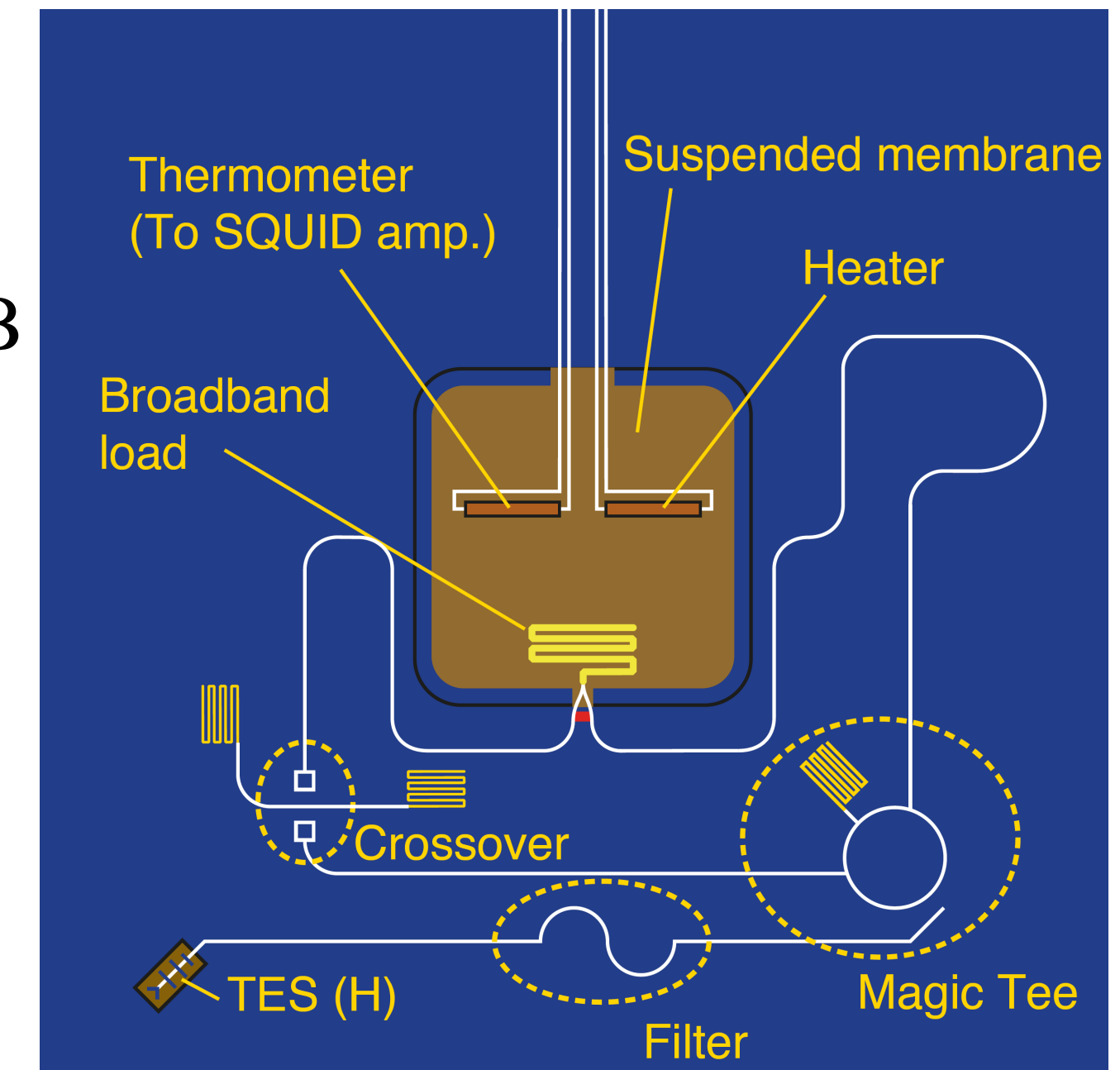
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INTRODUCTION

- Feedhorn-coupled, dual-polarization, transition-edge sensor (TES) bolometers, developed at NASA Goddard, on a single-crystal dielectric substrate with integrated electromagnetic shielding have been demonstrated on the Cosmology Large Angular Scale Surveyor (CLASS) experiment [1, 2]. These detectors hold the potential to enable the next-generation CMB space missions like the Probe of Inflation and Cosmic Origins (PICO).
- To further demonstrate and develop this technology, we have designed, fabricated, and tested on-chip broadband load calibrators [3, 4] integrated with CLASS W-band pixel designs. The broadband loads allow a precisely-controlled and variable power to be sent down a microstrip line for element-by-element and full circuit characterization of TES bolometers.
- This in-situ testing approach provides rapid and efficient characterization of various pixel designs in order to optimize the optical efficiency and control of systematic effects of the detectors, without the need for an external blackbody source. We added complementary tests of spectral response through development of on-chip filter-bank spectrometers.



Schematic of the on-chip broadband load highlighting various key detector circuit elements that we tested

DESIGN & FABRICATION

- The broadband load consists of a membrane-isolated island with a broadband resistive termination coupled to outgoing microstrip transmission line. A resistive heater and a Johnson-noise (JN) thermometer on the island allow the temperature of the load to be controlled and measured.
- We designed 20 mm × 20 mm test pixels with broadband loads coupled to TES detectors through various circuit elements. We have also developed 8-way power dividers that enable a greater range of tests per pixel and mitigate possible systematic effects in the measurement due to fabrication tolerances. The test pixels were fabricated in a 4×4 grid on a 100 mm silicon wafer.

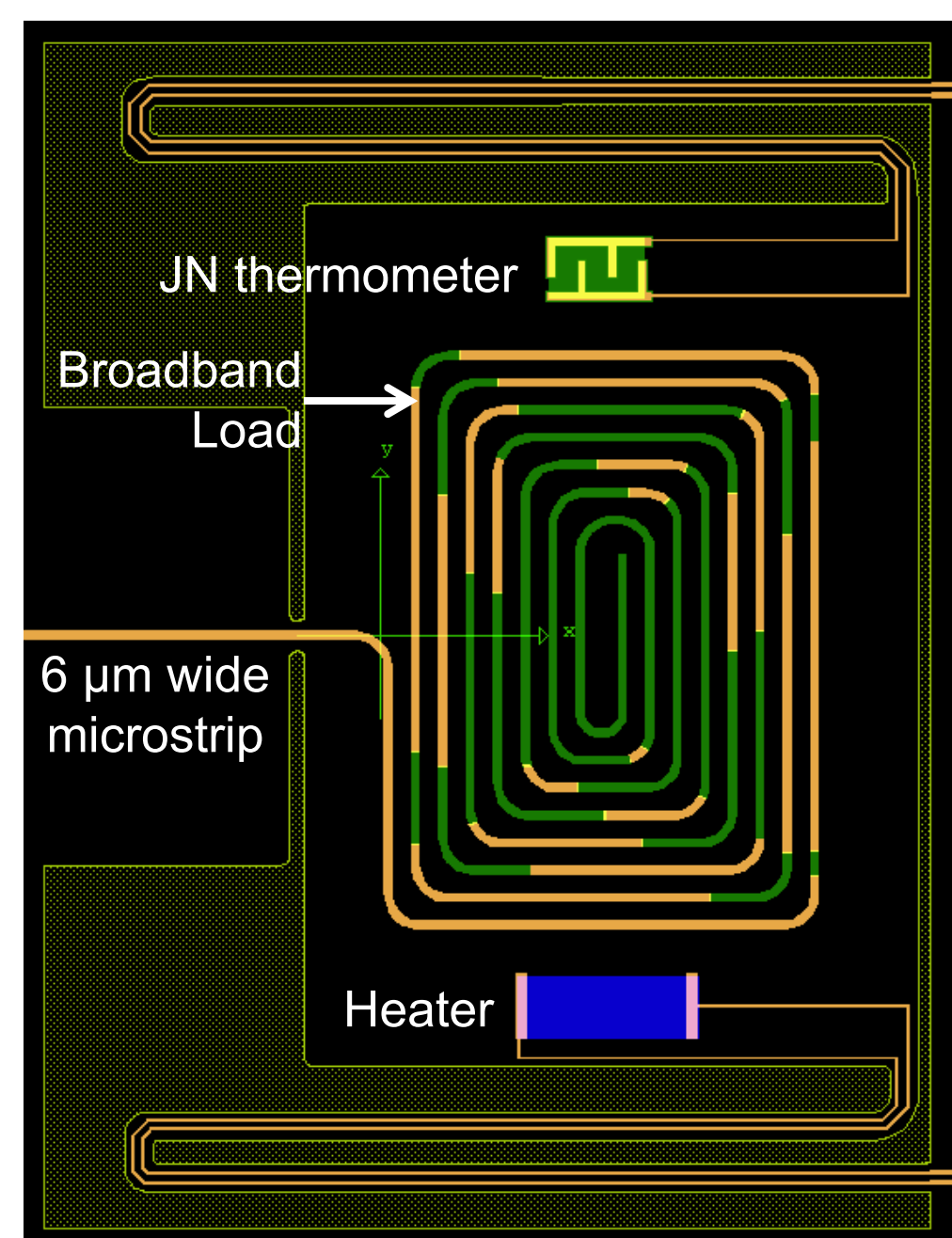
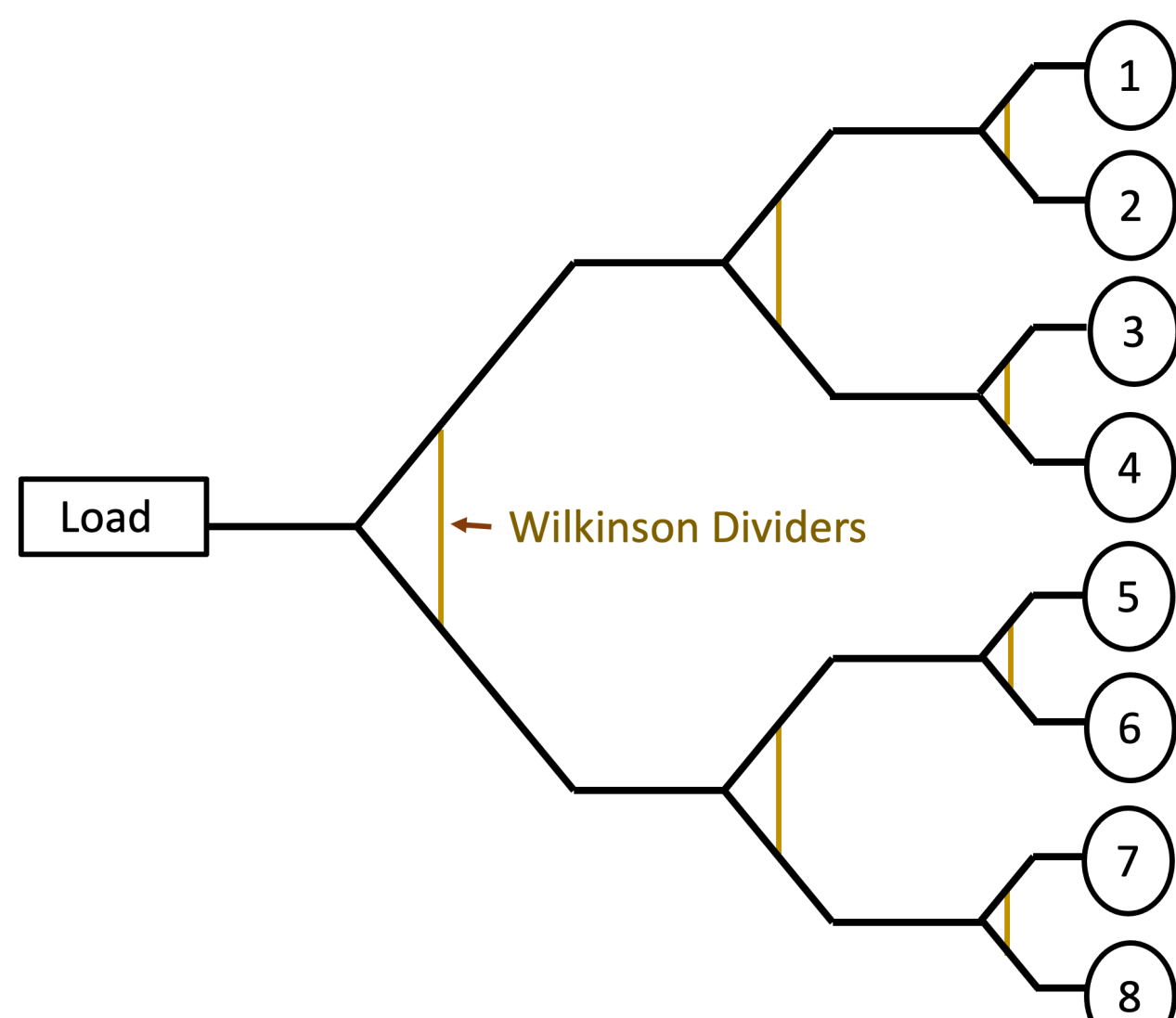
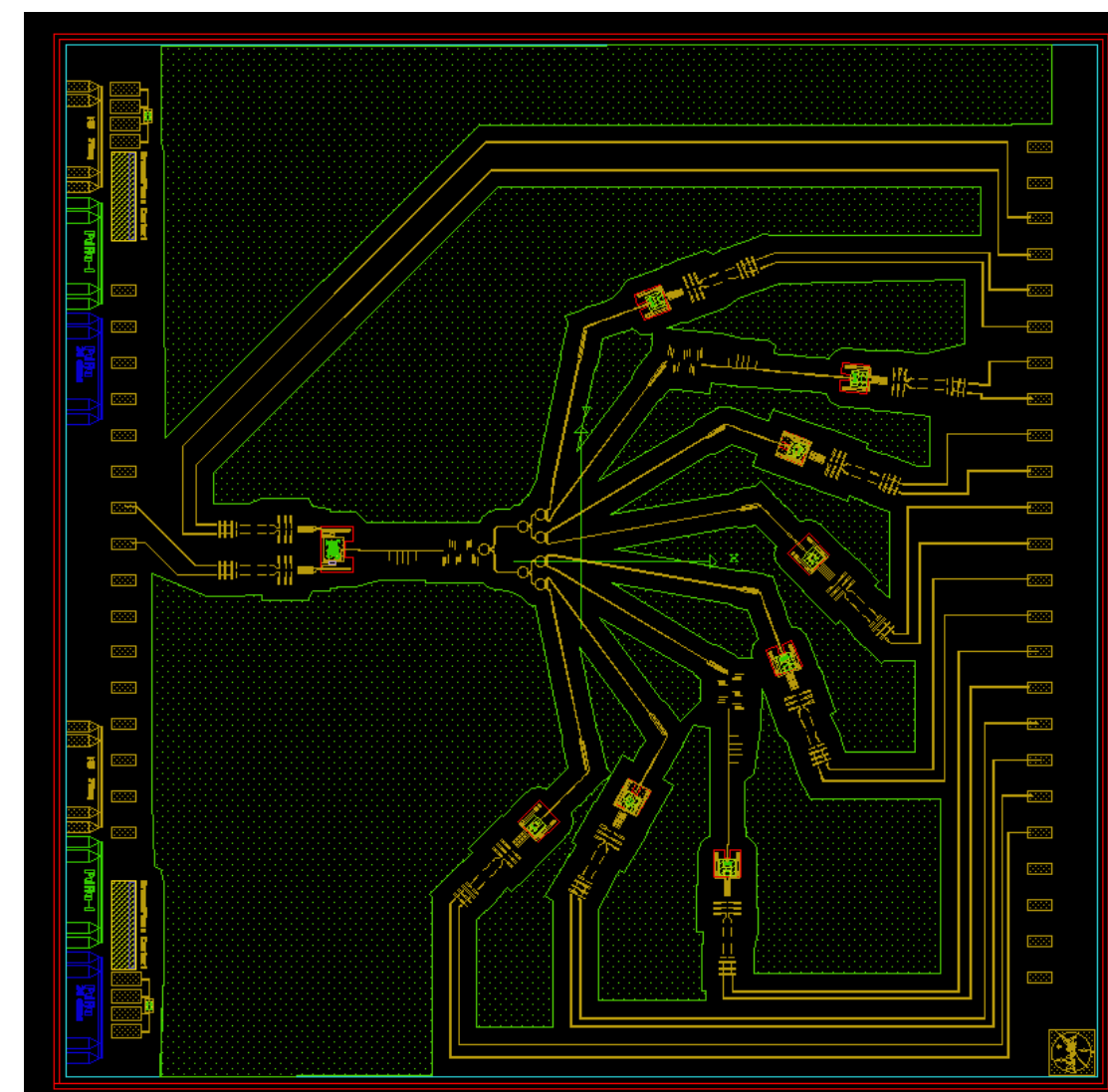


Diagram of the broadband load design

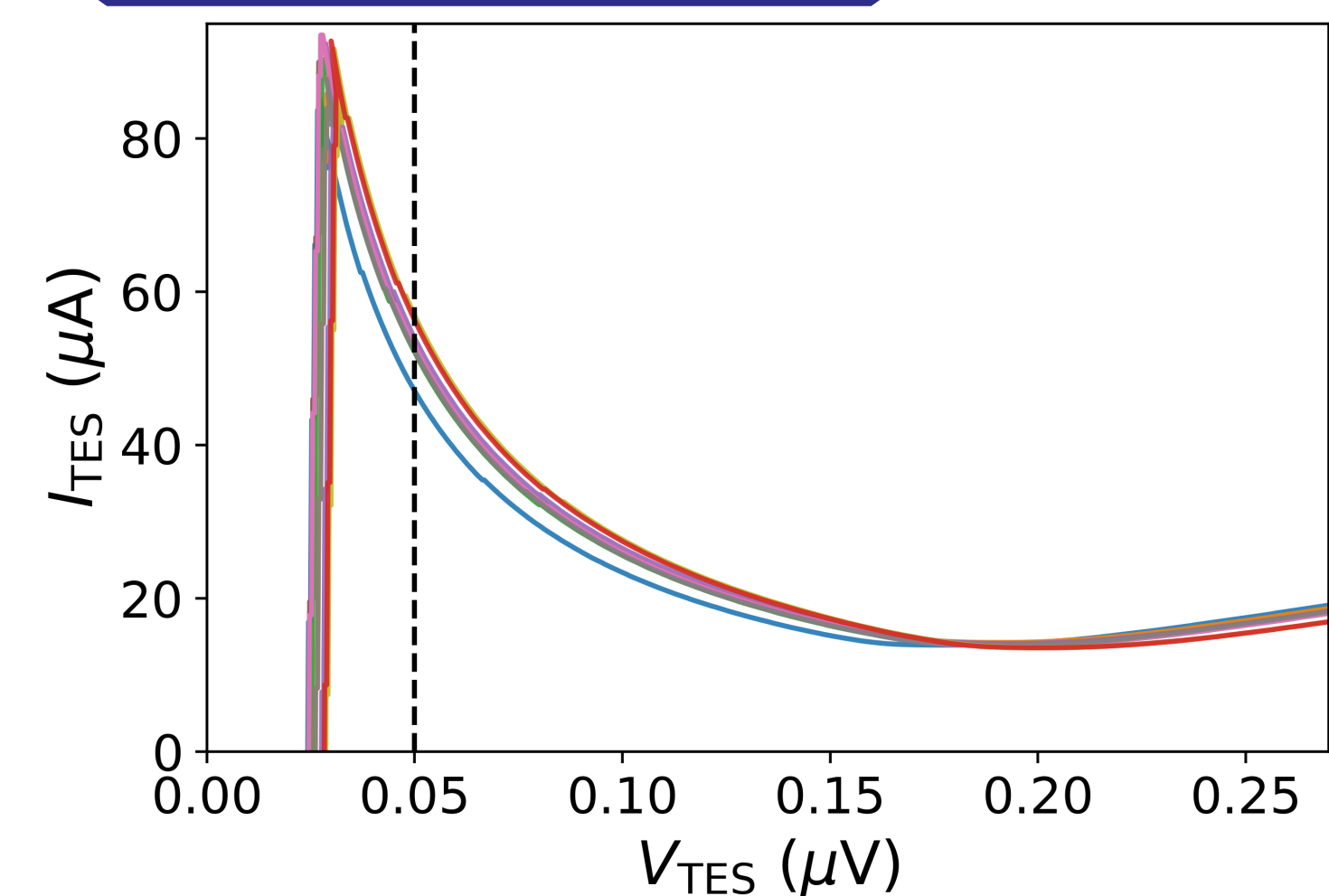


(Left) Schematic of a representative 8-way power divider. Each number represents a TES termination with a specific circuit element being tested. (Right) Implementation of the power divider network on a test pixel

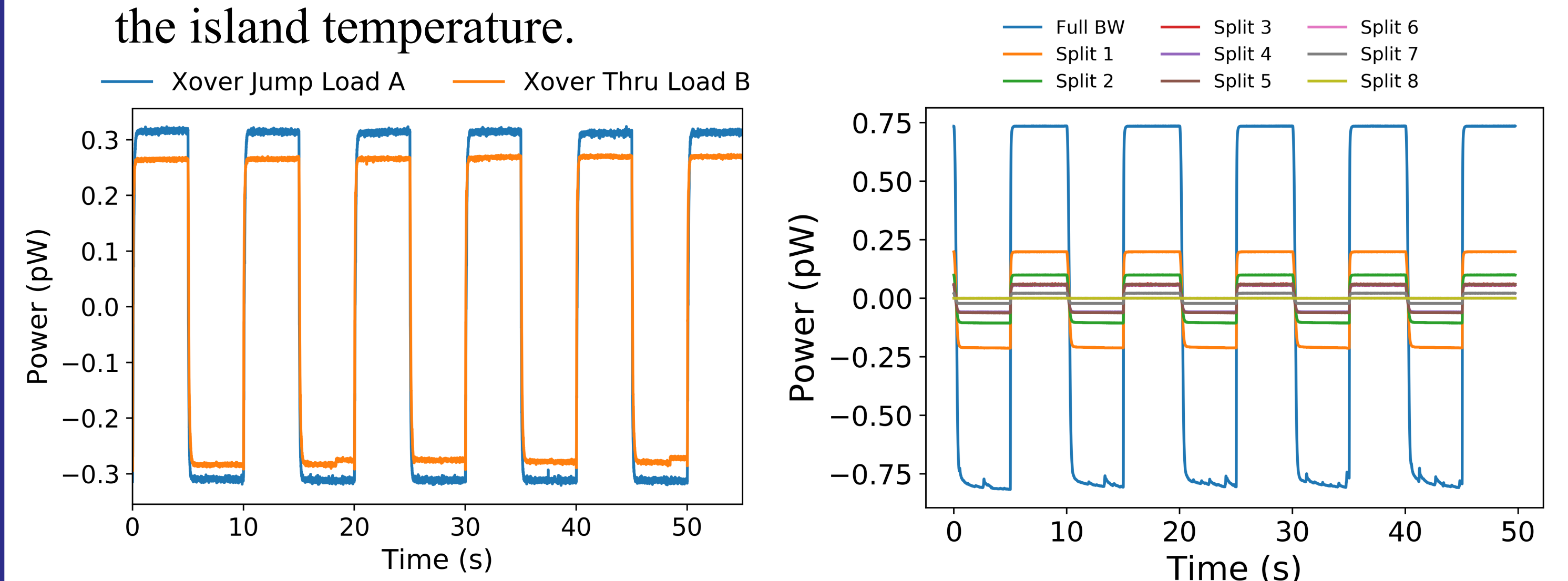


INITIAL RESULTS

- To characterize TES bolometer parameters and select proper biasing, we acquired I - V curves by first ramping up the TES bias voltage (V_{TES}) to drive the detectors normal and then stepping down the voltage while recording the TES current response (I_{TES}).
- To measure the desired signal from the load at a level well above the detector noise ($\sim 25 \text{ aW}\sqrt{\text{s}}$), we bias the heater with a square wave such that the load island temperature fluctuates between $\sim 1.0 \pm 0.05 \text{ K}$.
- While we observe the expected square wave TES response, the overall test pixel thermally fluctuates with the load island, adding significant systematics to our data. An error in the JN resistor design also decreased the thermometer's sensitivity below that required to precisely measure the island temperature.



I - V curves acquired at 30 mK bath for TESs on one of the test pixels. The vertical dashed line shows the selected bias for this set of I - V s.

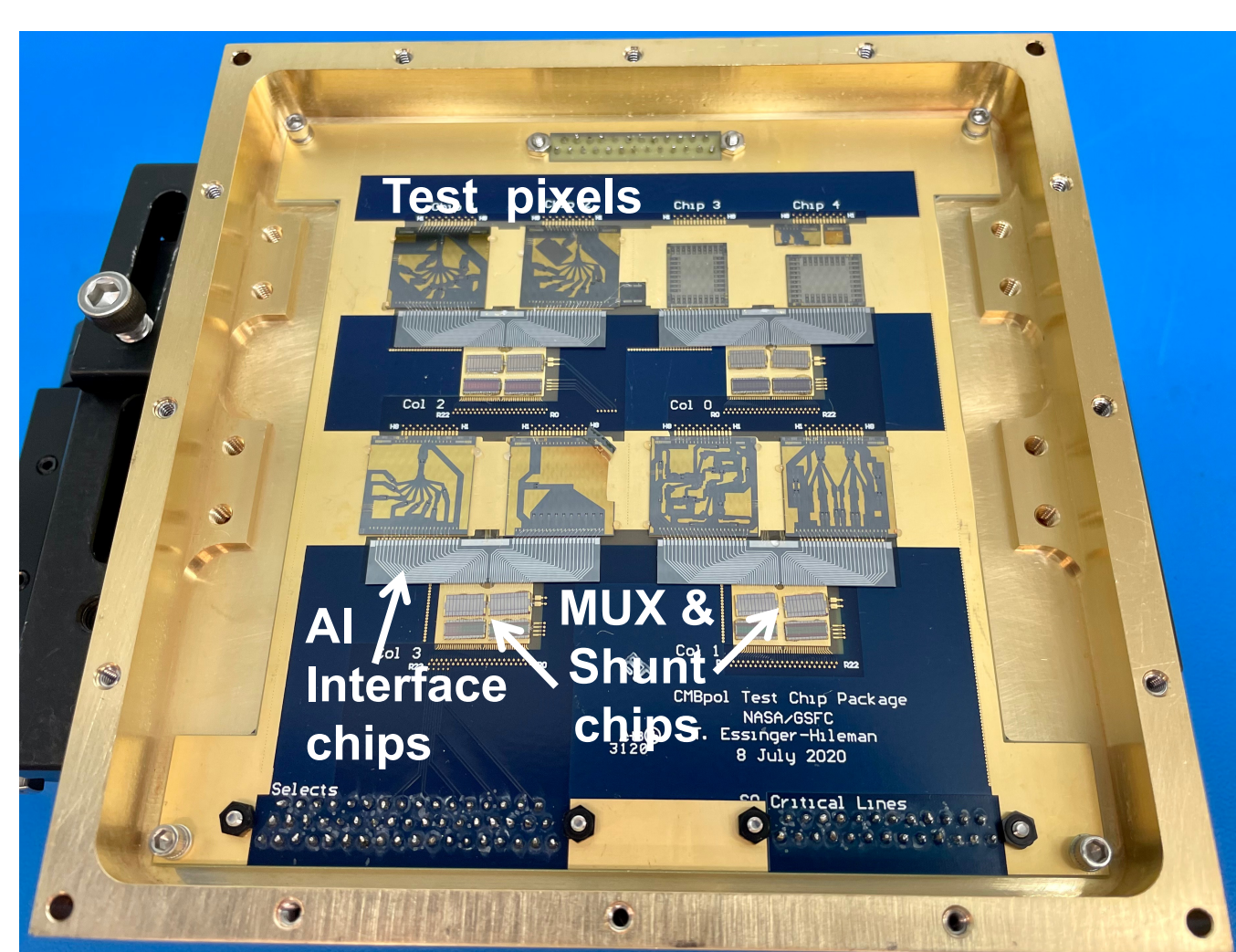


(Left) Responses from two TESs connected through different signal paths of via-less crossovers. Since the loads are on different islands in this case, lack of precise JN temperature data makes the comparison of the two power levels difficult. (Right) Responses from nine TESs connected to the same load through different frequency channels in the filter-bank spectrometer. While the channel with the full detector bandwidth measures the highest power as expected, systematics from the chip thermal fluctuations limit our understanding of the full result.

- While the initial results show the promise of the basic technique, thermal fluctuations that mimic the signal of interest and sub-optimal JN thermometers limit our current measurements.

TESTING

- With six test pixels, we investigate detector frequency response, loss on microstrip transmission lines, and performance of various designs of magic-tees, via-less crossovers, and signal terminations on TESs.
- The pixels are glued onto a PCB with arathane and heat sunk through Au bonds. The detectors are read out using time-division multiplexer (MUX) chips wire-bonded through shunt and interface chips. The PCB is bolted inside a light-tight Au-coated copper package mounted onto the mixing chamber plate of a dilution refrigerator cooled to $\sim 30 \text{ mK}$ (well below $\sim 150 \text{ mK}$ T_c of the detectors).



Test package with six test pixels and readout/interface chips. The two smaller chips on the top-right contain reference detectors from prior tests for evaluating package systematics.

FUTURE WORK

- Reduction of Johnson noise thermometer resistance to increase measurement accuracy
- Increased physical separation of on-chip loads from TESs to reduce sensitivity to chip thermal fluctuations
- Reduction of on-chip load thermal conductance to reduce power required to drive loads to their target temperature of 1 K.

References:

- [1] T. Essinger-Hileman et al., Proc. SPIE 9153, 91531I (2014)
- [2] K. Harrington et al., Proc. SPIE 9914, 99141K (2016)
- [3] D.E. Prober et al., IEEE Trans. Appl. Super-Con., 17:241 (2007)
- [4] K. Rostem et al., J. Appl. Phys., 105:084509 (2009)