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Venus Surface Environmental Chamber Test of SiC JFET-R Multi-Chip Circuit Board

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Abstract. This poster describes a first attempt to demonstrate a multi-chip prototype lander control and sensor signal digitization electronics circuit board comprised of ten NASA Glenn IC Generation 11 SiC JFET-R IC chips in 460 °C, 9.4 MPa harsh Venus surface conditions. The lander circuit ceased electrical operation prematurely at 107 °C as the Venus chamber heated up. Optical and SEM post-test inspections indicate fatal dielectric cracks occurred on only one of the ten SiC chips.

Motivation: Long-mission Venus surface landers NOT FEASIBLE without electronics durable in 460 °C, 9.4 MPa caustic environment (Fig. 1) [1,2].

Prior Work: NASA Glenn demonstration of *individual* semiconductor integrated circuit (IC) chips in Venus environment chamber 60 days (Fig. 2) [2].
- SiC Junction Field Effect Transistor – Resistor (JFET-R) IC Gen. 10 chips
- SINGLE CHIP demonstration of clock ICs (< 200 transistors/chip)

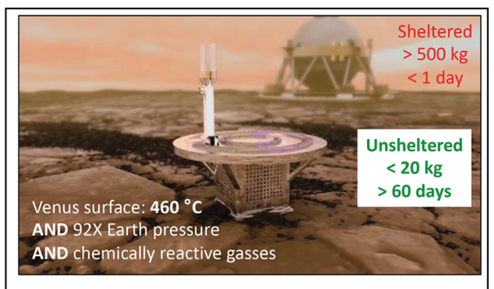


Fig. 1. Comparison of Venus lander missions. Lander that requires sheltering of non-durable electronics from Venus atmosphere (background) is much heavier and shorter-mission than unsheltered SiC electronics lander (foreground) [1].

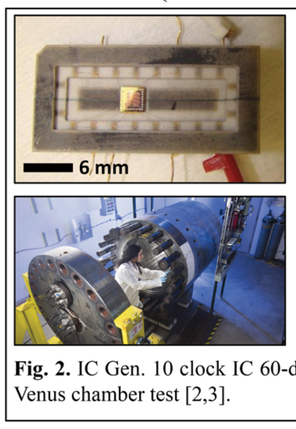


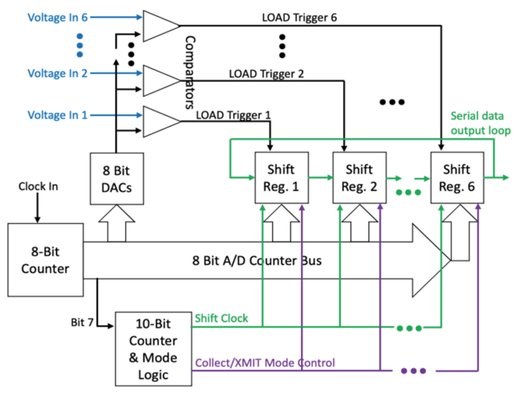
Fig. 2. IC Gen. 10 clock IC 60-day Venus chamber test [2,3].

Goal of This Work: First demonstration of a *multi-chip circuit board* (i.e., lander subsystem) in NASA Glenn Venus environment chamber.

Circuit Board Design and Construction

Function: Analog-to-digital conversion (ADC) of multiple sensor voltages into sequence serial data

IC Gen. 11 ADC and Serial Data Output Circuit
Continuous sequence of two operating modes:
Collect Mode: Parallel digitize voltage data into shift registers.
XMIT Mode: Shift register data repeatedly pings serial data output.



Circuit design criteria:
- Low power (for prolonging battery life)
- Autonomous operation when powered
- Reconfigurable number of sensor channels
- Made from ***IC Generation 11*** chip designs
  - Up to 706 transistors/chip

Circuit revisions during IC & board fabrication
- Very low IC Gen. 11 chip yield at probe-test
  - See [4] for details of fabrication issues
- Sensor channel count decreased from 12 to 6
- No fully working 8-bit and 10-bit counters
  - Counters with 6 working bits used
  - 6-bit ADC instead of 8-bit ADC
- External clock (instead of on-chip clock)

Fig. 3. Functional block diagram of the prototype IC Gen. 11 multi-chip Venus lander subsystem circuit board that was constructed and tested. As part of a Venus lander mission this board would digitize multiple analog sensor signals and ping the corresponding digital bitstream to a transmitter.

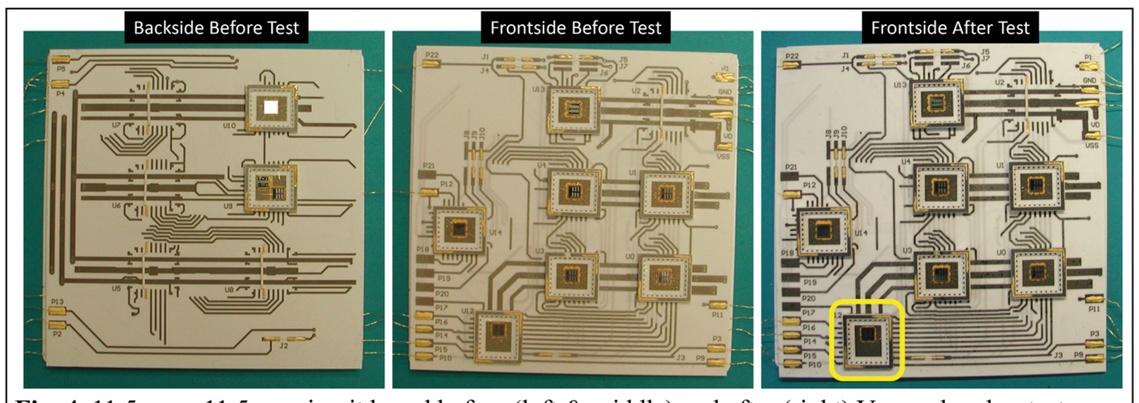


Fig. 4. 11.5 cm x 11.5 cm circuit board before (left & middle) and after (right) Venus chamber test.

Ceramic circuit board with four interconnect layers and 10 SiC chips (in 9 ceramic packages)
- Circuit board and chip packages commercially manufactured to NASA design specifications
- Empty chip packages & jumpers attached to circuit board PRIOR to chip die-attach into packages
- Chip die attach process exposes chips to 2-3 hours at 600 °C anneal in air.
- Final step in packaging flow is manual gold wire (ball) bonding to connect chips to packages

See Ref. [5] for additional chip packaging materials and processing details.

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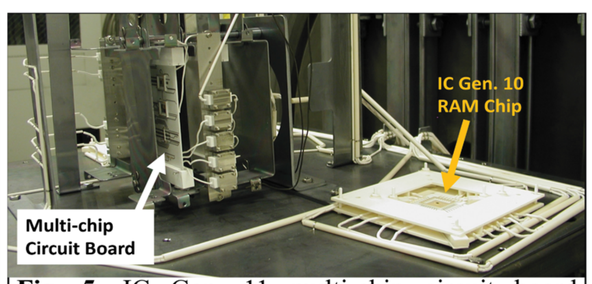

Fig. 5. IC Gen. 11 multi-chip circuit board mounted and ready for testing inside the Venus environmental chamber. An IC Gen. 10 memory chip that successfully operated throughout the 11-day test is seen nearby.

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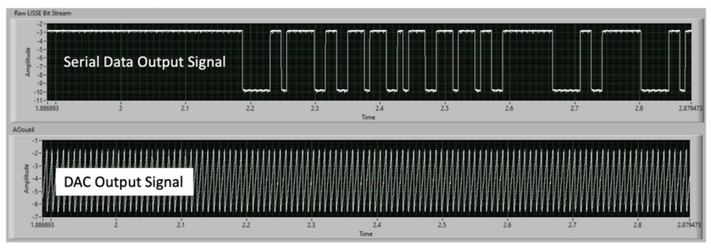
Venus Chamber Electrical Test Results

Board electrically FAILED as Venus chamber was heated up past 107 °C

Output waves at 107 °C before failure



Output after failure

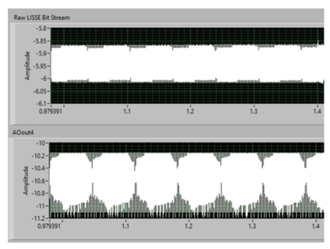


Fig. 6. Circuit output signals measured with board inside Venus chamber (left) just prior to failure at at 107 °C and (right) after failure. The measured diagnostic signal of the bottom left trace is a repeating ramp staircase generated by counter IC driving a diagnostic output DAC. The top left trace shows the start of serial data output as operating mode transitioned from collect mode to transmit mode.

Post-Test Microscopic Failure Analysis

Dielectric crack and metal discoloration were evidenced on only 2 of the 10 SiC chip surfaces.
- Appearance (Fig. 7) consistent with prior SiC JFET-R IC failure mechanism studies in [6,7].
  - Crack enables oxidation, swelling of underlying $TaSi_2$ causing rapid lateral crack expansion.
- Location in circuit-critical regions consistent with observed electronic circuit failure mode.
- No evidence of package, circuit board, wire bond, or die-attach failure detected.

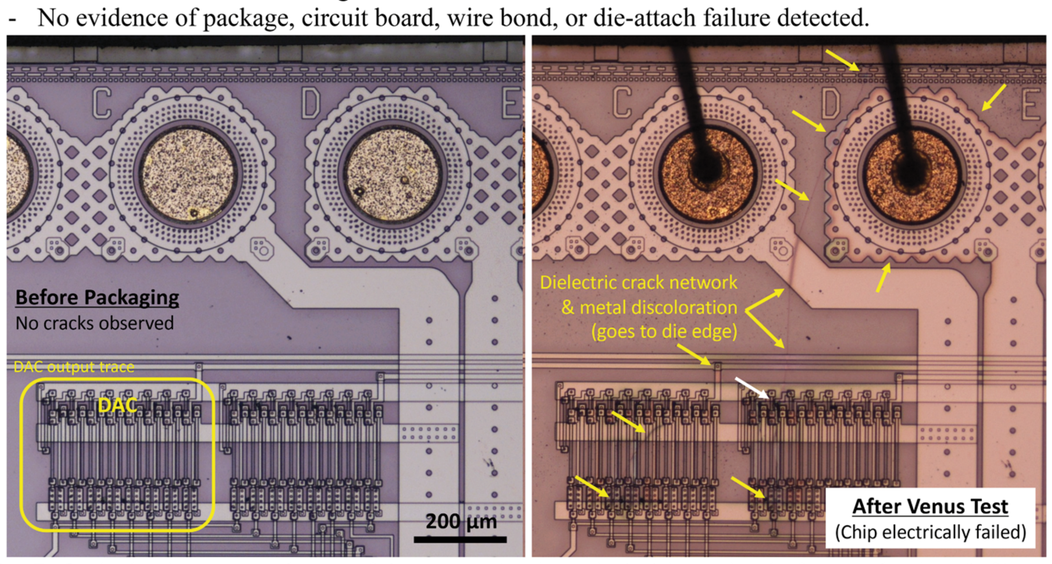


Fig. 7. Optical microscope photos of the same circuit-critical chip region before packaging (left) and after packaged Venus chamber testing (right). The crack network passes through electrically critical circuit regions including a major power supply bus and Digital to Analog (DAC) subcircuit on the chip denoted by the yellow box annotation in Fig. 4 that failed.

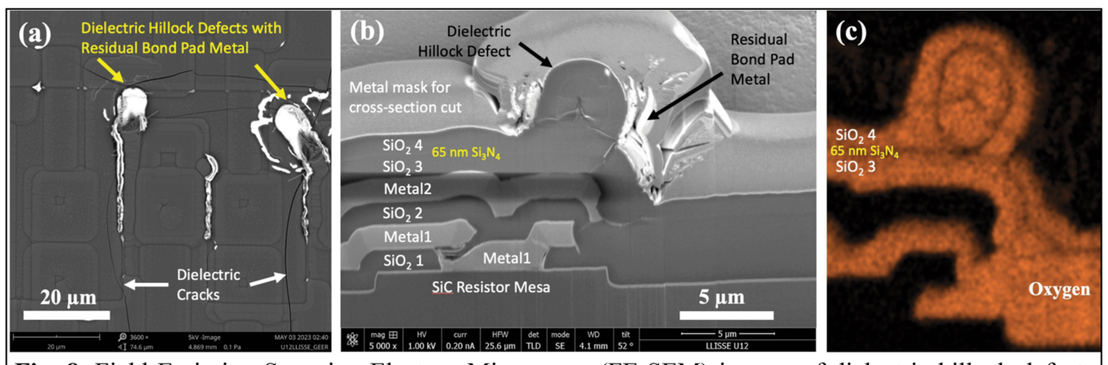


Fig. 8. Field Emission Scanning Electron Microscope (FE-SEM) images of dielectric hillock defects that corresponded to most of the dielectric cracks found on the failed chip. (a) Top view under imaging conditions highlighting residual metal leftover from the bond pad etch. (b) Cross-sectional image of hillock defect structure and prevalence of residual surrounding bond pad metal. (c) Energy dispersive X-ray spectroscopic oxygen elemental map of part (b) defect resolving top two oxide layers suggesting defect originated near start of SiO_2 3 layer deposition.

Most dielectric cracks on the failed chip correlated with "dielectric hillock" defects.
- Hillocks (Fig. 7) were few micrometers in height and formed during deposition of 3rd SiO_2 layer.
  - ***Suspected root cause: SiO_2 3 deposition onto localized Metal2 photoresist etch mask remnants.***
- Dielectric topography also caused incomplete removal of metal during bond pad patterning etch.
  - Local stress from larger thermal coefficient of expansion mismatch of bond pad metal stack.
- Hypothesis: Majority of cracking/discoloration occurred during 600 °C die attach air anneal.
  - Circuit failed too early during test for cracks to have initiated in Venus chamber.

Mitigations for IC Gen. 12 fabrication:
- Revise metal patterning etch processing to eliminate photoresist residue.
- Increase bond pad patterning over-etch to eliminate metal residue at texture.

Concluding Summary

- **IC Gen. 11 multi-chip circuit built & Venus chamber tested.**
- **Failure of single SiC chip, initiated at Metal2 etch step.**
- **Revised metal etch processing is key to IC Gen. 12 success.**

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