2023 NCCAVS Joint User Group Meeting *1:10-1:40 PM Sep. 13, 2023*

Pt/HTCC Alumina based Electronic Packaging System and Integration Processes for High Temperature Harsh Environment Applications

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Background

Prototype pre-fired alumina package with Au thick-film metallization have facilitated SiC JFETs based ICs developed at NASA for thousands of hours test at 500 °C

- Package assembly process not compatible with packaging industry standard
- Two side metallization PCB

Pt/HTCC material system proposed and tested for 500°C applications

- Dielectric constant and dielectric loss of HTCC alumina characterized
  - In the temperature range T_R – 550°C, Frequency range 100Hz – 1 MHz
  - HTCC alumina outperform 96% alumina and other selected LTCC ceramic substrates
  - Pt /HTCC alumina fabrication compatible to HTCC industry

A prototype Pt/HTCC packaging system developed, characterized, and tested with SiC ICs at high temperature

- Tested for 10k hours at 500°C, briefly above 850°C
- 60 days in simulated Venus surface environment

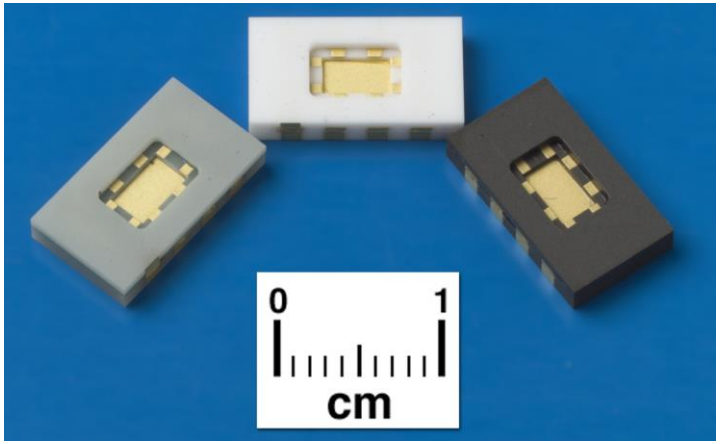
This talk concentrates on Pt/HTCC system and compatible die-attach, component-attach, wire-bonding

Background – Ceramic Packages based on Pre-fired Substrates

Ceramic Electronic Packages for High Temperature ICs

96% Al_2O_3

AlN



90% Al_2O_3

- Three types of ceramic substrate and Au thick-film metallization based chip-level packages
- 96% alumina for better high temperature dielectric performance
- AlN for better thermo-mechanical properties – lower CTE
- 90% alumina easier for fab
- Au thick-film metlalizations
- Three layers stacked, not in a way suitable for mass production

Chen and Hunter, 2005 HiTEN

Dielectric Properties of HTCC Alumina

Dielectric Constant of Alumina Substrates

HTCC alumina tested and compared with selected 96% alumina, 99.6% alumina, and LTCC alumina (with glass)

- Frequencies: 120Hz, 1kHz, 10kHz, 100kHz, and 1 MHz
- Temperatures: T_R, 50°C, 100°C, 150°C, 200°C, 250°C, 300°C, 350°C, 400°C, 450°C, 500°C, and 550°C

Compared with 96% alumina:

- Dielectric constants of 92% and 99.6% alumina are higher and increase more at 120Hz, 1kHz, 10kHz, 100kHz, and 1 MHz
- Dielectric constant of HTCC alumina is lower and increases less at 120Hz, 1kHz, 10kHz, 100kHz, and 1MHz at T > 350°C

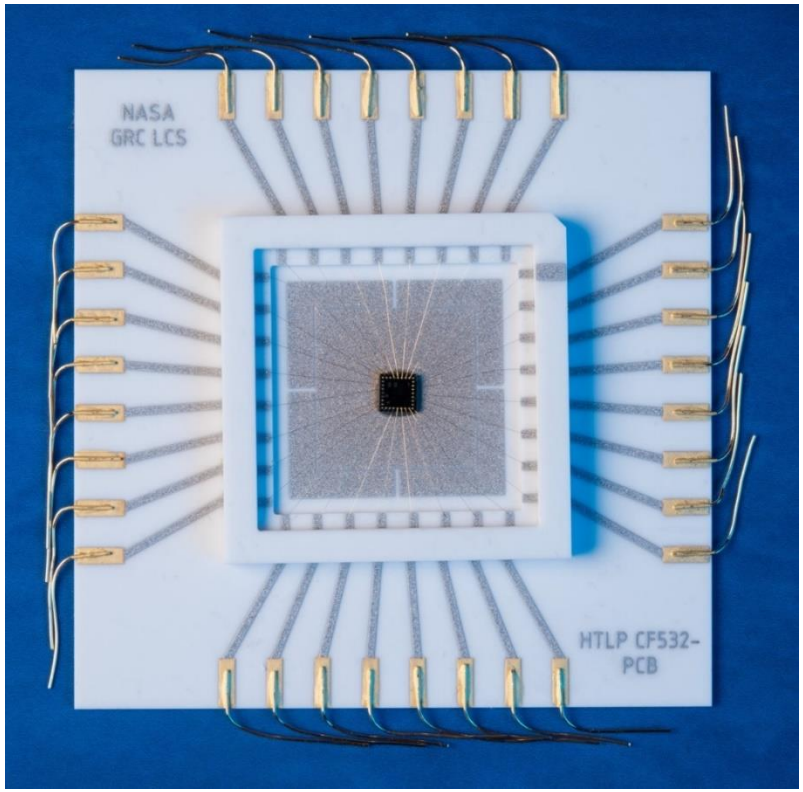
Compared with 96% alumina:

- Conductivities of 92% and 99.6% alumina are higher at temperatures above 200°C at the frequencies of 120Hz, 1kHz 10kHz, 100kHz, and 1MHz
- AC conductivity of HTCC alumina is always lower and increases less with T at 120Hz, 1kHz, 10kHz, 100kHz, and 1 MHz at T > 300°C

Chen, 2012 HiTEC

32-pin Pt/HTCC Alumina Chip-level Packages

Pt/HTCC alumina Packaging System for 500°C Operation



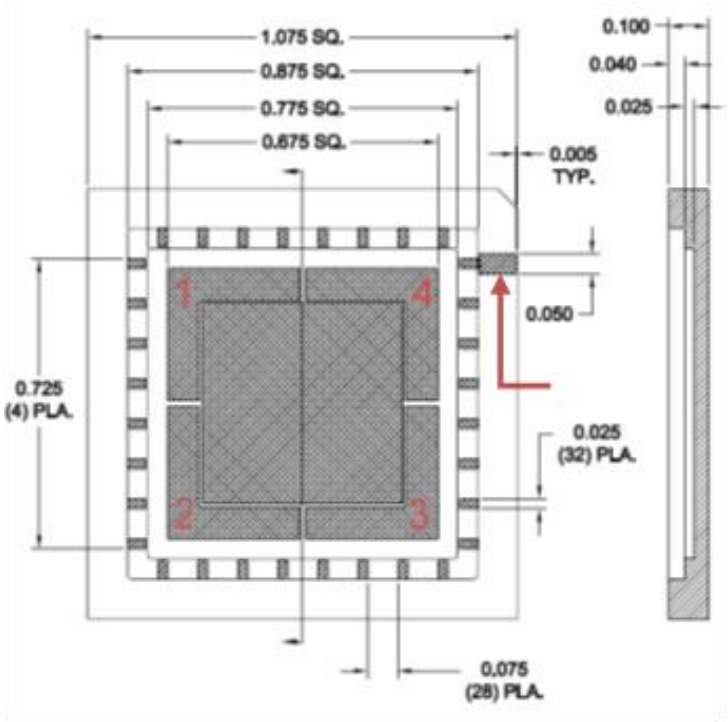
0.5 Inch

- Pt/HTCC alumina
- 32-IOs
- For low power circuits
- Pt via connecting pads
- 1 inch x 1 inch package
- Surface mount
- Tested with SiC JFET ICs
- Characterized for parasitic parameters
- Commercially fabricated

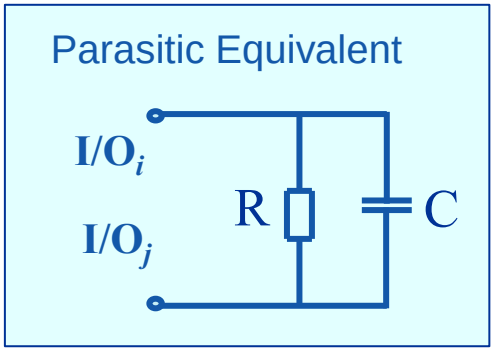
Chen et al, 2015 MS&T

32-pin Pt/HTCC Alumina Package

Parasitic R//C of Neighboring I/Os



1.07 inches



R//C model

R – DC leakage and AC dielectric loss

C – Dielectric polarization

$$1/Z(T,\omega) = G(T,\omega) + j\omega C(T,\omega)$$

R//C measured between I/O1 - I/O2, and I/O2 - I/O3

- I/O1 connected to all five bias pads

DC resistance measured separately

L. Chen, P.G. Neudeck, D.J. Spry, G.M. Beheim, and G.W. Hunter, iMAPS HiTEC, 2016.

32-pin Pt/HTCC Alumina Package

AC Parasitic Capacitance and Conductance of Neighboring I/O1 – I/O2

T (ºC) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
120	1.0	0.7	0.6	0.4	0.3	0.5	0.4	0.6	0.7	1.4	1.4
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.001	<0.001
1K	0.4	0.2	0.5	0.5	0.3	0.4	0.5	0.5	0.5	0.5	0.4
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
10K	0.5	0.4	0.5	0.5	0.4	0.4	0.4	0.5	0.5	0.4	0.4
	<0.001	0.0013	<0.001	<0.001	<0.001	<0.001	<0.001	0.003	<0.003	<0.003	<0.003
100K	0.5	0.3	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.4
	0.01	0.016	0.014	0.016	0.016	0.011	0.014	0.029	0.035	0.026	0.045
1M	0.5	0.4	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.5
	<0.010	<0.010	0.013	0.012	0.011	0.006	0.009	0.018	0.021	0.022	0.026

> 50°C margin above 500°C

pF
µS

C < 1.5 pF, R > 20 MΩ

Usable for many envisioned 500°C SiC ICs

L. Chen, P.G. Neudeck, D.J. Spry, G.M. Beheim, and G.W. Hunter, iMAPS HiTEC, 2016.

32-pin Pt/HTCC Alumina Package

AC Parasitic Capacitance and Conductance of Neighboring I/O2 – I/O3

T (°C) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
120	0.7	0.6	0.5	0.4	0.3	0.4	0.4	0.6	0.5	0.6	0.6
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
1K	0.3	0.3	0.4	0.4	0.2	0.4	0.3	0.5	0.3	0.5	0.5
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.0013	0.001	<0.001
10K	0.4	0.3	0.4	0.4	0.3	0.3	0.4	0.4	0.4	0.4	0.3
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
100K	0.3	0.3	0.4	0.4	0.2	0.3	0.3	0.4	0.4	0.4	0.3
	0.005	0.005	<0.005	<0.005	<0.005	0.005	0.013	<0.010	0.014	0.012	<0.010
1M	0.3	0.4	0.4	0.4	0.2	0.3	0.3	0.4	0.4	0.4	0.3
	<0.010	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020

> 50°C margin above 500°C

pF
µS

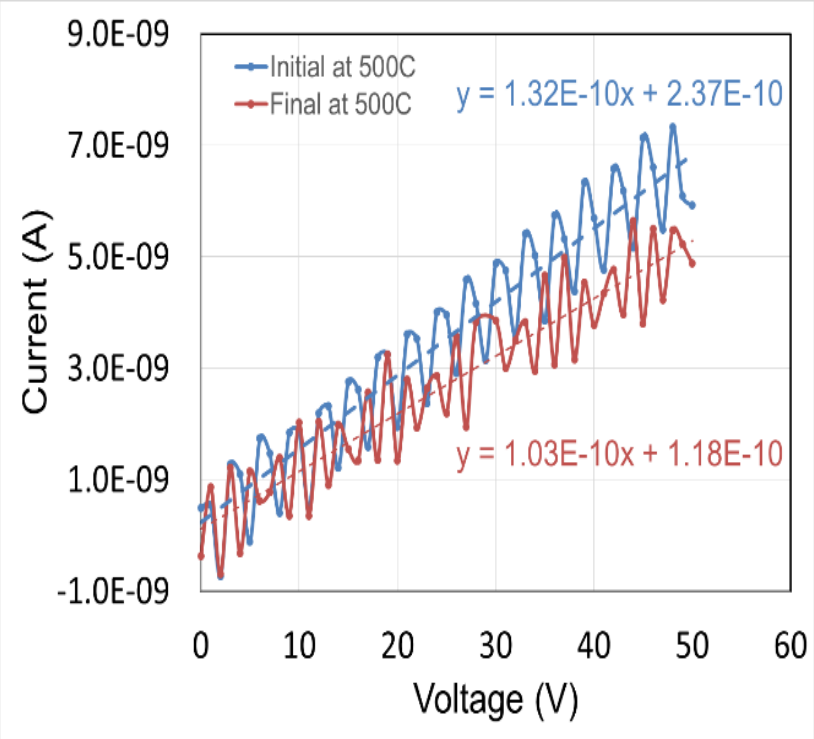
C < 1.5 pF, R > 20 MΩ

Usable for packaging many envisioned 500°C SiC ICs

L. Chen, P.G. Neudeck, D.J. Spry, G.M. Beheim, and G.W. Hunter, iMAPS HiTEC, 2016.

32-pin Pt/HTCC Alumina Package

DC Resistance of Neighboring I/Os



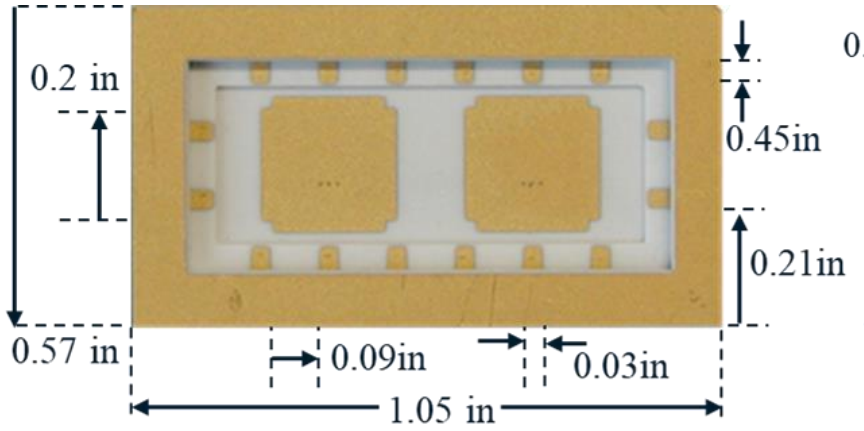
DC I-V Curves

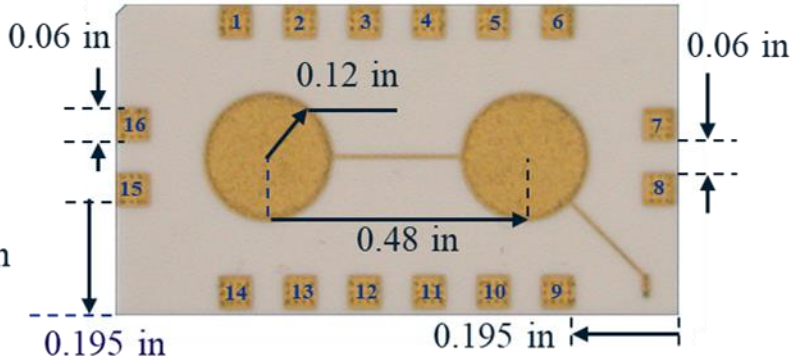
- I-V curve between I/O27 and I/O28
- 500°C
- Wide DC bias range: 0 - 50V
- SMU: integration time 16.67 msec, time delay 0.1 sec
- I/O28 not connected to SiC die, I/O27 connected to isolated two-terminal test structure on SiC die
- Package mounted on PCB
- Slope of linear fits: 7.6 GΩ initially 9.7 GΩ after 69.4 hrs
- DC resistance slightly underestimate
- Noise from running oven

L. Chen, P.G. Neudeck, D.J. Spry, G.M. Beheim, and G.W. Hunter, iMAPS HiTEC, 2016.

16-pin HTCC Package

CF516 Package





- 1.05 in x 0.58 in x 84 mil (thick), with 16 pads
- Fits two of 5 mm x 5mm die, die-attach pads connected to the seal ring
- 30 mil x 45 mil wire-bond pads, ≥ 90 mil spacing
- 60 mil x 60 mil bondpads on the backside, ≥ 60 mil spacing
- Two round shapped mounting pads on the backside
- Pt surfaces plated
- Compatible lid composed of same material sytem
- T ≤ 500°C and 10Hz ≤ f ≤ 1 MHz: C ≤ 2 pF, R ≥ 10 MΩ, DC insolation resistance ≥ 150 M Ω

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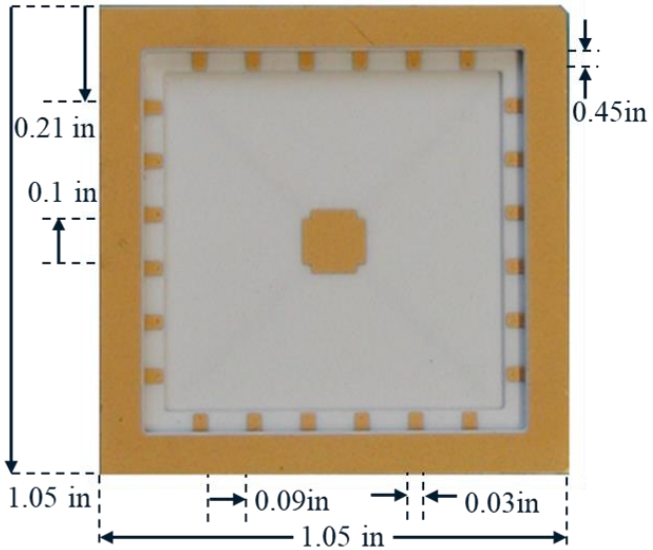
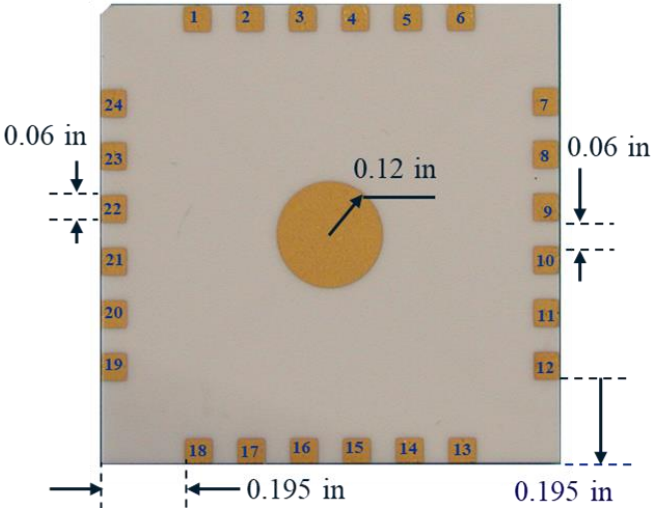
24-pin HTCC Package

CF524 Package





- 1.05 in x 1.05 in x 84 mil (thick), with 24 pads, Au plated
- Fits one 2.4 mm x 2.4mm die
- 30 mil x 45 mil wire-bond pads, $\geq$ 90 mil spacing
- 60 mil x 60 mil bondpads on the back, $\geq$ 60 mil spacing
- A round shapped mounting pads on the backside
- Pt surfaces plated Au
- Compatible lid composed of same material sytem
- $T \leq 500°C$ and $10Hz \leq f \leq 1$ MHz: $C \leq 1$ pF, $R \geq 20$ MΩ, DC insolation resistance ≥ 150 M Ω

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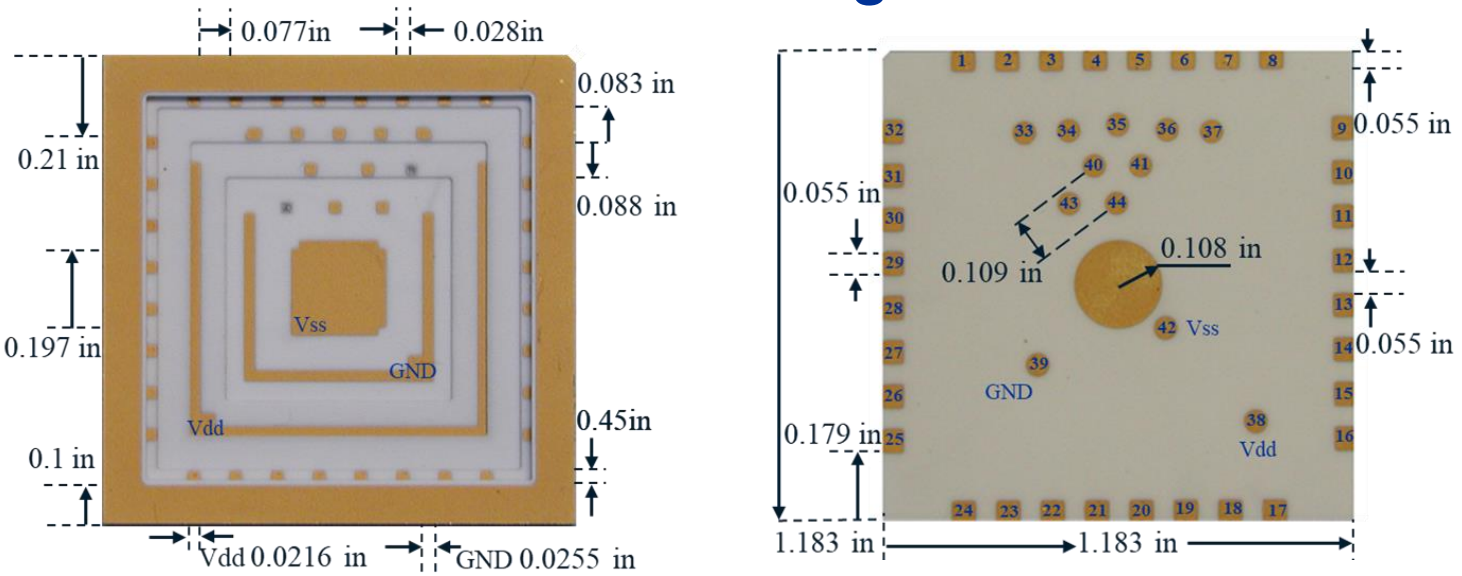
44-pin HTCC Package

CF544 Package



- 1.18 in x 1.18 in x 84 mil (thick), with 44 pads
- Fits one 5 mm x 5mm die
- 27.5 mil x 27.5 mil wire-bond pads, ≥ 77 mil spacing along edges and over 62 mil horozontal spacing between array pads
- 55 mil x 55 mil bondpads on the back, ≥ 55 mil spacing
- Traces for consollidated Vss, Ground, Vdd connections. Ground connected to the seal ring
- Array type of pads for overall package dimension control and mitigation of parasitic effect
- Compatible lid composed of same material system
- T ≤ 500°C and 10Hz ≤ f ≤ 1 MHz: C ≤ 2 pF, R ≥ 20 MΩ, DC insolation resistance ≥ 150 M Ω

L. Chen, P.G. Neudeck, D.J. Spry, and G.W. Hunter, iMAPS HiTEC 2022.

500°C Conductive Die Attachment

Au Paste Based Conductive Die-attach

- In-house processed commercial Au paste
  - DuPont 5063D Au paste
  - Improved viscosity by drain 10-15% organic carrier, by solid particles precipitated or using a centrifuge
- Die-attach Process
  - Pt die-attach pad plated with Au thin-film
  - SiC IC die backside with thin film Au
  - Stamping or micro-dispensing DuPont 5063D on die-attach pad
  - While the Au paste is wet, the IC die picked up and paced onto the wet Au paste pad
  - Dried at 150°C for 15-20 min, cured at 600°C for 2-3 hours in air with a box oven, with ramp rate of 3°C/min
  - Naturally cool down after curing
  - The optimal thickness of cured 5063D layer between IC die and the die-attach pad is ~ 30μm

Au Wire-bonding for 500°C Operation

Wire Bonding

Wire material

- Electro-migration issue of conductors under electrical bias at high temperature
- 1 mil diameter 98% pure Au wire from K&S Wire
- Impurities in Au wire diffuse to surface at high temperature and form oxides and stay
- Surface-oxide layer slows down electro-migration process

Wire-bonding process

- Thermo-sonic ball-wedge bonding, normal bonding parameters
- Ball bond first on Pt/Au surfaces of bond pads on SiC ICs (T=150°C)
- Second wedge bond on Au thick-film pads of packages (T=150°C)

Wire annealing

- Electro-migration occurs under electrical bias and high temperature
- A gradual process
- High temperature exposure during high temperature (500°C) test of packaged device

Au Wire-bonding for 500°C Operation

Component / Wire Attachment to Circuit Board

Wire material

- Pure Au wire with 10 mil diameter for board level I/Os
- Connecting the board to instruments outside oven

Bond pad on board and attaching wire

- Co-fired Pt pads on HTCC package, coated with DuPont 5063D, fired at 850°C in air
- Coated both Au wire and precoated Au/Pt pad with preprocesses DuPont 5063D (same as for die-attach)
- Lay the wire with wet Au paste onto the bond-pad with wet Au paste

Heat process

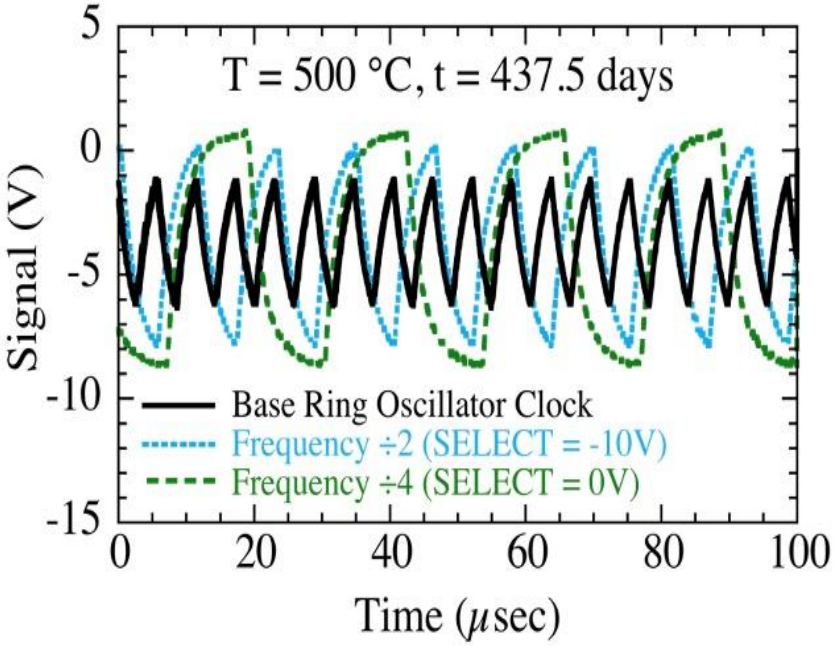
- The assembly dried at 150°C for 15 min in air
- Cured at 850°C for 20 min in air to solidify the Au paste
- The oven naturally cooled

Extending attached short Au wires with foot long wires with fiber glass sleeve

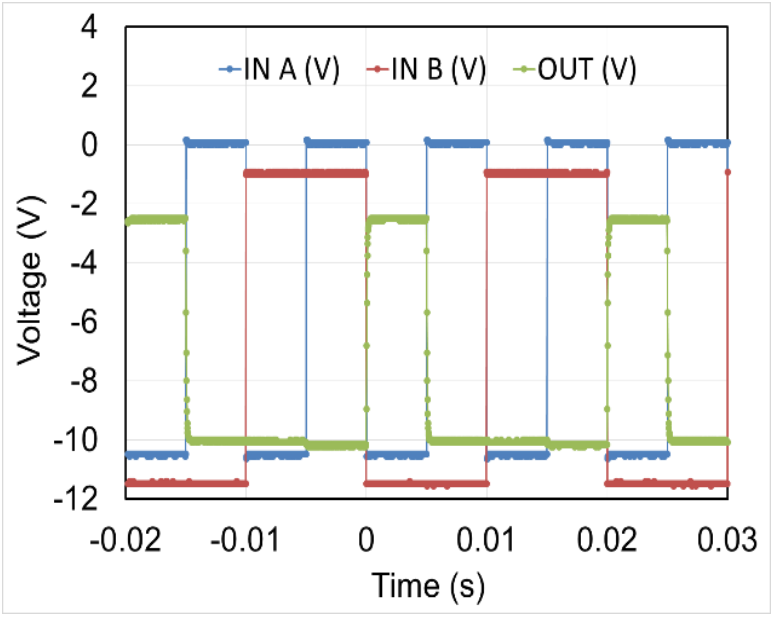
Components: Packages attached the same way with Au paste applied to the Au/Pt metallization pads on both packages and board, then heat treated

Test Results of Packaged SiC ICs at 500°C and 700°C

Test Data of Packaged SiC ICs



Output waveforms of a packaged SiC JFET ÷2/÷4 Clock IC waveforms recorded at 437.5 days of 500 °C testing.

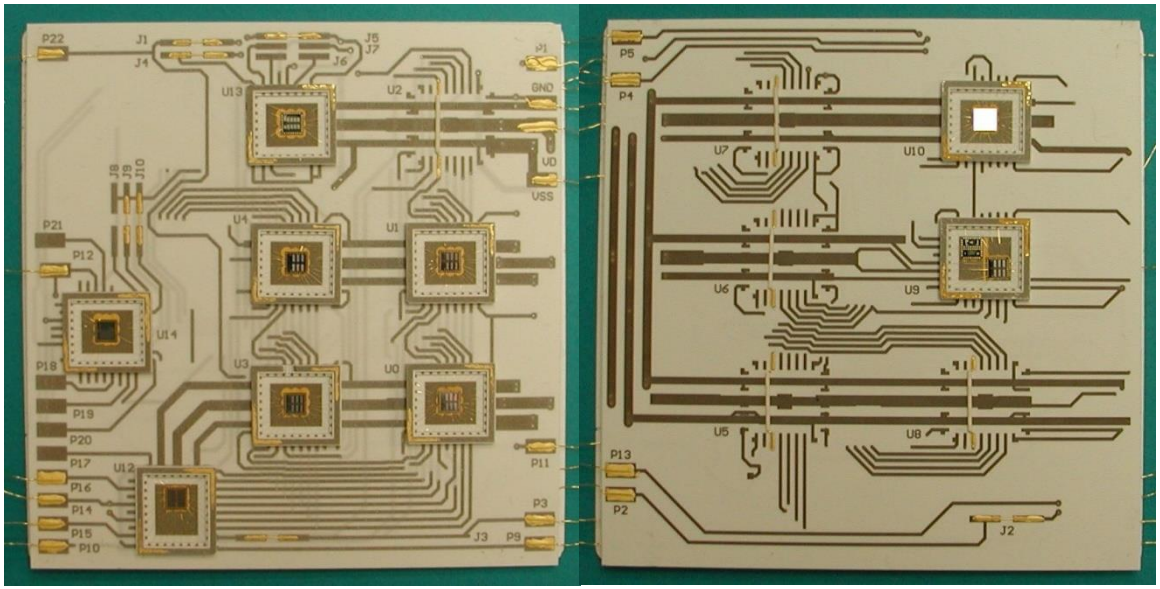


Inputs and output waveforms of a packaged SiC two-inputs NOR logic gate, recorded at 700 °C after 143.5 hours test. Input B is shifted -1 V to avoid overlapping.

Neudeck, et al, iMAPS JMEP, October 2018.

Double sided multilayer circuit board with multiple chips integrated

Double-sided Multilayers HTCC Circuit Board



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- 4.5 in x 4.4 in HTCC alumina circuit board with four layers of conductor
- Pt surface metallization, and hermetic Pt via
- Nine packages with total of ten SiC IC chips integrated on the board
- I/O wires and jumpers attached
- Examined at room temperature, tested in simulated Venus environment

* P.G. Neudeck, D.J. Spry, M. Krasowski, L. Chen, 80th Device Research Conference 2022

Packaging Sequence Discussion

Packaging Sequence

1. Circuit board assembly

- I/O Wires attachment
  - Au thick-film paste fired at 850°C
- Packages attachment
  - Au thick-film paste fired at 850°C same as wire attachment

Both I/O wire and package attachment need 850°C heating, in order to avoid unnecessary exposure of SiC ICs to such high temperature, chip-level packaging (die-attach, wire-bonding) accomplished after package-attach step

2. Chip level packaging

- Die-attach using home made paste: 500°C
- 98% Au wire-bonding at 150°C

This sequence order differs from packaging sequence used in mainstream IC packaging and assembly

Lower processing temperatures for package attachment required to adopt mainstream packaging sequence in industry

Summary

- A Pt/HTCC alumina high temperature packaging system demonstrated
- A series of chip-level packages have been designed, fabricated, and characterized
- Both chip-level packages and multilayer circuit board commercially made
- Compatible Au-paste based die-attach developed and tested
- Au-paste based component and Au wire attachment developed and tested
- Packaged SiC JFET ICs tested in 500°C air ambient for 10,000 hours, short term tested in air ambient above 800°C
- Multiple packaged SiC ICs have successfully integrated on a double sided multilayer HTCC circuit board
- Process for attaching package on circuit board to be improved to adopt conventional packaging sequence

Thank You Very Much for Your Attention!

Acknowledgements

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