An Examination of Heavy Ion-Induced Persistent Visual Error Signatures in an Electronic Display Driver Integrated Circuit

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***Abstract*— Heavy ion irradiation of a display driver integrated circuit (DDIC) was performed, and persistent visual error signatures were captured. Based on the heavy ion results, error signatures were localized to configuration registers motivate potential mitigation techniques and observations relating to single event effect susceptibility. DDICs serve as an integral component of integrated display systems that will require the development of single event effects test methodologies in anticipation of extensive use in crewed spacecrafts outside of the Earth's geomagnetic protection.**

***Index Terms*— Electronic Displays, Display Driver Integrated Circuit (DDIC), Organic Light Emitting Diode (OLED), Single Event Effect (SEE), Single Event Upset (SEU), Single Event Functional Interupt (SEFI)**

I. Introduction

THE recent autonomous flight of the Orion spacecraft underscores a renewed interest in sending humans beyond the protection of the Earth's atmosphere and magnetosphere to the lunar surface and beyond. Critical components utilized in space-based applications must reliably operate through a variety of hostile environments such as particle radiation environments comprised of trapped particle belts, solar particle emissions, and galactic cosmic rays [1]. These highly energetic particles interact with materials at the atomic level, temporarily distorting free charge carrier populations that can disrupt complex electronic circuitry. While integrated electronic displays are utilized extensively on the International Space Station and on space tourism vehicles, these applications are intentionally confined to well-shielded spacecraft in low earth orbit altitudes with non-polar orbits. Crewed missions to the lunar surface will subject electronic displays to particle radiation environments without geomagnetic shielding and in some cases with little to no shielding at all (e.g., displays on an unpressurized rovers, surface-based instrumentation, etc.) [2].

The maturation of the commercial electronic display market sector has underpinned the proliferation of systems with integrated electronic displays ranging from small biometric monitors to high resolution command modules. Notionally, an integrated electronic display can be decomposed into a video/image generation element, pixel screen, and a display driver integrated circuit (DDIC) that provides a critical interconnect of image data and the necessary control signals to drive the screen. This functional decomposition emphasizes the lack of existing radiation test data and assessments for DDICs (compared to the upstream video generation elements [3]-[4]) in the radiation effects community that complicates both qualitative (e.g., error signatures) and quantitative (e.g., testing techniques, error rates, etc.) risk assessments for mission critical systems. In anticipation of extensive usage in future crewed missions, preemptive identification of single event effect (SEE) sensitivity of commercially available electronic displays serves to reduces the risk volatility posed by the inclusion of electronic displays in upcoming crewed mission (NASA HEOMD-405 Integrated Exploration Capability Gaps List Tier 1 Gap 02-02).

The complexity of a DDIC in conjunction with a multitude of high throughput output signal channels necessitates a broader system-level SEE assessment methodology utilizing a display screen to natively convert DDIC output signals into a digestible visual output. This assessment methodology introduces challenges with 1) in-situ visual monitoring of a "high" resolution display screen and 2) definition of visual SEE signatures (formally referred to as a single event functional interrupt (SEFI)) that should be considered an error for the purposes of non-destructive rate predictions and mitigation strategies. In service of defining the range of potential radiation-induced failure modes of a generic DDICs a commercially available DDIC driving an OLED screen was monitored for visual error signatures during heavy ion irradiation; error signatures were catalogued, and the likely functional origin identified via instruction set modification. This error signature cataloguing approach facilitates benchtop emulation of error signature for perception-based criticality analysis as well as investigation of potential mitigation techniques. The intention of this manuscript is to socialize the impending need of systems utilizing radiation-tolerant electronic displays, demonstrate a subset of persistent visual error signatures that can be expected from SEEs originating in the DDIC of an electronic display, and examine the potential impact these error signatures have on system design and reliability.

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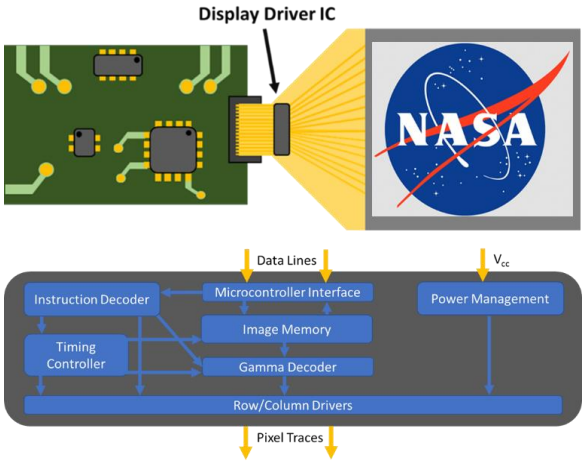

Fig. 1. Notional schematic of display boards and the modifications used in this measurement campaign. The screen containing the individual pixels are attached to an electronic board and DDIC with a flexible tape connector. This allows for "unfolding" the display to provide backside access to the DDIC. A functional diagram of the DDIC is provided for reference.

II. Device Under Test

Notionally, an electronic display sub-pixel can be simplified to a light modulation element (e.g., light emitting diode, liquid crystal, etc.) with a parallel storage capacitor that can be charged during a brief period and used to maintain light modulation even when the subpixel is not actively being driven; a color pixel is constructed from a red, green, and blue subpixel. The illuminance of an individual sub-pixel, and by extension color mixing of a color pixel, is dynamically controlled by the charging duration or orientation of liquid crystals. An electronic display screen would then be a pixel array with individual pixels being indexed by transistors or conductors connected to row and/or column signal traces [5].

A DDIC is responsible for transcribing image information from a video processing element (e.g., FPGA, microcontroller, processor, etc.) into the temporal control signals necessary to drive every sub-pixel of a display screen. Functionally, a display driver consists of a 1) receiver for receiving configuration information and image data, 2) temporary storage for image data, 3) timing controllers, digital-to-analog converters, and gamma correction for generating control signals, and 4) row/column drivers that drive the individual sub-pixels of the display screen (Fig.1). Oftentimes pixel technologies require voltage higher than typical CMOS voltages and require inclusion of additional power management electronics within an DDIC [6]-[7].

This manuscript focuses on the testing approach and error signature cataloguing of a commercially available CMOS electronic DDIC designed for small form-factor passive matrix OLED manufactured by Solomon Systech (part number SSD1351 [8]). This DDIC is configured to drive a 128x128 OLED display screen with 18-bit color control that requires an 18V output voltage to drive the OLEDs. While the drive capacity of this DDIC would be considered small, it contains the same functional building blocks as larger DDICs and therefore serves as an informative test vehicle for heavy ion-induced error signatures.

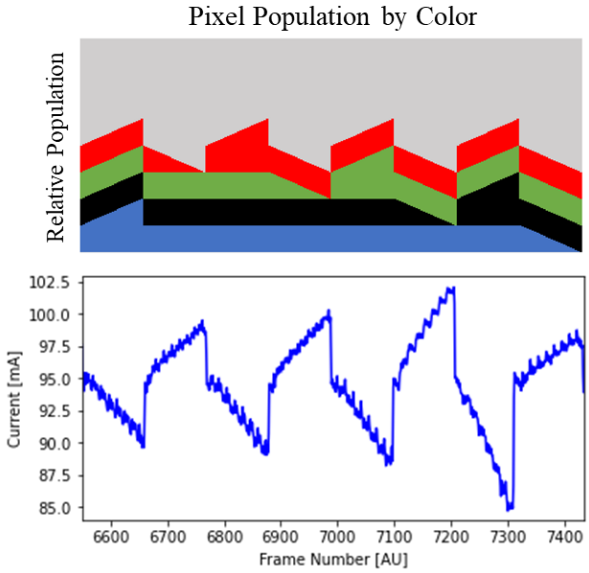

Fig. 2 A pictographic representation of subpixel population as a function of "time" for the test pattern utilized in this work. The simultaneous modulation of two subpixel populations in an emissive electronic display can be monitored via board level monitoring that can be used in test characterization and system-level mitigation techniques.

III. Test Pattern

It is common in emissive electronic displays for each color of subpixel to have unique current contrast value to allow for post-fabrication adjustment of relative pixel intensity for color mixing. Given that the power consumption of emissive displays is predominately driven by light emission in the pixels, the population of each subpixel color illuminated for an on-screen image will be reflected in the board-level current measurements (e.g., white screen requires more current than red screen). Through careful control of subpixel populations via test patterns, distinctive board-level current draw behavior serves an additional mechanism for in-situ monitoring of persistent error states during test campaigns and demonstrates current monitoring of integrated electronic displays as an error indicator for system-level mitigation techniques (Fig. 2).

In-situ monitoring of electronic display screens require periodic test patterns that exercise the full range of display functionality, such as illuminating every subpixel, while maintaining sufficient video integrity from monitoring in less-than-ideal conditions (e.g., off-angle, high zoom, background lighting, etc.). "Movement" of test patterns on screen should be slow compared to the frame rate of the monitoring camera to reduce the impact of visual artifacts created from facility noise and aliasing induced by the mismatch of camera frame rate and pixel refresh rate. For current monitoring at the board level, the modulation of subpixel populations should occur at a rate and quantity that that is resolvable by the electrical measurement setup.

The test pattern utilized in this work is constructed from an initial image of eight equally sized contiguous regions of pixels (red, green, blue, black and four white rectangles) that begin to slowly move toward the bottom of the screen. To modulate the population of subpixels in the test pattern, the region at the top of the screen is slowly extended while the region at the bottom of the screen is slowly truncated until the region at the bottom

completely disappears and appears at the top returning the screen to the equally sized contiguous regions (Fig. 3). This implementation creates a unique current signature with periods of current increase/decrease (associated with increasing /decreasing population of white pixels) with the total current change further impacted by the population modulation of the red, blue, green, and black pixels as each requires distinct current draw for emission.

IV. Testing Approach

This irradiation campaign focused on the use of small form factor, commercially available electronic displays that could be controlled with external microcontrollers with housing that could be easily modified for testing. The DDIC is located on the thin tape connector between display board and the display screen allowing for manipulation of the electronic display such that the backside of the driver IC has a direct line-of-sight to the ion beam while still allowing in-situ visual monitoring of the display screen with a camera located safely to the side of the beam. To ensure that errors can be isolated to the DDICs, the other on-board support electronics were left untouched in traditional part packaging (i.e., insufficient ion range) and the microcontroller was located away from the ion beam. The electronic display board and microcontroller were powered and monitored via individual power supply channels with a sample time on the order of 50 ms.

Heavy ion irradiation was performed in air at Lawrence-Berkely National Laboratory utilizing the 16 MeV/amu ion cocktail with an ion species of Neon (surface incident linear energy transfer of 1.2 MeV·cm^2/mg) to maximize particle range through the driver die [9]-[10]. A microcontroller was used to initialize the display driver (prior to irradiation) and then display a periodic test pattern that can be monitored for visual error signatures during irradiation. The visual test pattern is described in detail in the previous section. While this test pattern is simple, it allows for visual monitoring of a wide variety of radiation-induced error modes in the DDIC operation such as color mixing/saturation, memory-to-pixel mappings, and control states (e.g., idle, black/white, locked) [11]-[12].

Once a persistent visual error is identified the beam can be shuttered and the electronic display board and/or microcontroller can be power cycled remotely via their respective power supply channels to reinitialize the display and clear the error. Following a reset, the microcontroller performs an initialization routine that writes control data to the internal driver IC configuration registers before entering a perpetual routine to generate individual frames that are transmitted to the driver IC and stored in the internal memory (Fig. 4). Critically, this pseudo-code description emphasizes that 1) configuration bits within the driver IC are not being maintained by the microcontroller during irradiation and 2) the driver IC is not responsible for any computation for constructing a frame image to be displayed. Since the microcontroller is not being irradiated, any identified error should be evaluated from the perspective of erroneous display function (e.g., the loss of color, image orientation, etc.) rather than an error in the image generation process.

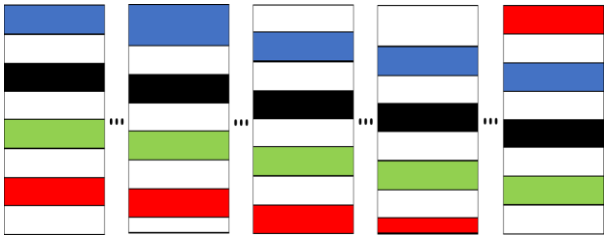

Fig. 3. A pictographic representation of the test pattern used during irradiation. The color bars slowly scroll down the display and simultaneously modulate the subpixel populations of the regions at the top and bottom of the electronic display screen.

Algorithm 1: Microcontroller Test Routine

```
//Configuration Register Initialization
ConfigBits ← ScreenResolution;
ConfigBits ← RefreshRate;
...
InitalizeDDIC(ConfigBits);

while True do
    BlueVertices ← ModUpdateVert(BlueVertices, dt, Width);
    GreenVertices ← ModUpdateVert(GreenVertices, dt, Width);
    RedVertices ← ModUpdateVert(RedVertices, dt, Width);
    BlackVertices ← ModUpdateVert(BlackVertices, dt, Width);
    WhiteVertices1 ← ModUpdateVert(WhiteVertices1, dt, Width);
    WhiteVertices2 ← ModUpdateVert(WhiteVertices2, dt, Width);
    WhiteVertices3 ← ModUpdateVert(WhiteVertices3, dt, Width);
    WhiteVertices4 ← ModUpdateVert(WhiteVertices4, dt, Width);

    ImageArray ← ConstructImage(UpdatedVertices);
    TransmitToDDIC(ImageArray);
    SleepUntilNextUpdate(dt);
end
```

Fig. 4. Pseudocode of the microcontroller routines used to generate the test pattern. Note that configuration register initialization occurs once at the start of the test routine at microcontroller reset.

V. Results

Due to the complexity of DDICs it is germane to outline potential non-destructive SEE sensitivities (CMOS technology implies potential destructive latch-up sensitivity) and how that would be perceived as the optical output of the electronic display. The most natural way to access the criticality of SEEs is to understand how long the SEE should persist; temporary SEEs are expected to occur in the row/column drivers and the temporary memory that holds the image that is to be displayed. The charge associated with single event transients that coincide with the control signals governing the charging of sub-pixels would produce a change in luminosity and color mixing of a pixel for a single frame (e.g., flickering pixel). Single event upsets (SEUs) in a memory cell of the image memory results in an error in the associated pixel in successive frames until a pristine image is written to the image memory. In contrast, visual errors resulting from SEUs in configuration registers are likely to persist until the registers are updated (often during power cycles).

From a mission concept-of-operations perspective, it is unlikely that temporary distortions in individual pixels during nominal operation (i.e., periodic image and frame updating) would be considered an error requiring intervention. Therefore, this work focuses on cataloguing persistent visual error signatures that require intervention and could result in a non-trivial impact on the system availability. Figure 5 provides a variety of persistent visual error signatures that were observed during irradiation; each state persisted until the microcontroller was power cycled. It should be noted that while care was taken

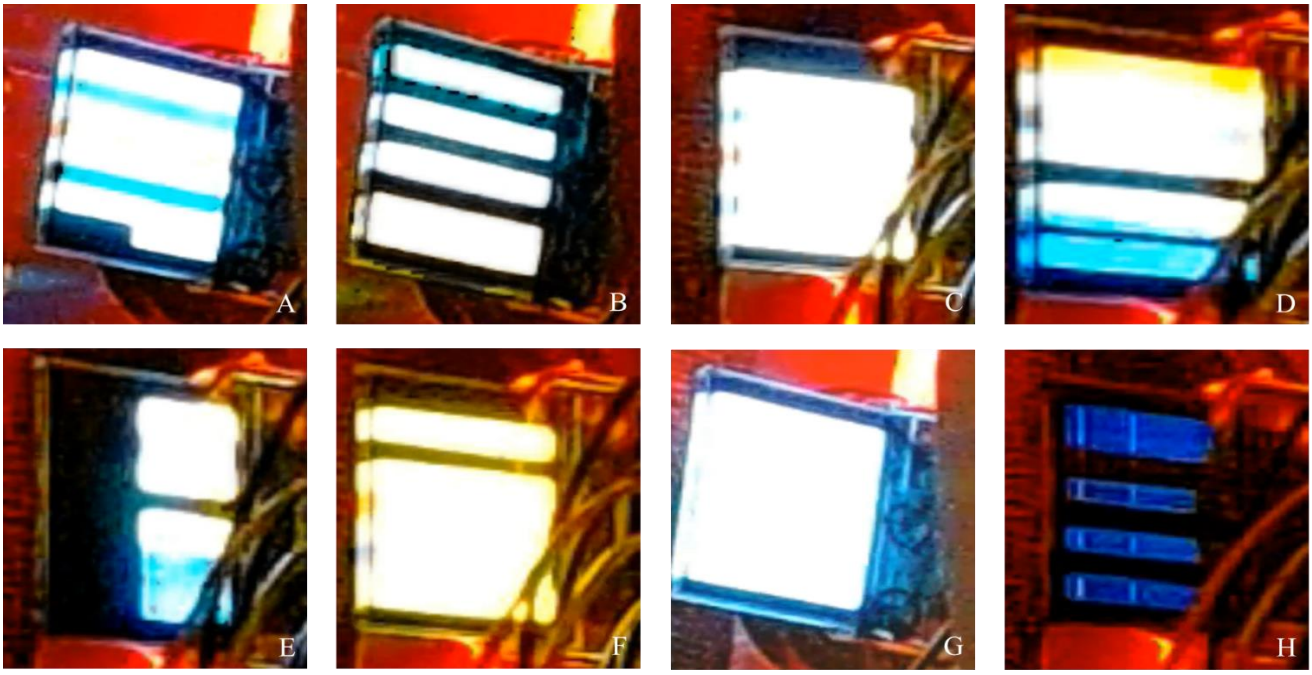

Fig. 5. Examples of persistent visual error signatures: a) loss of control for a subregion of the display screen, b) loss of color (monochrome), c) oversaturation, d) loss of image integrity, e) change in screen resolution, f) incorrect color mixing (decrease in blue light output), g) locked to all white screen, and h) complete loss of image clarity. Note that the image quality was impacted by the red safety lights at the heavy ion facility and color balancing of the web camera.

to clear an error as soon as it was observed to avoid aggregating errors, it is possible that some error signatures are the superposition of multiple error modes.

Utilizing the manufacturer's instruction set intended for microcontrollers interfacing with the DDIC, individual error signatures can potentially be "localized" to a memory register location through a simplified, manual "fault injection" process that reproduces error signatures through command modification [13]. As a demonstration, the errors identified at the test facility were reproduced in a laboratory setting with the compromised configuration registers summarized in Fig. 6. Localization of persistent errors to control registers within the DDIC allows for bench top emulation of error modes for empirical human-based criticality assessment (e.g., shift in display contrast renders the display illegible) for a representative audience.

Error Signature	Command Set
Overall Brightness	Master Contrast Current Control
Changing Color Mixing	Set Contrast Current for Color A,B,C
Inverted Colors	Set Display Mode
Scrolling Direction of Color Bars	Horizontal Scroll
Speed of Scrolling Color Bars	Set Front Clock Divider
Loss of Screen Segment	Set Multiplex Ratio or Set Display Offset
White Screen	Set Display Mode
Black Screen	Set Display Mode or Set Sleep Mode
Static Image	Set Command Lock

Fig. 6. An example table of error signatures and associated instruction set that was used to emulate the error signature on a test bench.

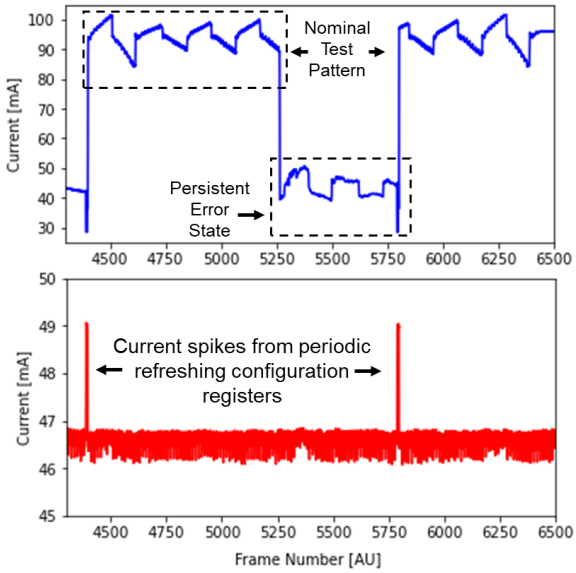

Fig. 7. A demonstration of the capability for a refresh of configuration registers to clear persistent errors. (Top) Board-level current trace that transitions from nominal to locked-state before returning to nominal on configuration refresh. (Bottom) Microcontroller current draw indicating configuration refresh instructions.

VI. Mitigation Considerations

From a system-level perspective, the power cycling of the microcontroller to clear a persistent visual error was equivalent to reinitializing the DDIC control registers as nominal operation implements this routine once prior to entering a control loop. Provided that there is suitable software-level design input, inclusion of a "house-keeping" routine to periodically update control registers to their intended values would "autonomously" clear some error states without requiring manual intervention and incurring additional system downtime. Potential performance penalties from any mitigation software routines could be balanced by tuning the duration between register updates and a maximum duration that a visual error can be tolerated on the display screen.

To demonstrate the potential of autonomously clearing persistent visual error states via manipulation of configuration

registers, a modified microcontroller test routine was implemented that periodically refreshes the configuration registers to pre-irradiation values. Since microcontroller and electronic display board are monitored on individual current channels, the brief increase in the current draw of the microcontroller associated with the writing to the configuration registers of the DDIC can be used to independently indicate when a reconfiguration has occurred in the current draw of the electronic display board. An example of this behavior is provided in Fig. 7 where a screen with nominal behavior erroneously enters a screen disabled/locked state that persists until a refresh of the configuration registers. It should be noted that not all persistent errors were resolved with this methodology and required power cycling to the electronic display board and microcontroller.

Though configuration registers might be thought of 1 or 2-bit registers selecting an operating mode from a small list, it should be noted that quantities like contrast control are many bits long. SEUs in configuration registers responsible for global contrast settings for a single sub pixel will impact both color mixing and total luminosity of a pixel with the significance of these impacts highly dependent upon both the pristine register value and the individual bit that is toggled (example in Fig. 9). An example of this principle for color mixing is provided in Fig. 9-10 where the color range that a white pixel could be perceived following an SEU can be modulated via careful selection of pristine values. This type of color degradation has the potential to be much more significant that radiation-induced degradation of the pixel technologies within the screen [15].

It is worth noting that while this work focuses on testing of a small-form factor electronic display that would be more associated with a resource-constrained system, high resolution and refresh rate displays typically require high performance DDICs and sometimes utilize multiple DDICs concurrently. DDICs operating with shorter clock periods in-turn are likely more susceptible to error states that might be masked in the operation of the driver IC examined in this work while the synchronization of multiple driver ICs likely introduce additional sensitivities that could impact sub-regions of a display.

VII. Conclusion

Given the ubiquity of electronic displays integration in human-based systems, the impending mission critical, space-based applications of electronic displays will necessitate SEE assessment of components unique to electronic displays. A commercially available DDIC designed to drive a small form factor OLED was visual monitored during heavy ion irradiation to catalogue radiation induced persistent visual error signatures that require manual intervention (i.e., power cycling) to return to nominal function. These error signatures were able to be reproduced via modification of configuration register values utilizing the instruction set intended for interfacing a microcontroller with the DDIC. This approach to emulation of heavy-ion induced errors on a table top assists with human perception based criticality analysis as well as development of mitigation techniques.

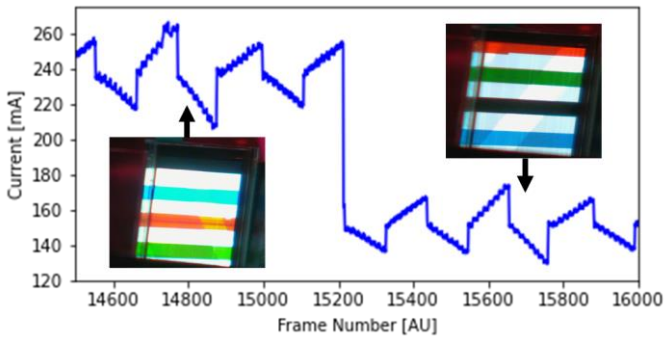

Fig. 8. A demonstration of a heavy-ion induced shift in the master current contrast control in the DDIC. An upset in the 8-bit master current contrast resulted in the total reduction of current used in pixel emission, resulting reduced visual output, and reduced total current draw from board-level current draw. It should be noted the shift in the offset of the current measurements affirm that the upset occurred in the master contrast control registers not in a subpixel contrast control.

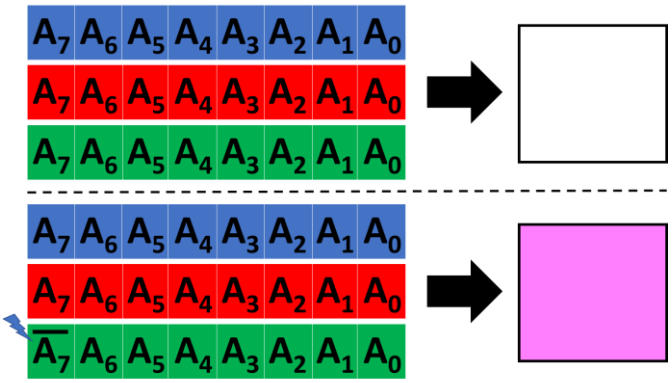

Fig. 9. Pictographic representation of the impact on color mixing of an SEU in a memory register associated with the 8-bit value for sub-pixel luminosity. For this example, the pristine register values were set to 0b11111111 and there was a bit flip in the most significant bit of the register associated with the green subpixel.

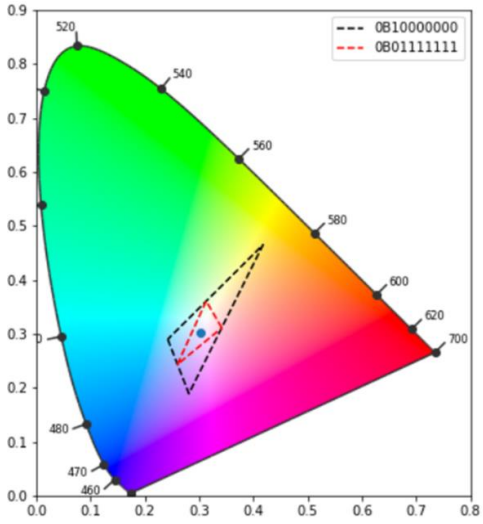

Fig. 10. Color space diagram (CIE 1931 [14]) for demonstrating the range of colors that a pristine white pixel could appear as from a single SEU in a memory register associated with one 8-bit sub-pixel luminosity. The black and red dashed line correspond to a pristine register value of 0b1000000 and 0b01111111 respectively.

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