Technical Primer on Design and SPICE Modeling of Circuits for NASA Glenn SiC JFET IC Generation 13 Prototype Wafer Run Part 1: SiC JFET Behavior and SPICE Modeling

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Version 3 (Major Update): October 2023 based upon Secondary Ion Mass Spectroscopy (SIMS) measurements conducted upon IC Gen. 13 prototype wafer.

THIS VERSION SUPERCEDES/REPLACES prior versions of IC Generation 13 JFET SPICE Modeling Technical Primers (that 2023 SIMS results indicate are significantly less accurate).

Outline

Goal: Enable anyone to SPICE-model and design 500 °C durable integrated circuits for their intended application.

IC Technology Overview:

- SiC n-channel JFETs
- SiC n-channel Resistors

Part 1: SiC JFET Behavior and SPICE Modeling

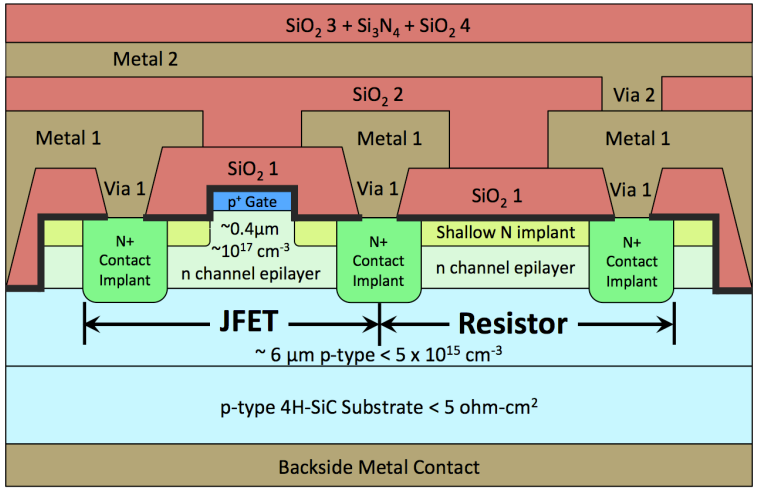
Part 2: SiC Resistor Behavior and SPICE Modeling (separate presentation)

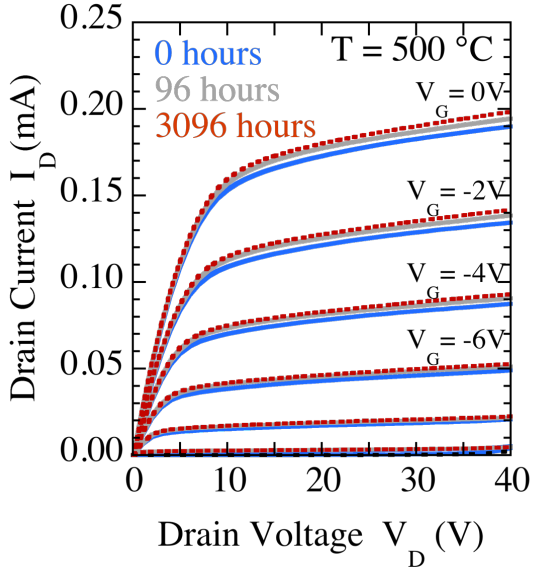
NOTE: Background information in web links provided in these presentations are key to technology understanding.

Device Approach

Most applications require long-term circuit operation.

SiC n-JFETs and n-resistors offer the highest durability and stability for long-term circuit operation at T ≥ 500 °C.





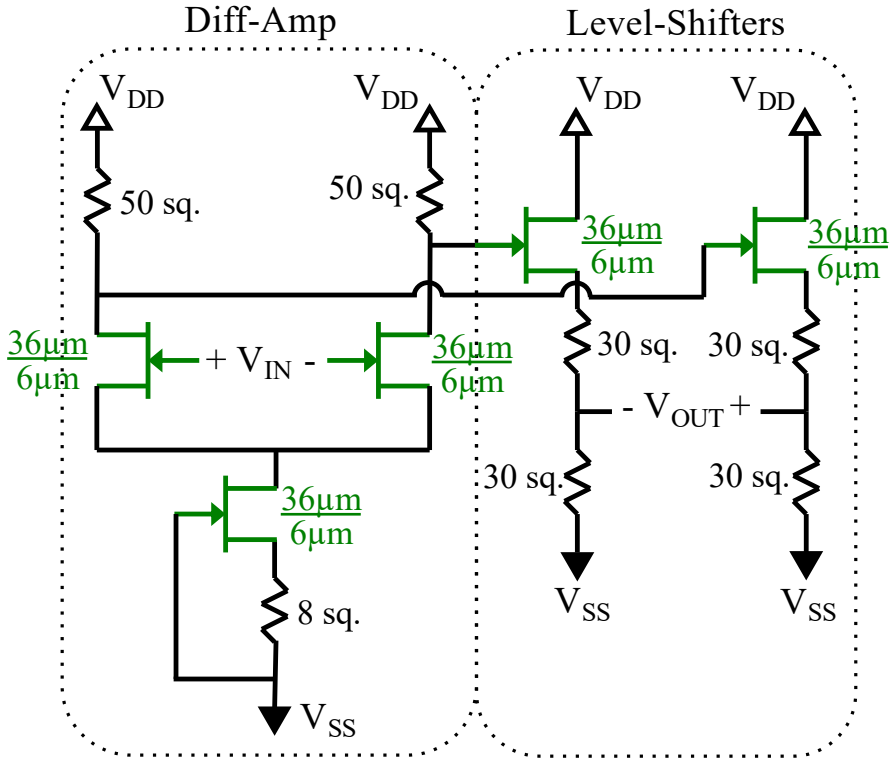
Other device structures and materials have yet to demonstrate 1000+ hours of 500 °C stable electrical operation.

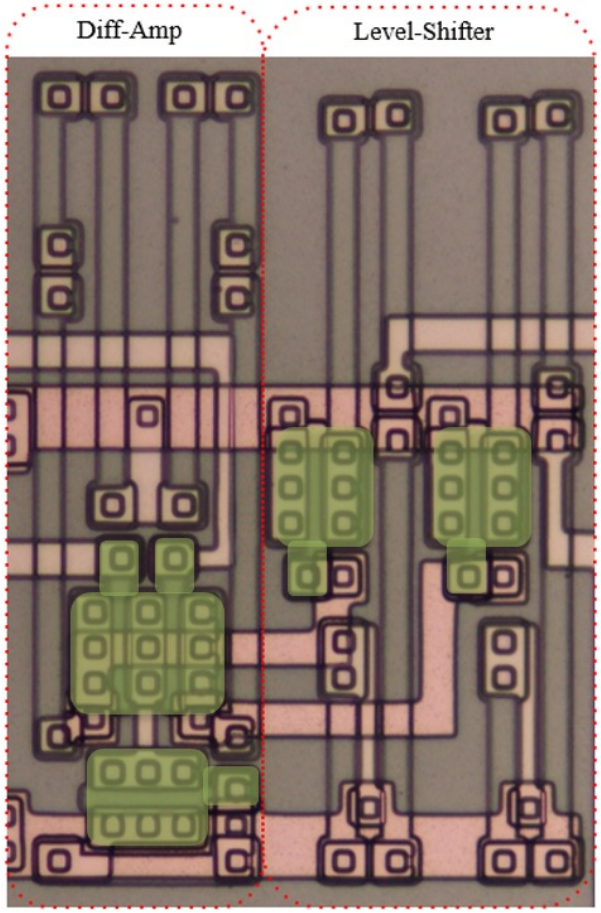
See: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180003391.pdf

Circuit Approach

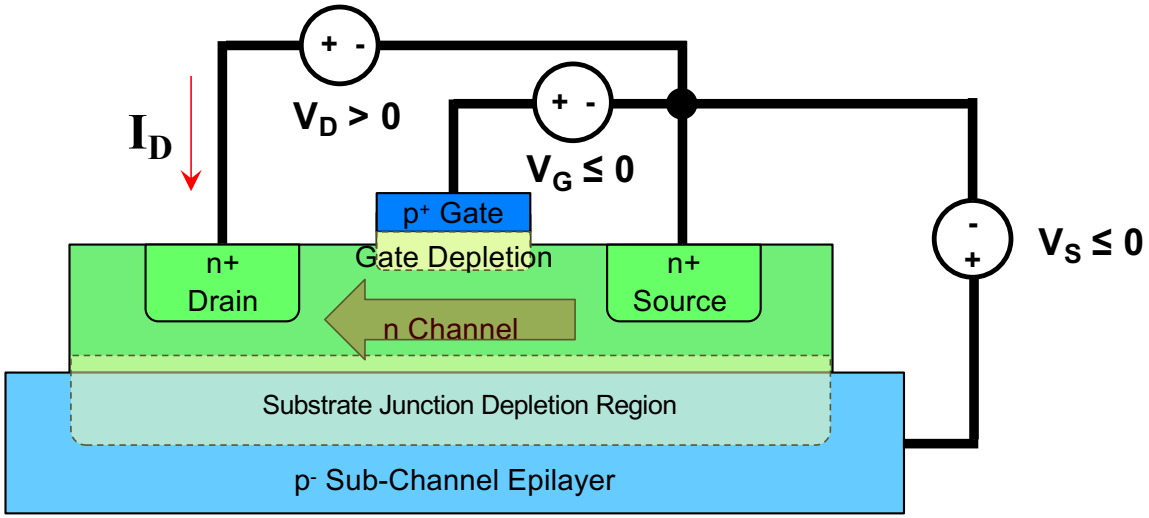
See: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014879.pdf

All integrated circuits in this project are comprised of interconnected 4H-SiC n-JFET's and 4H-SiC n-resistors.





N-Channel JFET Bias Limitations



N-channel electron current flow from Source to Drain is modulated by Gate voltage V_G.

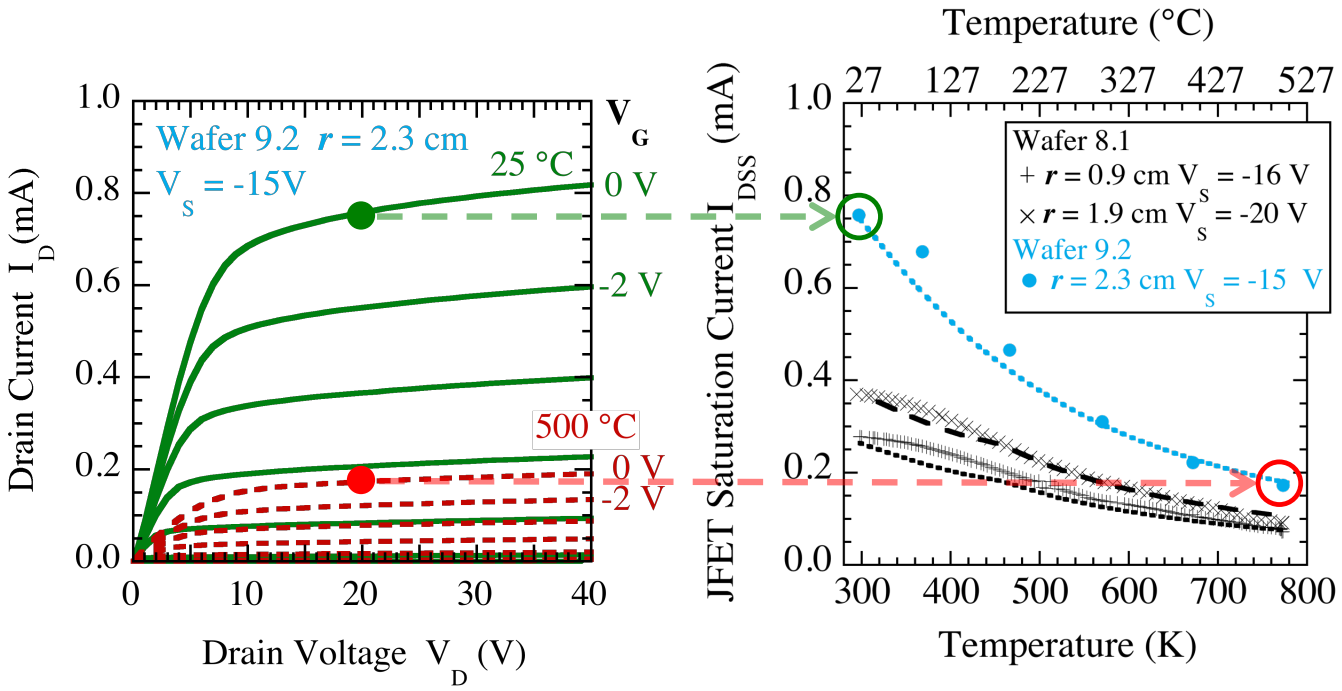
Forward bias of gate pn junction and substrate pn junction is to be avoided.

- Keeps desired signal currents confined/isolated to n-channel.

JFETs are "normally ON" - n-channel is "on" to current flow at $V_G = 0$ V.

- JFET "turn-off" requires application of $V_G \leq V_T$ "Threshold Voltage" < 0 V.
- N-channel epilayer control is not yet sufficient for "normally OFF" JFET approach
- $V_S < 0$ is needed to guarantee substrate pn junction reversed bias in all circuits.
  - Impacts JFET current-voltage characteristics through "body bias effect"
  - See: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160005307.pdf

SiC JFET Dependence on Temperature



Significant change in JFET parameters with increasing T, consistent with prior works.

- Some channel mobility loss offset by more negative JFET threshold voltage.

See: https://ntrs.nasa.gov/api/citations/20160014886/downloads/20160014886.pdf

IC Gen. 13 JFET Epilayer Specifications vs SIMS Profile Measurements

JFET n-channel epilayer measured by SIMS is thinner than specification but remains functionally acceptable.

- Reduces integrated circuit power supply VDD and VSS voltages to less than 10 V.

JFET n-channel epilayer measured by SIMS is uniform in both doping and thickness.

- *Eliminates changing JFET SPICE models as function of radial wafer position r, simplifies circuit design/simulation.*
- Mitigates electrical chip matching challenges during multi-chip circuit board construction.

Description of epilayer structure in IC Gen. 13 wafer procurement specifications:

On the front of each wafer, there shall be the following singe-crystal homoepitaxial SiC epilayers, specified and verified by secondary ion mass spectroscopy (SIMS) analysis.

(Layer #1) Deposited on top of the wafer substrate, a p-type aluminum-doped homoepitiaxial SiC layer of 2 x 10^{18} cm^{-3} ± 1.0 x 10^{18} cm^{-3} of 4.0 ± 1 micrometers thickness.

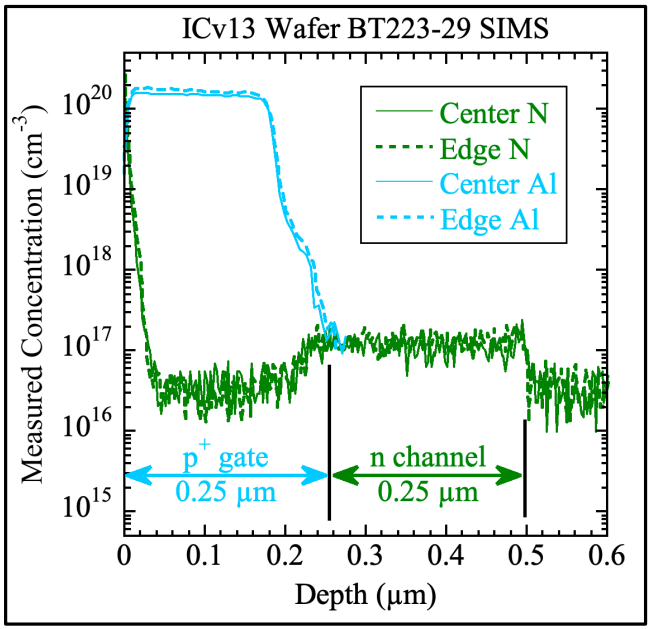
(Layer #2) Deposited on top of the Layer #1 p-layer described above, a p-type homoepitaxial SiC layer of less than 5 x 10^{15} cm^{-3} of 6.0 ± 1 micrometers thickness. Lower doping is desired on a "best effort" basis, but the entire layer shall remain of p-type conductivity.

(Transition Layer) Deposited on top of the Layer #2 described above, a doping transition layer from the p-type doping achieved in Layer #2 to the n-type doping described for Layer #3 below. The doping of this transition layer shall not anywhere exceed the n-type doping described for Layer #3 below anywhere in or between Layers #2 and #3. The thickness of this transition layer shall not exceed 0.04 µm in thickness, and smaller thickness is desired so long as the doping specification described above is met.

(Layer #3) Deposited on top of the Transition Layer described above, an n-type homoepitaxial SiC layer of **9.0 x 10^{16} cm^{-3} ± 2 x 10^{16} cm^{-3} of 0.35 ± 0.05 micrometers thickness.**

(Layer #4) Deposited on top of the Layer #3, a p-type homoepitaxial SiC layer of greater than **1.7 x 10^{18} cm^{-3} of 0.05 ± 0.02 micrometers thickness.**

(Layer #5) Deposited on top of the Layer #4, a p-type homoepitaxial SiC layer of greater than **1.0 x 10^{20} cm^{-3} of 0.2 ± 0.02 micrometers thickness**. Higher doping is desired (up to 1 x 10^{21} cm^{-3}) on a "best effort" basis.



NASA Glenn SiC JFET SPICE Modeling Approach

Many different SPICE versions and enhancements are available, but most share “baseline” features and device models from original SPICE version (developed at UC Berkeley).

However, baseline version SPICE JFET model **DOES NOT include body bias effect** that significantly impacts electrical behavior of NASA-implemented IC devices.

Baseline SPICE NMOS LEVEL 1 model (n-channel MOSFET, that includes body effect via SPICE model parameter GAMMA) is therefore employed to model SiC JFET’s to first-order accuracy PROVIDED:

- Forward bias IS AVOIDED for gate and substrate pn junctions.
- Wafer substrate bias voltage (body bias effect) is connected to all devices.
- Situationally correct SPICE JFET (and resistor) models & parameters are employed.

Handle JFET temperature by selecting the corresponding JFET SPICE model (from the table on the next slide).

- DO NOT change the SPICE TEMP (temperature) parameter from its default value (of 27 °C).
- NASA Glenn uses “.include” SPICE statement to load the corresponding SPICE model file from the “ICv13Models” folder.

Estimated SPICE Models for NASA Glenn IC Generation 13 JFETs

(October 2023 update based upon measured SIMS profiles of IC Gen. 13 epiwafers)

Below models are ESTIMATED via 1-dimensional calculations, they are NOT exact and NOT proven.

- Generation13 IC technology is not yet experimentally implemented or electrically characterized.

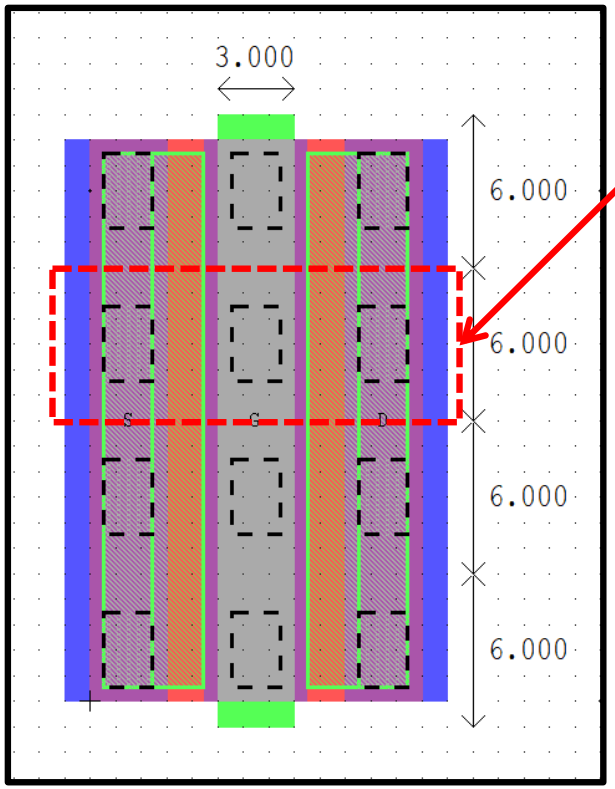
T	SPICE Model for IC Gen. 13 JFETs (3rd Revision, October 2023)
25 °C	.MODEL JFETModel NMOS LEVEL=1 VTO=-2.886 KP=1.310E-5 GAMMA=0.4771 LAMBDA=0.0200 RSH=0.000E+0 CJ=5.962E-5 PB=2.868 CGDO=7.671E-10 CGSO=7.671E-10 JS=0.00E+0 PHI=1.434 RD=1603 RS=1603
460 °C	.MODEL JFETModel NMOS LEVEL=1 VTO=-3.411 KP=3.075E-6 GAMMA=0.4771 LAMBDA=0.0200 RSH=0.000E+0 CJ=7.022E-5 PB=2.067 CGDO=8.186E-10 CGSO=8.186E-10 JS=0.00E+0 PHI=1.034 RD=2981 RS=2981
500 °C	.MODEL JFETModel NMOS LEVEL=1 VTO=-3.465 KP=2.782E-6 GAMMA=0.4771 LAMBDA=0.0200 RSH=0.000E+0 CJ=7.158E-5 PB=1.990 CGDO=8.245E-10 CGSO=8.245E-10 JS=0.00E+0 PHI=0.995 RD=3159 RS=3159
800 °C	.MODEL JFETModel NMOS LEVEL=1 VTO=-3.906 KP=1.490E-6 GAMMA=0.4771 LAMBDA=0.0200 RSH=0.000E+0 CJ=8.562E-5 PB=1.390 CGDO=8.761E-10 CGSO=8.761E-10 JS=0.00E+0 PHI=0.695 RD=4739 RS=4739

The above SPICE models apply across the entire wafer.

Differing SPICE models as function of wafer position ARE NO LONGER REQUIRED for IC Gen. 13, thanks to improved epilayer uniformity (revealed/measured in 2023 by SIMS).

Instancing JFETs

Layout Drawing of M=4
L_G=3µm, W_G=22µm SiC JFET



All JFETs in NASA Glenn Generation 13 IC process have gate length L_G = 3 µm

Gate width W_G is effectively *approximated* by:

W_G = M * 6µm (M = Integer)

SPICE models represent a "Unit Cell JFET" of gate dimensions W_G = 6 µm / L_G = 3 µm

Larger JFETs (such as W_G = 22 µm / L_G = 3 µm depicted) must be approximated using SPICE parallel instance parameter M (such as M = 4 for this JFET).

Example SPICE text instance (of depicted device):

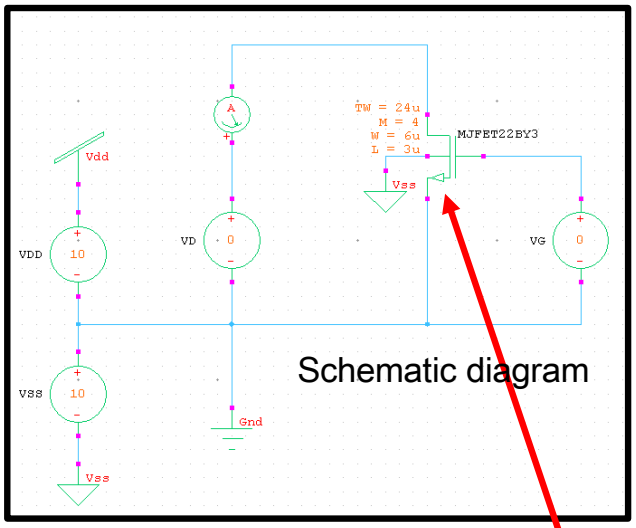
MJFET22BY3 D G S B JFETModel L=3u W=6u AS=39p AD=39p **M=4**

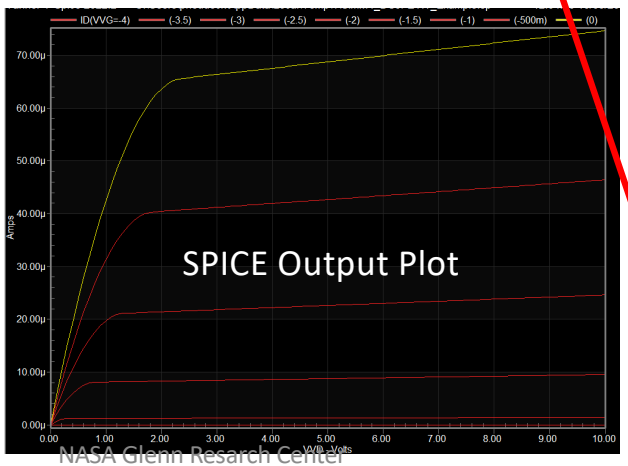
For correct Version 13 SPICE modeling:

- **ONLY CHANGE M**
- **NEVER CHANGE L OR W from values shown above.**
  - **Changing W instead of M will lead to incorrect SPICE simulations (due to incorrect accounting of device contact resistances).**

Example SPICE Simulation of SiC JFET I-V Characteristics

Simulation of a W=22um x L=3um SiC JFET (layout depicted in previous slide) at T=460 °C



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*SPICE Simulation of SiC JFET DC Drain I-V Characteristics
.INCLUDE "..\ICv13_Models\ICv13Models_460C.txt"
MMJFET22BY3 N_2 N_3 Gnd Vss JFETModel W=6u L=3u M=4 AS=39p PS=36u AD=39p PD=36u
VVD N_1 Gnd DC 0
VVDD Vdd Gnd DC 10
VVG N_3 Gnd DC 0
VVSS Gnd Vss DC 10
VID N_1 N_2 0v
.PRINT DC ID=I(VID)
.DC VVD INCR 0.1 0 10 SWEEP VVG INCR -0.5 0 -4
.end
```

Included "**ICv13Models_460C.txt**" file (same "JFETModel" from 2nd row of slide 9):

```
*SPICE Models for NASA JFET IC Generation 13 T=733.0 K (460.0 C).
.MODEL JFETModel NMOS LEVEL=1 VTO=-3.411 KP=3.075E-6 GAMMA=0.4771 LAMBDA=0.0200 RSH=0.000E+0
CJ=7.022E-5 PB=2.067 CGDO=8.186E-10 CGSO=8.186E-10 JS=0.00E+0 PHI=1.034 RD=2981 RS=2981
.MODEL RSheetModel R RSH=1.289E+4
.MODEL RBodyBiasModel  NMOS LEVEL=1 VTO=-182.167 KP=4.258E-7 CJ=7.033E-5 PB=2.056 PHI=1.028
RSH=0.000E+0 GAMMA=1.00E-12 RS=333 RD=333 JS=1.00E-25
.MODEL RSourceImplant R RSH=607.0
```

The FET body/bulk terminal is always connected to VSS supply!

- This accurately reflects the way FETs are employed in NASA Glenn SiC JFET ICs.
- JFET I-V characteristics change with body/bulk substrate bias.

Key Online Technical References

Yearlong 500 °C Operational Demonstration of Up-Scaled 4H-SiC JFET Integrated Circuits (2018):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180003391.pdf
Presentation: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20190001885.pdf

Processing and Characterization of Thousand-Hour 500 °C Durable 4H-SiC JFET Integrated Circuits (2016):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014879.pdf
Presentation: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170001674.pdf

First-Order SPICE Modeling of Extreme-Temperature 4H-SiC JFET Integrated Circuits (2016):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014886.pdf

Experimental and Theoretical Study of 4H-SiC JFET Threshold Voltage Body Bias Effect from 25 °C to 500 °C (2016):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160005307.pdf

Inclusion of Body Bias Effect in SPICE Modeling of 4H-SiC Integrated Circuit Resistors (2018):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180000657.pdf
Poster Presentation: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170009460.pdf