Power Hibernation for Low-Cost Solar Powered Lunar Missions

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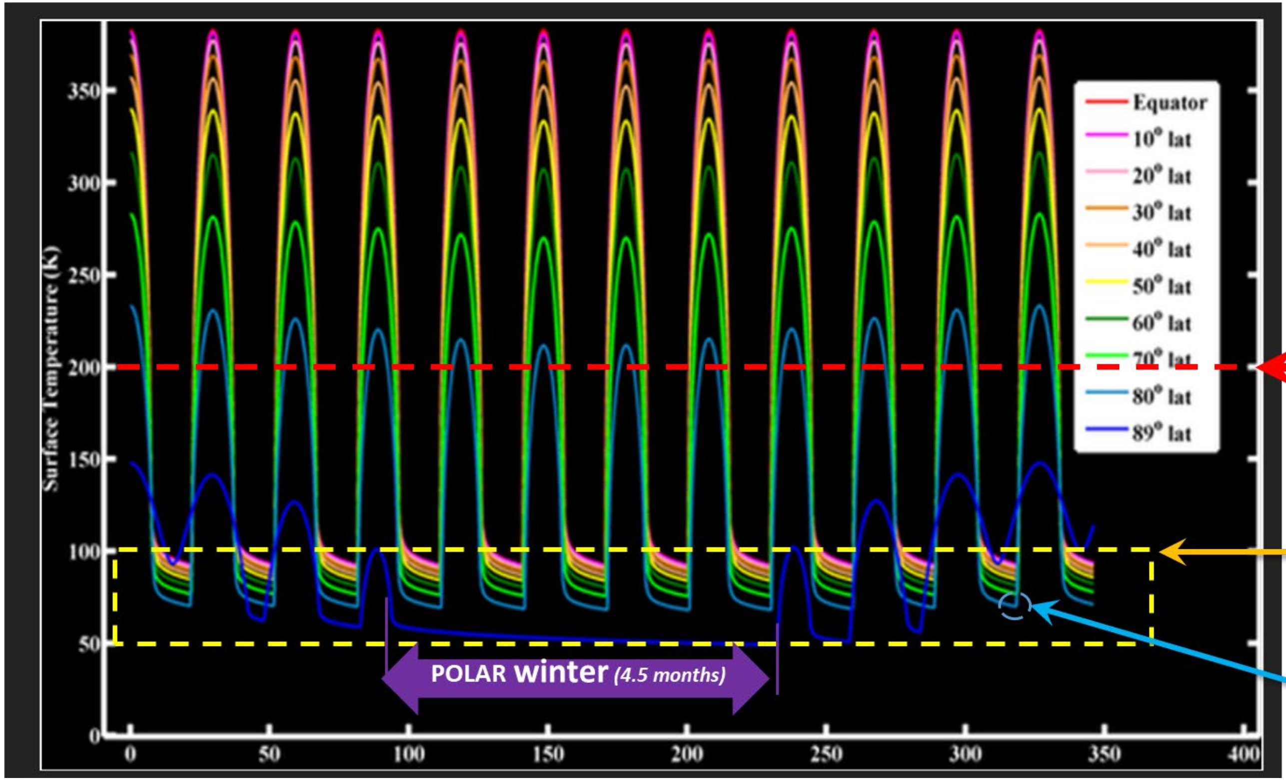
Lunar Environment

LRO DIVINER: Lunar Day/Night Temperature Range by Latitude

Thermal model calculations of monthly & annual lunar surface temperature variations at various latitudes



- **Day**: 150-400 K highs based on latitude
- **Night**: 50-100 K lows *all latitudes*

  Duration (non-polar): ~354 hrs (~14.75 Earth days)
- **Lunar Polar Winter:** Sun is below horizon for ~4.5 months

Li-ion battery approx. freeze temperature

Lunar night is extremely cold *everywhere*

Lunar dawn

Lunar Power Hibernation Approach

Aimed at low-cost solar powered spacecraft (CLPS missions)

- CLPS = Commercial Lunar Payload Services
- Low-cost missions & short development cycle
- Nuclear and Radioisotope solutions out of reach

Intended to extend the missions beyond a single lunar cycle

- Passively surviving the lunar night
- Reactivate power at lunar dawn
- Progressively restore full functions

Hibernation minimizes design impact on existing spacecraft

- Enables multiple lunar cycles while minimizing redesign and development costs
- Changes are limited to the main bus of the power system
- Minimizes the impact on system size and payload capacity

Lunar Power Hibernation Approach

Hibernation is *Enabled* by a Li-ion cell's demonstrated ability to survive extreme cold

- Early test results indicating that Li-Ion 18650 cells tolerate freeze/thaw cycle
- 18650 cell is widely used for both small and large spacecraft batteries.
- NASA procures 18650 in lots of tens of thousands.
- Highly controlled sourcing and chain of custody.

Tests Demonstrated

- Voltage drops to zero when frozen ~200K (-73°C)
- Cells tested to 77K (-196°C)
- Recovers its state-of-charge (SOC) when returned to normal temperatures
- May also be applicable to similar cylindrical formats (21700, 22700, 26650, etc.)

Lunar Power Hibernation Approach

Cryo-Tolerant Batteries for Hibernation

Prior cryogenic 18650 tests raised a number of questions

- How many freeze/thaw cycles can be tolerated?
- What are potential degradation mechanisms?
- Why do cells survive despite dire expectations?
- Can they tolerate 50K (-223°C)

Cell Technology

- Need a thorough characterization of the Li-Ion cell freeze/thaw process
- Electro-chemical and thermal-mechanical characterization and modelling

Battery Development

- Will need thermal management
- In-flight cell management and diagnostics
- Detection of faults (if possible while in the frozen state)

Lunar Power Hibernation Approach

Dawn Recovery from Hibernation is enabled by Cryo-Electronics

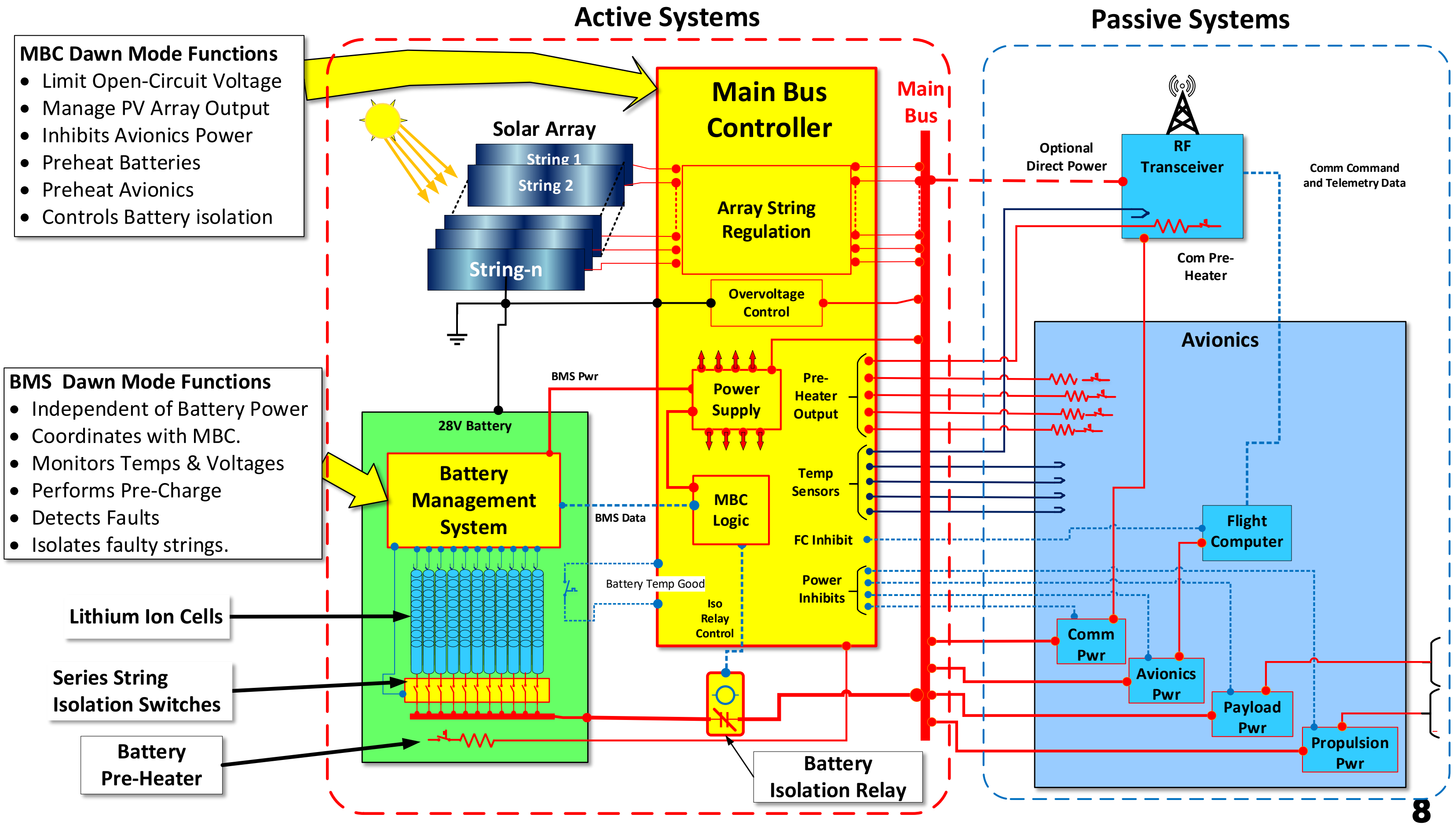
- **Two types defined for hibernation, Cryo-Tolerant & Cryo-Operable**
- **All systems need to be Cryo-Tolerant**
  - Circuits need to survive the extreme cold
  - Passive survival enables the use of COTS or legacy electronics
  - Requires component screening and substitution with cryo-tolerate components.
  - Requalify existing designs for Cryo-Tolerance.
- “**Main Power Bus” circuits must be Cryo-Operable**
  - Capable of a “Cold-Start” at cryogenic temperatures
  - Stable operation over a wide temperature range (400K – 50K)
  - Lunar Dawn may be as low as 50K

Lunar Power Hibernation Approach

Lunar Dawn illumination of Solar Arrays triggers a recovery operation “Dawn Mode”

- Dawn recovery is handled by Main Bus Controller (MBC)
- Prevent a PV Array Overvoltage
- At Lunar Dawn the Battery is still *frozen and isolated*
- MBC must provide stable operation on solar array output alone (Power Quality Issue)
  - No Battery to stabilize the main bus
  - Limit loads to resistive loads (minimize transients)
  - Keep general power distribution and avionics isolated
- Focus energy on thermal recovery
  - Pre-Heat battery and Avionics up to normal temperatures
  - Pre-Charge battery as needed to match bus voltage
- Reconnect battery to main bus and restart operations

Lunar Dawn Power Recovery Functions



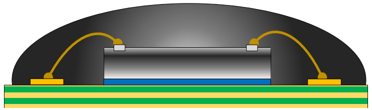
Lunar Power Hibernation Approach

<u>Cryo-Tolerant</u> electronics tolerate cryogenic temperature cycles without degradation.

- Cryo-Tolerance is a device and circuit packaging issue.
- Managing "coefficient of thermal-expansion" (CTE) is key
  - Copper cladding on fiberglass reinforced epoxy are closely matched.
  - *Size Matters,* Small devices have lower thermal joint stress
  - Connection compliance reduces joint stress.
  - Epoxy Encapsulation can break joints over time.
  - Expect limited cycle life from conventional PC boards.
- Good thermal management minimizes thermal stress
  - Lunar environment rate of change is slow.
  - Solar illumination can create localized heating.

Wire Bonding

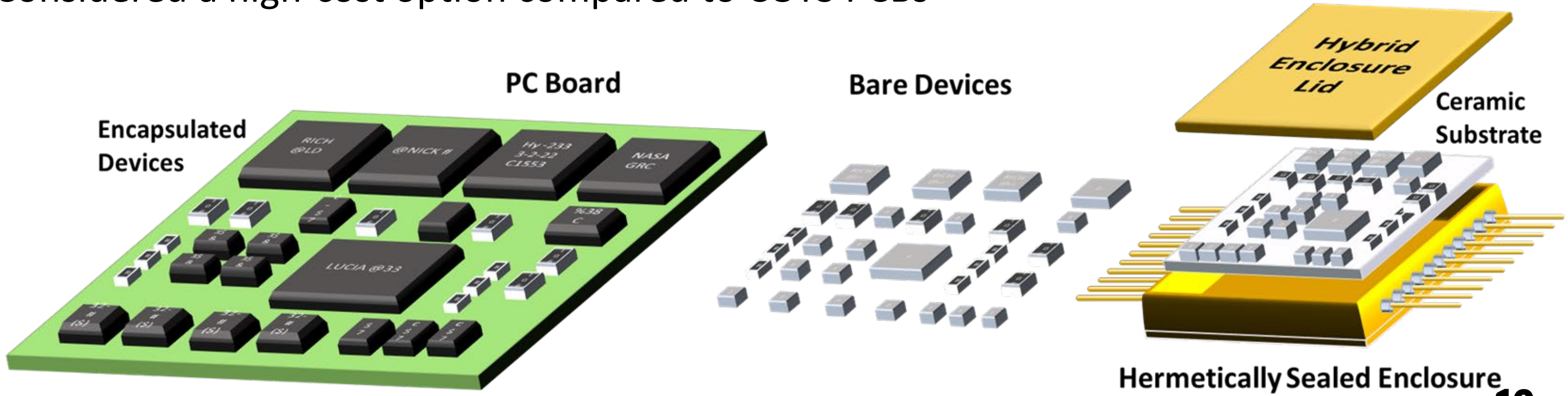
Flip-Chip with Underfill



Chip-on-Board Encapsulated

Cryo-Tolerant Electronics: Hybrid Circuit Packaging

- **Hi-Reliability (hybrid circuits) encapsulates multiple devices in a hermetically sealed enclosure**
  - Commonly used to harden a circuit for harsh (typically hot) environments.
  - Bare (active/passive) devices assembled on a low-CTE ceramic substrate
  - Connected directly to thick film traces via wire-bond or flip-chip technique
  - Eliminates thermal stress of plastic encapsulants on electrical joints
  - Reduces overall size while improving thermal conductivity
  - Considered a high-cost option compared to COTS PCBs



Lunar Power Hibernation Approach

Cryo-Operable Electronics

Capable of cold starting and stable operation in cryogenic temperatures

- All semiconductors see parameter shifts with declining temperature
- Transistor architecture can dramatically affect cryo-operability

Circuit-level cryo-operability (400K to 50K)

- Many circuits use mixed semiconductor and transistor technologies.
- Need to account for differing behaviors over a wide temperature range
  - Flat response to temperature is ideal for circuit stability
  - May need device level temperature compensation techniques

Lunar Power Hibernation Approach

Cryo-Operable Electronics Physics

- **Carrier Freezeout:** is a phenomenon at cryogenic temperatures, where electrons do not have sufficient energy to jump to the conduction band.
- The freeze-out range is where the reduced thermal energy means electrons have less energy and thus the population of electrons in the conduction band decreases as the temperature decreases.
- The conduction electron population can be increased at low temperatures by increasing the number of doped impurities.
- Increased doping can adversely affect electron mobility.

Lunar Power Hibernation Approach

Cryo-Operable Electronics Physics

- **Carrier Mobility:** Related to how fast electrons move through the semiconductor for a given electric field.
- Scattering effects govern how long it takes to move through the semiconductor.
- At normal temperatures Lattice (thermal) Scattering dominates.
  - Low Temps-> Less Scattering -> Shorter Transit Time -> Higher Carrier Mobility
  - Semi-conductor performance tends to increase at lower temps.
- As Lattice Scattering diminishes as Charge Scattering dominates.
  - At extremely low temperatures, electrons jumping to the conduction band have less initial velocity and are easily deflected by localized charged atoms.
  - Ionized “Doping” atoms are the main cause of Charge Scattering at low temperatures

Lunar Power Hibernation Approach

Cryo-Operable Electronics: Impact of transistor architecture

Bi-Polar Junction Transistors (BJT)

- BJT devices performance peaks at low temperature, but the combination of Carrier Freezeout and Charge Scattering eventually degrades performance until they are inoperable at extreme temperatures.
- The exception is Silicon-Germanium (SiGe) where conduction at extremely low temperature is maintained by “electron-tunneling”.

Field Effect Transistors (FET) [Note that FETs come in many flavors]

- FET technology is less dependent on doping, thus less subject to charge scattering more likely to work at extremely cold temps.
- Digital circuits using CMOS FETs maintain good performance at extremely low temperatures.

Lunar Power Hibernation Approach

Cryo-Operable Electronics: Impact of transistor architecture

- **High Electron Mobility Transistors (HEMT)** usually Gallium-Nitride (GaN) exhibit high speed switching and well suited to power and RF comm applications.
- **GaN HEMT** devices seem to have a nearly flat response to temperature
  - May be best for operating over a wide temperature range
  - GaN is best suited to Power and RF applications
  - GaN is already appearing in Space Applications.
  - More work on cryo-temperature performance is needed.

Current NASA Space Technology Research

NASA STRG Early Career Faculty (ECF) Investigations

ECF22: Hibernation & Recovery of Solar-Powered Systems for Lunar Missions

- **Prof. Hatzell of Princeton University**: Specifically investigating electro-chemistry and thermo-mechanics of 18650 cells during the Freeze/Thaw process. This PI is using X-ray computed tomography involving a synchrotron source (Brookhaven National Lab) to acquire internal images of a cell as it goes through freezing and thawing cycle.
- **Prof. Zhu of U of Cal- Santa Barbara**: Investigating Li-ion cell freeze/thaw dynamics and its effects on cell performance using micro-Raman spectroscopy. She is also examining thermo-mechanical and electrochemistry changes during freeze-thaw transition using Transient Grating Spectroscopy.
- **Prof Zhang of Rensselaer Polytechnic Institute:** This PI investigating Gallium-Nitride HEMT devices and performing characterization tests over the 400K to 50K temperature range. He is also designing, modelling and evaluating GaN based power circuits suited for power system recovery from hibernation.

Current NASA Space Technology Research

Lunar Surface Technology Research (LuSTR) Investigations

LuSTR21: ***Cold-Tolerant Electronics and Packaging for Lunar Surface Exploration***

- Investigates the both Cryo-Operable and Cryo-Tolerance issues for extreme environments (not just hibernation)
  - Three University Team (Auburn U, Georgia Tech, U of Tennessee)
  - Key members were involved with recent Mars missions (Curiosity & Perseverance)
- Designing, Fabricating and Testing Silicon and Silicon-Germanium technology for cryo-operable applications, (Si and SiGe foundry on contract)
- Developing a precise A/D converter for cryo-operations.
- Exploring “Back-Gate” control for temperature compensation for Silicon devices based on Silicon-On-Insulator (SOI) technology.
- Investigating methods for improving circuit board cryo-tolerance. Trying to avoid the high cost of developing custom hi-reliability circuits.

Hibernation work at Glenn Research Center

Cryo-Tolerant Li-Ion Batteries to 50K

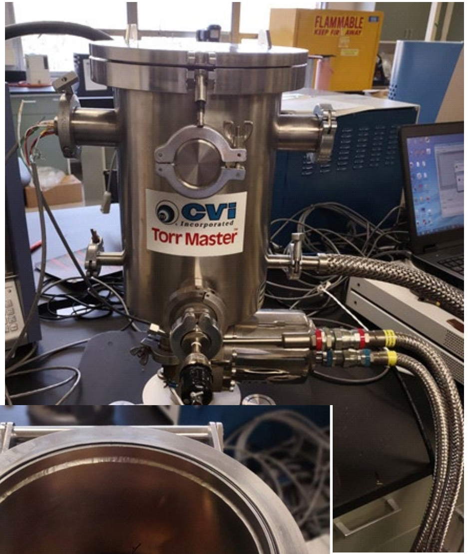
- Investigating multi-cell battery interactions through multiple freeze/thaw cycles
- Looking for degradation patterns
- How sensitive are the batteries to non-uniform temperature?
  - Warmer cells may charge colder cells, potential internal damage
  - Thermal control design should focus on temperature uniformity.
- May impact how batteries are assembled
  - Normally cells are grouped in parallel (virtual cells) then arranged in series.
  - May be desirable to arrange cells in series strings then parallel
    - Easier to detect faults
    - Easier to isolate a battery string (graceful degradation).

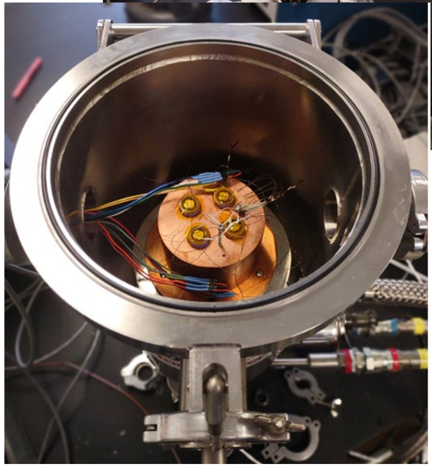
Hibernation work at Glenn Research Center

Cryo-Tolerant Li-ion Batteries

Successfully demonstrated lunar hibernation survivability to 50K

- Satisfactorily demonstrated several freeze/thaw cycles on NASA JSC's Strategic Reserve 18650 Li-Ion cells with dwell times of 14 days.
- Cells Tested
  - LG model INR18650 M36
  - Molicel model INR18650-M35A
- Little to no loss of capacity nor mass loss
- Investigated performance at 0%, 20%, and 40% SOC under the lunar hibernation exposure
- Demonstrated series and parallel connections for maintaining balance





Current NASA Space Technology Research

Internal work at Glenn Research Center

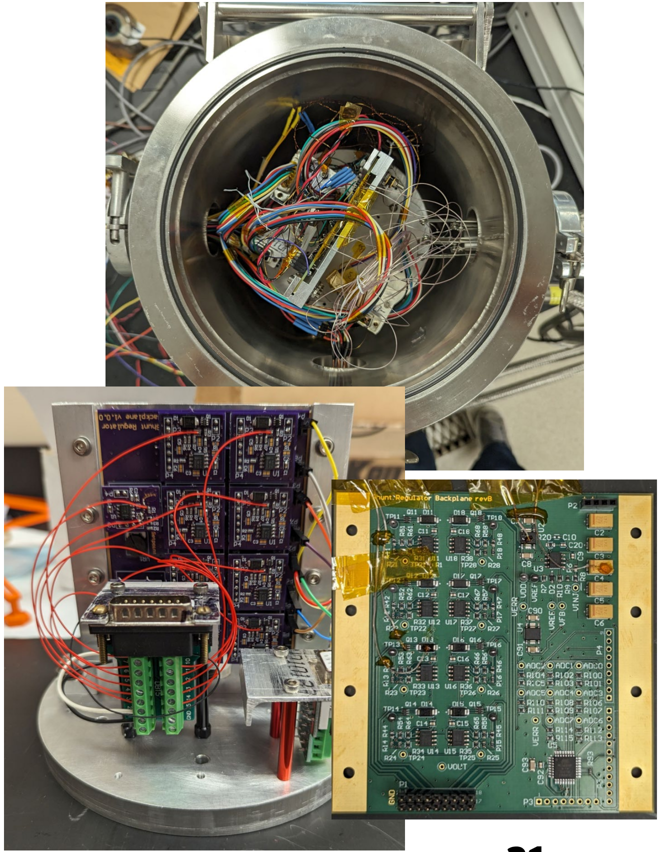
Cryo-Operable Main Bus Power Electronics to 50K

- Using commercial devices and PC board fabrication technologies.
- No Cryo-performance data was provided so characterization testing was performed.
- Employing lessons learned from 2022 technology assessment.
  - Analog circuits primarily silicon-based devices
  - Field-effect devices (less sensitive to temperature)
  - Low to medium level integration and small physical footprint
  - Simple Solar Array Series Shunt Regulator (a lunar dawn function)
  - Successfully operated to 57K
- Further work
  - Will continue to push toward 50K for all components
  - Incorporate digital controls and other functions (ex heater control)

Current NASA Space Technology Research

Internal work at Glenn Research Center

- **Designed a small Sequential Switching Shunt Regulator (S3R) for regulating a simulated solar array.**
  - Circuit board is comprised entirely of COTS components.
  - Used a shortened 3U card with edge conductive cooling.
  - Test fixture simulated a conduction cooled 3U chassis.
- Fully operational in a vacuum environment at approx. 57 K (-216 °C).
  - Demonstrated a "cold start" after an unpowered 24-hour cold soak (no residual heat due to self-heating)
  - Operated with no battery to stabilize the bus.
  - Physically tolerated <50K
  - Certain op-amps acted up below 57K, still investigating



Infusion of Hibernation Technologies

Adopting Hibernation Approach

- Growing evidence that Hibernation and Recovery is viable
- Many COTS or Legacy Circuits can be made cryo-tolerant
- Many COTS devices are cryo-operable.
- **Biggest barrier appears to be the engineering side**
  - Lack of manufacturers cryo-temperature data. (typ. 125°C to -55°C)
  - Internal (proprietary) details are obscured by manufacturers.
  - Developers forced to perform device characterization tests.
  - Need component screening, engineering design, and test guidelines
  - Need updated design and simulation tools for cryo-electronics.
- Device-to-Device compatibility may require temperature compensation.
- The long-term reliability of conventional PC Boards is still an open question.
- High-Reliability packaging still the best choice for long life.

Infusion of Hibernation Technologies

Guidelines and design tools are needed to aid spacecraft/payload developers infuse new technology.

- **Cryo-Tolerant battery design and operational guidelines**
  - Cryo-tolerant chemistries
  - Batteries packaging design to ensure uniform thermal environment
  - Diagnostics (cold battery) and fault isolation
- **Cryo-Tolerant electronic device & circuit level fabrication guidelines**
  - Screening and modification of COTS circuits may be practical.
  - Hybrid or Hi-Reliability design practices may still be required.
- **Cryo-Operable electronics data and engineering tools**
  - Characterization of devices and passive components for 400K to 50K
  - “Physics-Informed” modelling and simulation tools

Next Step: **Lunar Power Hibernation Approach**

- **NASA Engineering and Safety Center (NESC)**
- Planning to perform a technology assessment of the cold-electronics in 2024.
    - Cold Electronics Workshop
    - Assessment of the State of the Art
    - Recommendations for design, fabrication and testing
- **Technology developments continues under NASA funding**
    - In-house development of Hibernation Electronics continues in 2024.
    - Early Career Faculty work on batteries and GaN electronics extends to 2025.
    - LuSTR work on cryo-electronics (SiGe and Si completes in mid 2024.)
- **Potential Hibernation Technology Demonstrator for a spacecraft application**.
    - Infuse directly into the spacecraft power system.
    - A Flight Tech Demo as a payload may be needed.
    - May combine with other night survival technologies (lunar night operations)
    - ***Will need an industry partner***

Summary

- **Lunar Power Hibernation extends capabilities & duration of solar powered lunar missions**
- **Reduces dependency on radioisotopes and pre-established infrastructure**
- **Minimize the impact on spacecraft design**
- **Hibernation and Recovery Depends On**
  - Cryo-tolerant Li-ion batteries: 18650 cells survive lunar night down to 50K
  - Cryo-tolerant electronics: All electronics physically survive the night to 50K.
  - Cryo-operable electronics: Electronics that reliably “cold start” at lunar dawn.
- **Hibernation Applications**
  - Commercial Lunar Payload Services (CLPS)
  - Robotic or remotely operated surface elements of the Artemis Program
  - Lunar in-situ resource utilization (ISRU) systems operating in polar regions
- **Systems that are innately compatible with the lunar environment improve survival & recovery options in contingency situations**

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