Best Practices for Fabrication of Microelectronic Devices

Material degradation during the fabrication of microelectronic devices has plagued the space industry for many years owing to the layering of many dissimilar metals to create these devices. Often, commonly used materials and systems are overlooked as potential sources of material degradation. This technical bulletin highlights extensive research to isolate probable causes of this degradation.

Motivation

NASA Goddard Space Flight Center has observed material degradation issues in their superconducting microelectronic devices, including material discoloration, dissolution, and surface structure modification. To mitigate these issues, the NESC surveyed recent device anomalies in terms of handling, chemical and environmental exposures, operation and test histories, and full details of failure indications. Following this survey, an in-depth investigation was conducted into the issues surrounding a superconducting microelectronic device that was fabricated through physical vapor deposition, reactive ion etching, and wet chemistry on a silicon wafer. This device experienced a discoloration of the layered molybdenum / niobium / molybdenum (Mo/Nb/Mo) leads that worsened over time.

Analytical Procedures

Detailed imaging and compositional analyses of the device was undertaken using the following techniques: scanning and transmission electron microscopy (SEM/TEM), atomic force microscopy, x-ray photoelectron spectroscopy (XPS), Fourier transform infrared spectroscopy, inductively coupled plasma spectroscopy, two-wire resistance measurements, and electroanalysis.

Technical Findings

- Electroanalytical experiments and XPS studies of the processing fluids, including solvents, revealed no concerns of galvanic corrosion at dissimilar metal interfaces.
- Electron microscopy revealed the presence of metal oxides, including molybdenum oxide (MoOx) and aluminum oxide (AlOx) in the discolored regions. For example, a 7-layered structure on the leads was discovered when a 3-layered structure was Expected (Figure 1.) Studies to determine origin of oxidation and unexpected metals (i.e. Al) revealed three possible sources: (1) prolonged oxygen plasma exposure, (2) residual materials in fabrication chamber from previous users, and (3) exposure to deionized water (DIW). For Mo thinfilms, microscopy and resistance measurements revealed that

DIW caused a discoloration and an increase in the electrical resistance of the devices. Extended exposure to DIW led to Mo dissolution.

 Materials and processes were implemented in the creation of recent devices without a full understanding of the material interactions and impacts. In addition, inadequate process controls, including quality control measures, were present.

Process Improvement Recommendations

- Monitor effect of common use chemicals on microelectronic device fabrication. Conduct a full materials investigation before incorporating new materials into fabrication processes. If possible, understand long-term stability and interactions of materials used.
- Ensure integrity of etching and deposition chambers. Conduct dummy deposition runs to ensure unwanted contaminants from prior runs are removed and to verify desired surface chemistry is achieved. Develop requirements for chamber cleanliness.
- 3. Avoid long exposures to oxygen plasma and understand effects of various exposure conditions to the surface chemistries of the microelectronic device.
- Avoid using DIW on certain substrates and initiate hermetic sealing, if necessary, to avoid long-term degradation of the microelectronic devices.

Organizational Process Recommendations

- Re-verify fabrication processes after any process change or off-nominal result.
- 2. Introduce inspection test points to collect objectively verifiable data to ensure process conformity.
- Collaborate outside of sphere of influence to determine and set verifiable requirements at onset of work.

References

 Parker, D.; Beamesderfer, M.; Brown, A. Assessment of Degradation in Microfabricated Detectors and MEMS Devices. NESC-RP-21-01640.

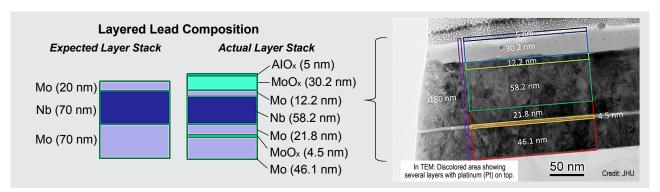


Figure 1. (left) Expected material layer stack of the superconducting leads of a detector. (center) Actual layer stack as determined through TEM cross-sectional analysis (right).



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