OPTIMIZING CHANNELIZATION FOR FUN AND PROFIT

PREPARED FOR RAMS 2024

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ALBUQUERQUE, NM, US

Gwyer Sinclair,
National Aeronautics and Space Administration,
Marshall Space Flight Center

WHAT'S THE BOTTOM LINE?

Design for reliability by ordering your multiplexer's channels.

With optimal channelization, software can detect, correct, and eliminate critical outcomes due to addressing failures.

Reliability: The probability that a system will perform its intended function adequately for a specified period of time.

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Multiplexer: A EEE device which selects between several input signals and forwards one (1) selected signal to output. (Also known as a data selector or MUX)

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Channel: A MUX's input signal which has a sensor or device attached.

Un-assigned channels output GND or 0 V when selected. (channels 5-7 in example)

8 to 1 MUX	
Channel	Sensor
0	Pressure Sensor 1
1	Pressure Sensor 2
2	5V Voltage Reference
3	Temp. Sensor 1
4	Temp. Sensor 2
5	N/A
6	N/A
7	N/A

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Channelization: The order in which sensors/signals are connected to the MUX inputs

8 to 1 MUX	
Channel	Sensor
0	Pressure Sensor 1
1	Pressure Sensor 2
2	5V Voltage Reference
3	Temp. Sensor 1
4	Temp. Sensor 2
5	N/A
6	N/A
7	N/A

WHAT'S THE BOTTOM LINE?

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With optimal channelization, software can detect, correct, and eliminate critical outcomes due to addressing failures.

Addressing Failure: a failure in the software, logic circuit, or MUX itself which causes the wrong channel to be requested or transmitted.

WANT

GET

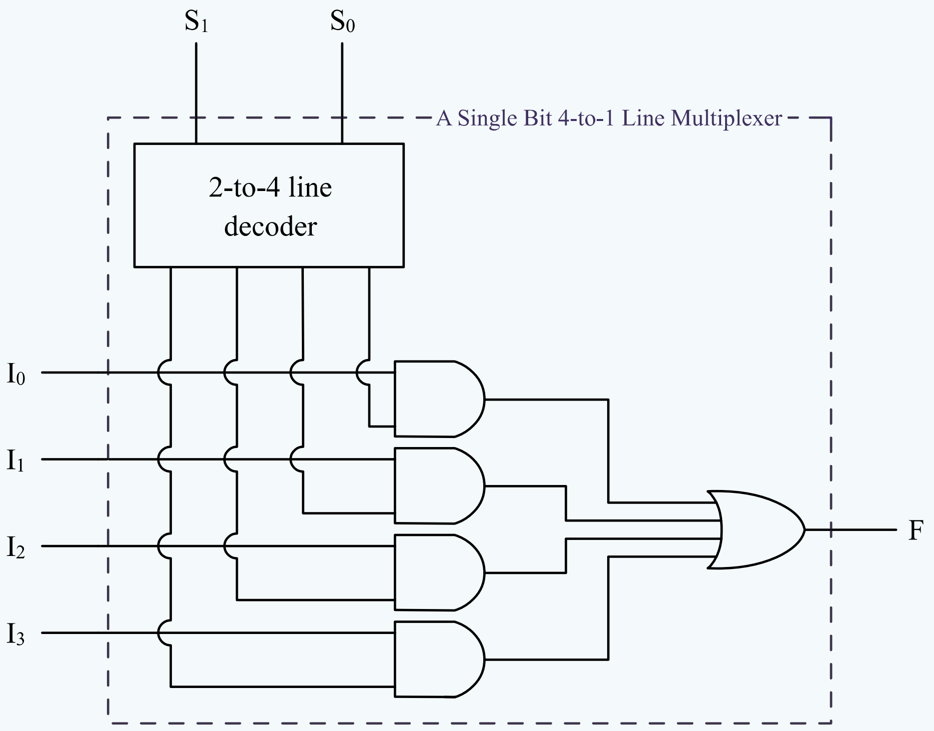
8 to 1 MUX	
Channel	Sensor
0	Pressure Sensor 1
1	Pressure Sensor 2
2	5V Voltage Reference
3	Temp. Sensor 1
4	Temp. Sensor 2
5	N/A
6	N/A
7	N/A

MULTIPLEXER MECHANICS

A MUX uses ‘select lines’ and logic gates to control which input is sent to output. In a 4-to-1 MUX there are 2 select lines (S0, S1). Select digits form the channel # in binary.

4 to 1 MUX		
Channel	S1	S0
0	0	0
1	0	1
2	1	0
3	1	1

A short (unintended connection) between any number of input or select lines will force them to share the same voltage.



Truth Table

S_1	S_0	I_3	I_2	I_1	I_0	F
0	0	0	0	0	0	0
		0	0	0	1	1
		0	0	1	0	0
		0	0	1	1	1
		0	1	0	0	0
		0	1	0	1	1
		0	1	1	0	0
		0	1	1	1	1
		1	0	0	0	0
		1	0	0	1	1
		1	0	1	0	0
		1	0	1	1	1
		1	1	0	0	0
		1	1	0	1	1
		1	1	1	0	0
		1	1	1	1	1

S_1	S_0	I_3	I_2	I_1	I_0	F
0	1	0	0	0	0	0
		0	0	0	1	0
		0	0	1	0	1
		0	0	1	1	1
		0	1	0	0	0
		0	1	0	1	0
		0	1	1	0	1
		0	1	1	1	1
		1	0	0	0	0
		1	0	0	1	0
		1	0	1	0	1
		1	0	1	1	1
		1	1	0	0	0
		1	1	0	1	0
		1	1	1	0	1
		1	1	1	1	1

S_1	S_0	I_3	I_2	I_1	I_0	F
1	0	0	0	0	0	0
		0	0	0	1	0
		0	0	1	0	0
		0	0	1	1	0
		0	1	0	0	1
		0	1	0	1	1
		0	1	1	0	1
		0	1	1	1	1
		1	0	0	0	0
		1	0	0	1	0
		1	0	1	0	0
		1	0	1	1	0
		1	1	0	0	1
		1	1	0	1	1
		1	1	1	0	1
		1	1	1	1	1

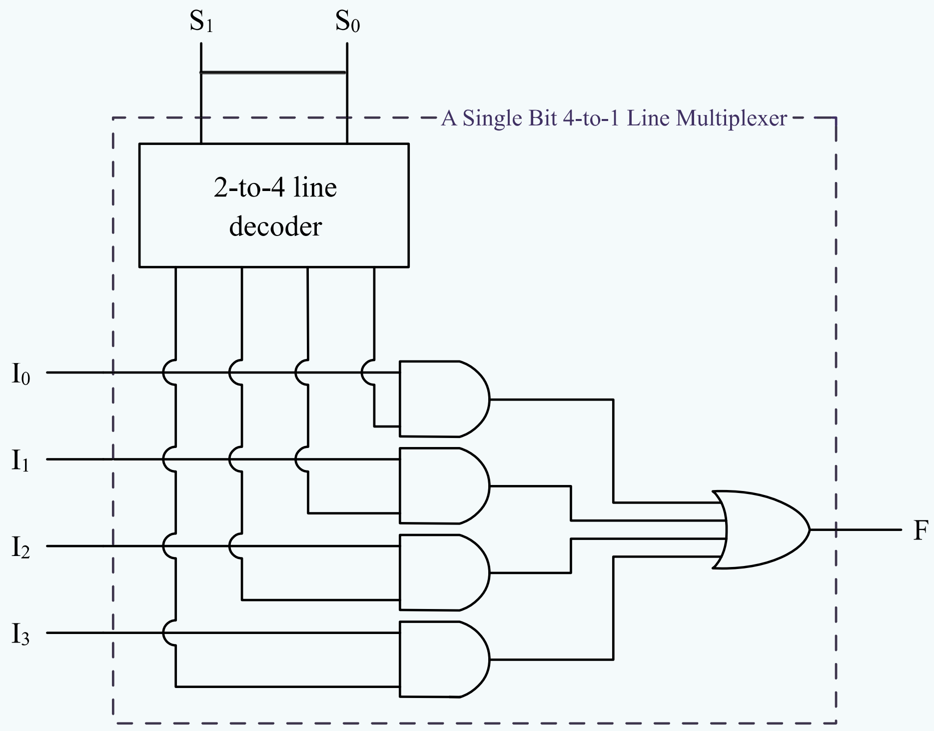
S_1	S_0	I_3	I_2	I_1	I_0	F
1	1	0	0	0	0	0
		0	0	0	1	0
		0	0	1	0	0
		0	0	1	1	0
		0	1	0	0	0
		0	1	0	1	0
		0	1	1	0	0
		0	1	1	1	0
		1	0	0	0	1
		1	0	0	1	1
		1	0	1	0	1
		1	0	1	1	1
		1	1	0	0	1
		1	1	0	1	1
		1	1	1	0	1
		1	1	1	1	1

ADDRESSING FAILURE MECHANICS (MUX CAUSE)

Here, a short between S1 and S0 will cause both lines to be ‘1’ if either is ‘1’

Channels 1 and 2 are unreachable states

Any failure, erratic, or unintended behavior from EEE elements like the logic gates can cause unpredictable channel selection



Truth Table

S_1	S_0	I_3	I_2	I_1	I_0	F
0	0	0	0	0	0	0
		0	0	0	1	1
		0	0	1	0	0
		0	0	1	1	1
		0	1	0	0	0
		0	1	0	1	1
		0	1	1	0	0
		0	1	1	1	1
		1	0	0	0	0
		1	0	0	1	1
		1	0	1	0	0
		1	0	1	1	1
		1	1	0	0	0
		1	1	0	1	1
		1	1	1	0	0
		1	1	1	1	1

[illegible]	S_0	I_3	I_2	I_1	I_0	F
0	[illegible]	0	0	0	0	0
		0	0	0	1	0
		0	0	1	0	1
		0	0	1	1	1
		0	1	0	0	0
		0	1	0	1	0
		0	1	1	0	1
		0	1	1	1	1
		1	0	0	0	0
		1	0	0	1	0
		1	0	1	0	1
		1	0	1	1	1
		1	1	0	0	0
		1	1	0	1	0
		1	1	1	0	1
		1	1	1	1	1

[illegible]	S_0	[illegible]	I_2	I_1	I_0	F
[illegible]	[illegible]	[illegible]	0	0	0	0
		0	0	0	1	0
		0	0	1	0	0
		0	0	1	1	0
		0	1	0	0	1
		0	1	0	1	1
		0	1	1	0	1
		0	1	1	1	1
		1	0	0	0	0
		1	0	0	1	0
		1	0	1	0	0
		1	0	1	1	0
		1	1	0	0	1
		1	1	0	1	1
		1	1	1	0	1
		1	1	1	1	1

S_1	S_0	I_3	I_2	I_1	I_0	F
1	1	0	0	0	0	0
		0	0	0	1	0
		0	0	1	0	0
		0	0	1	1	0
		0	1	0	0	0
		0	1	0	1	0
		0	1	1	0	0
		0	1	1	1	0
		1	0	0	0	1
		1	0	0	1	1
		1	0	1	0	1
		1	0	1	1	1
		1	1	0	0	1
		1	1	0	1	1
		1	1	1	0	1
		1	1	1	1	1

ADDRESSING FAILURE MECHANICS (OTHER CAUSE)

- A short involving non-MUX components
- A short or sneak path which circumvents the MUX
- Blown res. or cap. causes open circuit ahead of a select line
- Short to voltage or signal source ahead of a select line
- IC manufacturing defects

- Memory or buffer errors
- Hackers
- Firewalls
- Trojans
- URLs
- Phishing Emails
- The Three Laws of Robotics

ADDRESSING FAILURE MECHANICS - EXAMPLE

Now, when expecting telemetry from channel 0, values from channel 4 are transmitted instead. When channels 1-3 are expected, the transmitted signal is from channels 5-7 instead. N/A channels output 0V.

Expected					Received				
Channel	A2	A1	A0		Channel	A2	A1	A0	
0	0	0	0	Pressure Sensor 1	4	1	0	0	Temp. Sensor2
1	0	0	1	Pressure Sensor 2	5	1	0	1	N/A
2	0	1	0	5V Voltage Reference	6	1	1	0	N/A
3	0	1	1	Temp. Sensor 1	7	1	1	1	N/A
4	1	0	0	Temp. Sensor2	4	1	0	0	Temp. Sensor2
5	1	0	1	N/A	5	1	0	1	N/A
6	1	1	0	N/A	6	1	1	0	N/A
7	1	1	1	N/A	7	1	1	1	N/A

DETECT THESE ERRORS WITH CHANNELIZATION

This is possible due to the different expected ranges of each channel.

- Sensors each return a voltage which is interpreted by software
- Different makes, models, and use cases of sensors have different exp. voltage ranges
- Reference or constant voltage signals will always have a known value
- Unassigned channels will have a voltage of GND or 0V

When a system suffers an addressing error, it may or may not receive a signal within the expected range. A signal outside the expected range can be detected with hardware (voltage based switching) or a software solution.

Can we channelize these sensors in such a way that an addressing failure always causes the MUX to telemeter a detectably incorrect channel?

LET'S ASK RICHARD!

- Richard Hamming (1915 – 1998)
- American mathematician
- CPE and Telecom : Hamming code, Hamming window, sphere-packing, Hamming Distance.
- Manhattan Project

"The purpose of computing is insight, not numbers"

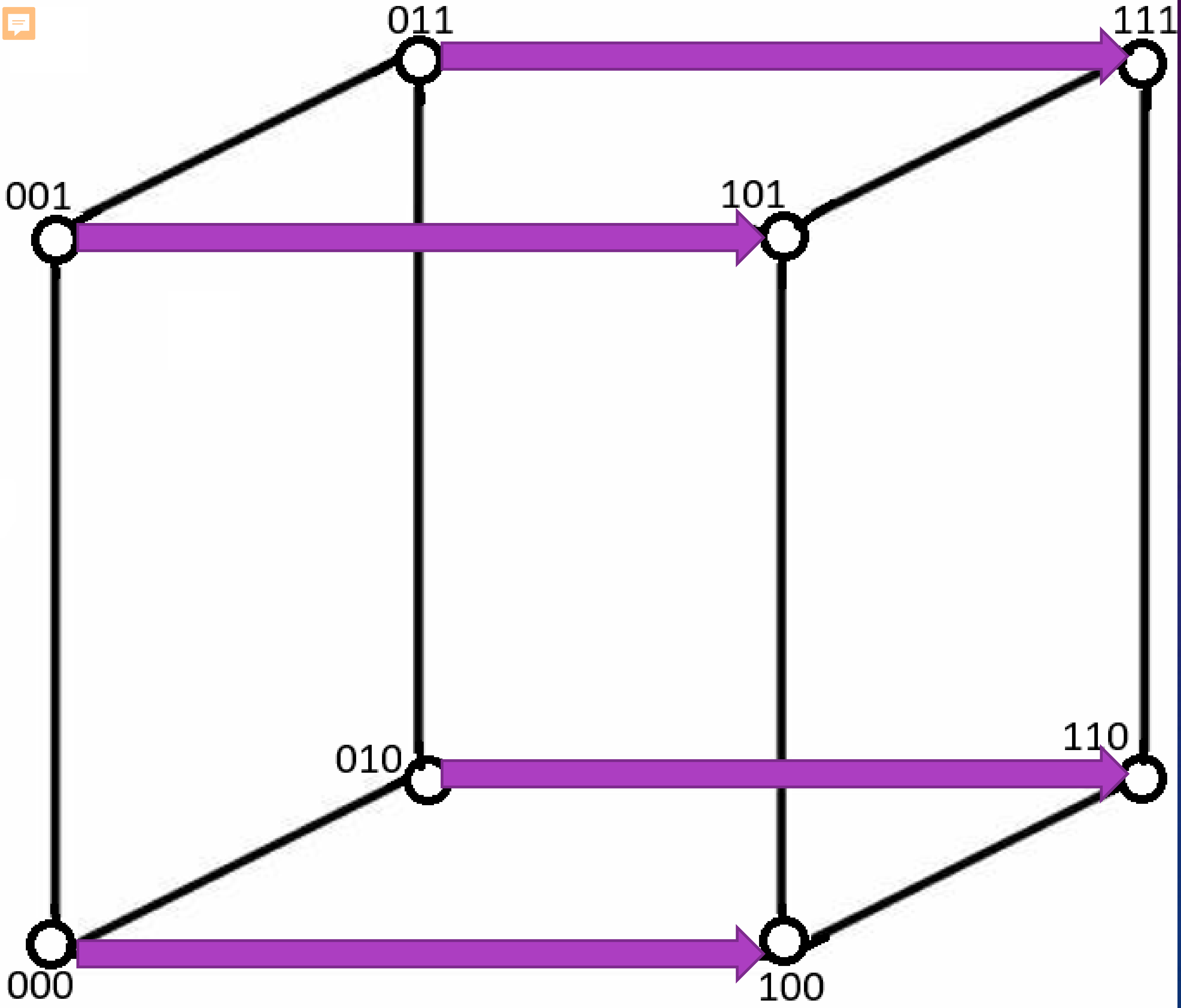
HAMMING DISTANCE

The Hamming Distance between two binary expressions of equal length is the number of bit positions in which the two bits are different.

Expression A			Expression B			Hamming Distance
0	0	0	0	0	0	0
0	0	0	0	1	1	2
0	1	0	1	0	1	3

In an 8-to-1 MUX (3 binary digits), a single addressing failure means that the expected channel could be replaced by **any of the channels within a Hamming Distance of 1.** I will call these channels Hamming-Adjacent.

100 -> 000, 110, or 101

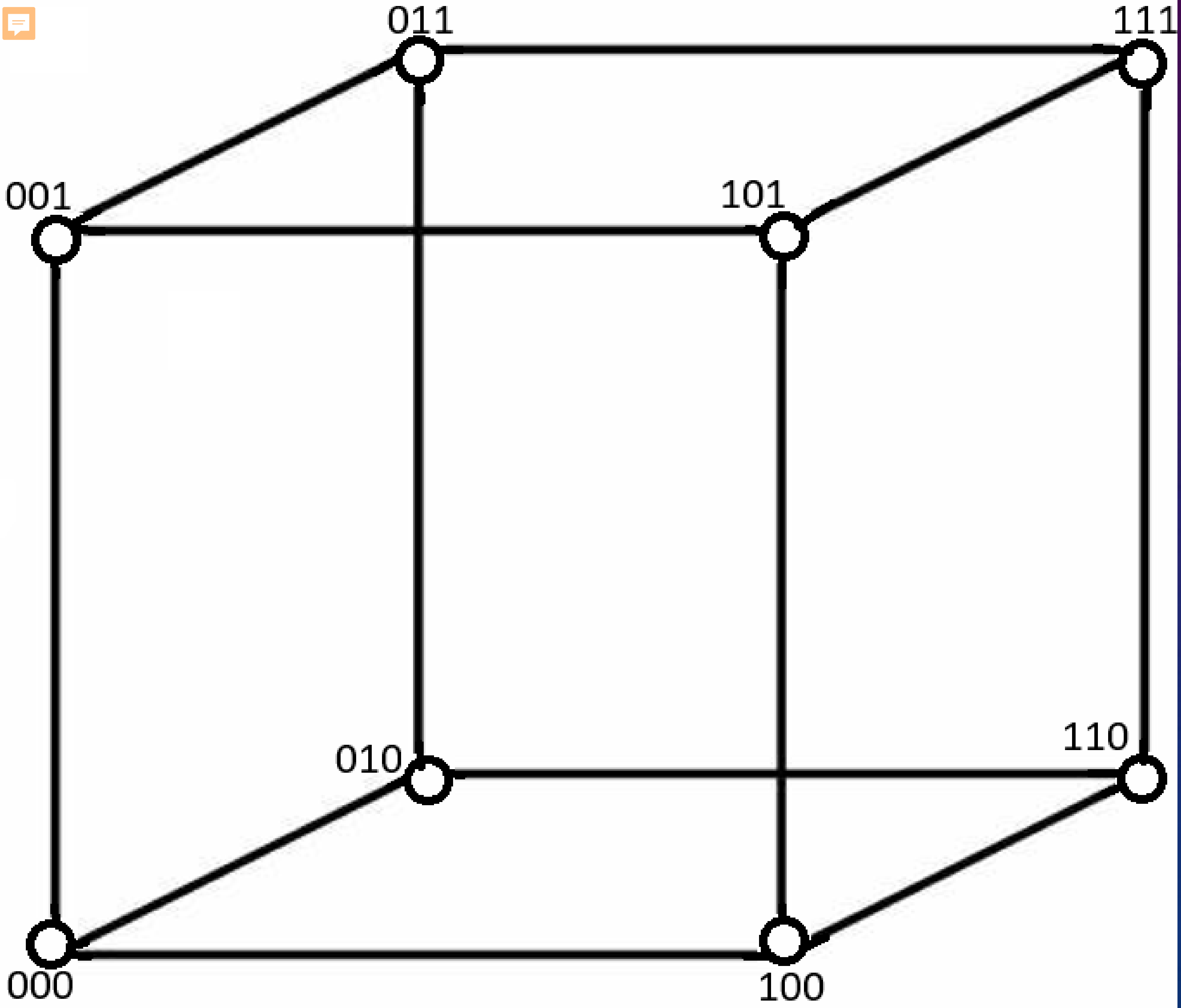


HAMMING CUBE

8 POSITIONS

Visualize the addressing failure from our example, A2 (leading bit) stuck high.

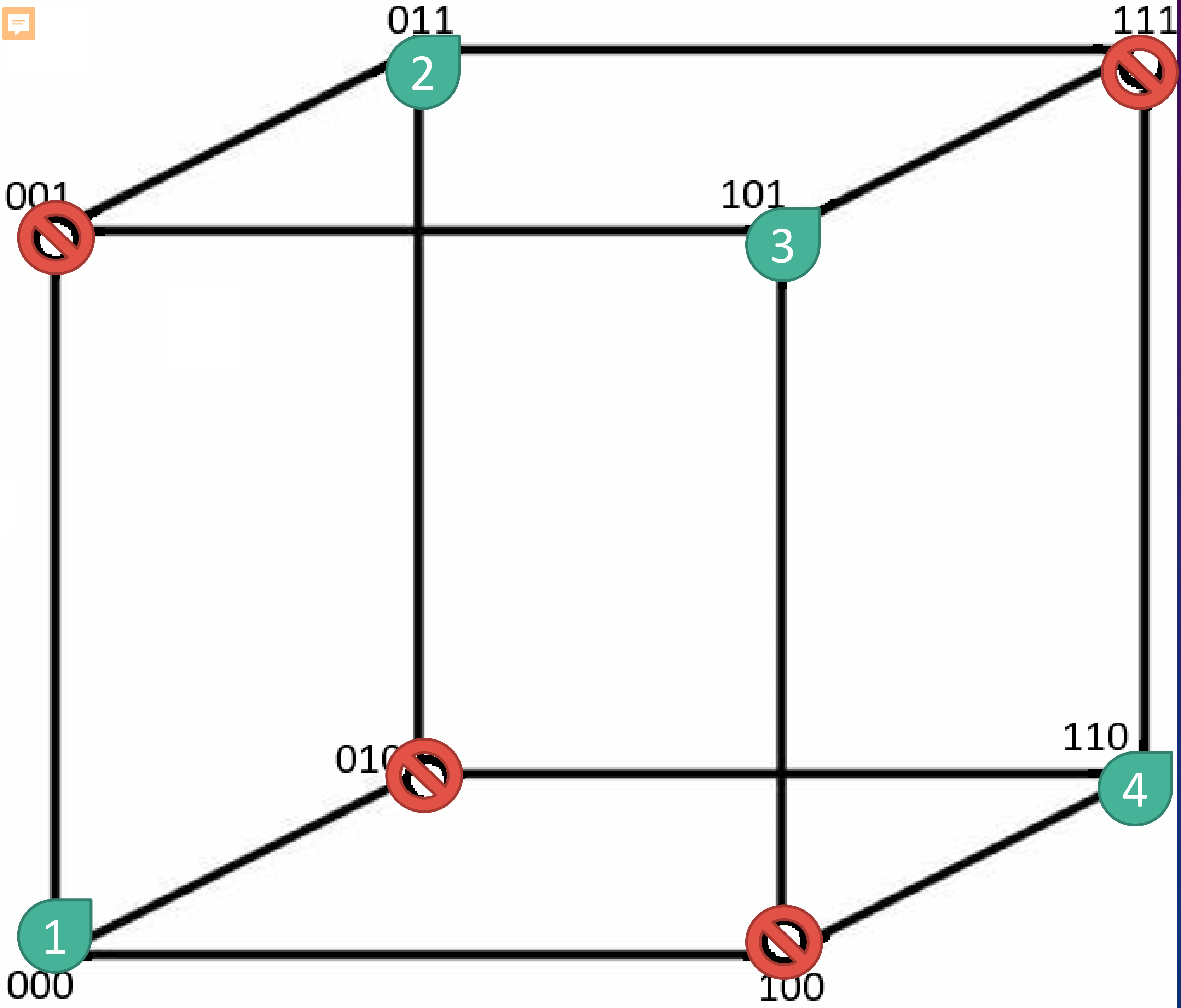
000 fails to 100
001 fails to 101
Etc…



HAMMING CUBE
8 POSITIONS

Any two vertices on this cube which are connected by an edge have a Hamming Distance of 1. (Hamming Adjacent)

In the event of an addressing failure, they would be susceptible ‘fail-over’ channels.



HAMMING CUBE

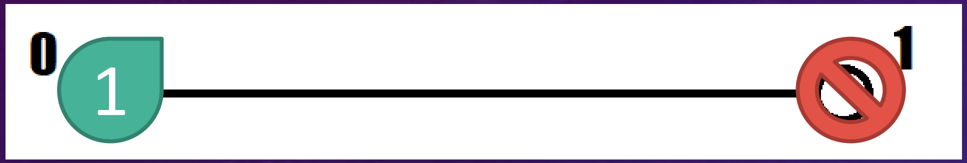
8 POSITIONS

Let's use this cube to place signals in sets that are failover-proof.

If we begin by placing one of our signals in 000, that means 001, 010, and 100 should be in a different set.

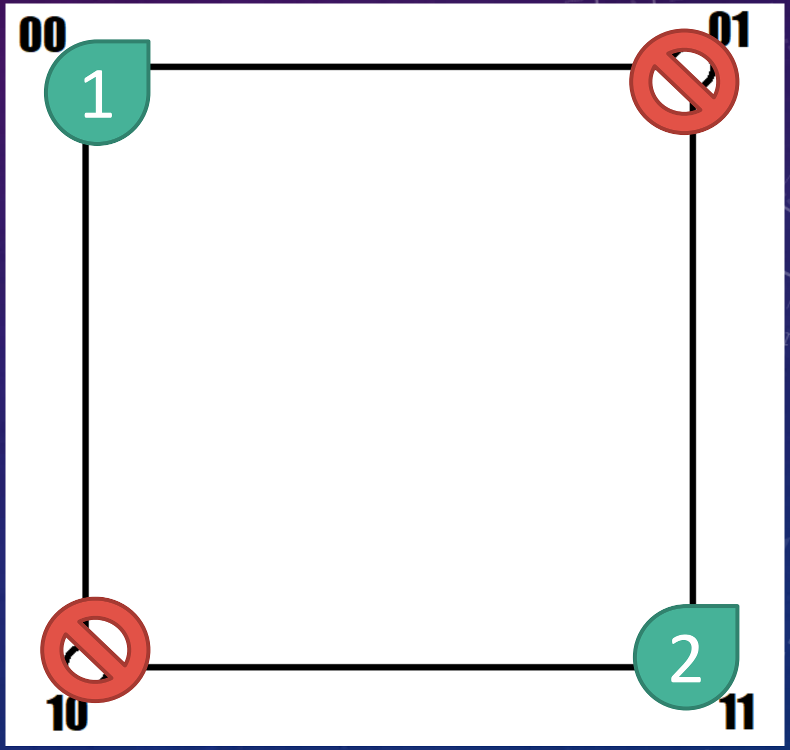
This is an application of graph theory called Vertex Coloring or K-Coloring

HAMMING LINE
2 POSITIONS

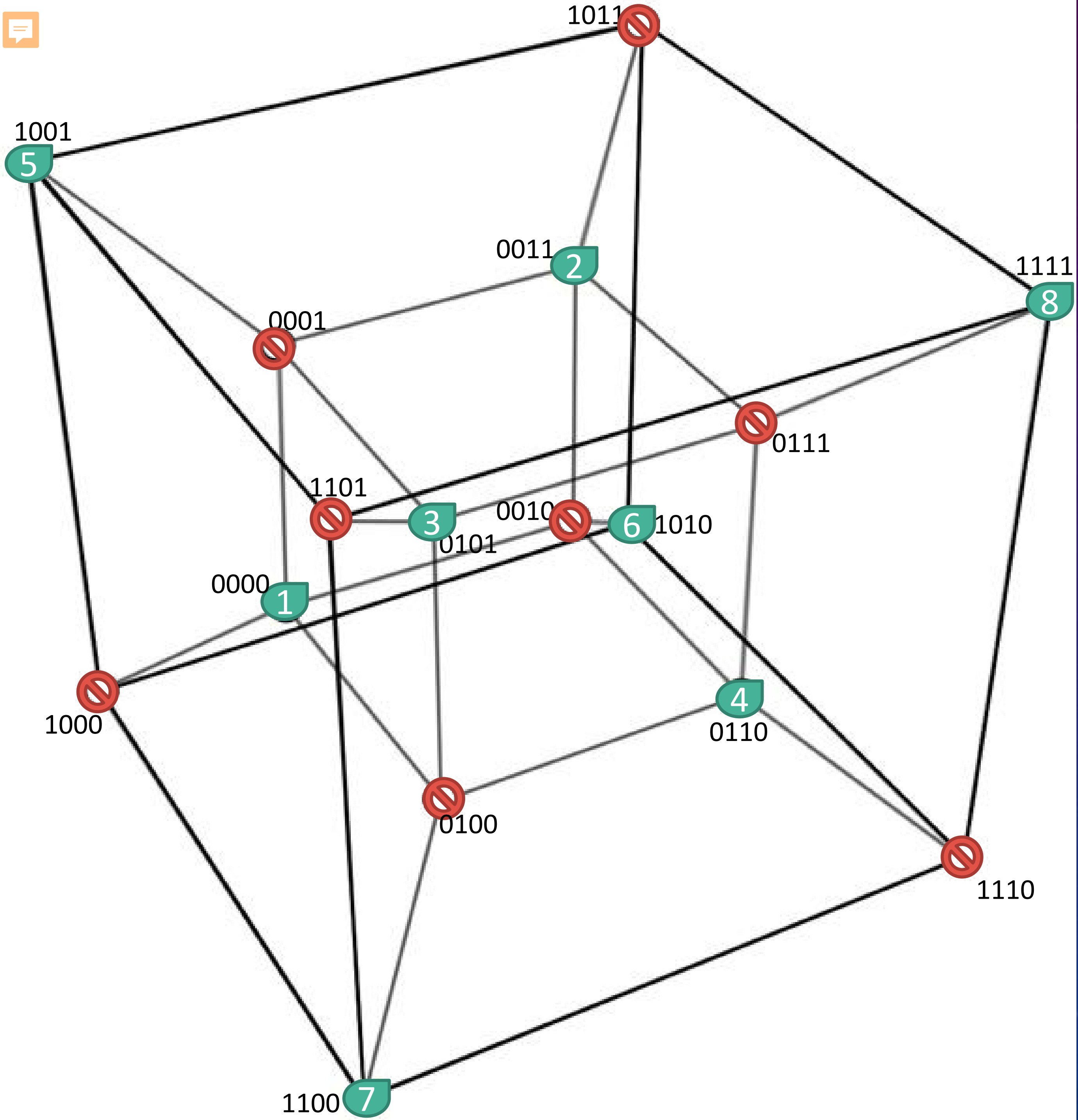


A 2-to-1 MUX (switch) has a maximum set size of 1

HAMMING SQUARE
4 POSITIONS

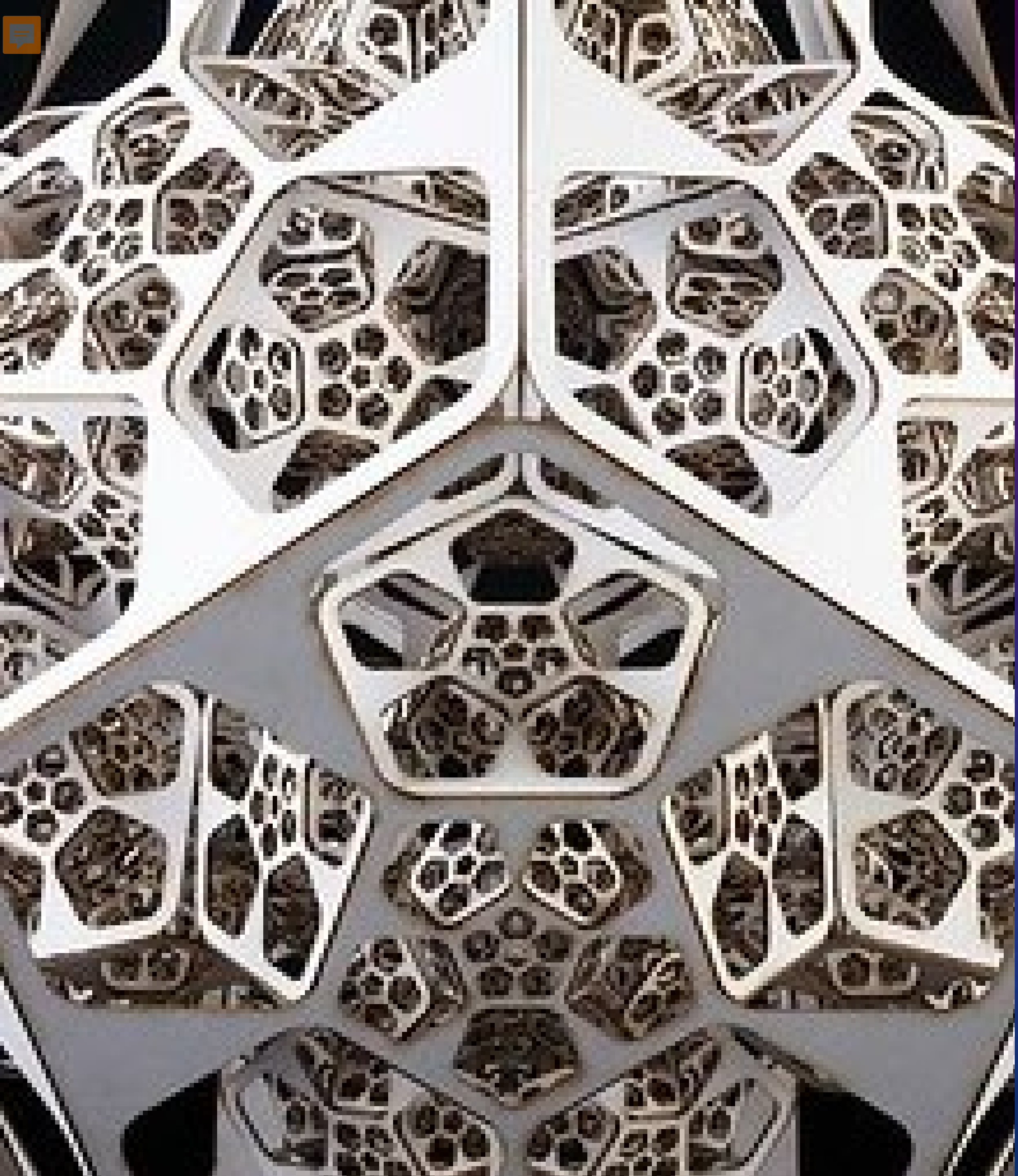


A 4-to-1 MUX has a maximum set size of 2



THE TESSERACT
16 POSITIONS

A 16-to-1 MUX has a maximum set size of 8



BEYOND THE LIMITS OF THE FEEBLE HUMAN MIND
N POSITIONS
N -> ∞

A 2^n-to-1 MUX has a maximum set size of 2^{n-1}

OPTIMAL CHANNELIZATION

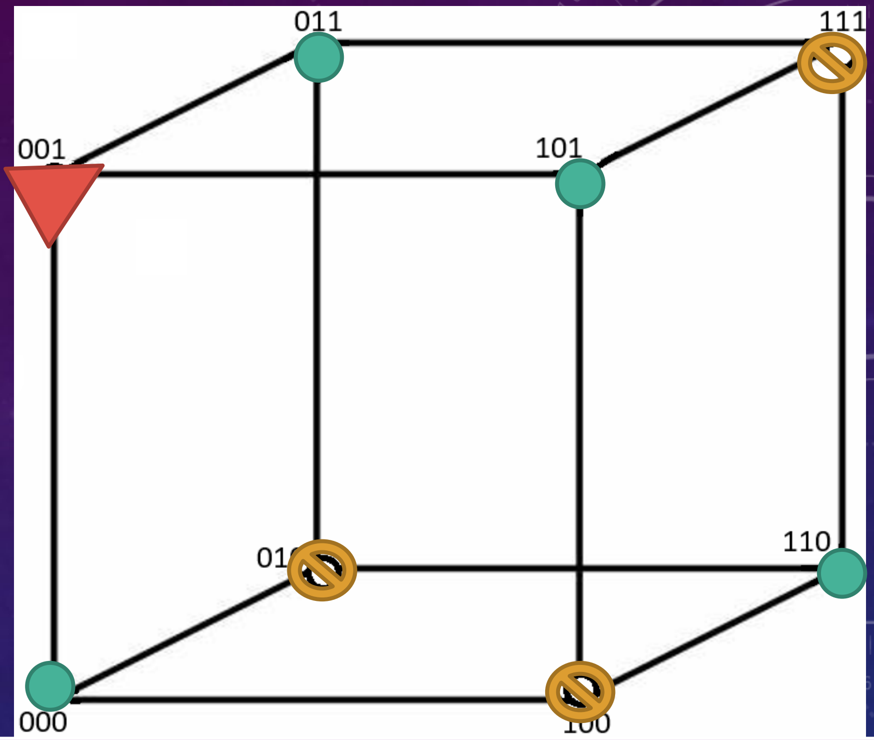
Apply this principle to our example:

The four sensors share an EVR and are one set

The 5V Reference has its own set

The unassigned channels have an expected value of 0V, different from all the others – so they are their own set

Our new channelization:



8 to 1 MUX				
Channel	A2	A1	A0	Sensor
0	0	0	0	Pressure Sensor 1
1	0	0	1	5V Voltage Reference
2	0	1	0	N/A
3	0	1	1	N/A
4	1	0	0	Temp. Sensor 2
5	1	0	1	Temp. Sensor 1
6	1	1	0	Temp. Sensor 2
7	1	1	1	N/A

CURRENT STATE-OF-THE-ART

- Random channelization
- Alphabetical channelization
- Based on hardware physical location

What I have communicated is a best-practice which improves on this state-of-the-art by offering a technique to increase reliability… the only cost is the development of a monitoring algorithm that compared the received value to the expected.

SUMMARY

- An addressing error causes the software to request, or the MUX to telemeter, a Hamming-Adjacent channel instead of expected
- If the incorrect data is used in calculations, expect errors
- Make sure addressing errors always cause your sensors to telemeter an out-of-range value, by placing un-assigned channels or sensors with incompatible ranges in Hamming-Adjacent channels
- Develop detection for out-of-range sensor outputs
- Detected errors can be diagnosed, fixed, or prevented from propagation

GWYER SINCLAIR - Contact gwyer.q.sinclair@nasa.gov

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