Nuclear and Emerging Technologies for Space (NETS 2024)
Santa Fe, New Mexico, May 6-10, 2024

Overview of Advanced Stirling Convertor Dual Convertor Controller Development and Testing at NASA Glenn Research Center

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For over two decades, NASA Glenn Research Center (GRC) has been supporting the development of Radioisotope Power Systems (RPS). NASA desires higher conversion efficiency RPS options that are reliable and robust with long life design. Dynamic conversion, such as Stirling offer the potential for higher conversion efficiencies than current RPS but have yet to be demonstrated in a flight application. GRC has integrated key aspects of a non-nuclear RPS by integrating a pair of Advanced Stirling Convertors (ASC), a Dual Convertor Controller (DCC), electrical heaters, and associated support equipment. The DCC was designed by the Johns Hopkins University/Applied Physics Laboratory (JHU/APL) to actively control a pair of ASCs. Based on lessons learned, three generations of DCCs were developed over the past decade. After each generation of the DCC was completed, tests were performed to verify functionality. These tests include acceptance testing, fault testing, characterization testing, and testing with the Radioisotope Power System Systems Integration Laboratory (RSIL). Acceptance testing verifies that the DCC can control a pair of ASCs to produce full convertor power output. The fault testing verifies that the DCC can maintain control of the ASCs during either internal or external faults. Characterization testing verifies the functionality of the DCC over a range of bus voltage values. RSIL provides insight into the electrical interactions between a representative radioisotope power generator, its associated control schemes, and realistic electric system loads. The DCC design, development, lessons learned, test results, and future work are presented in this paper.

I. Introduction

The Dual Convertor Controller (DCC) is an active controller for a Radioisotope Power System (RPS) using two Advanced Stirling Convertors (ASCs). The RPS is a power source that may be used in space, on the Moon's surface, or the surface of other extraterrestrial objects, providing approximately 150 Watts of continuous power for 17 years. The RPS includes the DCC, two ASCs, and an integrating structure providing thermal insulation and radiators, and power shunts; its thermal input power comes from attached and insulated Pu238-fueled General Purpose Heat Source (GPHS) modules. The first and second generation DCCs were developed as part of the Radioisotope Power System (RPS) Technology Advancement Project and the third generation DCC was developed as part of the Dynamic Radioisotope Power System (DRPS) project in support of the Radioisotope Power System program at NASA Glenn Research Center (GRC)[1].

Development of the DCC began in 2012 and since then three generations of the DCC have been developed as described in Table I. Each generation of the DCC was designed based on lessons learned from the previous. Each DCC board contains the power handling, data acquisition, signal processing, and secondary voltage conditioning circuits needed to control a convertor and deliver DC power to the spacecraft. A total of four boxes, each box houses a DCC board, were built and are interchangeable to make a fault tolerant DCC. The DCC boards were upgraded with hardware and software changes as lessons learned were implemented in each generation of the DCC. Through each generation of the DCC, the mass (1.9 kg) and size (10.7"x7.2"x1.7") of each box remained the same.

TABLE I. Description of the generations of the DCC.

DCC Board	Generation	Description
1-4	1	Operates a pair of ASCs with 55-turn alternators.
1a-4a	2	Operates a pair of ASCs with 55- or 77-turn alternators.
1b-4b	3	1. Phase adjustment capability. 2. Change from 2-level to 3-level H-bridge switching. 3. Expand the allowable Stirling convertor operating frequency range.

The DCC key requirements include:

1. Perform an AC to DC conversion of the convertor outputs.
2. Synchronizing the convertors to reduce disturbance force.
3. Controlling the convertors' operating frequency and voltage.
4. Deliver power to a space vehicle (SV) electric power system (EPS) bus.
5. Receive and execute a command set from the SV.
6. Provide state of health as telemetry to the SV.
7. Respond to faults at the SV load interface.
8. Respond to faults within a Stirling Convertor.
9. Maintain Stirling convertor operation in the event of an internal controller failure.
10. Prevent propagation of faults to other boards within the controller.

The first generation of the DCC was designed for ASCs with 55-turn alternators to support operation of the ASCs being designed by Sunpower, Inc. Based on program direction, a convertor with a 77-turn alternator was designed with increased alternator voltage and therefore lower current to minimize power loss. The DCC was updated to control both types of convertors, and this became the second generation DCC. Testing of the second generation DCC revealed that the DCC was providing 9W less DC output power to the spacecraft than expected. After troubleshooting to identify the root cause of the DCC output power loss, the DCC was updated and became the third generation. Other requirements were identified to include in third generation of the DCC. These include expanding the convertor operating frequency range and allowing for commanding of the phasing between Stirling convertors.

Test racks are used for each of the tests described in this paper and are customized to support each type of controller test. Each test rack provides the means for measuring and collecting data for observing operating trends. It provides the interfaces needed for the controllers and provides mechanisms to ensure the safety of the convertors. Each test article is instrumented to measure output characteristics such as alternator voltage, current, power, and operating frequency. Controller support hardware includes a DC electronic load, ground support equipment (GSE) DC power supply, and external shunt resistors. The hot end of the convertor is heated with electric cartridge heaters. The cold end of the convertor is maintained with a water/glycol bath. The data system utilizes LabVIEW (National Instruments) hardware and software to acquire data, monitor the test, acquire telemetry from the DCC, and send DCC commands. Commands are sent to:

- Change the voltage set point that controls piston motion amplitude.
- Change the convertor operating frequency.
- Connect or disconnect from the spacecraft.
- Operate with or without a backup board.
- Inject faults, enable/disable faults, and monitor faults.

II. First Generation DCC

This section describes the development of the first generation of the DCC, testing completed after delivery to NASA GRC, and the lessons learned.

II.A. Development

The DCC, shown in Figure 1, design is based on the SCC[2,3]. The first generation DCC can operate an ASC with an alternator voltage up to 15 V. It was designed for flight use, but only a mechanically equivalent, non-flight engineering model (EM) was built. The DCC uses a field programmable gate array (FPGA) to implement control algorithms and other functionality. It uses power electronics technology to eliminate the need for tuning capacitors to compensate for alternator inductance[4]. The DCC incorporates high-frequency pulse-width modulated (PWM) switching of an H-bridge to control the convertors. The DCC's two primary functions are to match the electrical load on both ASCs to the power they supply and to perform AC to DC electrical power conversion of each ASC alternator output. The DCC provides the DC power to the SV EP bus. Once the ASCs are fueled, by attaching a GPHS module to each convertor, the RPS operates continuously. By adjusting the load presented to each ASC alternator, the DCC controls the phase as well as amplitude of piston motion to minimize forces applied to the host spacecraft. The DCC accepts sensor signals from each ASC and provides this data along with its own state of health information as telemetry to the SV. It accepts external commands including a command that sets the ASC operating point. Once the set point is commanded, the DCC operates largely autonomously including detecting and responding to faults in the controller, ASCs, and SV load. Data within the DCC telemetry stream can be used to determine what faults occurred and the DCC's response. The command/telemetry stream can be used to diagnose detected faults and restore operation.

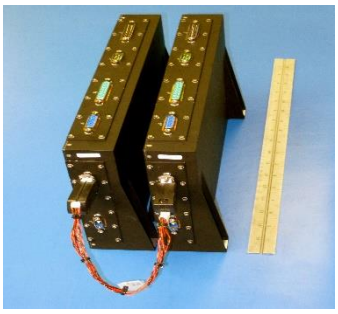

Fig. 1. Photograph of the DCC.

A block diagram of the DCC connected to a pair of ASCs and a typical redundant spacecraft is shown in Figure 2. Figure 3 shows a block diagram of the DCC. The DCC not only provides power to the spacecraft, but it also must regulate ASC operation to avoid damage to internal components and maintain safe thermal conditions after fueling. A single fault-tolerant[5] DCC consists of two identical controller boards packaged in separate chassis. Each controller board contains the power handling, data acquisition, signal processing, and secondary voltage conditioning circuits needed to control a convertor and deliver DC power to the spacecraft. A total of four boxes, each box containing a DCC board, were built. One box is actively controlling the convertor, while the other is available as a backup in the event of a fault. When the active unit detects a fault, it stops controlling the convertor and the hot spare is activated. A combination of analog circuits, FPGA logic, and microcontroller software monitor DCC operation and detect and correct potential faults. A functional failure mode effects analysis (FMEA) was developed to determine possible functional failures in the circuits. The impact of such failures and mechanisms to detect and correct them were identified and implemented in the detailed design. Fault detection requirements for the DCC include:

- Maintain ASC operation in the event of an internal controller failure.
- Maintain command and telemetry communication between the spacecraft and the controller communication bus.
- Prevent propagation of faults to other boards within the controller.

After detecting a controller fault and isolating the failed board, modeling showed that the backup controller has less than 20 ms to reestablish control to avoid unstable convertor operation. Modeling also showed that an open or short must be removed in less than 5 ms to avoid internal damage to convertor components. Analysis and simulation of the methods used to detect and recover from faults without damage to the ASCs as well as the ASC control algorithm are described in reference 5. Some of these faults include:

- Control fault where real alternator voltage significantly differs from the expected value.
- Commanded demotion of the active controller.
- Output buck regulator Field Effect Transistor (FET) short/open.
- Output buck regulator sync FET short/open.
- Commanded A/D value override.
- Excessive current into the spacecraft load.
- Excessive current from the spacecraft load into the controller.
- H-Bridge voltage too low.
- Housekeeping voltage too low.
- Backup controller power supply overcurrent.
- Disconnecting from the spacecraft when the bus voltage goes above 36V or below 22V. Once disconnected from the spacecraft, the user must command the DCC to reconnect; this is not done autonomously.
- Faults that can be injected into the DCC during testing are described in Table VII.

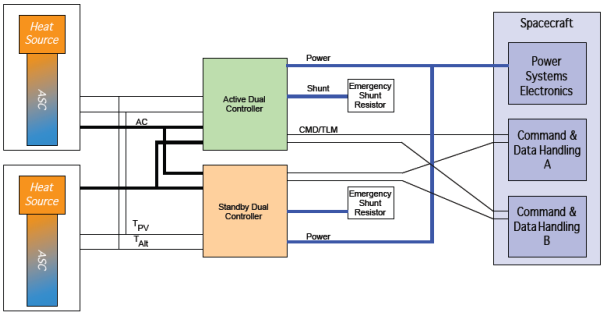

Fig. 2. Block Diagram of a typical DCC redundant spacecraft application.

If a board has failed and cannot recover from a fault, the DCC has the capability to repair a failed controller board. One board maintains control while the backup is removed and repaired/replaced.

Spacecraft power needs may briefly exceed the capacity of the ASC power source. If auxiliary power is not supplied from another source, the power bus voltage may be pulled too low and trigger a spacecraft fault. A battery frequently acts as the auxiliary power source to ensure that an adequate bus voltage is maintained during these power transients. Alternatively, a large capacitor bank may provide backup power if the expected power transients are short, and the energy storage capacity of the capacitor is adequate. Thus, the DCC was required to support either a battery or capacitive power bus spacecraft architecture.

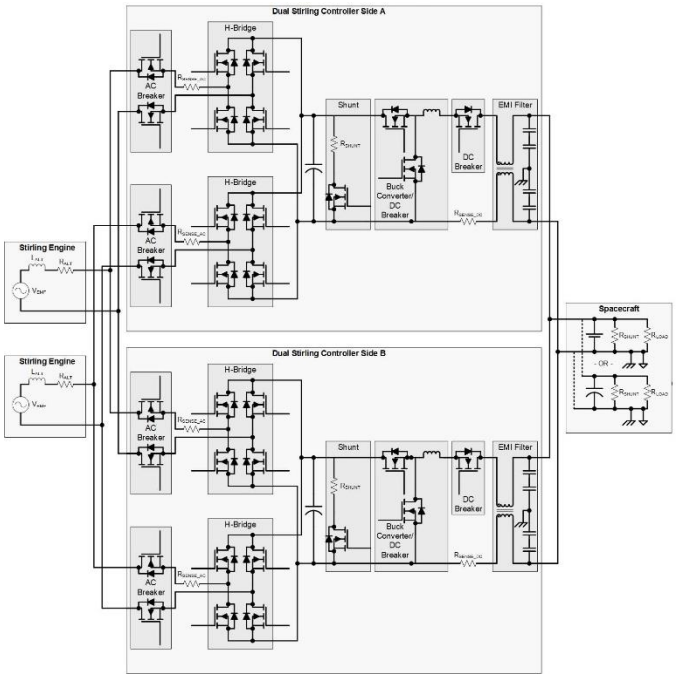

Fig. 3. Block diagram of the DCC power path.

II.A.1. FPGA

The control law inputs, and key status analog voltages are digitized by a 12-bit analog to digital (A/D) converter and processed by logic in an FPGA. The control law is implemented digitally by a co-processor in the FPGA. The co-processor contains an Institute of Electrical and Electronics Engineers (IEEE) single precision compliant data path controlled by a finite state machine sequencer programmed to implement the control law algorithm. A 16-bit microcontroller, also implemented in the FPGA, adjusts control law parameters, accepts user commands, and produces status telemetry.

II.A.2. Virtual Capacitor

The DCC implements the mathematical characteristics seen by an ASC convertor connected to a power source through a coupling capacitor. That capacitor is referred to as virtual since no such physical component is present but is instead simulated by the switching of transistors in an H-Bridge circuit within the DCC. A DCC input command can change the value of the virtual capacitor control law parameter.

At system start-up time, one of the DCC boards is made active and the other stays in back-up mode until a fault is detected in the active DCC board. When that happens, the active DCC board de-asserts a signal that indicates to the backup board that it is no longer the active board. The active board then disconnects its input port from the alternator coil and its output port from the spacecraft load circuit. The backup DCC board then: (a) waits 1-millisecond while the failed DCC board finishes disconnecting from the alternator and spacecraft load circuits, (b) connects its input port to the alternator coil and uses a temporary control algorithm to accept power from the engine and synchronize to the phase of its AC voltage source, and then (c) transitions to the normal control. If fault detection is enabled, the DCC can detect a control fault if the actual alternator voltage differs by more than a threshold value parameter from the expected value computed internally by the DCC control algorithm. The threshold value can be independently set on each channel. During control handover between sides of the DCC, there are a few milliseconds of time when the active controller is not simulating a virtual capacitor but instead provides a pure resistive load to the alternator. By restively loading the convertor, its oscillations are damped until there is positive going zero crossing of current. At that time, the controller initiates virtual capacitor control at a known phase angle thus maintaining continuous current control of convertor without needing to pass phase between the failed and backup DCC boards. The value of resistance is an input parameter to the control law calculation and may be independently set for each convertor.

II.A.3. AC & DC Breaker

Power flows from each convertor through an electronic switch for each ASC that acts as an AC circuit breaker. The AC circuit breaker is opened in the event of a fault to isolate the convertor from the failure and allow the redundant board to initiate control. Transient suppression devices on each controller board clamp voltage spikes that may occur when an AC breaker is opened. When the output regulator/DC breaker FETs are open, convertor power flows to an external shunt resistor controlled using a pulse width modulated FET-based regulator to maintain a fixed H-bridge output voltage.

II.A.4. H-Bridge

A FET H-bridge PWM is determined by the control law implemented in the FPGA. The H-bridge output is a DC voltage but with a large ripple current. An electromagnetic interference (EMI) filter on the board limits switching noise propagating from the controller to the spacecraft load. If a short occurs in one of the H-bridge FETs, an inductor limits the rate of increase of back-flow current from the spacecraft load circuit to the shorted H-bridge and allows the fault detector enough time to sense that a fault has occurred and turn off the DC disconnect FET before damage and/or significant voltage drop has occurred in the load circuit. However, a capacitor is needed at the H-bridge output terminal to limit the amount of switching ripple to acceptable levels.

II.A.5. Shunt

The shunt consists of a FET and a 5-ohm resistor. The DCC controller uses a PWM scheme to adjust the power dissipated in the external resistor as needed to maintain normal convertor operation. The external shunt is used during convertor testing, after the convertors are fueled but prior to integration onto the host spacecraft, and in case of a possible fault that prevents the spacecraft from absorbing power. The shunt controller is designed to output a signal that is always on, always off, or pulsing. The shunt controller output signal drives the gate of a PWM FET that grounds an external load connected to the H-bridge node. When the FET is grounded, power flows through the external resistor and the H-Bridge voltage is reduced. While the FET is open, the H-Bridge voltage rises as current from the convertor alternator is accumulated on the H-bridge capacitance. When a new H-bridge voltage reading is available from the ADC controller, the shunt controller does a comparison between the actual value and the baseline value. The duty cycle of the PWM FET is adjusted to maintain ≤60V so that the shunt will maintain ~60V at the output of the H-bridge. Under normal bus loads, the H-bridge voltage will be lower hence the shunt will not be active. If the shunt is active, the controller DC breaker is expected to be open so that all convertor power is dissipated in the shunt and no power flows to the spacecraft.

II.A.6. Interlock Signals

The interlock signals are RS-422 signals between the redundant units, so interlock_out from one DCC goes to interlock_in on the other DCC. It is essentially a circular handshake between the state machines. If there is a fault on either line that breaks the circle, the rest of the interfaces will settle to find a valid state, with one DCC or the other in control. These signals will read as '1' when open or when the driver is unpowered. The active unit drives interlock_out to '0' when it is active and '1' when it is a backup or unpowered. When in active or standby mode, each DCC monitors the state of interlock_in to make sure that it is consistent with the controller state. So, the active controller changes its interlock_out to '1' when it switches to a backup, then the other DCC reads that transition and knows to start controlling. Similarly, if the active unit detects it interlock_in going to '0', it will drop control and let the backup unit take over control.

II.B. Testing

Three main tests were performed with the first generation of the DCC, these include acceptance, fault, and Radioisotope Systems Integration Laboratory (RSIL) testing. Acceptance testing verified that the DCC can control a pair of ASCs to produce full convertor power output. The fault testing verified that the DCC can maintain control of the ASCs during either internal or external faults. RSIL provided insight into the electrical interactions between a representative radioisotope power generator, its associated control schemes, and realistic electric system loads. All testing was successfully completed with a pair of ASC-1s[6].

II.C. Lessons Learned

One of the main lessons learned with the first generation of the DCC is that there is a high ripple current, 5 A, in the spacecraft load. because it is connected directly to the controller's internal H-bridge node. The high ripple current was addressed in the second generation DCC as well as design changes to accommodate a higher voltage ASC. These changes will be discussed in the next section.

III. Second Generation DCC

This section describes the development of the second generation of the DCC, testing, and lessons learned.

III.A. Development

The second generation of the DCC was designed to reduce the output current ripple to <100mA. A buck regulator was added in series with the H-bridge node to reduce the load current ripple. The H-bridge node has a DC voltage but with a large ripple current. The output buck regulator stage is designed to minimize ripple in spacecraft output load current rather than maintain a specific output voltage. The regulator also protects the controller from spacecraft load faults. An additional FET switch in series with the buck regulator will isolate the load and controller from load faults.

When the DCC is supplying power to a capacitor dominated load and the load voltage starts at or near zero volts, the buck converter will bring the load voltage up gradually without pulling the voltage at the output of the H-bridge down to the point where the H-bridge doesn't work correctly. The buck converter works by switching a series FET on and off at a specified duty cycle. When the FET is on, current flows from capacitor into the inductor; but when the FET is off, the inductance current comes from the diode and not the capacitor. Consequently, by starting with a small duty cycle and allowing it to increase slowly, the average current draw on the capacitor can be limited to a value that keeps the H-bridge output voltage up at a level that allows it to operate correctly.

The buck controller contains a two-level PWM generator that drives the output regulator FET gate signals. The PWM logic is enabled by a signal from the main controller state machine that governs operation of the FPGA.

An additional benefit of adding an output regulator stage is that the H-bridge voltage is not dependent on the output

load voltage as in the first generation DCC. Thus, the nominal H-bridge voltage can be chosen to always be above the highest allowable load voltage and the allowable output voltage limits are independent of the alternator input voltage. The same controller can handle either a 55- or 77-turn ASC alternator through commanded control parameter changes. No hardware changes are needed.

III.B. Testing

Three tests were performed with the second generation of the DCC and either a pair of ASC-1s or a pair of ASC-E2's (55-turn). The tests include acceptance, fault, and RSIL testing. During acceptance testing, it was observed that the DCC output was producing 9 W less power than expected. An extensive effort to determine the power loss was performed and several lessons were learned. These will be discussed in the next section. Fault and RSIL testing were successfully performed.

III.C. Lessons Learned

Four lessons learned, as described in Table IV, were identified from investigating the DCC output power loss.

III.C.1. ASC

When testing the second generation DCC with a pair of ASC-1s, the DCC output produced 9W less power when connected to the spacecraft load than when using the Dual Advanced Stirling Convertor Simulator (DASCS)[7] at the same input power (as measured using a low bandwidth power meter). Through further testing and improved modeling of the alternator inductor, we determined that the high frequency switching (~23kHz) of the H-bridge caused more alternator power loss in the ASC than in the DASCS. An impedance sweep of the ASC alternator and DASCS inductor array revealed that the real ASC exhibited more high frequency parasitic losses under switching current ripple than the DASC simulator. This resulted in lower measured output power from the ACS than the DASC simulator because power generated by the ASC was being consumed in the alternator core via eddy currents and magnetic hysteresis as well as in the wires through skin effect, etc.

III.C.2. Modeling

A model of the alternator was created in Simulink by APL to understand why the power loss was not seen in the APL model and to help identify how the power loss could be reduced. The effort showed that the source of error was incorrect inductor characteristics in the model. The inductance of the ASC-E2's alternator and the DASCS simulated alternator were characterized with an impedance analyzer from 500 Hz to 10MHz. This data was used in the Simulink model to better understand the loss that would be expected. Comparing the inductor in the ASC versus the original model showed that the characteristics were considerably different. This explained why the power loss was not seen in the model. A parallel resistance was added to the alternator model to represent the inductor dynamics and the model losses more accurately matched the alternator losses.

III.C.3. Testing

Alternator power was initially measured with a power meter that had a limited bandwidth and used a 500 Hz line filter that resulted in masking the alternator power loss. Even if the line filter is off, most of the harmonics of alternator power loss (due to the 23 kHz H-bridge switching) were not seen due to the 100 kHz bandwidth of the power meter. It was determined that the power meter bandwidth masked the impact of the harmonics generated by the DCC's switching frequency. Power flows into the DCC at the fundamental piston frequency of 102.2 Hz, however the 23 kHz PWM switching frequency of the DCC results in high frequency ripple components in the alternator current and voltage. These high-frequency harmonics in the alternator current drive high-frequency losses (hysteresis in the alternator core, proximity loss in the alternator windings, etc) and reduce the power extracted from the convertor. These high frequency components are beyond the bandwidth of the power meter previously used; hence that instrument was under reporting the true DCC input power. A power meter was identified with a bandwidth up to 1 MHz and was subsequently used to measure the input power to the DCC.

III.C.4. Controller

In the first and second generation DCC designs, the H-bridge used the 2-level H-bridge switching scheme. A study was conducted by APL to understand the alternator power loss when using 2-level and 3-level H-bridge switching techniques. Modeling showed that implementing 3-level H-bridge switching reduced the high-frequency losses generated by harmonics in the alternator.

In the 2-level switching scheme, two diagonally located MOSFETs will be switched on and off simultaneously to produce either $+V_{DC}$ or $-V_{DC}$ across the alternator. Figure 4-5, and Table II show one typical example of implementing the two-level switching modulation. A triangle waveform (V_{tri}) with a much higher frequency than the frequency of the reference voltage and an amplitude higher than that of the reference voltage signal is compared to the reference voltage signal to generate a modulated signal as shown in the V_{alt} waveform in Figure 4. If the instantaneous reference voltage is higher than the instantaneous triangle voltage, then Q_1 and Q_4 will conduct and the PWM signal will become V_{DC} as shown in Figure 5(a). Likewise, if the instantaneous reference voltage is

lower than the instantaneous triangle voltage, then Q2 and Q3 will conduct and the PWM signal will become $-V_{DC}$ as shown in Figure 5(b). A set of produced two-level voltage pulses will then be filtered by the alternator inductor to produce the desired sinusoidal waveform for the back-EMF. The voltage applied to the alternator dithers at twice the DC link voltage driving a current ripple with a peak-to-peak amplitude of approximately 0.5 amps. This current ripple results in rapid rates of change of magnetization in the alternator/magnet assembly and corresponding hysteretic losses.

TABLE II. Switching sequence for two-level switching for an inverter.

Condition	PWM Polarity	MOSFET /Diode on	V_{alt}	Switching Scheme
$V_{sine} > V_{tri}$	+	Q_1, Q_4	V_{DC}	Fig. 8(a)
$V_{sine} < V_{tri}$	−	Q_2, Q_3	$-V_{DC}$	Fig. 8(b)

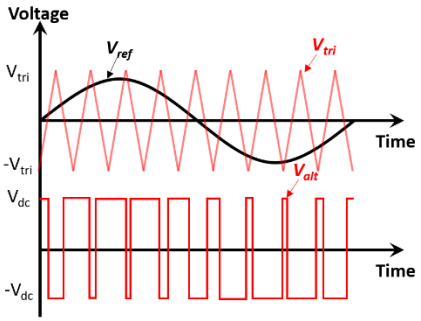

Fig. 4. Two-level switching waveform.

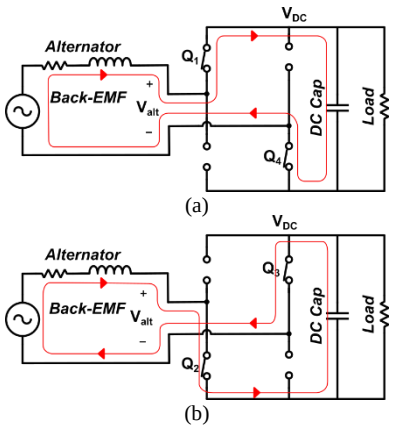

Fig. 5. Two-level switching schemes: (a) Q_1 and Q_4 are turned on ($V_{alt} = V_{DC}$) and (b) Q_2 and Q_3 are turned on ($V_{alt} = -V_{DC}$).

On the other hand, the third generation DCC uses the 3-level switching scheme to improve power efficiency and reduce EMI and waveform distortion by having three voltage levels: $+V_{DC}$, 0, $-V_{DC}$. One common example of the three-level switching scheme is shown in Figure 6 and the switching sequence is shown in Table III and Figure 7. In this switching scheme, a triangle waveform (V_{tri}) and its inverted signal ($-V_{tri}$) are used. If $V_{ref} > V_{tri}$ and $V_{ref} > -V_{tri}$, then Q_1 and Q_4 will conduct, and the alternator voltage will become V_{DC} (Figure 7(a)). If $V_{ref} > V_{tri}$ and $V_{ref} < -V_{tri}$ or $V_{ref} < V_{tri}$ and $V_{ref} > -V_{tri}$, then the alternator voltage will become zero (Figure 7(b) and Figure 7(c)). Finally, if $V_{ref} < V_{tri}$ and $V_{ref} < -V_{tri}$, then Q_2 and Q_3 will start conducting and the alternator voltage will become $-V_{DC}$ (Figure 7(d)). The voltage ripple across the alternator is reduced and therefore magnetic hysteretic as well as other high-frequency power losses are reduced. The high-frequency ripple current on the alternator inductance is reduced which in turn reduces high frequency parasitic losses in the alternator. Modeling comparison of the two switching methods showed that 3-level switching reduced core loss by about a factor of 4.

TABLE III. Switching sequence for three-level switching for an inverter.

Condition	MOSFET /Diode on	V_{alt}	Switching Scheme
$V_{ref} > V_{tri}$, $V_{ref} > -V_{tri}$	Q_1, Q_4	V_{DC}	Fig. 11(a)
$V_{ref} > V_{tri}$, $V_{ref} < -V_{tri}$	Q_1, Q_3	0	Fig. 11(b)
$V_{ref} < V_{tri}$, $V_{ref} > -V_{tri}$	Q_2, Q_4	0	Fig. 11(c)
$V_{ref} < V_{tri}$, $V_{ref} < -V_{tri}$	Q_2, Q_3	$-V_{DC}$	Fig. 11(d)

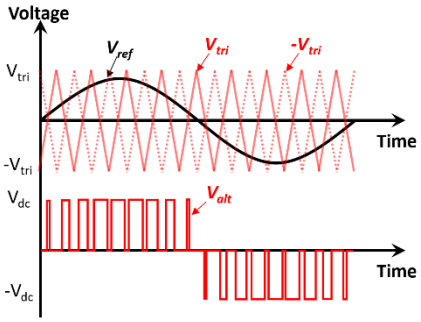

Fig. 6. Three-level switching waveform.

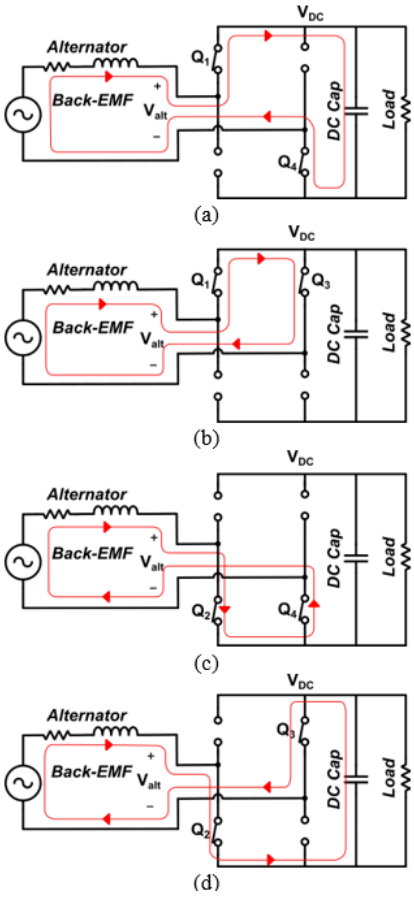

Fig. 7. Three-level switching schemes: (a) Q_1 and Q_4 are turned on (V_{alt}=V_{DC}), (b) Q_1 and Q_3 are turned on (V_{alt}=0), (c) Q_2 and Q_4 are turned on (V_{alt}=0), and Q_2 and Q_3 are turned on (V_{alt}=-V_{DC}).

TABLE IV. Summary of second generation DCC lessons learned.

Topic	Lesson Learned	Implementation
ASC	Inductor characterization is important.	Perform impedance sweep on each alternator when the convertor is received.
Controller	H-bridge switching techniques can impact alternator loss.	Change from 2-level to 3-level H-bridge switching in the DCC.
Modeling	Inductor characterization data should be included in the model.	Perform impedance sweep on each convertor and include it in the model.
Testing	Select a power meter with a high enough bandwidth so that the high-frequency component is measured.	Select a power meter with a bandwidth up to 1MHz.

IV. Third Generation DCC

This section describes the development and testing of the third generation of the DCC.

IV.A. Development

IV.A.1. H-Bridge Switching

The DCC was upgraded to use 3-level H-bridge switching and was tested with the ASC-E2's and ASC-E2/E3 (77-turn) to verify that 3-level H-bridge switching reduced the DC output power loss.

IV.A.2. Shunt

Approximately 2 W was dissipated in the shunt resistor when connected to the spacecraft at 36 V because H-bridge ripple exceeded the shunt trip point voltage at high spacecraft bus voltage. APL added capacitance to the H-Bridge node to reduce ripple so that the shunt was not activated. In addition, observation of the second generation DCC design noted that when connected to a spacecraft bus at higher load voltages, current ripple was increased. Under that condition there was insufficient voltage across the output stage, so it started to drop out of regulation. The added capacitance held enough charge so that the output stage always stays in regulation. Another benefit of additional H-Bridge capacitance is that convertor input power to the controller is better isolated from spacecraft load voltage variation. The underlying controller PWM algorithm in use since the first generation DCC reduces load voltage impact by correcting for some error caused by H-Bridge shoot through when the alternator voltage is near 0. The capacitance added to the third generation DCC improves output regulation at all bus voltages and thus further isolates the convertor from spacecraft load variations.

IV.A.3. Additional Functions

Two additional functions were added to the third generation of the DCC. These include expanding the convertor operating frequency range and phase adjustment. The extended frequency range will allow operation with additional types of convertors. A capability was added to

allow up to ±180° phase difference between the two convertor channels. The phase control capability could be helpful in reducing vibration induced by mismatch between the two convertors controlled by the DCC.

IV.B. Testing

Three main tests were performed with the third generation of the DCC with a pair of ASC-E2s (55-turn) and a pair of ASC-E2/ASC-E3 (77-turn). The tests include characterization, phase adjustment, and fault testing.

IV.B.1. Characterization Testing

Characterization testing of the DCC was performed with a pair of ASCs with 55-turn alternators and then repeated for operation with a pair of ASCs with 77-turn alternators.

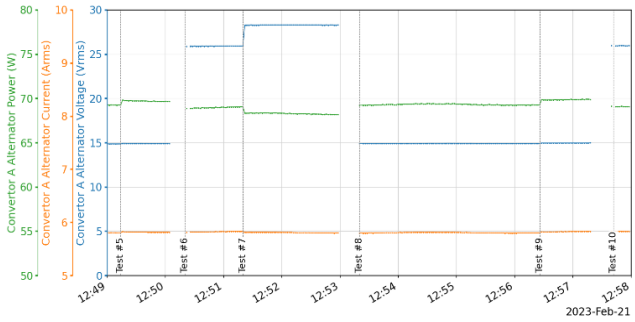

Fig. 8. Characterization testing alternator data, 77-turn alternators, 28 V spacecraft bus voltage.

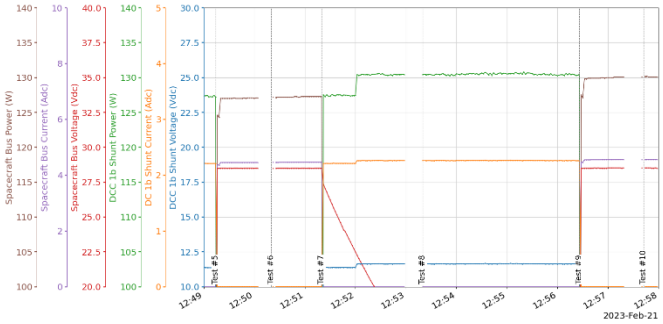

Fig. 9. Characterization testing DCC output data, 77-turn alternators, 28 V spacecraft bus voltage.

Characterization testing was performed over the spacecraft operating bus voltage range between 22 and 36 V, while connected to the spacecraft load, disconnected from the spacecraft load, DCC backup board power on and off, DCC fault detection on and off, and the power meter line filter on and off. A summary of the combinations of testing are shown in Table VI. Collecting data while connected and not connected to the spacecraft load gives some insight into the buck convertor efficiency. Testing with the DCC backup power on and off allows for calculation of the amount of power used by a warm (powered) backup board.

Figures 8 –9 and 10-11 show the performance of the DCC while operating 77-turn ASCs and 55-turn ASCs respectively. Table VI summarized the DCC configuration for each test number. The results presented are for 28 V spacecraft bus voltage. Tests performed at spacecraft bus voltages of 22, 34, and 36 V produced similar results and are not presented in this paper. Gaps in the data are due to stopping the LabVIEW data acquisition system while turning the power meter line filter on and off. The alternator voltage reads 28V during the tests when the line filter is turned off due to lack of filtering on the signal. The ramp down in DC bus voltage, after test #7, is due to the dc bus cap discharging. The data shows that when the DC output is connected to the spacecraft, the external shunt is not dissipating power. When the DC output is not connected to the spacecraft, all power is dissipated in the external shunt resistors.

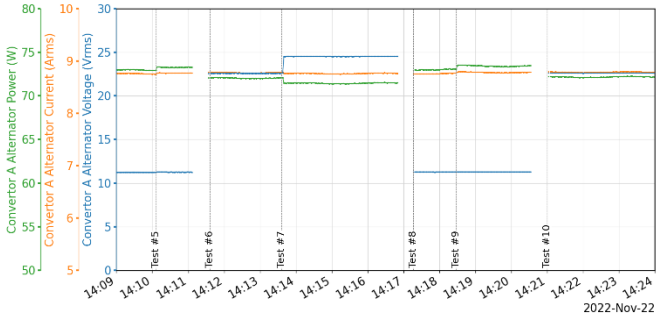

Fig. 10. Characterization testing alternator data, 55-turn alternators, 28 V spacecraft bus voltage.

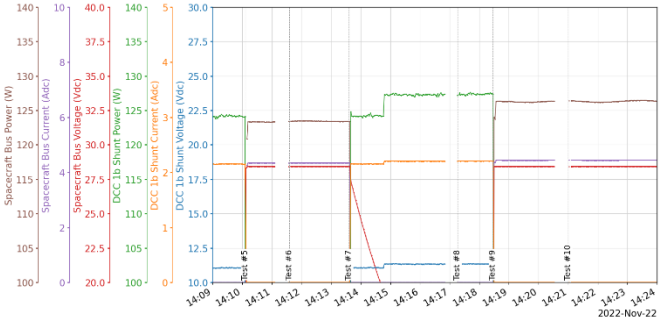

Fig. 11. Characterization testing DCC output data, 55-turn alternators, 28 V spacecraft bus voltage.

Table V summarizes the testing and some calculations from the data. DCC output power represents either power dissipated in an external shunt resistor or power being delivered to the spacecraft bus, represented by a DC electronic load in the test rack. DCC power loss is calculated as the difference in the input power at the DCC and the output of the DCC. Alternator core loss for operating with 77-turn ASCs was on average 1.5 W and for 55-turn ASCs an average of 2.5 W. The DCC efficiency is calculated as the DCC output power divided by the DCC

input power. The DCC efficiency is higher when operating ASCs with 77-turn alternators versus 55-turn alternators due to the lower alternator current. The highest efficiency is when operating with the backup DCC board not powered, the backup DCC board consumes approximately 3 W. The efficiency is higher when not connected to the spacecraft bus since the output regulator is not operating.

TABLE V. Third generation DCC efficiency.

Test # from Plot	Backup DCC Card Powered	On the S/C Bus	DCC Fault Detect	Power Meter Line Filter	DCC Eff. (%) 77-turn alt.	DCC Eff. (%) 55-turn alt.
5	Yes	Yes	On	On	88	86
6	Yes	Yes	On	Off	89	87
7	No	No	Off	Off	92	91
8	No	No	Off	On	91	89
9	No	Yes	Off	On	90	88
10	No	Yes	Off	Off	91	89

IV.B.2. Phase Testing

The third generation DCC had a new function added to change the phase of convertor B relative to convertor A. DCC phase adjustment capability allows for setting the phase to minimize vibration between convertor A and convertor B. The goal of phase testing with the DCC was to verify that the command for phase adjustment worked properly and the test was not intended to reduce the vibration between the convertors. For this test, the phase of the alternator current was changed from 0.1° to 10°. The phase adjustment commanding worked as expected

IV.B.3. Fault Testing

Table VI describes the faults tested with the third generation DCC. Figure 12 shows the results from simulating a short in the left upper FET of the H-bridge. All faults listed in Table VII produce similar results to those shown in Figure 12. During a fault, the DCC will switch control from the primary board to the backup board. During fault testing of the second-generation controller, DCC 1b was the primary board and DCC 3b was the backup. When the FET short fault was executed, the scope trace below shows that the DCC 3b H-bridge volage increases and the DCC 1b H-bridge voltage decreases indicating that DCC 3b is the primary controller board. The convertor A piston position and convertor B piston position increase slightly during the switchover but remains stable and there was no overstroke of the convertors. Convertor A alternator current and convertor B alternator current also increase slightly but remain stable. All faults were tested successfully. Fault testing of the third generation DCC had similar performance.

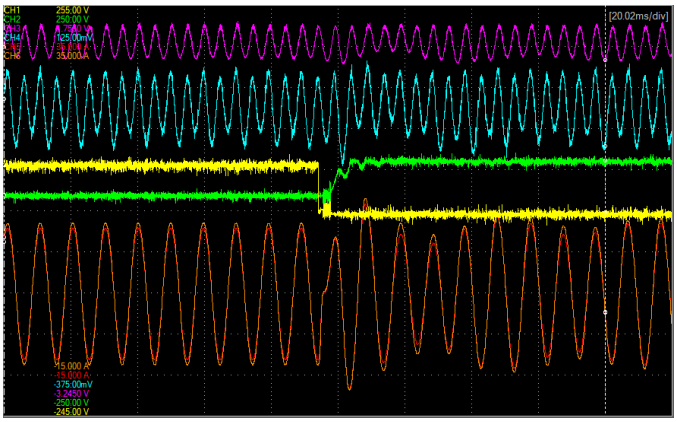

Fig. 12. Oscilloscope trace for H-bridge left upper FET short. Legend: green (DCC 3b H-bridge voltage), yellow (DCC 1b H-bridge voltage), pink (convertor A piston position), blue (convertor B piston position), red, (convertor A alternator current), orange (convertor B alternator current).

TABLE VI. Description of DCC fault injection capabilities.

Fault	Description
Emergency Shunt PWM FET Open	Demonstrates no load for convertor output power while not supplying power to the spacecraft. Equivalent to disconnecting the Stirling convertor from all loads. Control switches to the backup board.
Emergency Shunt Short	Demonstrates a short in the emergency shunt PWM FET. Control switches to the backup board.
Convertor A/B AC Breaker, Open	Demonstrates the AC breaker is open. Control switches to the backup board.
Convertor A/B, H-Bridge FET Short/Open	Demonstrates a short or open in any of the four H-bridge FETS for either convertor A or B. Control switches to the backup board.
Interlock	Demonstrates convertor control is maintained if there is a fault in the communication between DCC sides.

V. Future Work

Plans have been made to operate both a single and dual-opposed pair of Sunpower Robust Stirling Convertors (SRSC) [1] with the DCC. The SRSC, Sunpower's latest convertor design, was developed as part of the DRPS project. The DCC was not designed for use with the SRSC, but its alternator voltage and operating frequency is within the allowable range of the DCC. This test will verify that the DCC can control the SRSC at full convertor power

output with a single SRSC and then a dual-opposed pair of SRSCs. After operation of the DCC with a dual-opposed pair of SRSCs is confirmed, a test is being considered to operate two pairs, four SRSCs, with two fault-tolerant DCCs. This test would be performed with the DRPS testbed designed by GRC [1]. The DRPS testbed would be modified to operate with the SRSCs. The purpose of this test would be to verify operation of a flight-like controller with two pairs of Stirring convertors. This would be the first test of its kind.

VI. Conclusions

An extensive effort has been made to improve the DCC for operation with Stirling convertors. Three generations of the DCC were developed as lessons were learned and implemented. The first generation DCC produced a large, 5A, output current ripple. This was addressed in the second generation of the DCC along with changing the output buck regulator design to accommodate operation of higher voltage ASCs. Testing of the second generation of the DCC revealed that the DCC output produced 9 W less power than expected. An extensive investigation of the power loss resulted in several lessons learned that were implemented in the third generation of the DCC. The third generation DCC also incorporated two new requirements identified by the project: increasing the convertor operating frequency range and convertor phase adjustment capability. Testing of the third generation DCC, showed that the power loss issue was reduced and resulted in the most efficient version of the DCC. Table VII summarizes DCC generation's efficiency. Significant improvement was made in the third generation DCC efficiency.

TABLE VII. DCC efficiency comparison.

DCC	Efficiency (55-turn)	Efficiency (77-turn)
First Generation	82-84%	N/A
Second Generation	71-74%	N/A
Third Generation	86-91%	88-92%

ACKNOWLEDGMENTS

This work is funded through the NASA Science Mission Directorate. Thank you to Chris Barth at NASA GRC and Marty Fraeman at APL for the review of this document.

REFERENCES

1. S.M. Oriti, E. Wozniak, M. Yang, "Status of Dynamic Radioisotope Power System Development for NASA Missions", Nuclear and Emerging Technologies for Space 2023, Idaho Falls, Idaho, May 7-11, 2023.
2. G.M. Dugala, M. Fraeman, D. P. Frankford, D. Duven, A.Shamkovich, H. Ambrose, D. W. Meer: "Small Radioisotope Power System at NASA Glenn Research Center," AIAA paper 2011, 9th International Energy Conversion Engineering Conference, San Diego, California, July 31- August 3, 2011.
3. G.M. Dugala, M.E. Bell, S.M. Oriti, M. Fraeman, D. P. Frankford, D. Duven,: "Small Radioisotope Power System Testing at NASA Glenn Research Center," AIAA paper 2013, 11th International Energy Conversion Engineering Conference, San Jose, California, July 15-17 3, 2013.
4. Holliday, E.S., "Controller Computing a Virtual Tuning Capacitor for Controlling a Free-Piston Stirling Engine Driving a Linear Alternator," U.S. Patent 7,511,459, March 31, 2009.
5. Dennis J. Duven, Hollis H. Ambrose, Martin E. Fraeman and David P. Frankford, "Performance Analysis of a Fault Tolerant Controller for a Single Stirling Convertor", AIAA paper 2013, 11th International Energy Conversion Engineering Conference, San Jose, California, 15-17 July 2013.
6. Gina M. Dugala, Linda M. Taylor, Mark E. Bell, James L. Dolce, Martin Fraeman, and David P. Frankford, "Advanced Stirling Convertor Dual Convertor Controller Testing at NASA Glenn Research Center in the Radioisotope Power Systems System Integration Laboratory", AIAA paper 2015, Propulsion and Energy Forum, Orlando, FL, 25-27 July 2015.
7. Frankford, D.P., Ambrose, H.H., Duven, D.J., Fraeman, M.E., and Adams, J.D., "Real-Time Electrical Advanced Stirling Convertor Simulator," Nuclear and Emerging Technologies for Space (NETS) 2015, February 2015.
8. Dugala, G.M., "Stirling Convertor Controller Development at NASA Glenn Research Center," AIAA Propulsion and Energy Forum, pp. 9-11, July 2018