**PL&HA**

Precision Landing and Hazard Avoidance

Safe and Precise Landing – Integrated Capabilities Evolution

# A System to Provide Deterministic Flight Software Operation and Maximize Multicore Processing Performance: The Safe and Precise Landing – Integrated Capabilities Evolution (SPLICE) Datapath

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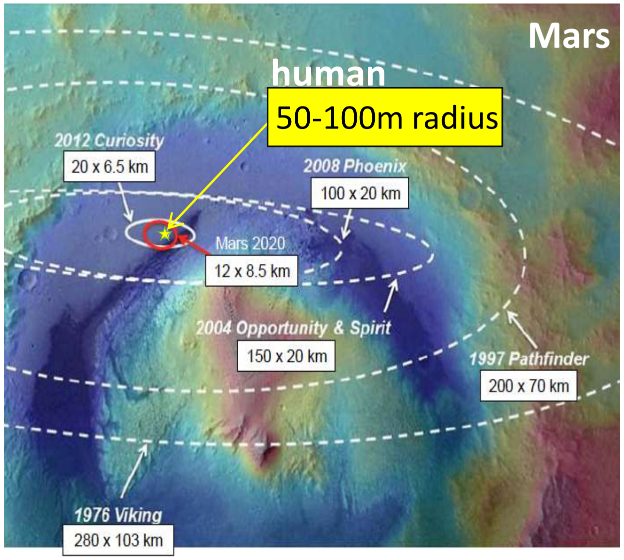
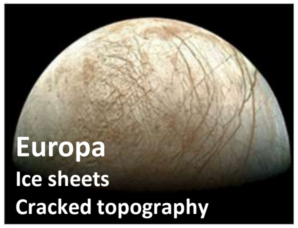
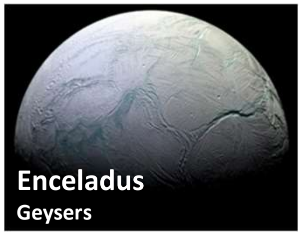
# The Motivation for PL&HA Technology

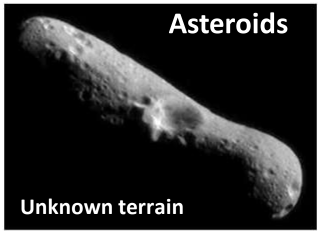
- Enable landing at locations that pose significant risk to vehicle touchdown or payload deployment (including near pre-positioned surface assets)
  - Multicore Processing
  - HPSC
  - Technology development (SPLICE)



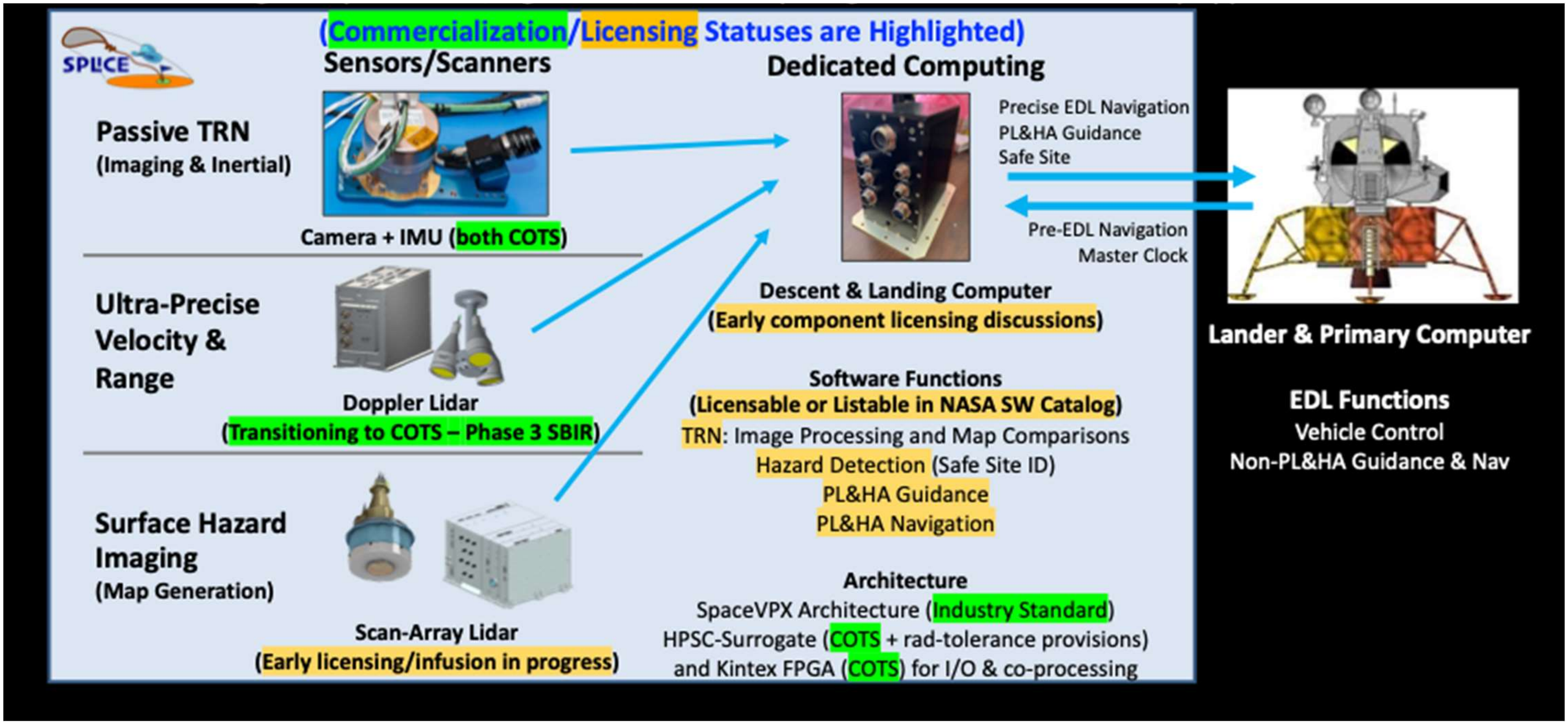


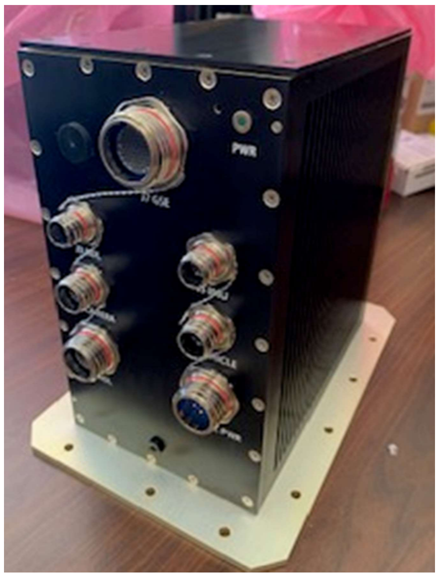



# SPLICE Components

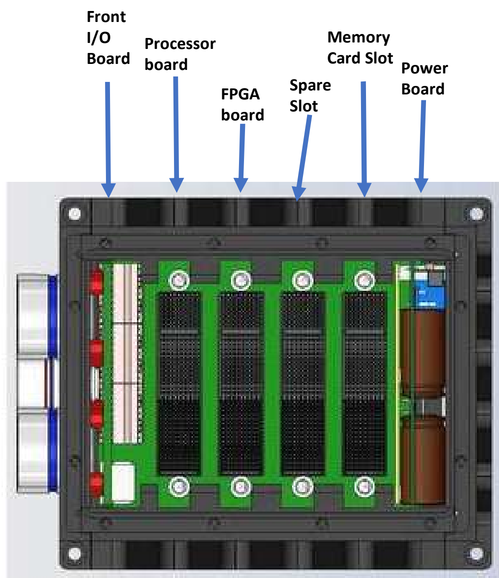


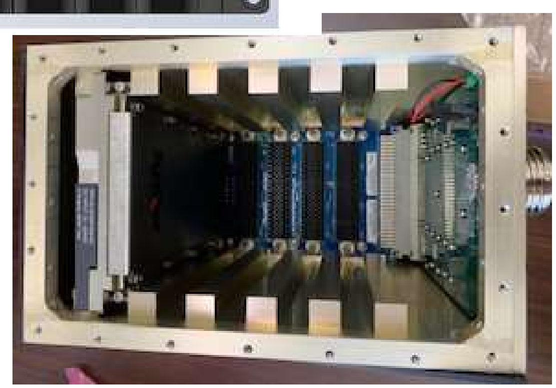
# SPLICE DLC EDU



COTS ½ ATR Enclosure from PIXUS

- 4-slot OpenVPX backplane
- Syncor PSU
- I/O Card with Glenair 805 connectors
- COTS SSD Card from RedRock



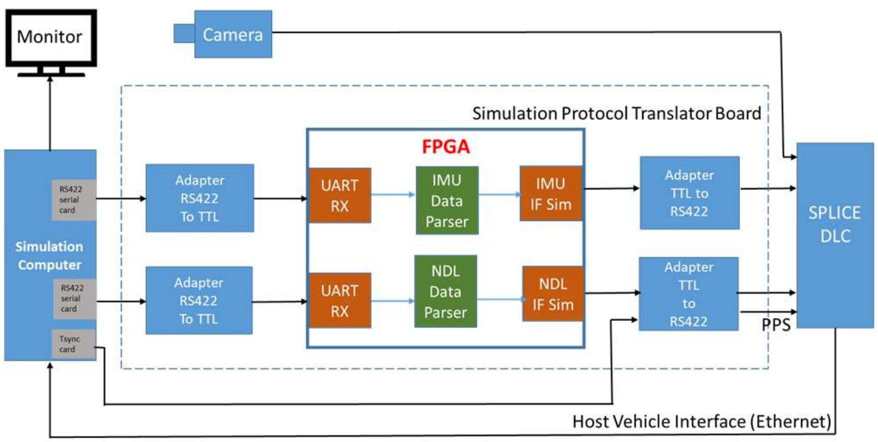



In-House Design &Development:

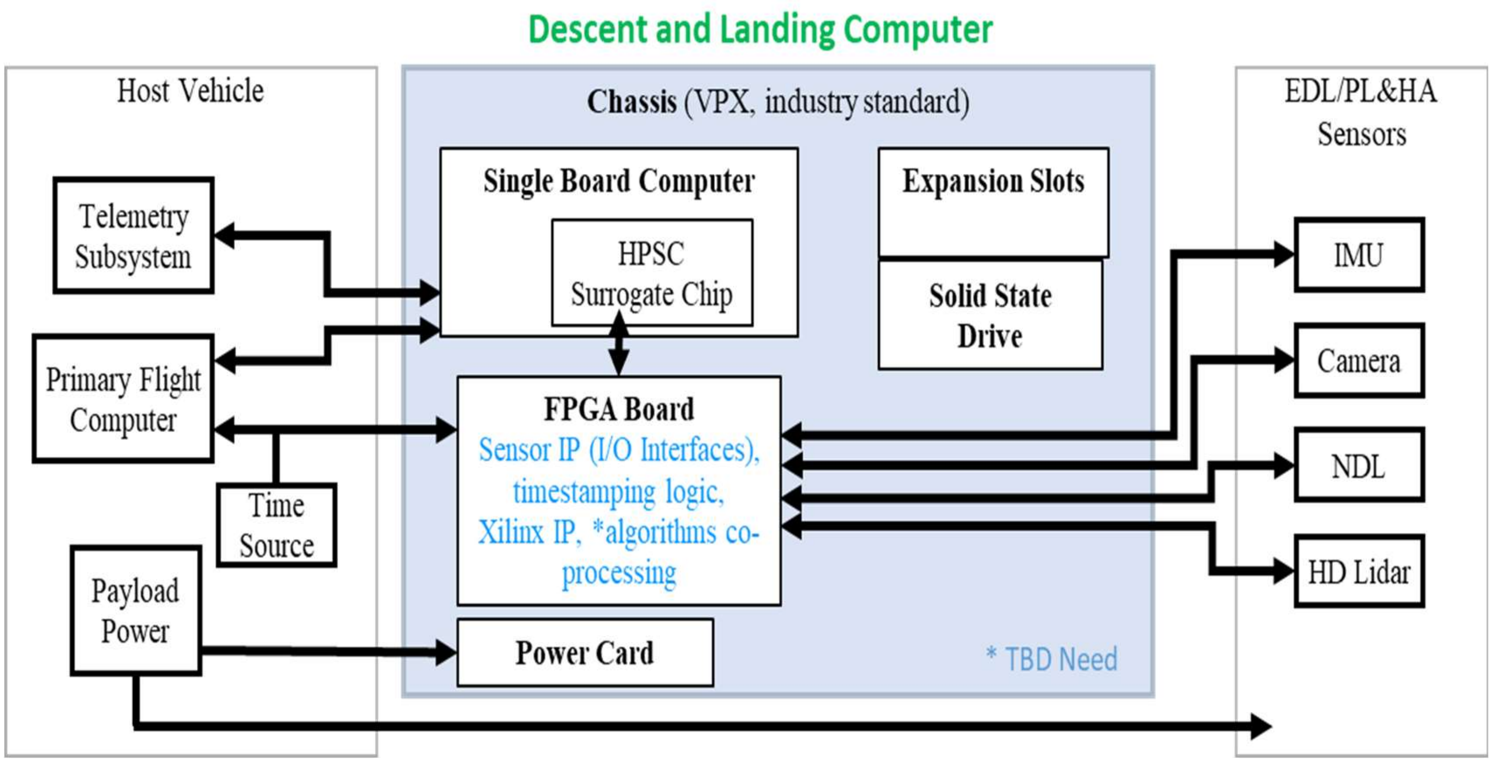
- Xilinx US+ MPSoC board
- Xilinx US Kintex FPGA board

# EDU Testing

- Suborbital flights on Blue Origin's New Shepherd rocket in 2020 and 2021
- HWIL simulation testing
- Workload performance measurements



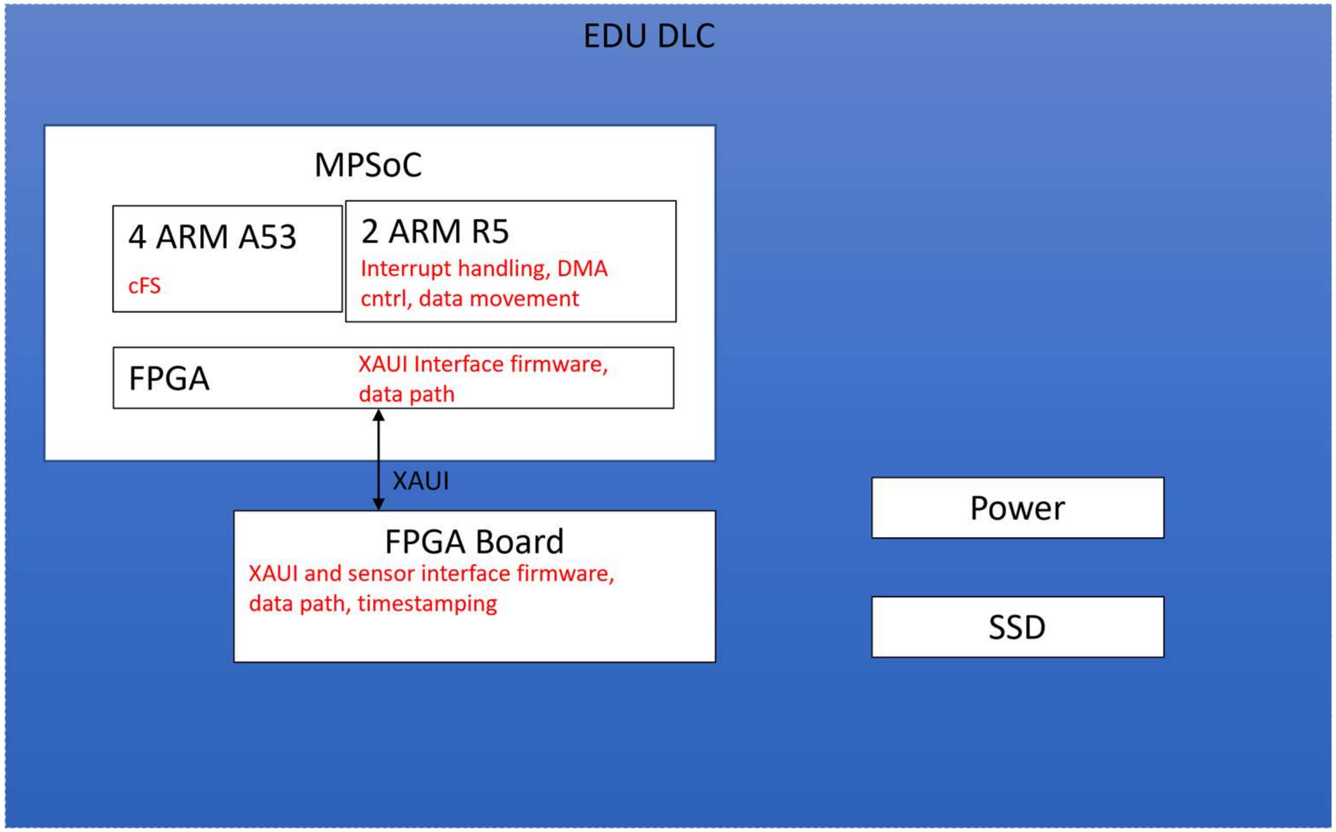

# DLC (EDU) and Interfaces



# PL&HA Sensor Data Bandwidth

| Sensor | Data Rate (Hz) | Packet Size (Bytes) |
|---|---|---|
| IMU | 400 | 48 |
| NDL | 20 | 280 |
| Camera | 10 | 1.6M |
| HDL | 1 | 30M |

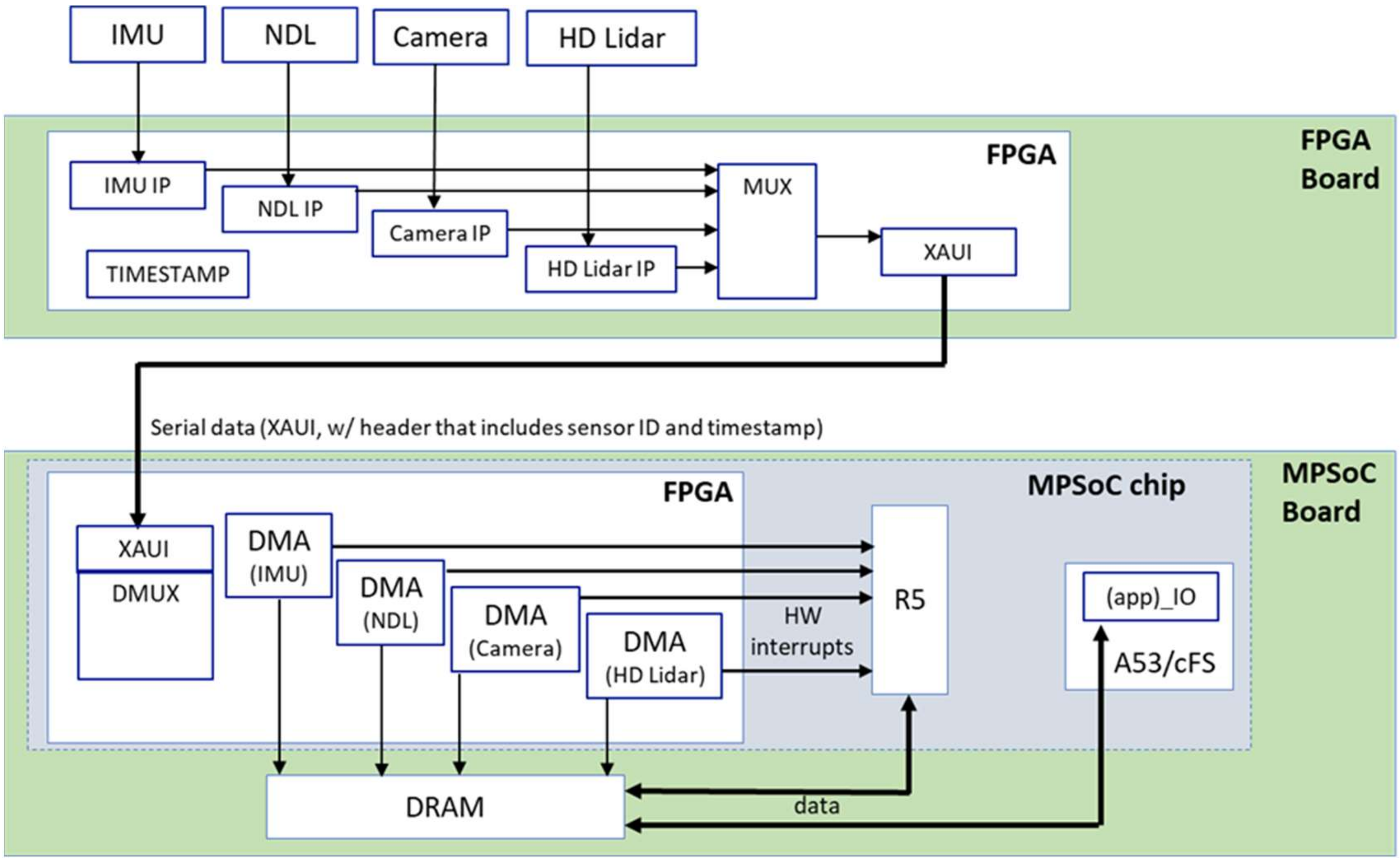
# MPSoC Architecture and Functional Allocations



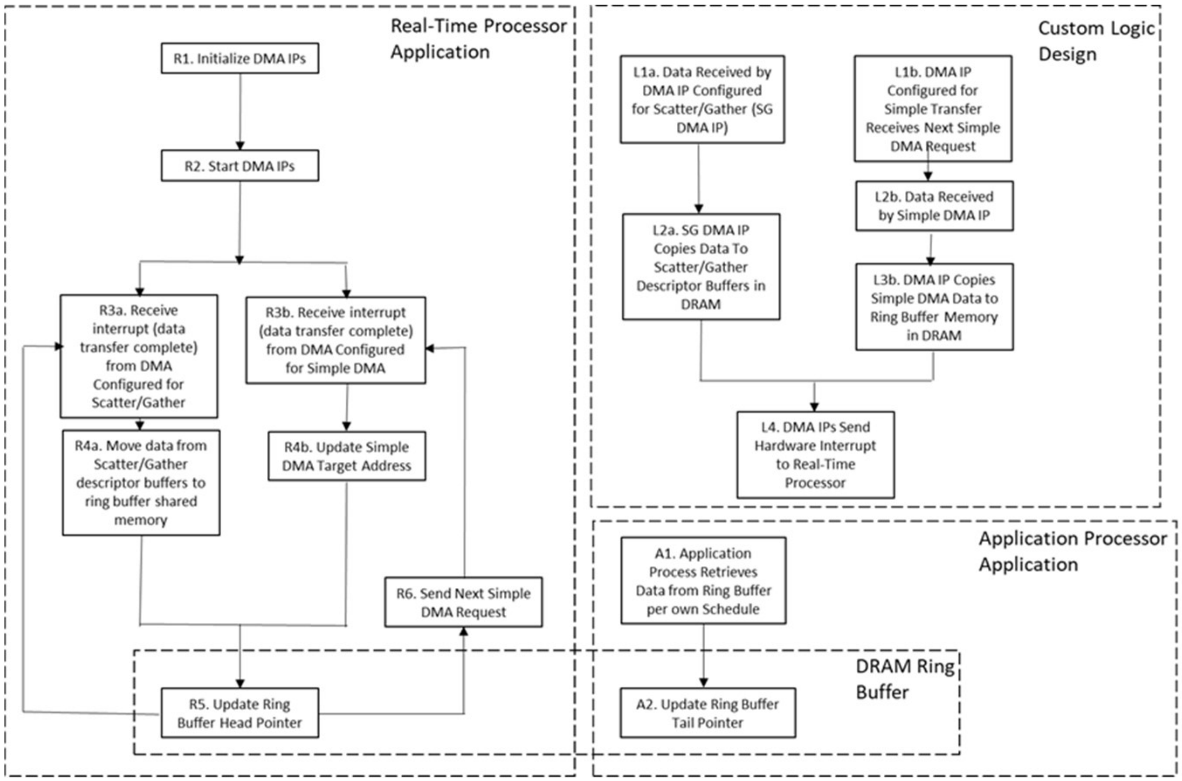
# Related Work

- SPLICE algorithms are complex, and must operate with low latency and deterministically to function in a real-time landing system
- Traditional systems often utilize a Real-Time Operating System (RTOS) to assure required performance
- Approach was to use embedded Linux OS and develop a datapath that isolates the application processors from interrupts associated with the sensor I/O to support deterministic operation.
  - Preserves the full set of application processors for SPLICE software
  - Departs from industry/vendor recommended template to manage communication between heterogenous processors

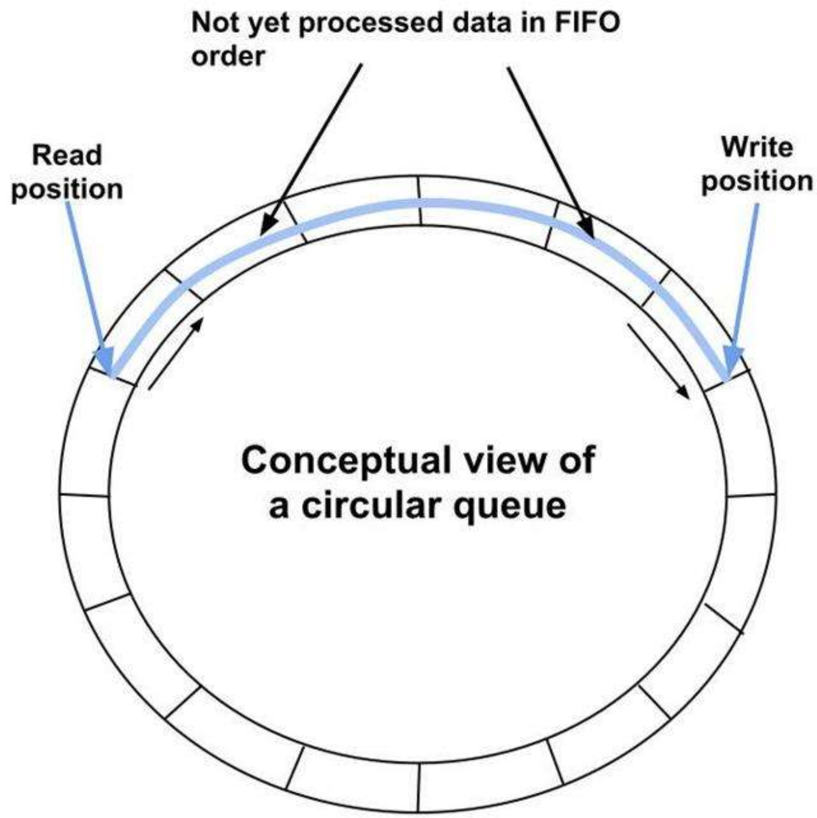
# SPLICE Datapath



# Datapath Event Sequence



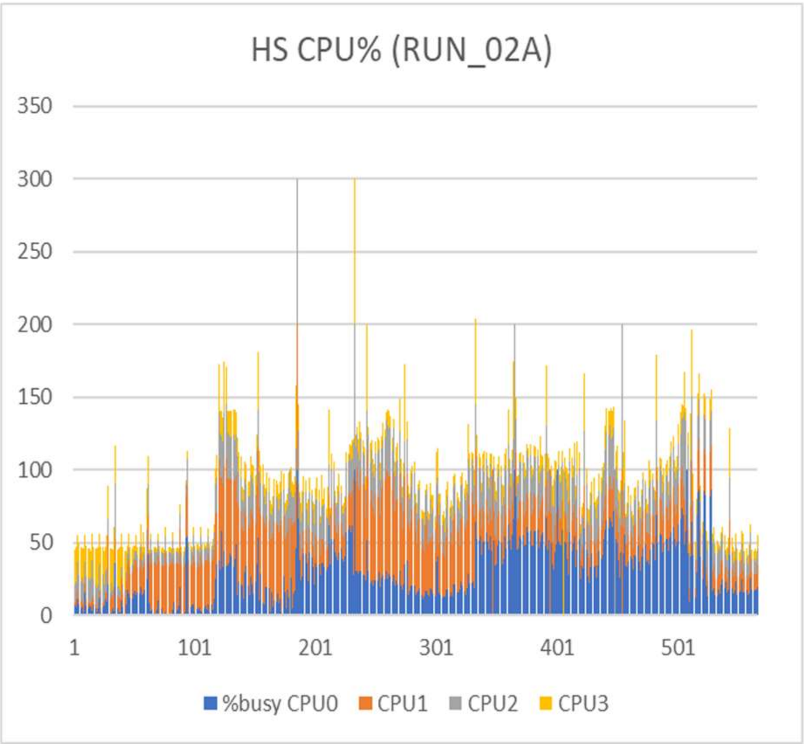
# Ring Buffer Queue

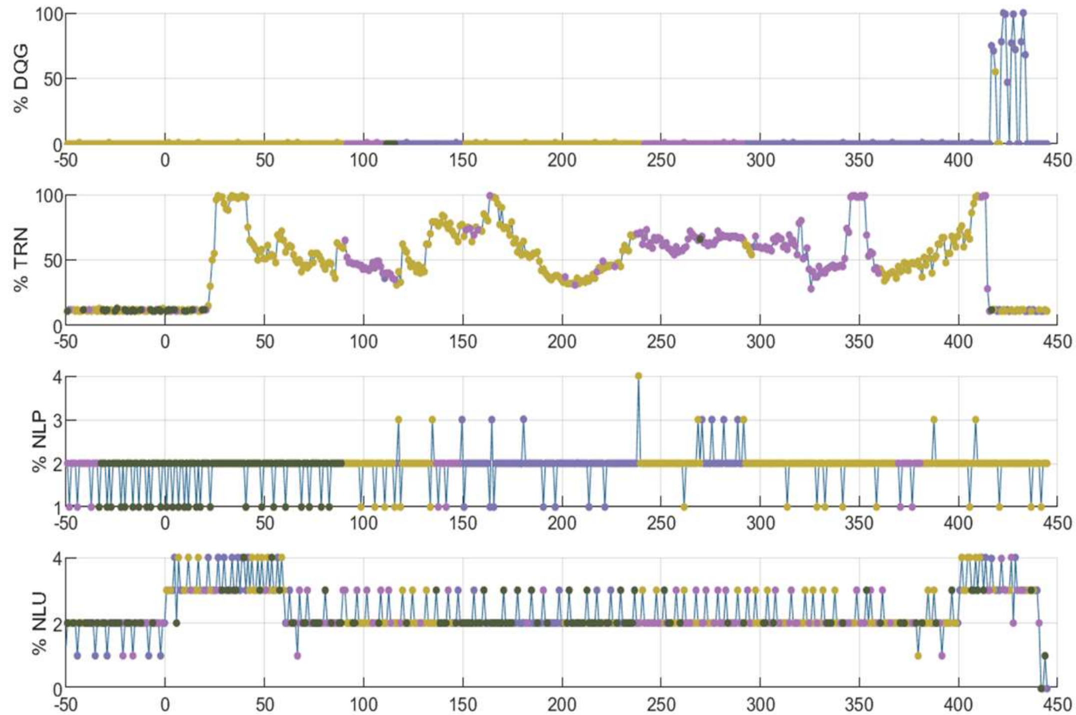


# Discussion

- Experimentation revealed that DMA scatter/gather was not efficient for larger packet size data (e.g. camera). Change to simple DMA increased image data rate from 2 to 10 Hz.
- Data path tested in HWIL simulation for adverse effects on the deterministic operation of the flight software
  - Run for many days straight without data packet drops or corrupted data
  - Over a dozen simulated flights using trajectories from flight tests showed no behavior that could be attributed to the datapath operation that was non-deterministic

# EDU DLC Processor Utilization During Simulated SPLICE Flight



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# Conclusions/Future Work

SPLICE

- Testing of the SPLICE EDU data path indicate that the design supports deterministic flight software operation while preserving application computing capacity on the DLC platform.
  - Accomplished without the use of a real-time operating system
- The data path design is being used in the next version of the DLC that is being developed to support a robotic lunar test flight.
  - Additional channels are being added for the Hazard Detection LIDAR sensor and a vehicle interface
  - Enhancements will be made to the command path of the interface (not discussed here.)