Design and Performance of the Hitomi/XRISM Adiabatic Demagnetization Refrigerator Controller

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ABSTRACT

The Resolve instrument in the recently launched X-ray Imaging and Spectroscopy Mission (XRISM) is a rebuild of the Soft X-ray Spectrometer (SXS) in Hitomi (aka Astro-H which had an unfortunately brief mission life in 2016). Resolve is a high-resolution non-dispersive soft x-ray spectrometer from nominally 0.3 keV to 12 keV based on a calorimeter detector array operating at 50 mK with a resolution better than 7 eV FWHM at 6 keV. For such sensitive cryogenic instruments, temperature stability has a strong impact on the detector's performance.

The Adiabatic Demagnetization Refrigerator Controller (ADRC) in the XRISM Resolve instrument is the electronics box (ebox) responsible for the high-precision sub-K temperature readout and control of the multi-stage Adiabatic Demagnetization Refrigerator (ADR) subsystem. To achieve the science objectives stated above, the ADRC must provide a thermal stability better than 2.5 μK RMS (over a 10-minute interval) for the calorimeter detectors in both cryogen (liquid helium) and cryo-free modes. The ADRC has direct telemetry/command and power interfaces with the spacecraft and also provides sensor read-out and heater circuits for decontamination of the filters in the cold aperture.

As a part of the discussion on the design and performance of the ADRC, this paper will also include an overall view of the 50 mK temperature control, plus monitor and control of the aperture filter temperature for de-contamination purpose.

Keywords: ADRC, ADR controller, thermal stability

1. INTRODUCTION

The Resolve instrument is a collaboration between JAXA and NASA Goddard Space Flight Center with contributions from SRON and ESA. NASA provides the Aperture Assembly (ApA, including filters), the ADRC, the X-ray Box (XBOX), the X-ray Mirror Assembly (XMA), and the XMA harnesses, in addition to the Calorimeter Spectrometer Insert (CSI) which includes the Detector System (DS), the 3-stage ADR, and the High Tc Superconductor leads (HTS). The CSI and ApA are integrated in a dewar provided by JAXA's contractor Sumitomo Heavy Industry. The ADRC and XBOX are mounted on the spacecraft panel in the same area with other JAXA-provided Resolve electronics. The XMA is mounted on top of the fixed optical bench (FOB). Figure 1a shows the locations of the Resolve dewar and electronics boxes in a model view of the XRISM spacecraft. Figure 1b shows the nominal relative position of the ADRC from the dewar (in a photograph of the instrument level test set up). Figure 1c shows a photograph of the ADRC.

X-ray photons become current pulses from calorimeter detectors measuring induced temperature changes in the absorbers. The detector array is mounted inside the calorimeter thermal sink (CTS) [1] which is thermally connected to the cold stage (or first stage) of the 3-stage ADR. Temperature stability for detectors is crucial in this sensitive cryogenic soft x-ray spectrometer. The driving CTS thermal stability requirement for the Resolve instrument in XRISM is 2.5 μK RMS (over a 10-minute interval) at 50 mK. This is the same as Hitomi and amounts to 1.5 eV error contribution in the detector resolution budget. Listed below are three aspects to be considered simultaneously in the design of the ADRC, assuming reasonable environment control and stability.

1) Read out with sufficient accuracy
2) Control with sufficient resolution
3) Control algorithm with proper gain

Transmission of x-ray photons at energy below 3 keV through the aperture filters is reduced severely in presence of contamination by hydrocarbons or water ice. The ADRC maintains the temperature of the dewar main shell (DMS) filter at 320 K to prevent accumulation of contaminants from the spacecraft or environment. The ADRC can also elevate the temperature of aperture filters internal to the dewar to remove water ice molecules as needed via voltage control on relevant heaters. The driving requirement to assure filter integrity in the process is achieved via voltage step control to minimize thermal gradient across filters and current limits to prevent overheating.

XRISM has a requirement on science observation efficiency (≥ 90%). Science observation efficiency is the ratio of duration when detectors are thermally stable for science observations (i.e., the Resolve instrument meeting the CTS thermal stability requirement) relative to the overall duration of ADR operation (i.e., the Resolve instrument in nominal operation). Many factors can impact this observation efficiency. [2-4] All ADR cycling (and filter heater operations) is fully autonomous after initiation by commands for efficient space operations.

2. DESIGN IMPLEMENTATION FOR THERMAL STABILITY

The primary goal for the ADRC is to maintain the CTS at 50 mK with a stability requirement of is 2.5 μK RMS (over 10-minute interval). This section will describe implementations for the three aspects mentioned in the Introduction.

2.1 Sensor read out with sufficient accuracy (1.0 μK RMS)

2.1.1 Calibrated sensors

All thermometers (for both monitor and control) in the ADR, ApA, DS, and HTS subsystems are calibrated sensors selected for sensitivity in particular operation ranges for the hardware implementation.

2.1.2 Four-wire measurement

Every sensor is wired for the sensitive four-wire measurement to compensate for lead resistance. These are coordinated in advance among the subsystems including the harness design.

2.1.3 Independent current source for each sensor

Each sensor is stimulated by its own dedicated quiet AC source from the ADRC (in contrast to a DC current source in typical implementation). Stimulus current is applied to all sensors simultaneously to maintain constant self-heating. More details on the current source are described in section 3.2.1 and 3.2.2 for the AMC TM and control circuits.

2.1.4 Temperature Monitor (TM) calibration

TM calibration is essential in the sensor readout process by autocorrelation. Each channel has a dedicated precision resistor for either calibration purpose or to remove current stimulus for the particular sensor. The selection of the calibration resistor or sensor is switched via a series of mechanical relays. Figure 2a shows the calibration sequence. Figure 2b shows the result in which a sensor voltage signal is in phase with the TM sin/cos data in EEPROM after a phase adjustment in the stimulus current source sine wave. Numerically, this means a minimum value for the cosine (or real part) of the autocorrelation result. A calibration factor is determined by the ratio of the accumulated sum through the modified autocorrelation algorithm to the known resistance of the calibration resistor. The calibration process also includes a 0-ohm offset, i.e., a resistance measurement at zero current, which is stored for each channel and applied to subsequent measurements.

2.1.5 Readout by autocorrelation

The voltage waveforms for each thermometer are independently amplified, filtered, and then summed to form a composite waveform. The composite waveform is then sampled by a 16-bit DAC. A modified autocorrelation algorithm (similar to a Discrete Fourier Transform) is then used to process the composite waveform samples into resistance measurements at a nominal cadence of 1 HZ. Nominally, resistance measurements are produced once per second, but a dwell function is also employed to allow for 2, 4 or 8 second averaging should a channel become noisy.

2.1.6 Monitor channels (in groups of 8) are multiplexed.

At the end of TM calibration, the MUX tables are set for TM channels. Cold AMC uses 2 MUX tables, one each for 50 mK operation and ADR cycling. Nominally, all 8 TM channels are processed simultaneously, but a MUX table is employed to allow for channels to be processed separately or in groups.

2.1.7 Control channels (CTL) are read out independently

Each AMC has 2 CTL sensor readout circuits. The CTL sensor readout circuits use an algorithm similar to the TM circuit, but readout a single thermometer. Each circuit has relays to choose between two control thermometers (i.e., primary and redundant) and a calibration resistor.

2.2 ADR magnet control with sufficient resolution (1.0 μK RMS)

2.2.1 Dedicated quiet DC voltage source for each ADR magnet

Each AMC card provides a dedicated magnet driver voltage source capable of driving 2.1 A while holding 1 V at the magnet. The magnet driver has fly-back protection through a series of power diodes to prevent high voltages from building up in the event of unexpected loss of power.

2.2.2 PID feedback control to a single point

A Proportional Integral Derivative (PID) control loop is used to control the ADR magnet current or temperature via magnet voltage control. Each ADR stage has a dedicated PID controller. Figure 3 shows a PID loop for a single ADR. All PID terms are fully programmable.

2.2.3 Magnet voltage source is adjustable to 30 μV resolution

To achieve the CTS thermal stability at 2.5 μK, the cold stage ADR magnet control needs to achieve 1 μK RMS. The Resolve cold stage ADR has a heat load about 0.08 μW which equates to a drift about 0.35 μK/second. The ADR magnet is voltage controlled. For an estimated inductance of 200 H and cooling rate of 1.1 μK/μA, at +/- 1 V max voltage with a 16-bit digital to analog converter (DAC), that means a voltage step size in the order of 30 μV.

2.2.4 Set points were adjusted for predicted thermal change

Enabled by knowledge in the behavior of ADRs, heat switches and environmental parameters, the ADR magnet control algorithm is capable of adjusting the set points to compensate for anticipated changes to minimize control ripples.

2.2.5 Independent control of each heat switch

There are altogether four active gas gap heat switches in the ADR subsystem, and each has two getter heaters (primary and redundant) and two monitoring thermometers. Each heater driver is an independent current source at 500 μA for ~ 0.25 mW of power with a timing-adjustable relay control to select the heater. The current output is filtered to include a transition time constant about 100 msec for on-off state control by the getter temperature set point.

2.2.6 Independent control algorithm for each ADR stage but synchronized for coordination between stages.

The ADR magnet control algorithms (or sequencers) coordinate the independent ADR PID loops and HS operations. For example, in the cryogen-free mode, the second and third stage ADR are coordinated to maintain the temperature at the CSI interface at 1.4 K.

2.3 Control algorithm with proper gain

2.3.1 Tuning of control parameters in representative thermal environment

The performance of the ADR magnet control algorithms depends strongly on the actual hardware implementation and the thermal environment. Tuning of control gain parameters and verification in representative are required for precision and stability.

2.3.2 Fully programmable PID gain terms

The ADR magnet control algorithms initialize and configure all parameters in the PID loops for each ADR stage separately.

2.3.3 Different control sequencers for different operational modes (e.g., helium mode and cryo-free mode)

The ADR magnet control algorithms utilize different PID parameters depending on the thermal environment. Different algorithms are used for the helium and cryogen-free mode. Figure 4a and 4b show the algorithm flow charts.

3. DESIGN IMPLEMENTATION FOR THE ADRC EBOX

The ADRC is composed of a Spacecraft Interface, Temperature Monitor and Heater (SITH) board, three (3) ADR Monitor and Control (AMC) boards, a backplane, and a power supply module. The cold stage AMC card is really two cards due to additional circuitry needed for cold stage control. The ADRC takes its power input from the spacecraft bus and communicates with the spacecraft via a Space Wire Interface. Figure 5a shows a functional block diagram with interface to other NASA subsystems. Figure 5b shows a model view of the ebox configuration.

3.1 Spacecraft Interface, Temperature Monitor and Heater (SITH) board

The SITH board is responsible for initiating all bus communications. It houses two Electrically Erasable Programmable Read-Only Memory (EEPROM) chips, one field-programmable gate array (FPGA) chip, and a variety of discrete components. The SITH board's functions include the telemetry and command (T&C) interface, sequencer State Machines (SM), ADRC system bus arbiter and control, heater and magnet power supply controller, ApA heater drivers and 8 TM channels. The T&C interface is the only means of communication between the ADRC and the spacecraft management unit (SMU) via Space Wire dual ported (DP) Remote Memory Access Protocol (RMAP). The ADRC system bus is used for communication between boards. The ADRC has no micro-controllers. Much of the ADRC's control capability and flexibility results from the implementation of sequencer SMs contained within a FPGA. (A state machine reads a set of inputs and changes to a different state based on those inputs.)

3.1.1 The ADRC system bus arbiter SM

The ADRC system bus arbiter SM manages access to the bus at a 15.6-msec interval via a time slice algorithm and a 32-byte control mux table for the access sequence among six functions. The functions originate from the initialization and control (Init/Ctl) SM, three sequencer SM (0, 1, & 2), status and telemetry limit checking, and Error Detection And Correction (EDAC). Figure 6 shows the block diagram for the ADRC bus system arbiter.

3.1.2 Init/Ctl SM

Upon the ADRC power up or reset, the Init/Ctl SM disables the ADRC system bus arbiter and assumes uninterrupted bus access. The Init/Ctl SM then reads the default telemetry packet and limits from the Defaults EEPROM and initializes the ADRC telemetry table RAM with the contents of the EEPROM. After initialization, the Init/Ctl SM enables the arbiter and begins polling the Ctl First-In/First-Out (FIFO) for incoming Space Wire commands. One command is executed at the start of every 15.6 msec period when the Init/Ctl SM is granted bus access. Figure 7 shows the Init/Ctl SM block diagram.

3.1.3 Sequencer SM

Each of the three sequencer state machines can contain up to 127 command lines and 1 ABORT line and is associated with an external timer and a mailbox register. (This is an improvement from Hitomi's sequencer SM which had only 62 command lines.) The timer action register is for sequencer reference (e.g., for timeout conditions) and does not execute. The mailbox register may be used for sequencer commanding options or status reporting. All three sequencer SMs can be active simultaneously. Figure 8 shows the block diagram for an ADRC sequencer SM. For either the ADR magnet control or filter heater operations, a sequencer program is uploaded to the sequencer SM, and one command line is executed per second. Each command line includes definition of parameters and a function to be executed. The sequencer SM returns to the IDLE state upon completion of the entire program. The ABORT state is unique. If the sequencer SM enters the ABORT state, the abort command line is executed once per second including the associated parameter configuration. The intent is to prevent use of discrete commands until the conditions for ABORT are cleared.

3.1.4 Telemetry and Limits SM

The status and telemetry partition of DP RMAP RAM contains the ADRC status and telemetry packet which can be read via RMAP at any time. The telemetry and limits SM updates the telemetry packet RAM once per second. Any ADRC telemetry point may be included in the packet and have a high and low limit with an associated action on limit violation. Limit checking may be enabled or disabled per register setting. Figure 9 shows the block diagram for the telemetry and limits SM.

3.2 ADR Monitor and Control (AMC) boards

Each AMC board has eight TM channels, four HS controllers, a 2.1-Amp ADR magnet driver, a PID controller for the magnet driver, and two CTL thermometer channels. Each AMC card is capable of driving 4 HS getters simultaneously. The AMC boards have the capability of converting the measured thermometer resistance to temperature. The conversions are done automatically by the AMC FPGA for all CTL and TM channels once per second. The results (in unit of mK) of the conversion are stored in registers accessible via backplane reads. The AMC boards can also convert temperature to resistance. This function is used by the SITH sequencers for PID set point calculations.

3.2.1 TM Circuits

Each AMC card and the SITH Card have an 8 channel TM circuit. The TM circuit nominally measures the resistance of 8 thermometers simultaneously at a nominal cadence of 1 Hz. Each of the 8 sensor is driven by a dedicated AC current source at a unique frequency (within the group of 8). Each frequency value is a prime number to minimize cross talk. The current source peak amplitude is nominally 1 μA, but may be adjusted to 500 nA, 250 nA, or 125 nA. The drive frequencies are synthesized by a 16-bit DAC using samples stored in an EEPROM. The current limiter is a precision 5 MΩ resistor.

3.2.2 Control Thermometer Circuits

The 2 control thermometer readout circuits use the same basic algorithm as the TM circuit described above, but only use a single frequency. Each channel may select 1 of 2 sensor or the calibration resistor via a series of mechanical relays. The same peak current setting of 1 μA, 500 nA, 250 nA, or 125 nA are available for the 2 warmer-stage ADRs. The control channels for the cold stage (50 mK) peak current setting of 12 nA, 6 nA, 3 nA, or 1.5 nA. Nominally the 3 nA setting is used for operations. The control channels use a capacitor for the current limiter.

3.3 Metrology

Each board (SITH and AMCs) has a metrology circuit to monitor the voltages, currents, and temperatures on the board using a dedicated 16-bit ADC at a cadence of 1 Hz. TM calibration is recommended when the ADRC ebox temperature drifts significantly.

3.4 Power supply module (PSM)

The PSM provides the secondary DC voltage to the ADRC and shuts down gracefully outside the normal operating range, including unexpected loss of primary power. The spacecraft bus provides the primary power input to the PSM, nominally 32-52 V. This module includes a sync signal at 132 kHz (+15/-10%). All ADRC power converters are synchronized to the sync signal although the converters can operate normally independent of the sync signal.

4. PERFORMANCE

XRISM is presently in nominal operation. The Resolve instrument commissioning was finished in Feb 2024. A representative graph of the CTS thermal stability well below 2 μK RMS and sometimes below 1 μK RMS during commissioning is shown in Figure 10. In general, the CTS thermometers (control and monitor) follow the same trend although their RMS variations are not consistent. Temperature spikes due to cosmic rays or high energy particles on the thermometers are expected to cause discontinuity in the stability plot although the ADRC control algorithm has implemented a de-glitching routine to ignore the first two consecutive spikes above a threshold temperature change

(equivalent to 50 ohms in resistance). Figure 11 shows a graph on the DMS filter temperature and current. The simple proportional control for the DMS filter at 320 K is stable to better than +/- 0.4 K.

5. LESSONS LEARNED

The ADRs and ADRC in the Resolve dewar environment have worked phenomenally well together to achieve sub-μK stability at 50 mK. Listed below are some findings to aid future design and implementation of a similar instrument.

1) Radio Frequency (RF) switching noise from DC power supplies needs to be minimized to avoid transient fluctuation in self- heating of cold stage thermometers.

2) The control thermometer read out at 50 mK is sensitive to the thermal environment around the detector subsystem. A trade-off needs to be considered among hardware implementation, gain tracking capability in the analysis software, and operations.

3) Temperature spikes resulting from high energy particles on the control sensor were screened via the control sequencer, but that control needs reset after passing through the South Atlantic Anomaly.

6. CONCLUSION

The XRISM Resolve (and the Hitomi SXS) instrument as showcased is the first cryogenic spectrometer in space with sub-μK thermal stability at 50 mK, i.e., a contribution of less than 0.5 eV uncertainty (or error) in the detector resolution. The science observation efficiency is well above the requirement of 90%. The first and second stage ADRs have been cycled in the helium mode successfully more than 120 times either by command or automatically in the past 9 months in orbit.

ACKNOWLEDGEMENTS

The XRISM ADRC is the culmination of design efforts made for and lessons learned from the ASTRO-E, ASTRO-E2, and ASTRO-H missions. The authors would like to thank all those who contributed to those endeavors.

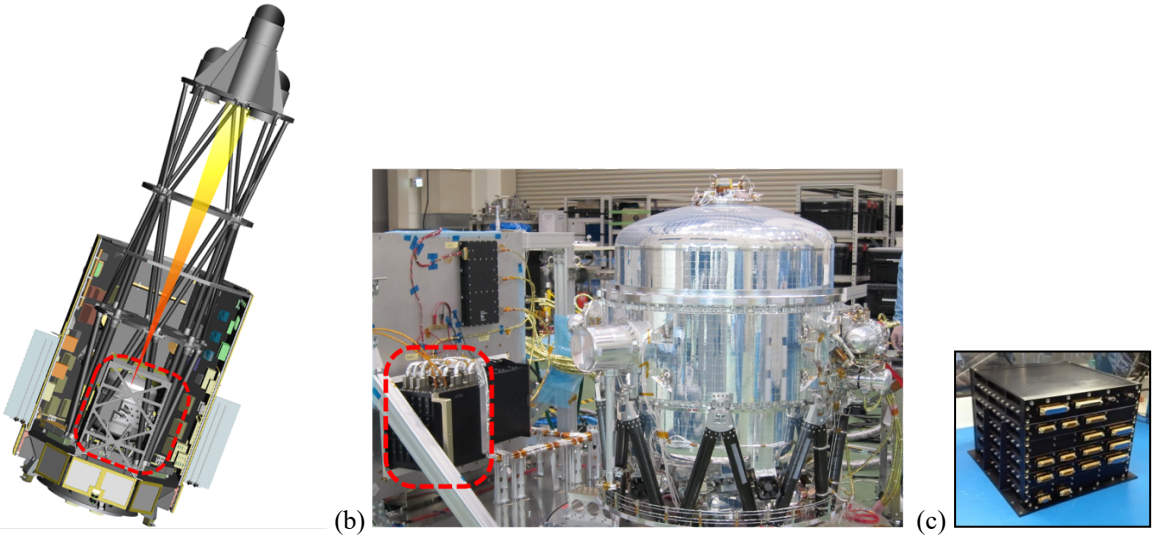
REFERENCES

[1] M. P. Chiao, J. Adams, P. Goodwin, C. W. Hobson, R. L. Kelley, C. A. Kilbourne, D. McCammon, D. S. McGuinness, S. J. Moseley, F. S. Porter, S. Shuman, and T. Watanabe, "System design and implementation of the detector assembly for the Astro-H soft x-ray spectrometer", Proc. SPIE 9905, Space Telescopes and Instrumentation 2016: Ultraviolet to Gamma Ray, 99053M (18 July 2016); https://doi.org/10.1117/12.2231897

[2] F.S. Porter, et al., "In-flight performance of the XRISM/Resolve detector system," Proceedings of SPIE 13093, Space Telescopes and Instrumentation 2024: Ultraviolet to Gamma Ray, paper number forthcoming (15 June 2024).

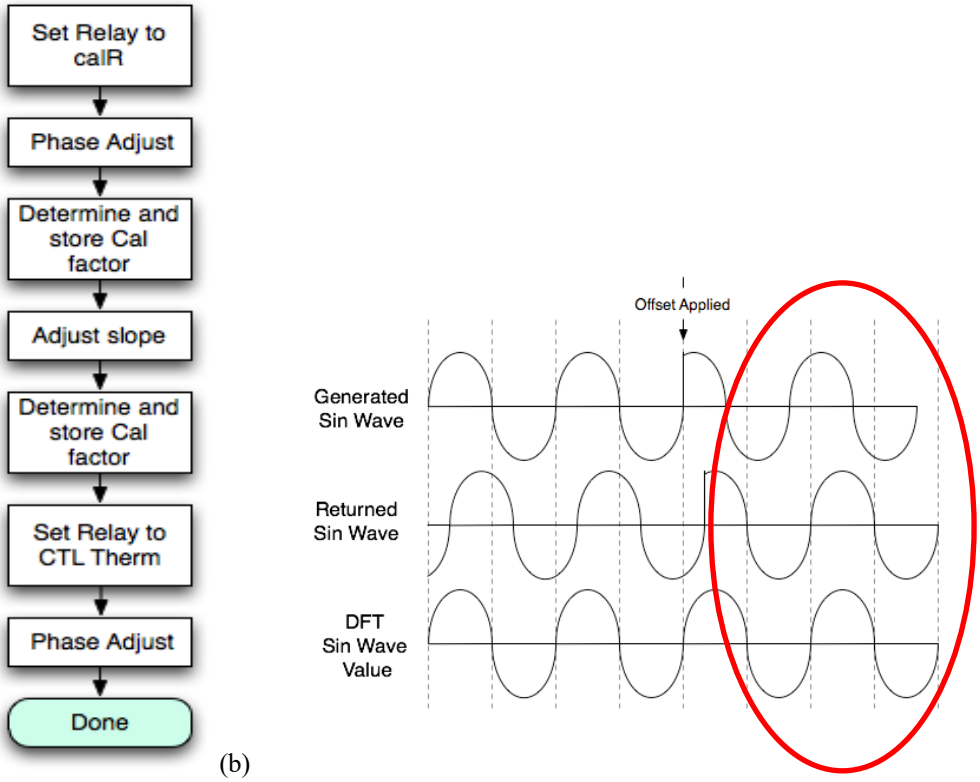
[3] P.J. Shirron, et al., "On-orbit performance of the Resolve Adiabatic Demagnetization Refrigerator on XRISM," Proceedings of SPIE 13093, Space Telescopes and Instrumentation 2024: Ultraviolet to Gamma Ray, paper number forthcoming (15 June 2024).

[4] G. Sneiderman, M. Tsujimoto, F.S. Porter, C.A. Kilbourne, M.P. Chiao, "In-orbit selection of cryocooler drive frequencies for XRISM/Resolve," Proceedings of SPIE 13093, Space Telescopes and Instrumentation 2024: Ultraviolet to Gamma Ray, paper number forthcoming (15 June 2024).



(a) (b) (c)

Figure 1. (a) a spacecraft model, showing the dewar and related electronics in the dashed red rectangle. (b) Resolve instrument test set up, showing the ADRC in the dashed red rectangle. (c) A photograph of the ADRC for XRISM.



(a) (b)

Figure 2. (a) Readout calibration flow chart. (b) Phase adjustment during readout calibration.

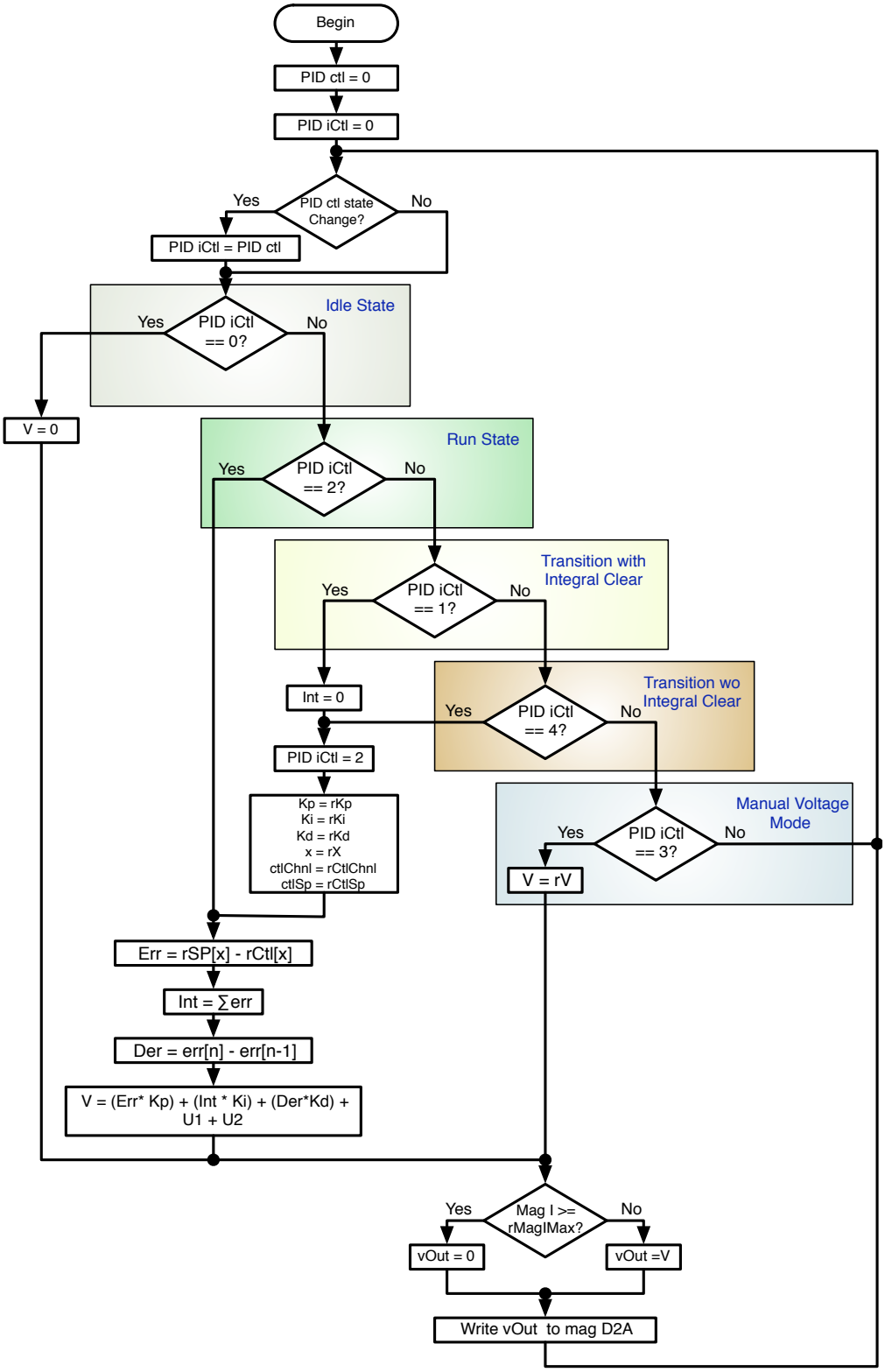
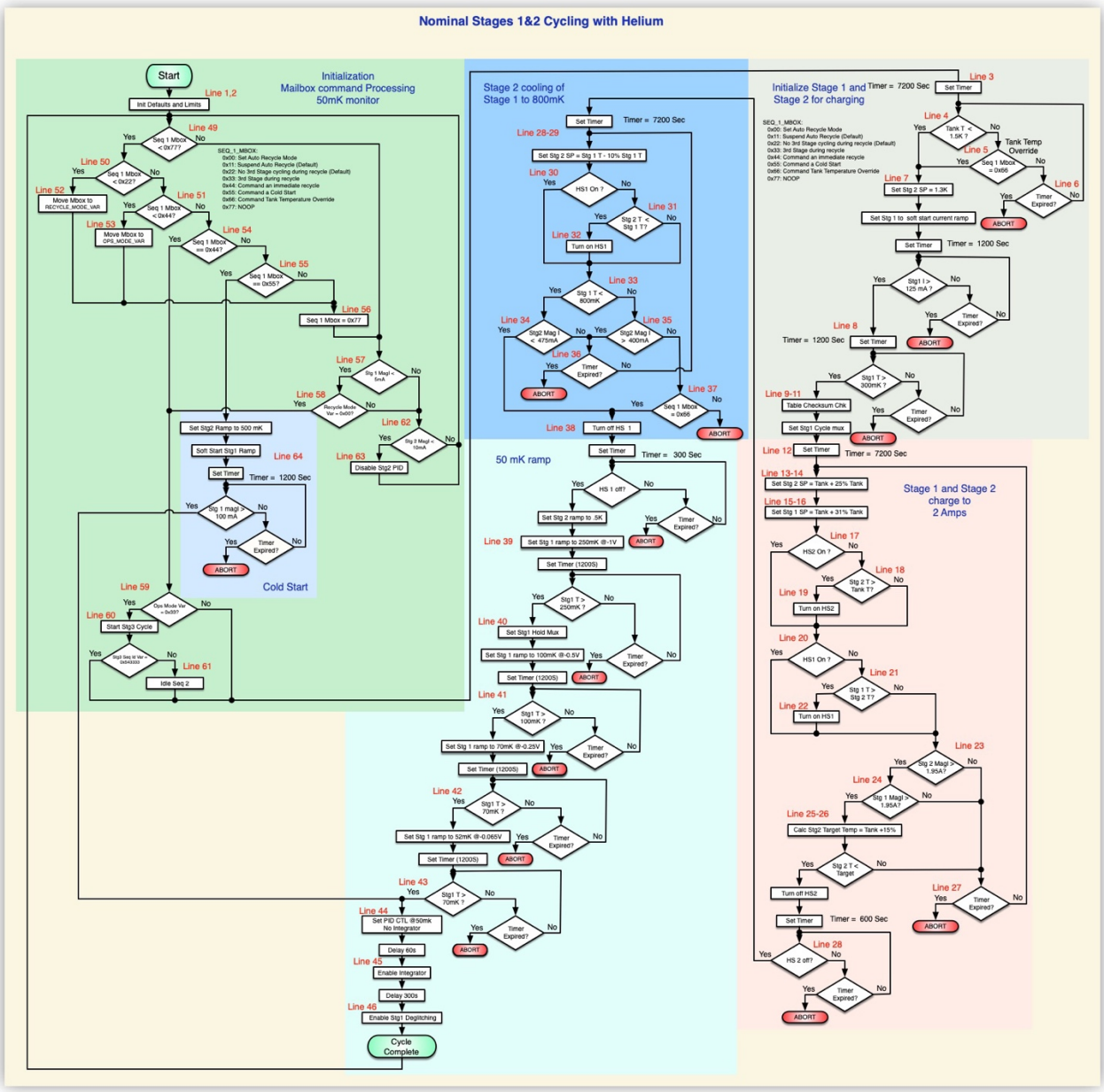
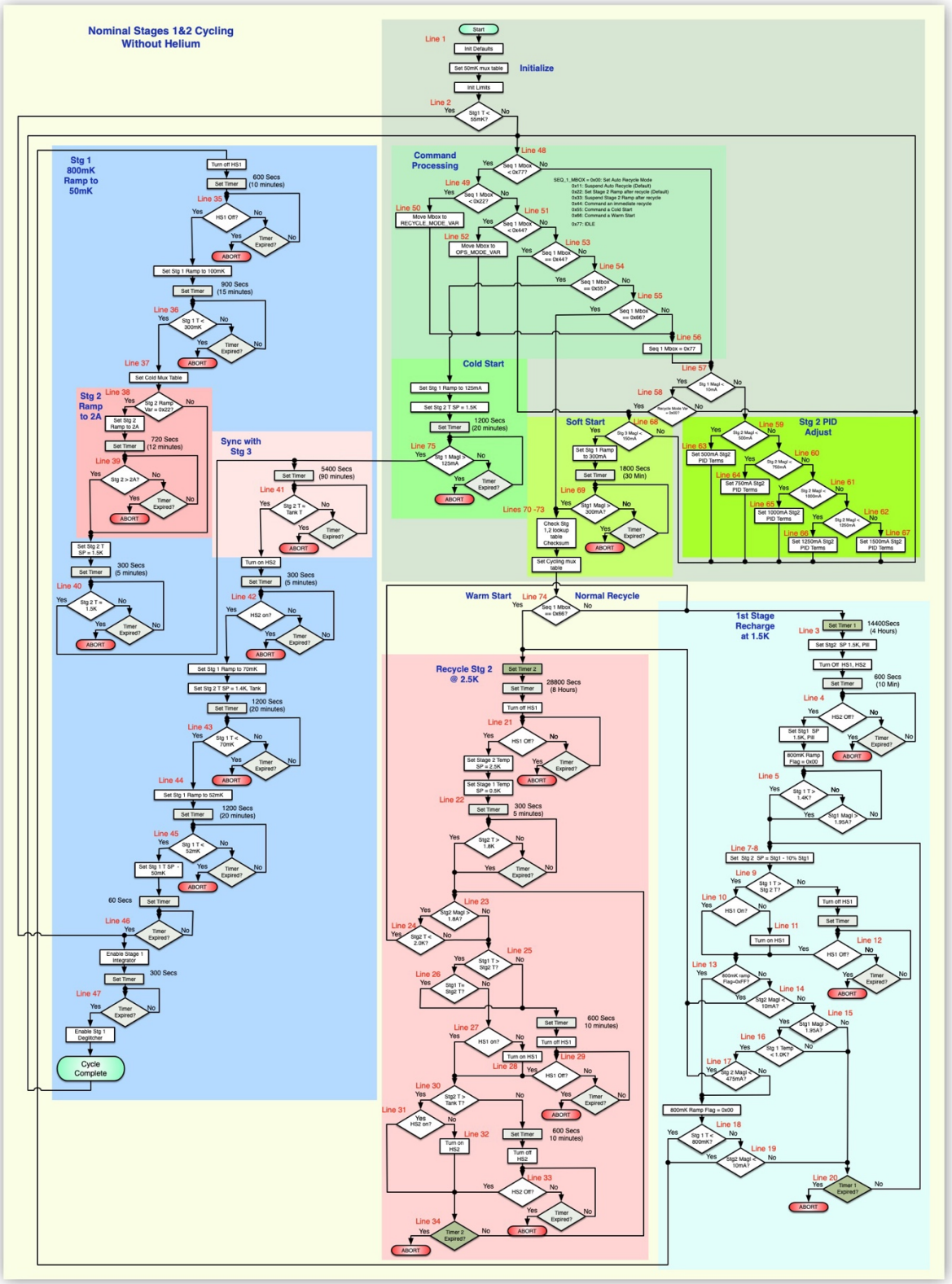


Figure 3. ADR magnet control PID loop.


Nominal Stages 1&2 Cycling with Helium
Start
Initialization
Mailbox command Processing
50mK monitor
Line 1,2
Init Defaults and Limits
Line 49
Seq 1 Mbox < 0x777
Line 50
Seq 1 Mbox < 0x227
Line 51
Seq 1 Mbox < 0x447
Line 52
Move Mbox to RECYCLE_MODE_VAR
Line 53
Move Mbox to OPS_MODE_VAR
Line 54
Seq 1 Mbox == 0x447
Line 55
Seq 1 Mbox == 0x557
Line 56
Seq 1 Mbox = 0x77
Line 57
Stg 1 Magl < 5mA
Line 58
Recycle Mode Var = 0x007
Line 62
Stg 2 Magl < 10mA
Line 63
Disable Stg2 PID
Set Stg2 Ramp to 500 mK
Soft Start Stg1 Ramp
Line 64
Set Timer
Timer = 1200 Sec
Stg 1 magl > 100 mA
Timer Expired?
ABORT
Cold Start
Line 59
Ops Mode Var = 0x007
Line 60
Start Stg3 Cycle
Stg3 Seq Id Var = 0x043333
Line 61
Idle Seq 2
SEQ_1_MBOX:
0x00: Set Auto Recycle Mode
0x11: Suspend Auto Recycle (Default)
0x22: No 3rd Stage cycling during recycle (Default)
0x33: 3rd Stage during recycle
0x44: Command an immediate recycle
0x55: Command a Cold Start
0x66: Command Tank Temperature Override
0x77: NOOP
Stage 2 cooling of
Stage 1 to 800mK
Line 28-29
Set Timer
Timer = 7200 Sec
Set Stg 2 SP = Stg 1 T - 10% Stg 1 T
Line 30
HS1 On ?
Line 31
Stg 2 T < Stg 1 T?
Line 32
Turn on HS1
Line 33
Stg 1 T < 800mK
Line 34
Stg2 Mag I < 475mA
Line 35
Stg2 Mag I > 400mA
Line 36
Timer Expired?
ABORT
Line 37
Seq 1 Mbox = 0x66
Line 38
Turn off HS 1
50 mK ramp
Set Timer
Timer = 300 Sec
HS 1 off?
Set Stg 2 ramp to .5K
Timer Expired?
ABORT
Line 39
Set Stg 1 ramp to 250mK @-1V
Set Timer (1200S)
Stg1 T > 250mK ?
Line 40
Set Stg1 Hold Mux
Set Stg 1 ramp to 100mK @-0.5V
Line 41
Stg1 T > 100mK ?
Set Stg 1 ramp to 70mK @-0.25V
Line 42
Stg1 T > 70mK ?
Set Stg 1 ramp to 52mK @-0.065V
Line 43
Stg1 T > 70mK ?
Line 44
Set PID CTL @50mk No Integrator
Delay 60s
Line 45
Enable Integrator
Delay 300s
Line 46
Enable Stg1 Deglitching
Cycle Complete
Initialize Stage 1 and
Stage 2 for charging
Timer = 7200 Sec
Line 3
Set Timer
Line 4
Tank T < 1.5K ?
Tank Temp Override
Line 5
Seq 1 Mbox = 0x66
Line 6
Timer Expired?
Line 7
Set Stg 2 SP = 1.3K
Set Stg 1 to soft start current ramp
ABORT
Set Timer
Timer = 1200 Sec
Stg1 I > 125 mA ?
Timer Expired?
Line 8
Timer = 1200 Sec
Set Timer
ABORT
Line 9-11
Stg1 T > 300mK ?
Table Checksum Chk
Set Stg1 Cycle mux
ABORT
Line 12
Set Timer
Timer = 7200 Sec
Line 13-14
Set Stg 2 SP = Tank + 25% Tank
Line 15-16
Set Stg 1 SP = Tank + 31% Tank
Stage 1 and Stage 2
charge to
2 Amps
Line 17
HS2 On ?
Line 18
Stg 2 T > Tank T?
Line 19
Turn on HS2
Line 20
HS1 On ?
Line 21
Stg 1 T > Stg 2 T?
Line 22
Turn on HS1
Line 23
Stg 2 Magl > 1.95A?
Line 24
Stg 1 Magl > 1.95A?
Line 25-26
Calc Stg2 Target Temp = Tank +15%
Stg 2 T < Target
Turn off HS2
Line 27
Timer Expired?
ABORT
Set Timer
Timer = 600 Sec
Line 28
HS 2 off?
Timer Expired?
ABORT

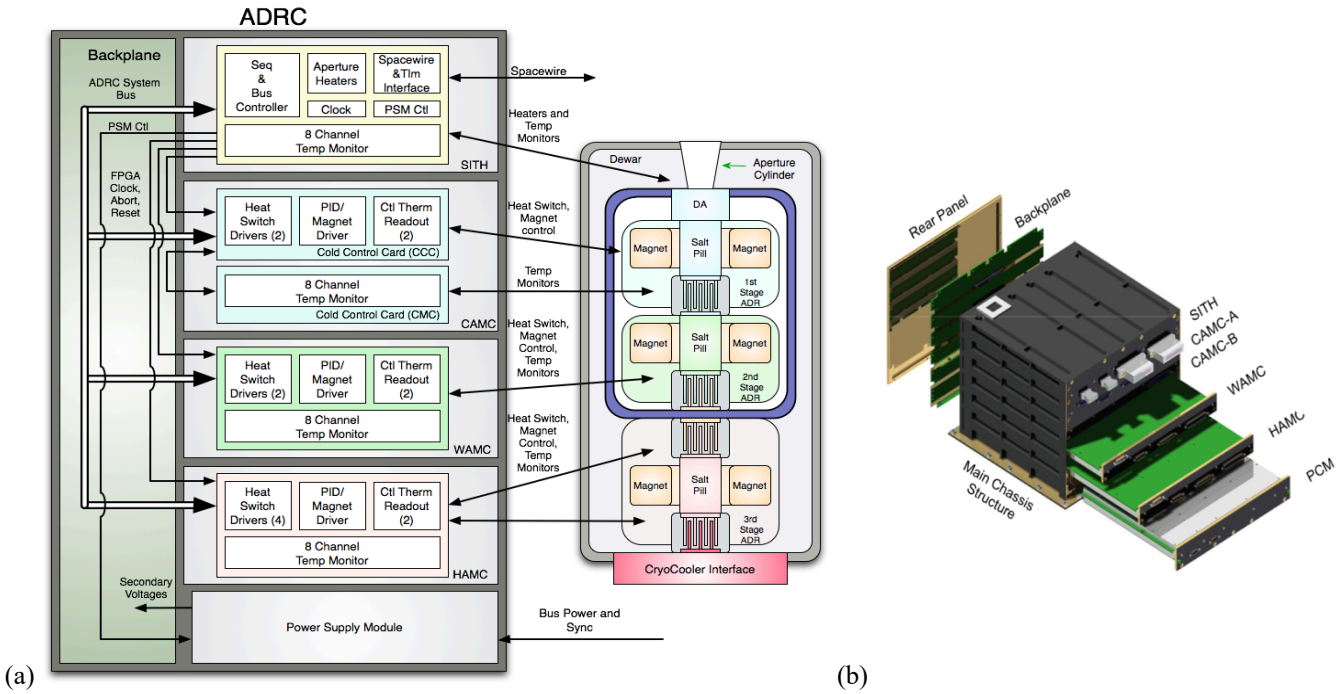
(a)



(b)

Figure 4. (a) Flowchart for the helium mode cycling for the first and second stage ADRs.

(b) Flowchart for the cryo-free mode cycling for the first and second stage ADRs.



(a) (b)

Figure 5. (a) ADRC functional block diagram, also showing the hardware interface with the ADRC. (b) A model view of the ADRC configuration.

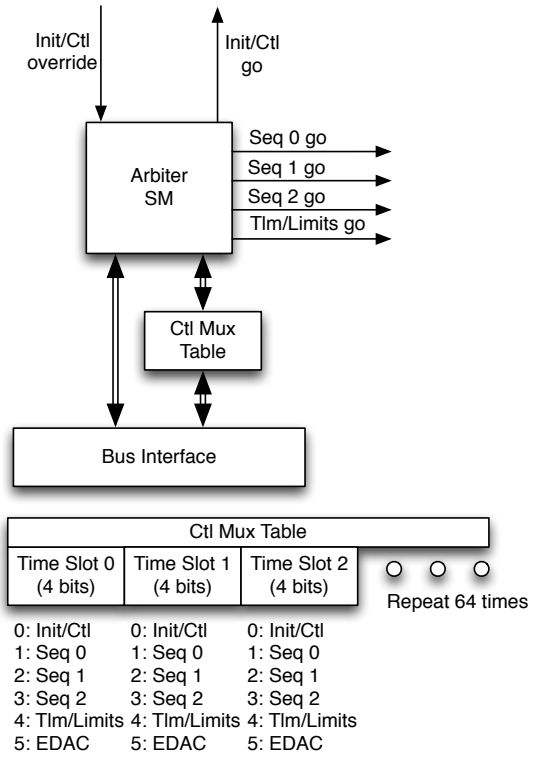


Figure 6. ADR bus system arbiter block diagram and control register format.

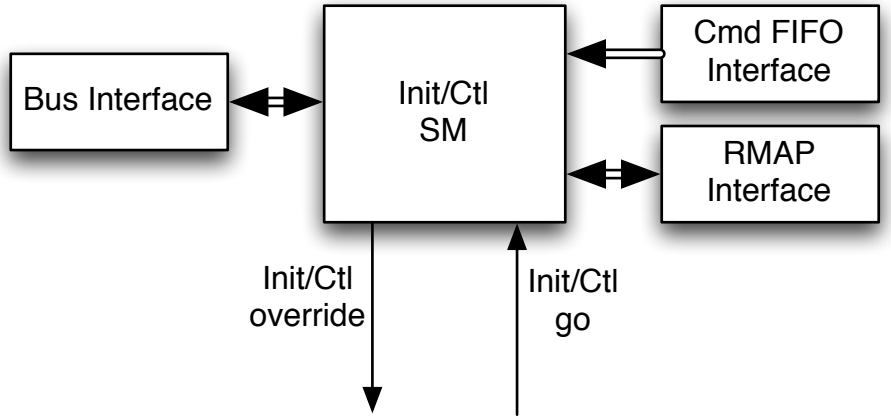


Figure 7. The Init/Ctl SM block.

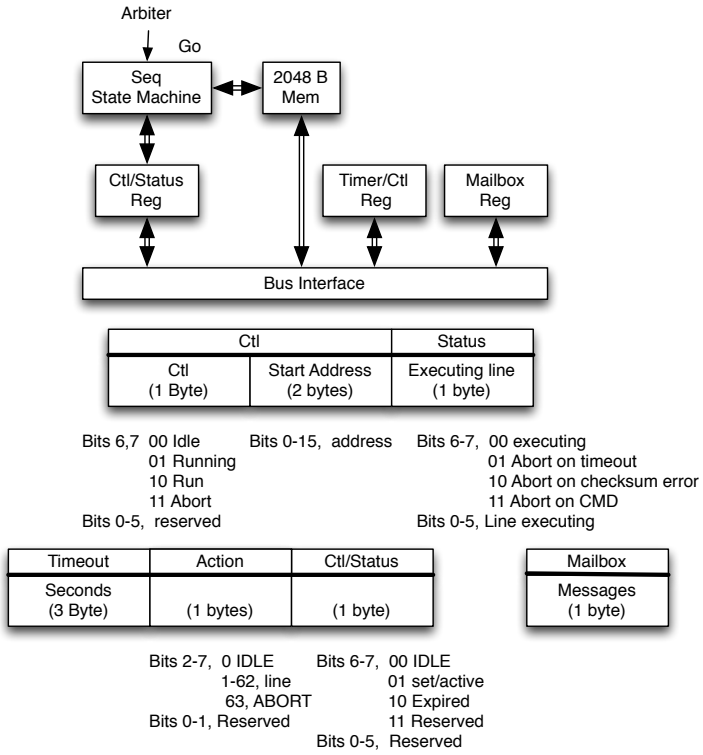


Figure 8. The sequencer SM block diagram and control register format.

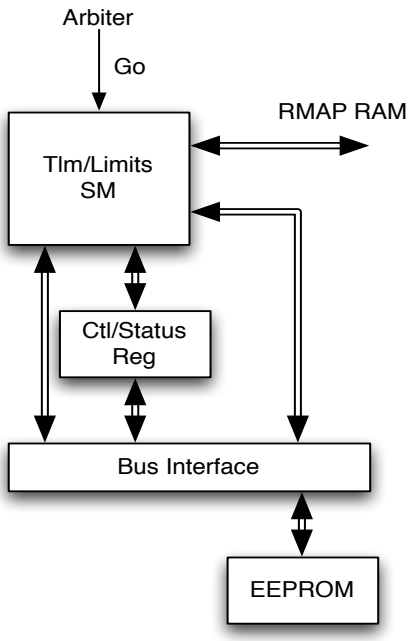


Figure 9. The telemetry and limits SM block diagram.

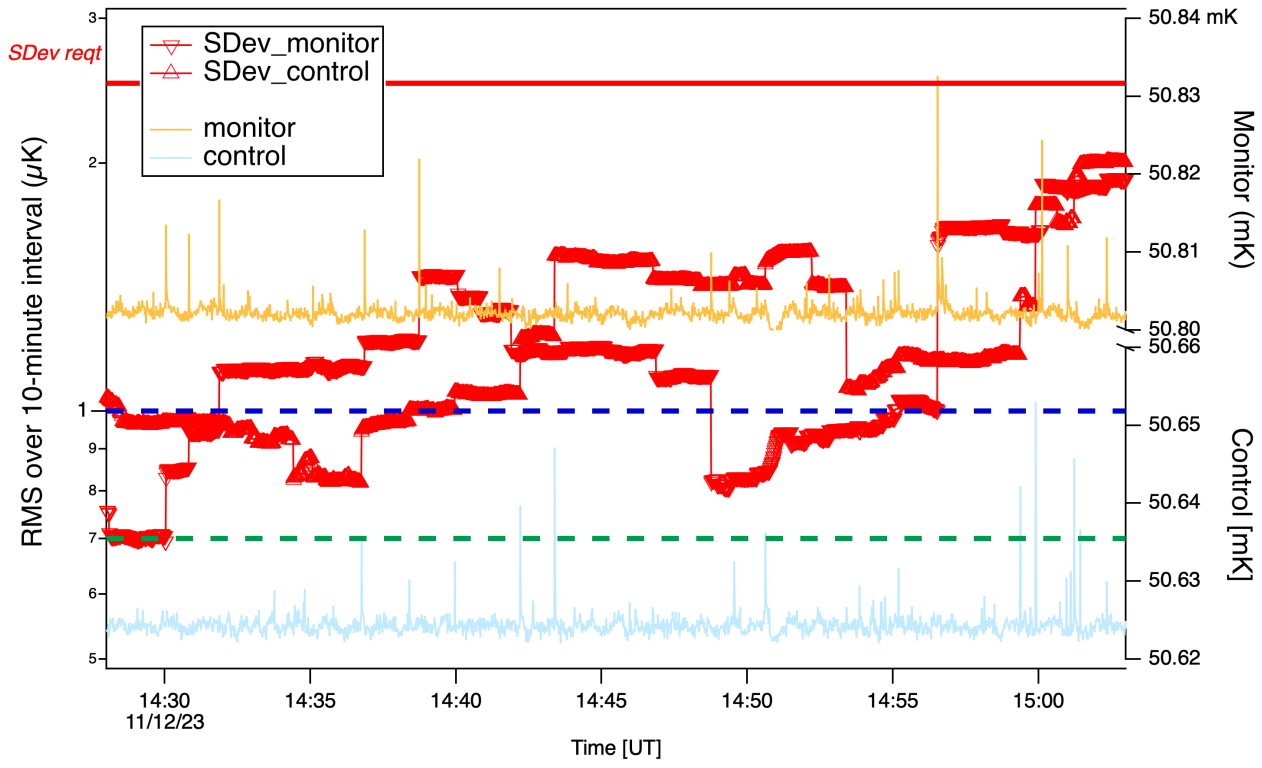


Figure 10. Thermal stability better than 2.5 μK RMS at 50 mK.

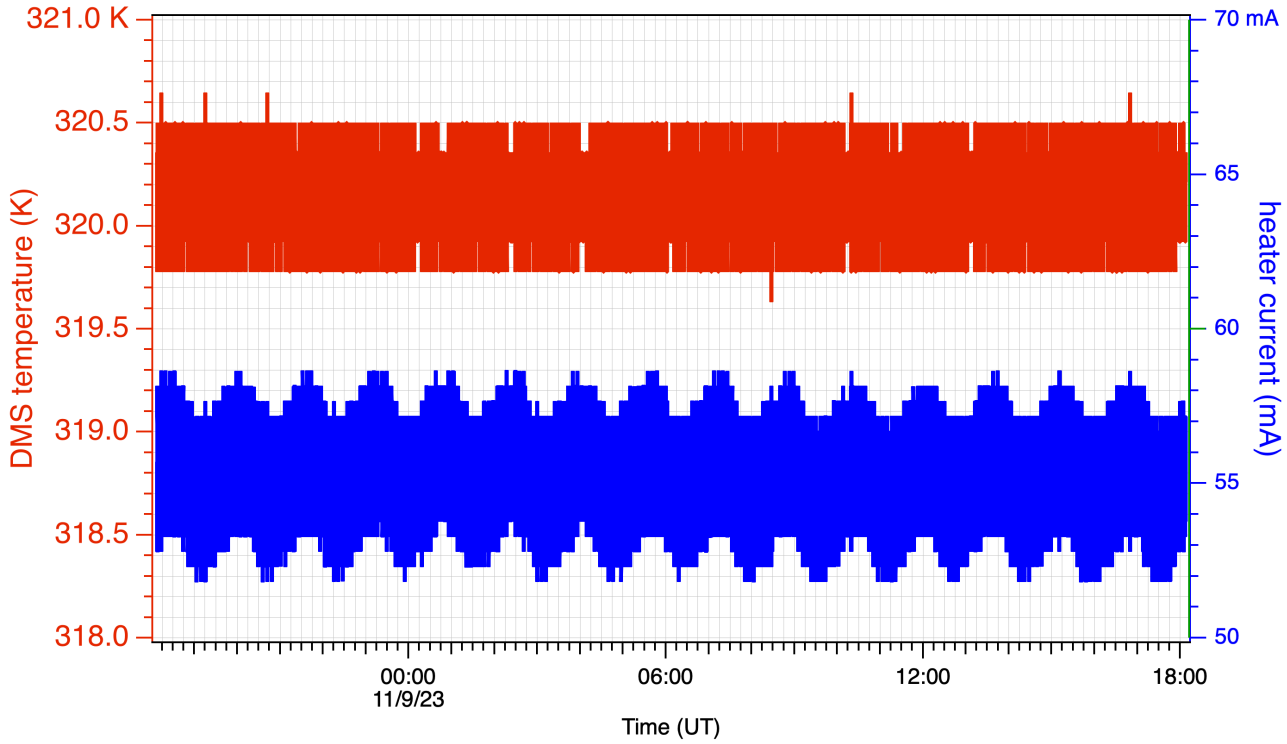


Figure 11. DMS filter controlled at 320 K to prevent contamination.